MP6616A

18V, 2A, Single-Phase BLDC Motor Driver with an Embedded Hall-Effect Sensor and Closed/Open-Loop Speed Control

DESCRIPTION

The MP6616A is a single-phase brushless DC (BLDC) motor driver with an embedded Hall-effect sensor and integrated power MOSFETs. It can achieve up to 2A of output current (I_{OUT}) across a 3.3V to 18V input voltage (V_{IN}) range.

The MP6616A controls the motor speed with closed-loop or open-loop control via the pulse-width modulation (PWM) signal on the PWM pin. The device features a configurable soft commutation angle and Hall offset angle. The hall offset angle can be flexibly optimized for low-speed and high-speed performance across the full speed range.

The MP6616A also features a rotational speed detector (the FG/RD pin). FG/RD is an open drain that outputs a high or low voltage relative to the internal Hall comparator's output.

Protection features include input over-voltage protection (OVP), under-voltage lockout (UVLO) protection, locked rotor protection, over-current protection (OCP), and thermal shutdown.

The MP6616A is available in a QFN-10 (2mmx3mm) package.

FEATURES

- 2mT Minimum Sensitivity Embedded Hall-Effect Sensor
- 3.3V to 18V Operating Input Voltage (V_{IN}) Range
- 2A Continuous Output Current (I_{OUT})
- 100mΩ Integrated Power MOSFETs
- Configurable Speed (40000rpm Max)
- Configurable Minimum Speed and Starting Duty
- Closed-Loop or Open-Loop Speed Control
- High-Speed Accuracy with Closed-Loop Mode
- Configurable Soft Commutation Angle (45° Max)
- Configurable Hall Offset Angle (±45° Max)
- 4-Step Configurable Current Limit (4A Max)
- 2kHz to 100kHz Pulse-Width Modulation (PWM) Input Range
- Configurable Soft-Start Time (t_{SS})
- 27kHz Fixed Switching Frequency (f_{SW})
- Standby Mode
- Locked Rotor Protection with Auto-Recovery
- Thermal Shutdown with Auto-Recovery
- Built-In Input Over-Voltage Protection (OVP), Under-Voltage Lockout (UVLO) Protection, and Auto-Recovery
- Available in a QFN-10 (2mmx3mm) Package

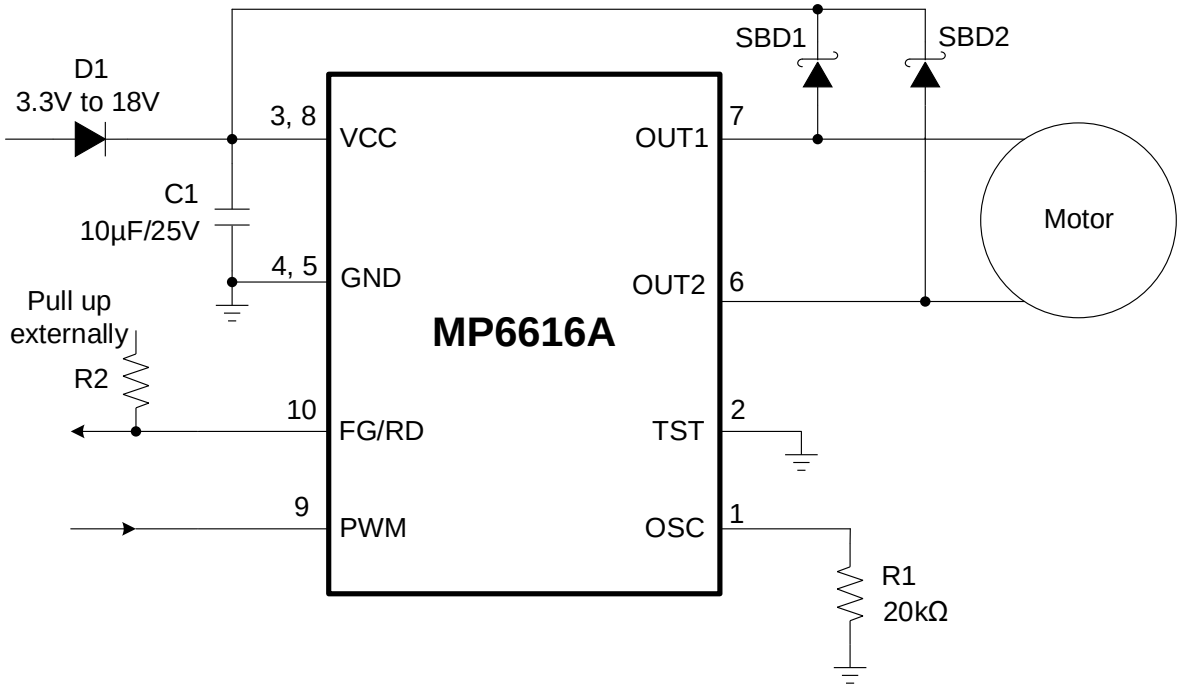
APPLICATIONS

- 1U and 2U Server Fans
- High-Current Cooling Fans
- Central Processing Unit (CPU) and Personal Computer (PC) Fans

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. "MPS", the MPS logo, and "Simple, Easy Solutions" are trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

TYPICAL APPLICATION



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP6616AGD-xxxx**	QFN-10 (2mmx3mm)	*See Below*	1

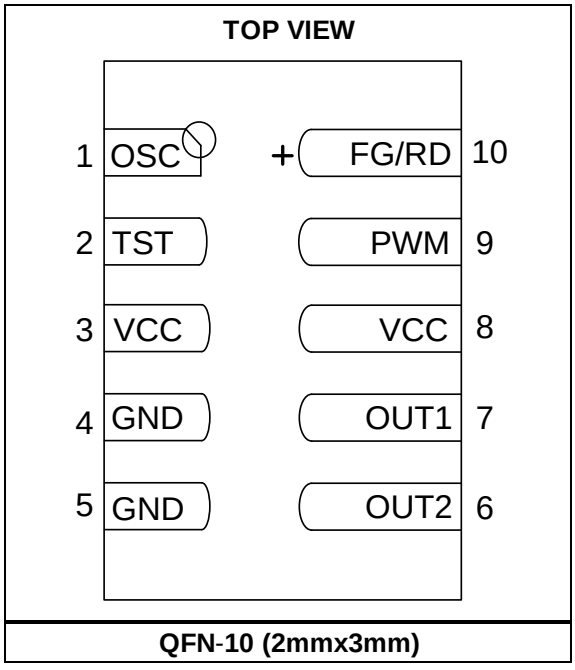
* For Tape & Reel, add suffix -Z (e.g. MP6616AGD-xxxx-Z).

** "xxxx" is the configuration code identifier. The first four digits of the suffix (xxxx) can be a hexadecimal value between 0 and F. Contact an MPS FAE to create this unique number, even if ordering the "0000" code.

TOP MARKING

BUN: Product code of MP6616AGD
Y: Year code
WW: Week code
LLLL: Lot number

PACKAGE REFERENCE



QFN-10 (2mmx3mm)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

PIN FUNCTIONS

Pin #	Name	Description
1	OSC	**Internal oscillator setting.** Connect a 20kΩ, high-accuracy resistor (with 1% or greater accuracy) between the OSC and GND pins.
2	TST	**Test pin.** Connect the TST pin to GND.
3, 8	VCC	**Input power.** The VCC pin must be bypassed locally. Place a bypass capacitor as close to the IC as possible.
4, 5	GND	**Ground.**
6	OUT2	**Motor driver output 2.** If the Hall-effect sensor outputs high, then the OUT2 pin is in a low state.
7	OUT1	**Motor driver output 1.** If the Hall-effect sensor outputs low, then the OUT1 pin is in a low state.
9	PWM	**Pulse-width modulation (PWM) input for speed control.** A 2kHz to 100kHz PWM signal is recommended for normal operation.
10	FG/RD	**Selectable speed or rotor lock indication.** The FG/RD pin is an open-drain output. FG/RD must be pulled up externally.

ABSOLUTE MAXIMUM RATINGS (1)

V_{CC}, $V_{FG/RD}$, V_{PWM} ..... -0.3V to +25V
V_{OUT1}, V_{OUT2} ..... -0.3V to V_{CC} + 0.3V
All other pins ..... -0.3V to +5V
Continuous power dissipation (T_A = 25°C) (2)
QFN-10 (2mmx3mm) 1.9W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -60°C to +150°C

ESD Ratings

Human body model (HBM) ..... ±2kV
Charged device model (CDM) ..... ±2kV

Recommended Operating Conditions (3)

Supply voltage (V_{CC}) ..... 3.3V to 18V
Operating junction temp (T_J) ..... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-10 (2mmx3mm) ..... 65 ..... 12 ... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{CC} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol		Min	Typ	Max	Units
Input under-voltage lockout (UVLO) rising threshold	$V_{IN_UVLO_RISING}$		2.7	3	3.3	V
Input UVLO hysteresis	$V_{IN_UVLO_HYS}$			0.17		V
Operating supply current	I_{CC}	No load		5.4		mA
Standby current	I_{STB}	PWM is low, STB = 1, T_J = 25°C		350	500	µA
Pulse-width modulation (PWM) input high voltage	V_{PWM_HIGH}		1.5			V
PWM input low voltage	V_{PWM_LOW}				0.8	V
PWM input internal pull-up resistance				200		kΩ
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)_HS}$	I_{OUT} = 100mA		52		mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)_LS}$	I_{OUT} = 100mA		44		mΩ
Cycle-by-cycle over-current protection (OCP) current limit	I_{OCP}	OCP_SEL = 11		4		A
Over-voltage protection (OVP) rising threshold	V_{OVP_RISING}		18	19	20	V
OVP hysteresis	V_{OVP_HYS}			1		V
PWM output frequency	f_{PWM}	R_{OSC} = 20kΩ, T_J = 25°C	26.73	27	27.27	kHz
FG/RD output low-level voltage	V_{FG/RD_LOW}	$I_{FG/RD}$ = 1mA, V_{PULL} = 5V, T_J = 25°C		0.19		V
Soft on angle at 100% PWM output duty	θ_{S_ON}	SON = 11111		45		deg
Soft off angle at 100% PWM output duty	θ_{S_OFF}	SOFF = 11111		45		deg
Locked rotor detection time	t_{RD}			0.6		s
Minimum recommended magnetic field					±2	mT
Thermal shutdown (5)	T_{SD}		150	160	180	°C
Thermal shutdown hysteresis (5)	T_{SD_HYS}			40		°C

Note:

5) Guaranteed by design.

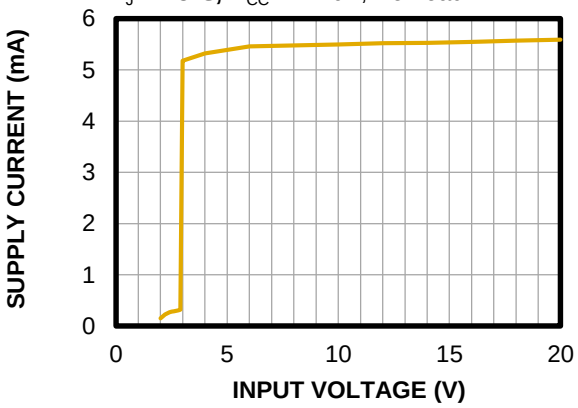
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 12V, T_J = -40 to +125°C, unless otherwise noted.

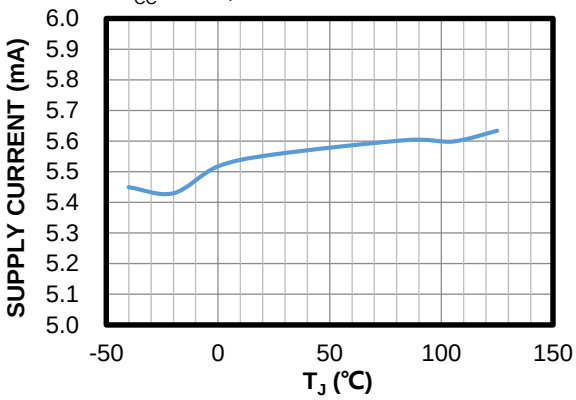
Supply Current vs. Input Voltage

T_J = 25℃, V_{CC} = 2-20V, No Load

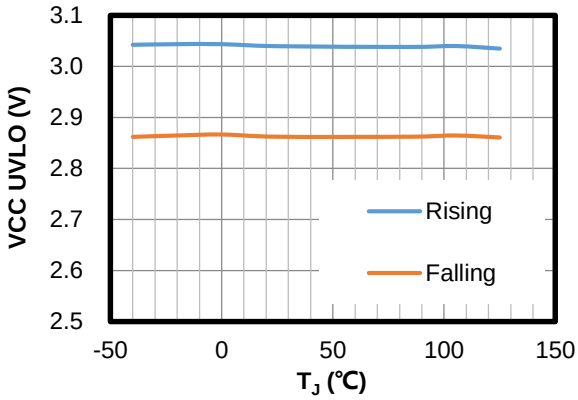


Supply Current vs. T_J

V_{CC} = 12V, No Load

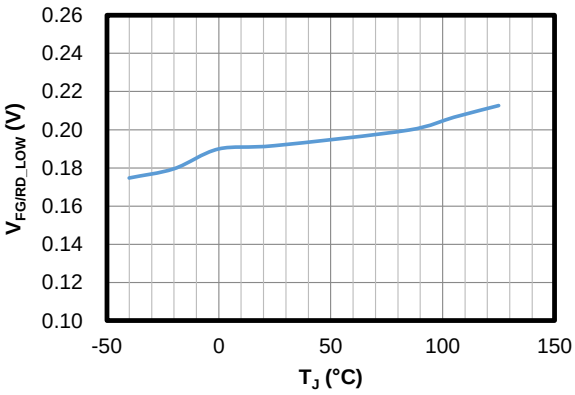


VCC UVLO vs. T_J

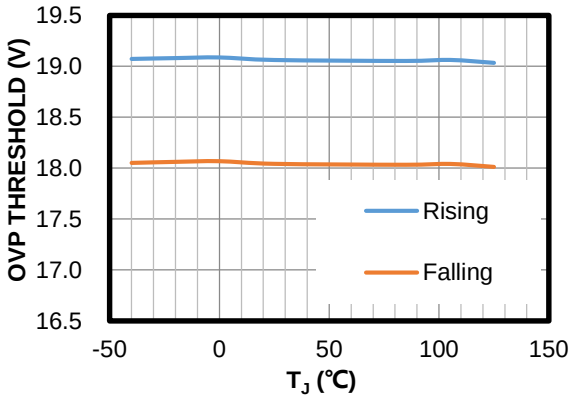


V_{FG/RD_LOW} vs. T_J

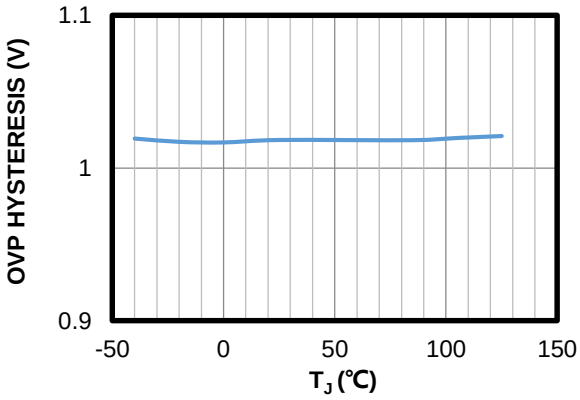
$I_{FG/RD}$ = 1mA, V_{PULL} = 5V



OVP Threshold vs. T_J



OVP Hysteresis vs. T_J



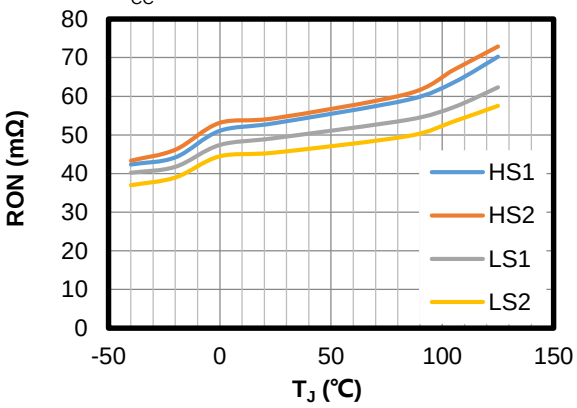
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{CC} = 12V, T_J = -40 to +125°C, unless otherwise noted.

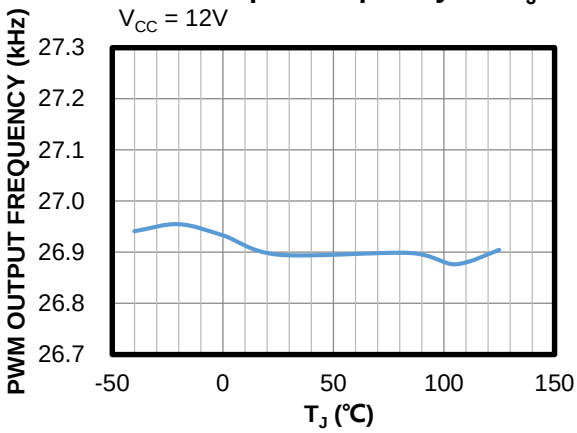
MOSFET RON vs. T_J

V_{CC} = 12V



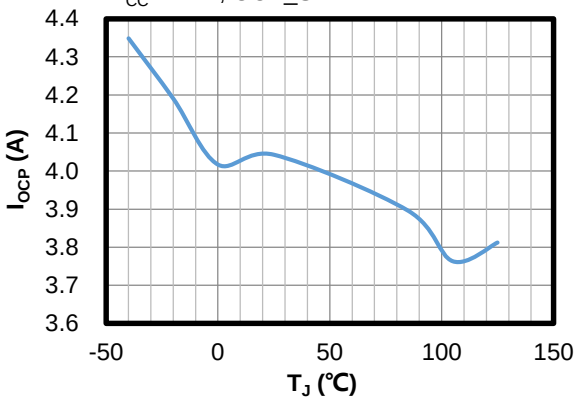
PWM Output Frequency vs. T_J

V_{CC} = 12V



I_{OCP} vs. T_J

V_{CC} = 12V, OCP_SEL = 11

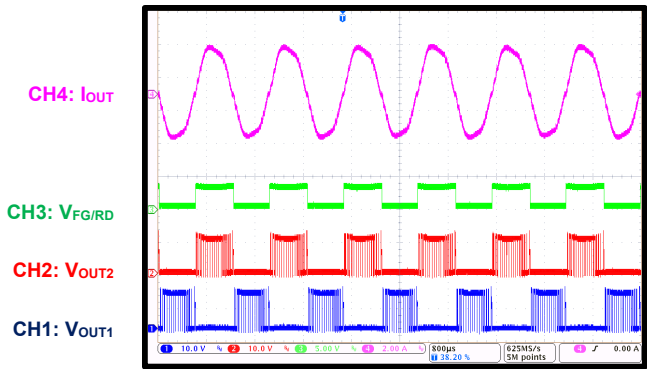


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

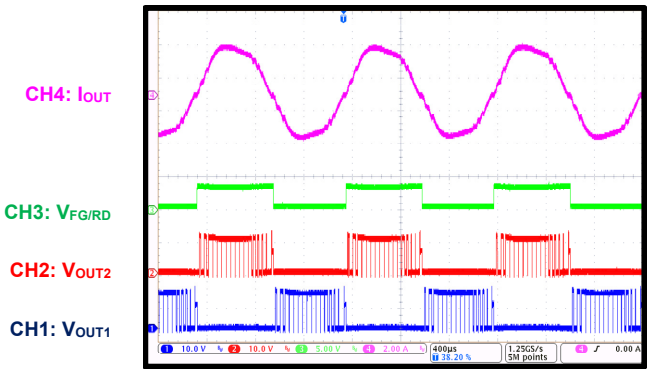
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 12V, f_{PWM} = 20kHz, tested on a 4cm server fan, max speed is 24000rpm unless otherwise noted.

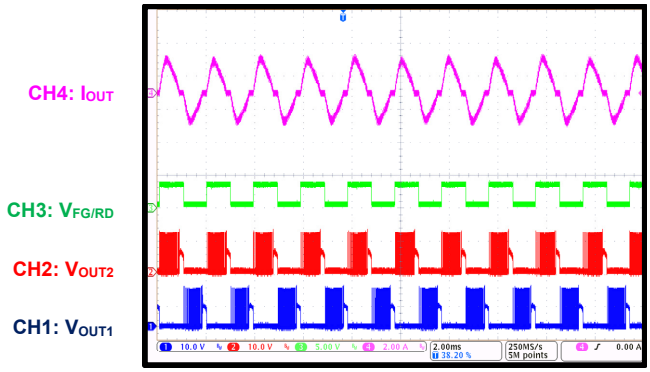
Steady State
PWM duty at 100%



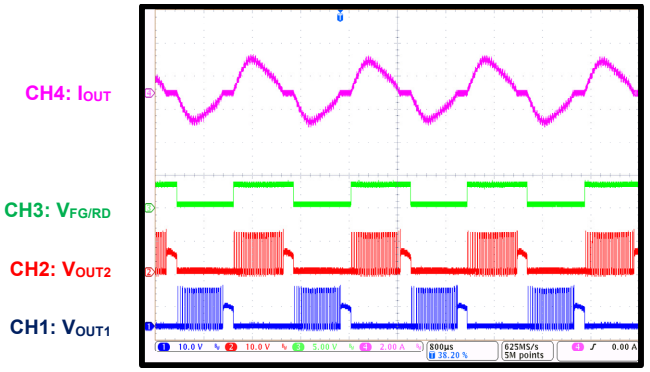
Steady State
PWM duty at 100%



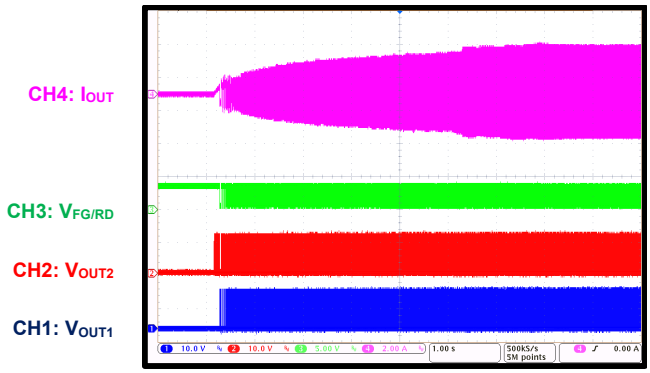
Steady State
PWM duty at 50%



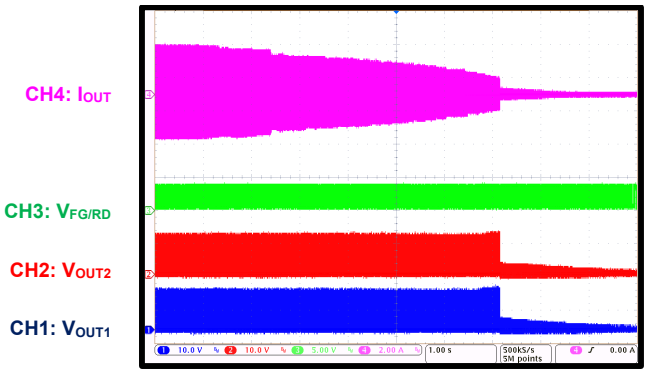
Steady State
PWM duty at 50%



PWM Signal On
PWM duty from 0% to 100%



PWM Signal Off
PWM duty from 100% to 0%

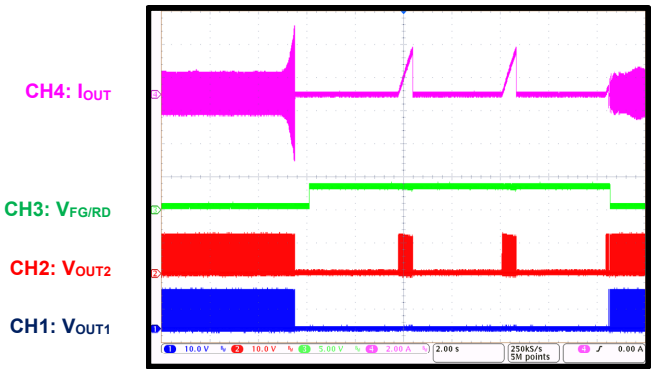


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

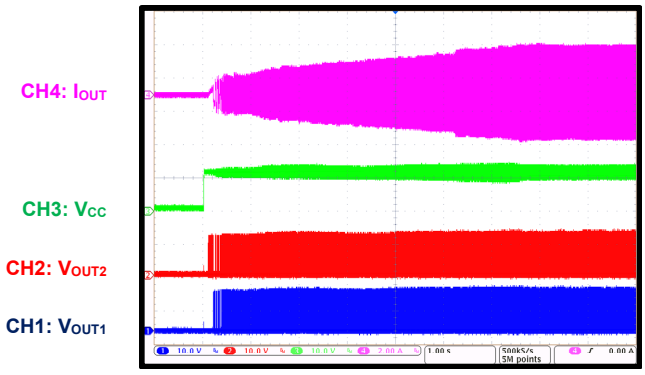
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{CC} = 12V, f_{PWM} = 20kHz, tested on a 4cm server fan, max speed is 24000rpm unless otherwise noted.

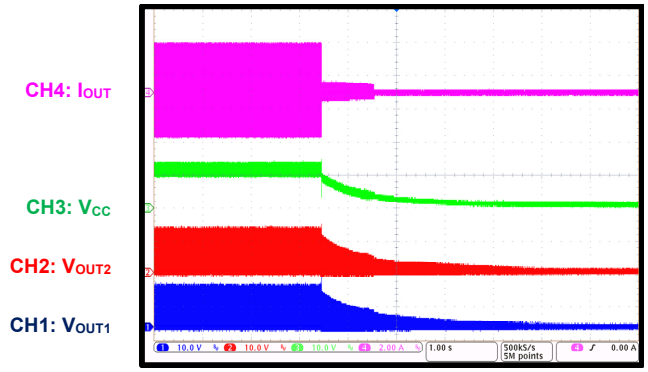
Rotor Lock
PWM duty at 25%



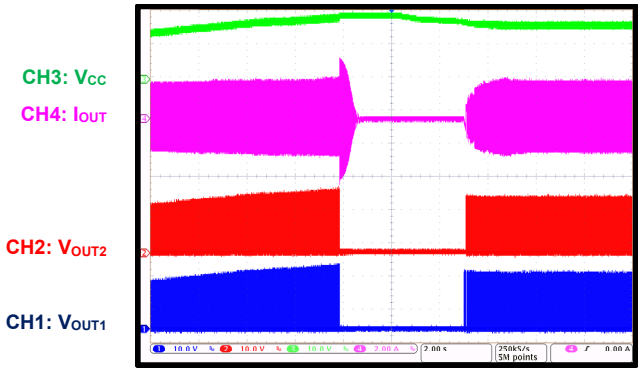
Start-Up through V_{IN}
PWM duty at 100%



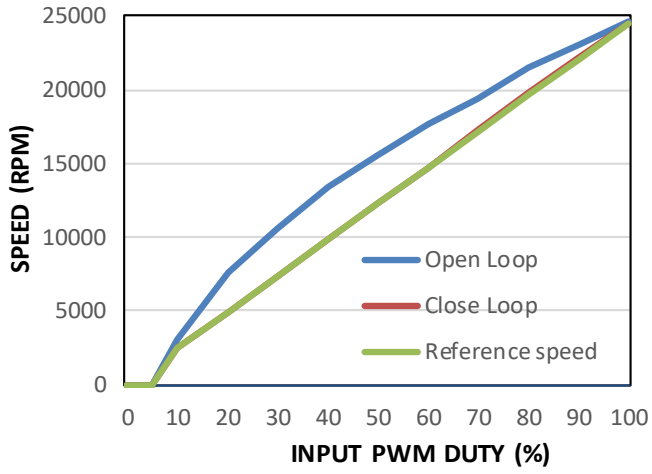
Shutdown through V_{IN}
PWM duty at 100%



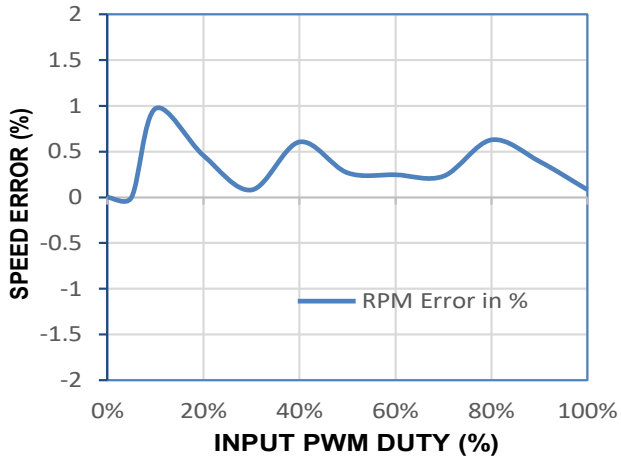
Over-Voltage Protection
PWM duty at 25%



Speed vs. Input PWM Duty



Speed Error vs. Input PWM Duty



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

FUNCTIONAL BLOCK DIAGRAM

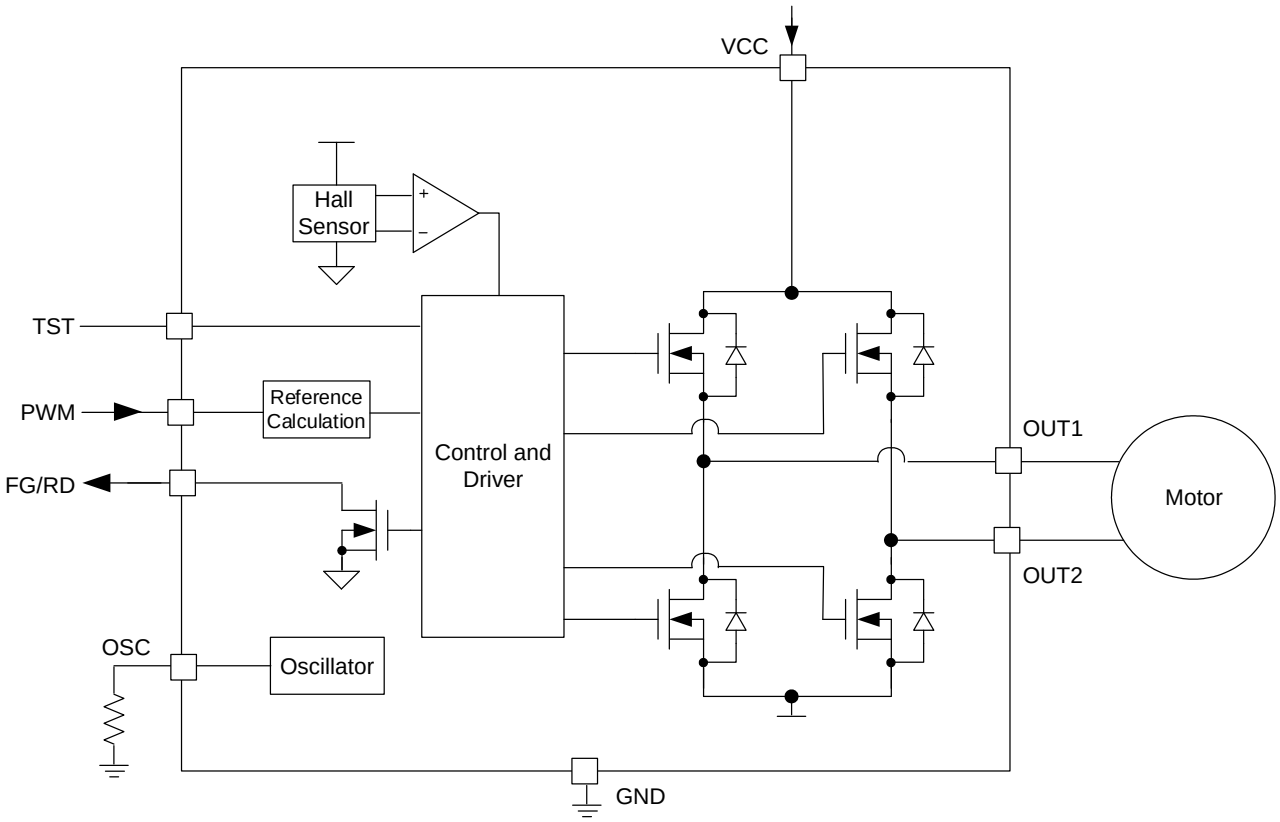


Figure 1: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

OPERATION

The MP6616A is a single-phase brushless DC (BLDC) motor driver with an embedded Hall-effect sensor and integrated power MOSFETs. The device controls the motor speed with closed-loop or open-loop control via the pulse-width modulation (PWM) signal on the PWM pin. The MP6616A features a configurable soft commutation angle and Hall offset angle. The hall offset angle can be flexibly optimized for low-speed and high-speed performance across the full speed range.

The MP6616A also features a rotational speed detector (the FG/RD pin). FG/RD is an open drain that outputs a high or low voltage relative to the internal Hall comparator's output.

Protection features include input over-voltage protection (OVP), under-voltage lockout (UVLO) protection, locked rotor protection, over-current protection (OCP), and thermal shutdown.

Speed Control

The PWM signal accepts a wide range of input frequencies (2kHz to 100kHz). There are two speed control modes: closed-loop mode and mixed mode.

Closed-Loop Mode

Closed-loop mode (DIN_OPEN = 0xFF) controls the motor speed by detecting the PWM signal duty cycle. In closed-loop mode, the Hall sensor's signal speed is detected internally and fed back to the control loop, which adjusts the PWM output duty. This makes the motor speed follow the reference.

The SPD_MAX register sets the maximum speed when the input PWM duty is 100%. The SPD_MIN register sets the minimum speed once the input duty starts corner duty, which is set by the DIN_MIN register.

If the PWM input duty is below the duty set by DIN_MIN, then the fan speed can support three modes, depending on the registers setting:

1. If SPD_ZERO = 0 and MAX_EN = 0, then SPD_MIN determines the speed (see Figure 2).

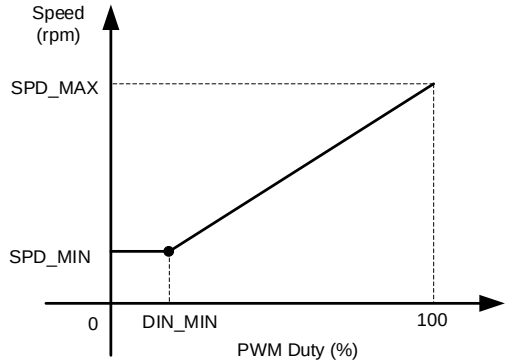


Figure 2: Speed Curve if SPD_ZERO = 0 and MAX_EN = 0

2. If SPD_ZERO = 0 and MAX_EN = 1, then SPD_MAX determines the speed (see Figure 3).

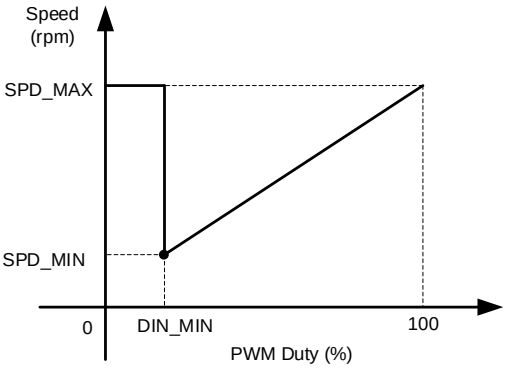


Figure 3: Speed Curve if SPD_ZERO = 0 and MAX_EN = 1

3. If SPD_ZERO = 1 and MAX_EN = x, then the speed is 0rpm (see Figure 4).

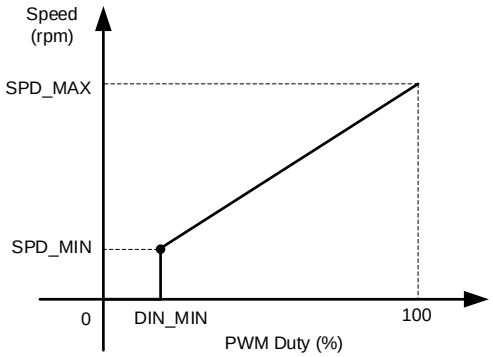


Figure 4: Speed Curve if SPD_ZERO = 1 and MAX_EN = x

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

Mixed Mode

Mixed mode employs closed-loop and open-loop operation. The DIN_OPEN register sets the closed-loop and open-loop control boundaries. If the PWM input duty cycle is below DIN_OPEN, then the IC operates with a closed loop. If the PWM input duty cycle is above DIN_OPEN, then the IC operates with an open loop. Figure 5 shows mixed mode.

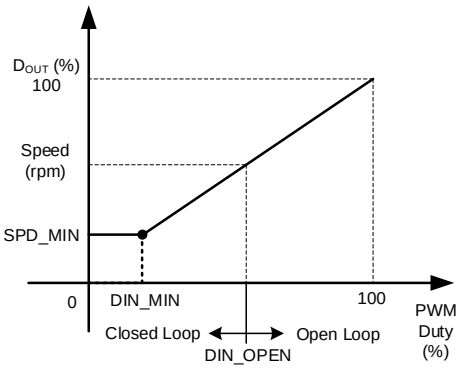


Figure 5: Mixed Mode

OUT1 and OUT2 Operation

To reduce speed variation and increase system efficiency during normal operation, the MP6616A controls the H-bridge MOSFET switching according to the timing sequence. The operation sequence is based on the embedded Hall-effect sensor signal:

- The HALL_TRIM signal has a Hall offset angle with a maximum 45° phase shift (lead or lag).
- If the HALL_TRIM signal is high, then OUT2 is low while OUT1 is the switching phase.
- If the HALL_TRIM signal is low, then OUT1 is low while OUT2 is the switching phase.

The hall offset angle is set by the corresponding registers with the PWM input duty cycle:

- If the input duty is below the DIN_HAL_L value (DIN_HAL_L/64), then the Hall offset angle is determined by HAL_ANG1.
- If the input duty is between DIN_HAL_L/64 and the DIN_HAL_H value (DIN_HAL_H/64), then the Hall offset angle is determined by HAL_ANG2.
- If the input duty is above DIN_HAL_H/64, then the Hall offset angle is determined by HAL_ANG3.

The hall offset angle lead and lag directions are set by HAL_FLAG.

Soft On Commutation

During soft on commutation, the switching phase output duty gradually increases from 0 to steady duty (see θ_{S_ON} in Figure 6). The maximum transition phase angle set by SON_ANG is 45°. The resolution is 1.4°.

Soft Off Commutation

During soft off commutation, the switching phase output duty gradually decreases from steady duty to 0 (see θ_{S_OFF} in Figure 6). The maximum transition phase angle set by SOFF_ANG is 45°. The resolution is 1.4°.

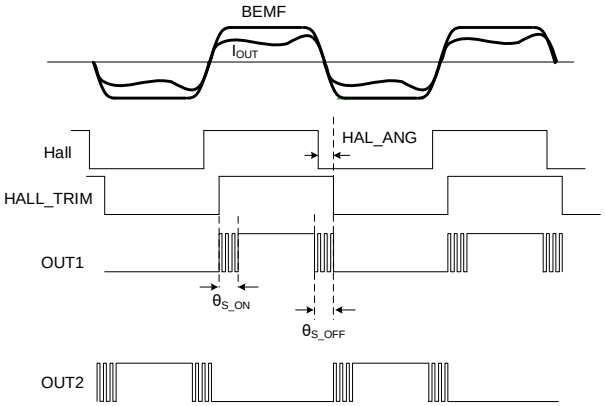


Figure 6: Soft Commutation and Hall Offset Angle

Advanced Soft Off Angle

The advanced soft off angle provides a leading non-zero angle to begin the soft off commutation. Figure 7 shows the advanced soft off angle (θ_{ADV}), which takes an advanced angle once soft off commutation begins. SOFFADV sets θ_{ADV}, which has a maximum angle of 45°.

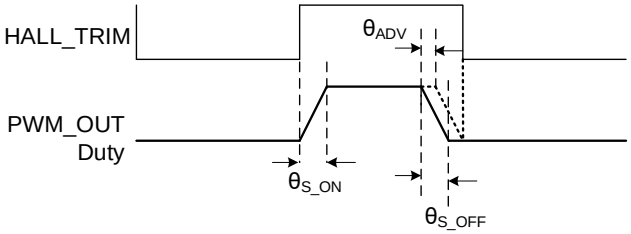


Figure 7: Advanced Soft Off Angle

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

Pre-Start Timer

Once V_{CC} is powered, the switching phase output duty increases gradually. DUTY_SLOPE, bits [1:0] can configure the output duty incremental slope.

Configured via DUTY_SLOPE:

- 0: 9.3ms timer
- 1: 4.6ms timer
- 2: 2.3ms timer
- 3: 1.2ms timer

During the pre-startup stage with a good pre-startup setting, the fan current increases smoothly and the fan spins up robustly.

A longer timer leads to a lower pre-startup current and longer pre-startup time.

Soft Start (SS)

After the pre-startup stage, the MP6616A initiates a soft start. TIME_SS sets the soft-start time (t_{SS}). In closed-loop control, TIME_SS sets the internal speed reference's increasing or decreasing slope. In open-loop control, TIME_SS sets the PWM output duty's ramp up and down time. The configurable t_{SS} reduces the input inrush current during start-up.

Closed-Loop Integrator Gain

In closed-loop mode, KI_TIMER, bits[1:0] and ERR_GAIN, bits[1:0] can configure the closed-loop integrator gain.

Configured via KI_TIMER:

- 00: 9.3ms integrator refresh timer
- 01: 1.2ms integrator refresh timer
- 10: 145µs integrator refresh timer
- 11: 18µs integrator refresh timer

Configured via ERR_GAIN:

- 00: Integrator gain coefficient of 1/8
- 01: Integrator gain coefficient of 1/4
- 10: Integrator gain coefficient of 1/2
- 11: Integrator gain coefficient of 1

A smaller KI_TIMER time or larger ERR_GAIN coefficient leads to a quicker loop response once the loop is steady.

Setting the Switching Frequency

To provide an accurate clock for speed control, connect a 20kΩ, high-accuracy resistor between the OSC and GND pins. It is recommended to use a resistor with a 1% or greater accuracy. The switching frequency (f_{SW}) is about 27kHz.

Digital Oscillator Frequency

The digital clock is used for all Hall angle calculations and closed-loop calculations. The digital clock is selected via the SPD_SEL bits. A higher frequency leads to a higher calculation resolution; however, it also leads to a higher minimum speed.

Standby Mode

The STB register bit turns standby mode on and off. Standby mode is off by default.

If standby mode is enabled while the PWM input remains low and there is no Hall signal edge for 600ms, then the MP6616A enters standby mode. In standby mode, most of the internal circuitries are turned off to conserve power. The standby current is about 350µA.

Once the PWM pulse is detected on the PWM pin, the MP6616A exits standby mode.

Cycle-by-Cycle Over-Current Protection (OCP)

If the current flowing through the H-bridge HS-FET exceeds the threshold set by OCP_SEL after a blanking time (about 1µs), then the HS-FET turns off and the LS-FET turns on. At the next switching cycle, the HS-FET turns on again and resumes normal operation. The over-current limit threshold has four configurable values: 1A, 2A, 3A, and 4A.

Speed Detection

The FG signal on the FG/RD pin outputs an internal Hall-change signal for speed indication. The FG frequency can be 1x, 1/2x, 2/3x, or 2x the Hall frequency, set via the corresponding register bits.

FG/RD is an open-drain output that must be pulled up externally.

Locked Rotor Protection

If the Hall signal polarity does not change

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

during the 0.6s detection time during a rotor lock fault, then the MP6616A turns both LS-FETs on and auto-restarts after a recovery time (set by LOCK_SEL).

If FGRD_SEL is set to 11, then the FG/RD pin is the rotor lock indicator (RD). Set RD_H_L to 1 to keep the FG/RD signal high during a rotor lock fault. Set RD_H_L to 0 to keep the FG/RD signal low during a rotor lock fault.

Over-Voltage Protection (OVP)

If the VCC pin voltage (V_{CC}) exceeds the over-voltage (OV) threshold (19V), then both HS-FETs turn off and the LS-FETs turn on. After V_{CC} drops below 18V, the MP6616A resumes normal operation.

Thermal Shutdown

Thermal shutdown prevents the device from operating at exceedingly high temperatures. If the IC's junction temperature (T_J) exceeds the thermal shutdown threshold (typically 160°C), then one phase's LS-FET remains on and the other phase's LS-FET goes into a tri-state. Once T_J drops below 120°C, the MP6616A resumes normal operation.

Under-Voltage Lockout (UVLO) Protection

If V_{CC} drops below the UVLO threshold, then the device shuts down and the internal logic is reset. Once V_{CC} exceeds the UVLO threshold, the MP6616A resumes normal operation.

Test Mode

The MP6616A includes a test mode to configure the internal register. In test mode, all of the internal registers can be read and written. After designs are finalized, the register values can be configured to the two-time programmable non-volatile memory. Refer to the MPS Fan Driver GUI Software (requested from an MPS FAE) for more information.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

APPLICATION INFORMATION

Input Capacitor

Place an input capacitor (C_{IN}) as close to the VCC and GND pins as possible to maintain a stable input voltage (V_{IN}) and reduce noise at the input. C_{IN} must have a low impedance at f_{SW}.

Ceramic capacitors with X7R dielectrics are recommended for their low ESR characteristics. The ceramic capacitance is dependent on the DC voltage rating. If the ceramic capacitor is biased to its DC voltage rating, then its capacitance drops below 50%.

Ensure the capacitor has a large enough voltage rating margin. The input capacitance must be greater than 10µF.

In some applications, an additional large, electrolytic capacitor may be required to absorb the motor's energy.

Embedded Hall-Effect Sensor

Figure 8 shows the position of the MP6616A's embedded Hall-effect sensor.

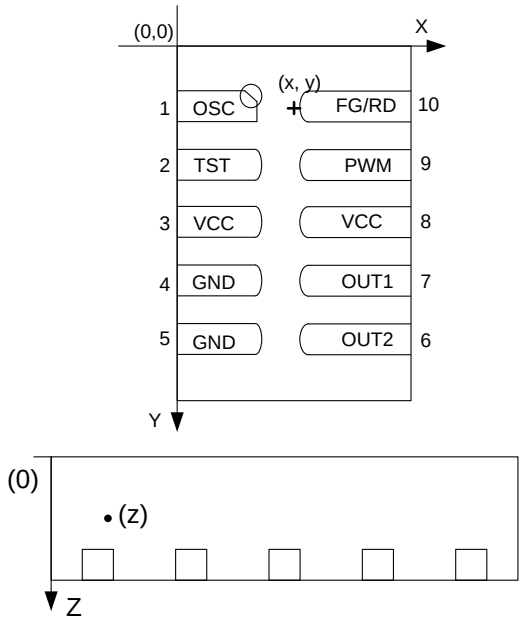


Figure 8: Embedded Hall Sensor (6)

Note:

6) x = 1003 ± 40µm, y = 620 ± 40µm, z = 370 ± 40µm.

Selecting a Reverse-Blocking Diode

A reverse-blocking diode is required while the fan is plugged in reversely to avoid damage. The reverse-blocking diode prevents the bus voltage from charging up via the fan's reverse current.

The blocking diode's maximum reverse voltage should exceed 30V, and the forward current rating of the blocking diode should exceed the input current (I_{IN}).

Selecting an OSC Resistor

A 20kΩ OSC resistor is required to set up the internal clock. A high-accuracy resistor is recommended. For most applications, a resistor with 1% or greater accuracy is sufficient.

Place the OSC resistor close to the IC. The OSC's resistor must be routed away from the power path to avoid changing the internal clock's frequency under different load currents.

Selecting the HS-FET Schottky Diodes

Two Schottky diodes (SBD1 and SBD2) are required. These diodes should be paralleled with the internal HS-FETs. To ensure that the supply voltage does not exceed the maximum reverse voltage (i.e. to ensure over rating does not occur), the maximum reverse voltage of the Schottky diodes must exceed 30V.

It is recommended to choose Schottky diodes with a higher forward current and lower forward voltage. When considering higher-temperature operations, choose the package with the lower thermal resistance.

If the Schottky diode can withstand the reverse voltage, then the Schottky diode's reverse current increases as the temperature rises. The Schottky diode's leakage current should be below 5mA, and under the MP6616A's maximum operating voltage and temperature.

Selecting an Input Clamping Circuit

A voltage-clamping circuit is required, particularly in large current applications and inertial fan applications, to avoid high voltage spikes caused by the energy stored in the motor inductor (see Figure 13 on page 23). For most 12V input applications, a 15V TVS diode or Zener diode in a SOD-123 package is sufficient. The clamping voltage should be below the OVP threshold. Typically, if the maximum operating ambient temperature rises, then ZD1's clamping voltage threshold rises.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

System-Level Electrostatic Discharge (ESD)

Some fan products may be required to pass a system-level electrostatic discharge (ESD) test. Figure 9 shows a typical human body model (HBM) ESD circuit.

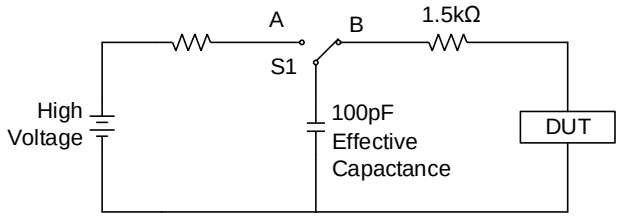


Figure 9: Typical HBM ESD Test Circuit

Figure 10 shows a system-level ESD circuit that follows the IEC61000-4-2 standard.

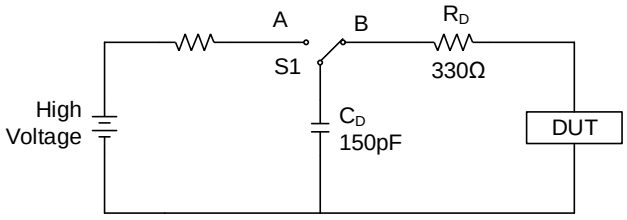


Figure 10: IEC ESD Test Circuit

The IEC ESD test circuit's discharge capacitance is greater than that of the HBM ESD test circuit. The IEC ESD test circuit's resistor is also smaller than that of the HBM ESD test circuit. The IEC ESD test has a greater energy and surge current than the HBM ESD test.

External ESD-enhanced circuits are required to pass the IEC61000-4-2 ESD test. Figure 11 shows an external ESD-enhanced circuit. The external resistors (R2 and R3) and external clamping diodes (ZD2 and ZD3) enhance ESD capability. For most applications, R2 and R3 should be between 30Ω and 100Ω. ZD2 and ZD3 should be Zener diodes, ESD diodes, or TVS diodes in SOD-323 or SOD-523 packages.

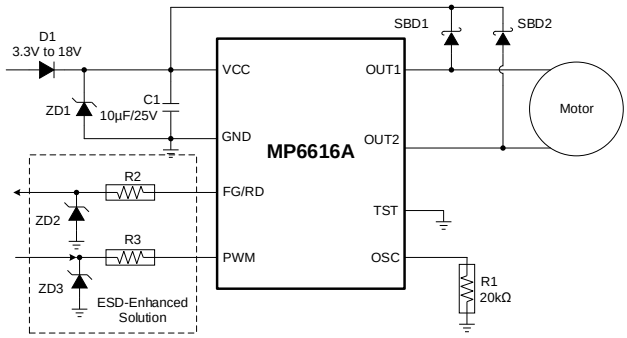


Figure 11: External ESD-Enhanced Circuit

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 12 and follow the guidelines below:

1. To reduce noise at the input, place a 10μF or greater input capacitor as close to the IC as possible.
2. To reduce high-frequency noise, place a 10nF to 100nF input capacitor in a small, 0402 package as close to the IC as possible.
3. Place the OSC resistor as close to the IC as possible. Route the OSC resistor away from any power paths.

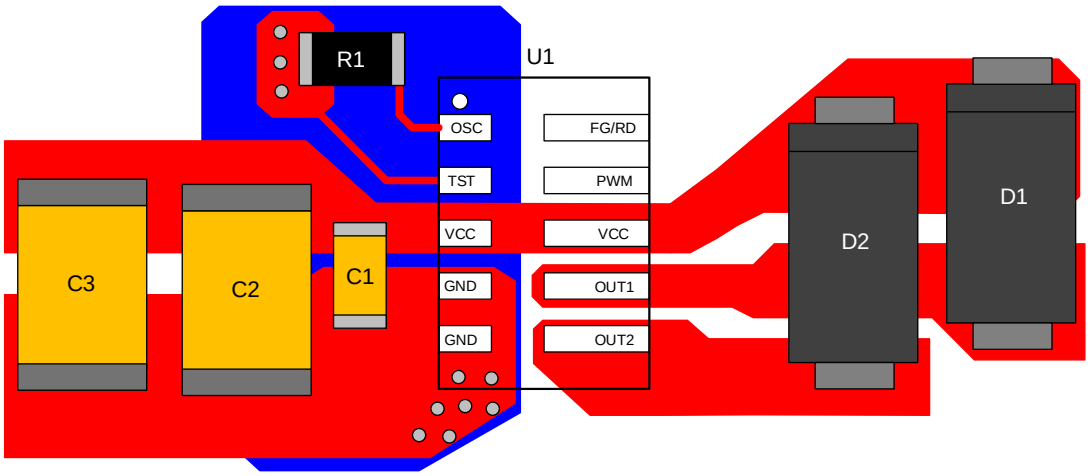


Figure 12: Recommended PCB Layout

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

REGISTER DESCRIPTION

Register Map

Address	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x00 (OTP/REG)	RESERVED	SPD_SEL[1:0]		SOFFADV[4:0]				
0x01 (OTP/REG)	SPD_MAX[7:0]							
0x02 (OTP/REG)	SPD_MAX[15:8]							
0x03 (OTP/REG)	SPD_MIN[7:0]							
0x04 (OTP/REG)	DIN_MIN[7:0]							
0x05 (OTP/REG)	DIN_OPEN[7:0]							
0x06 (OTP/REG)	TIME_SS[2:0]			RVSI_EN	KI_TIMER[1:0]		ERR_GAIN[1:0]	
0x07 (OTP/REG)	SPD_ZERO	OCP_SEL[1:0]		SON_ANG [4:0]				
0x08 (OTP/REG)	RD_H_L	LOCK_SEL[1:0]		SOFF_ANG [4:0]				
0x09 (OTP/REG)	Reserved		HAL_FLAG	HAL_ANG1[4:0]				
0x0A (OTP/REG)	RESERVED			HAL_ANG2[4:0]				
0x0B (OTP/REG)	DUTY_SLOPE[1:0]		RESERVED	HAL_ANG3[4:0]				
0x0C (OTP/REG)	FGRD_SEL[1:0]		DIN_HAL_L[5:0]					
0x0D (OTP/REG)	RESERVED		DIN_HAL_H[5:0]					
0x0E (OTP/REG)	RESERVED			STB	2FG	MAX_EN	RESERVED	
0x0F (REG)	OTP_PAGE[1:0]		RESERVED					

Register 0x00

Bits	Bit Name	Access	Default	Description
7	RESERVED	N/A	0	Reserved.
6:5	SPD_SEL[1:0]	OTP/REG	00	Selects the digital clock. A higher frequency leads to a higher calculation resolution; however, it also leads to a higher minimum speed. These bits indicate the supported minimum speeds. 00: 100r/min (default) 01: 400r/min 10: 800r/min 11: 1600r/min
4:0	SOFFADV[4:0]	OTP/REG	00	Advanced soft off angle. Sets the advanced angle after soft off commutation starts. 00: 1.4° (default) 01: 2.8° …1F: 45° 1.4° per step, θ_{ADV} = 1.4° x (SOFFADV + 1)

Register 0x01

Bits	Bit Name	Access	Default	Description
7:0	SPD_MAX[7:0]	OTP/REG	0x20	Sets the maximum speed. LSB of the maximum speed. This register works together with SPD_MAX[15:8] to set the speed when the PWM input duty is 100%. 1 LSB = 1rpm. These bits are set to 20000rpm by default.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

Register 0x02

Bits	Bit Name	Access	Default	Description
7:0	SPD_MAX[15:8]	OTP/REG	0x4E	Sets the maximum speed. MSB of the maximum speed. This register works together with SPD_MAX[7:0] to set the speed when the PWM input duty is 100%. These bits are set to 20000rpm by default.

Register 0x03

Bits	Bit Name	Access	Default	Description
7:0	SPD_MIN[7:0]	OTP/REG	0x33	Sets the minimum speed. Sets the speed once the PWM input duty = DIN_MIN in closed-loop control. The minimum speed = SPD_MIN x 32, and is set to 1632rpm by default. Sets the output duty once the PWM input duty = DIN_MIN in open-loop control. The output duty = SPD_MIN / 255, and is set to 20% by default.

Register 0x04

Bits	Bit Name	Access	Default	Description
7:0	DIN_MIN[7:0]	OTP/REG	0x33	PWM input starting corner duty. The starting corner duty is DIN_MIN / 255. The default duty is 20%.

Register 0x05

Bits	Bit Name	Access	Default	Description
7:0	DIN_OPEN[7:0]	OTP/REG	0x00	PWM input corner duty for closed-loop and open-loop control. If the input duty exceeds DIN_OPEN / 255, the IC operates in open-loop mode. If input duty drops below DIN_OPEN / 255, the IC operates in closed-loop mode.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

Register 0x06

Bits	Bit Name	Access	Default	Description
7:5	TIME_SS[2:0]	OTP/REG	010	Soft-transition time. 000: 2.4s 001: 4.8s 010: 7.2s (default) 011: 9.6s 100: 12s 101: 14.4s 110: 16.8s 111: 19.2s
4	RVSI_EN	OTP/REG	1	Enables the reverse current detection function. 0: Disabled 1: Enabled (default)
3:2	KI_TIMER[1:0]	OTP/REG	10	Controls the integral timer in closed-loop mode. 00: 9.3ms 01: 1.2ms 10: 145μs (default) 11: 18μs
1:0	ERR_GAIN[1:0]	OTP/REG	11	Controls the integral gain in closed-loop mode. 00: 1/8 01: 1/4 10: 1/2 11: 1 (default)

Register 0x07

Bits	Bit Name	Access	Default	Description
7	SPD_ZERO	OTP/REG	1	Indicates the speed when the PWM input duty < DIN_MIN. 0: Maintains the minimum or maximum speed 1: 0 (default)
6:5	OCP_SEL[1:0]	OTP/REG	11	Sets the current limit. 00: 1A 01: 2A 10: 3A 11: 4A (default)
4:0	SON_ANG[4:0]	OTP/REG	0x1F	Sets the soft on phase transition angle. 00: 1.4° 01: 2.8° … 1F: 45° (default) 1.4° per step, θ_{S_ON} = 1.4° x (SON_ANG + 1)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

Register 0x08

Bits	Bit Name	Access	Default	Description
7	RD_H_L	OTP/REG	1	Sets the FG/RD high/low output. 0: FG/RD outputs low during locked rotor protection 1: FG/RD outputs high during locked rotor protection (default)
6:5	LOCK_SEL[1:0]	OTP/REG	00	Sets the rotor lock retry time. 00: 3.6s (default) 01: 4.8s 10: 6s 11: 8.4s
4:0	SOFF_ANG[4:0]	OTP/REG	0x1F	Sets the soft off phase transition angle. 00: 1.4° 01: 2.8° … 1F: 45°(default) 1.4° per step, θ_{S_OFF} = 1.4° x (SOFF_ANG + 1)

Register 0x09

Bits	Bit Name	Access	Default	Description
7:6	RESERVED	N/A	0	Reserved.
5	HAL_FLAG	OTP/REG	0	Sets the Hall offset angle lead/lag. 0: Lag 1: Lead
4:0	HAL_ANG1[4:0]	OTP/REG	00000	Sets the Hall offset angle when PWM duty < DIN_HAL_L. 00: 1.4° (default) 01: 2.8° … 1F: 45° 1.4° per step, Hall offset angle = 1.4° x (HAL_ANG1 + 1)

Register 0x0A

Bits	Bit Name	Access	Default	Description
7:5	RESERVED	N/A	000	Reserved.
4:0	HAL_ANG2[4:0]	OTP/REG	00000	Sets the Hall offset angle when DIN_HAL_L < PWM duty < DIN_HAL_H. 00: 1.4° (default) 01: 2.8° … 1F: 45° 1.4° per step, Hall offset angle = 1.4° x (HAL_ANG2 + 1)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

Register 0x0B

Bits	Bit Name	Access	Default	Description
7:6	DUTY_SLOPE [1:0]	OTP/REG	00	Sets the pre-startup timer. 00: 9.3ms (default) 01: 4.6ms 10: 2.3ms 11: 1.2ms
5	RESERVED	N/A	1	Reserved.
4:0	HAL_ANG3[4:0]	OTP/REG	00	Sets the Hall offset angle when PWM duty > DIN_HAL_H. 00: 1.4° (default) 01: 2.8° … 0x1F: 45° 1.4° per step, Hall offset angle = 1.4° x (HAL_ANG3 + 1)

Register 0x0C

Bits	Bit Name	Access	Default	Description
7:6	FGRD_SEL[1:0]	OTP/REG	00	Selects the FG/RD pin output. 00: 1x (default) 01: 1/2x 11: RD If FGRD_SEL = 10, then the 2FG bit selects the FG/RD pin output (2/3x or 2x). See Register 0x0E for more details.
5:0	DIN_HAL_L[5:0]	OTP/REG	0x10	Sets the PWM input duty for Hall offset angle low threshold. Duty = DIN_HAL_L / 64. The default duty is 25%.

Register 0x0D

Bits	Bit Name	Access	Default	Description
7:6	RESERVED	N/A	0	Reserved.
5:0	DIN_HAL_H[5:0]	OTP/REG	0x30	Sets the PWM input duty for Hall offset angle high threshold. Duty = DIN_HAL_H / 64. The default duty is 75%.

Register 0x0E

Bits	Bit Name	Access	Default	Description
7:5	RESERVED	N/A	000	Reserved.
4	STB	OTP/REG	0	Enables standby mode. 0: Disabled (default) 1: Enabled
3	2FG	OTP/REG	0	Selects the FG/RD pin output (2/3x or 2x) when FGRD_SEL = 10. FGRD_SEL = 10, 2FG = 0: 2/3x (default) FGRD_SEL = 10, 2FG = 1: 2x
2	MAX_EN	OTP/REG	0	Enables the maximum speed when the PWM input duty < DIN_MIN. This bit is only active when SPD_ZERO = 0. 0: Disabled (default) 1: Enabled
1:0	RESERVED	N/A	00	Reserved.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

Register 0x0F

Bits	Bit Name	Access	Default	Description
7:6	OTP_PAGE[1:0]	REG	00	OTP page indicator, read-only. 00: No OTP (default) 01: 1st page of OTP is programmed 10: 2nd page of OTP is programmed.
5:0	RESERVED	N/A	N/A	Reserved.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUIT

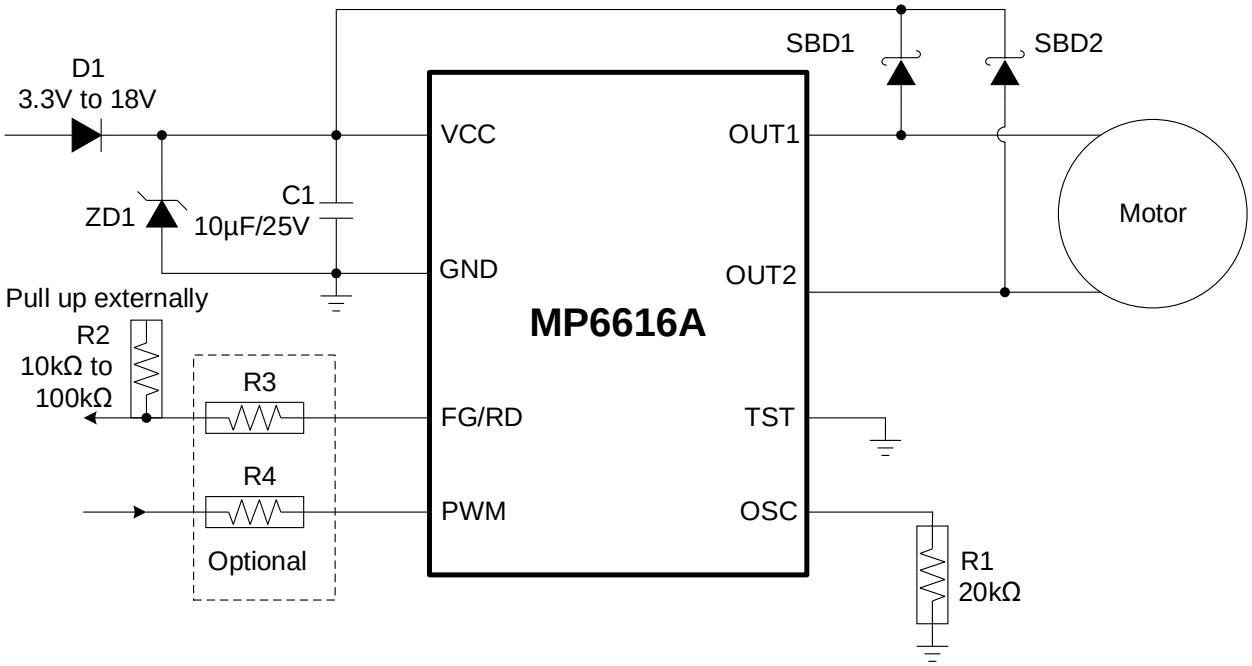
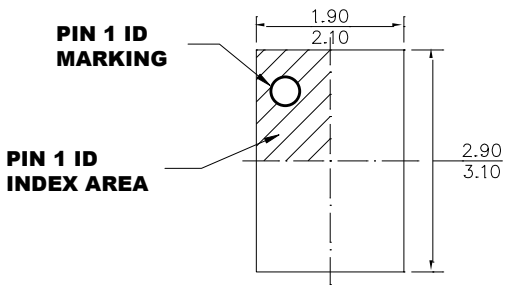


Figure 13: Typical Application Circuit

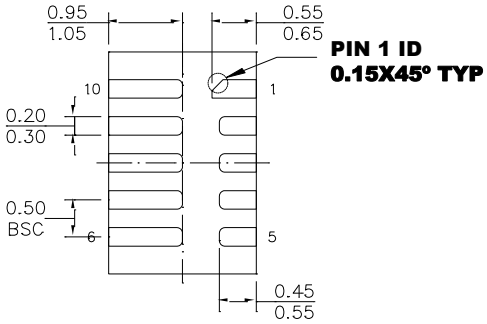
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

PACKAGE INFORMATION

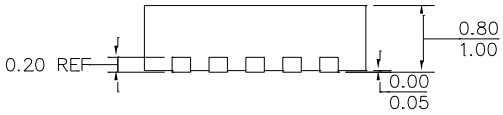
QFN-10 (2mmx3mm)



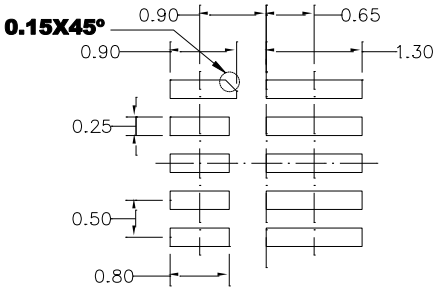
TOP VIEW



BOTTOM VIEW



SIDE VIEW



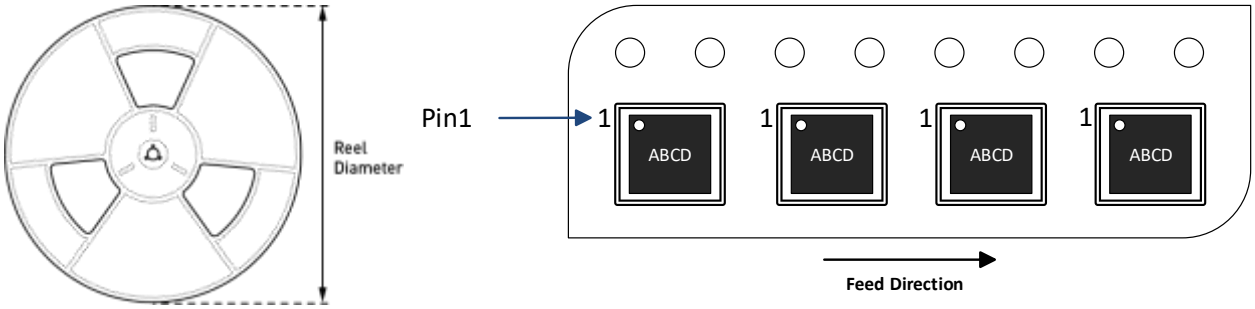
RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tray	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6616GD-Z	QFN-10 (2mmx3mm)	5000	N/A	N/A	13in	12mm	8mm

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/8/2022	Initial Release	-

Notice: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third-party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.