MP62170/MP62171

3.3V/5V, Single-Channel 1.5A Current-Limited Power Distribution Switch

The Future of Analog IC Technology

DESCRIPTION

The MP62170/MP62171 Power Distribution Switch features internal current limiting to prevent damage to host devices due to faulty load conditions. The MP62170/MP62171 analog switch has 75mΩ on-resistance and operates from 2.7V to 5.5V input. It is available with guaranteed current limits, making it ideal for load switching applications. The MP62170/MP62171 has built-in protection for both over current and increased thermal stress. For over current, the device will limit the current by changing to a constant current mode.

As the temperature increases as a result of short circuit, then the device will shut off. The device will recover once the device temperature reduces to approx 120°C.

MP62170/MP62171 is available in 8-pin MSOP and SOIC package without exposed pad.

FEATURES

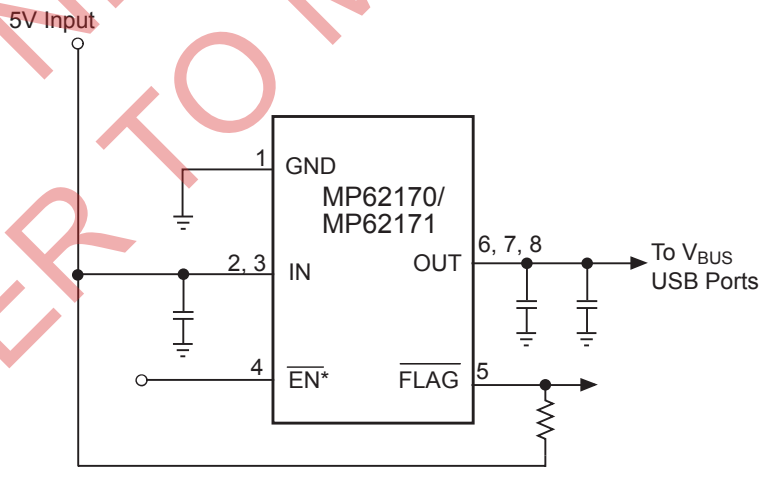
- 1.5A Continuous Current
- Accurate Current Limit
- 2.7V to 5.5V Supply Range
- 90uA Quiescent Current
- 75mΩ MOSFET
- Thermal-Shutdown Protection
- Under-Voltage Lockout
- 8ms FLAG Deglitch Time
- No FLAG Glitch During Power Up
- Reverse Current Blocking
- Active High & Active Low Options
- SOIC8 & MSOP8 Packages

APPLICATIONS

- Smartphone and PDA
- Portable GPS Device
- Notebook PC
- Set-top-box
- Telecom and Network Systems
- PC Card Hot Swap
- USB Power Distribution

"MPS" and "The Future of Analog IC Technology" are Trademarks of Monolithic Power Systems, Inc.

TYPICAL APPLICATION



* EN is active high for MP62171

SINGLE-CHANNEL

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP62550_MP62551

MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2010 MPS. All Rights Reserved.

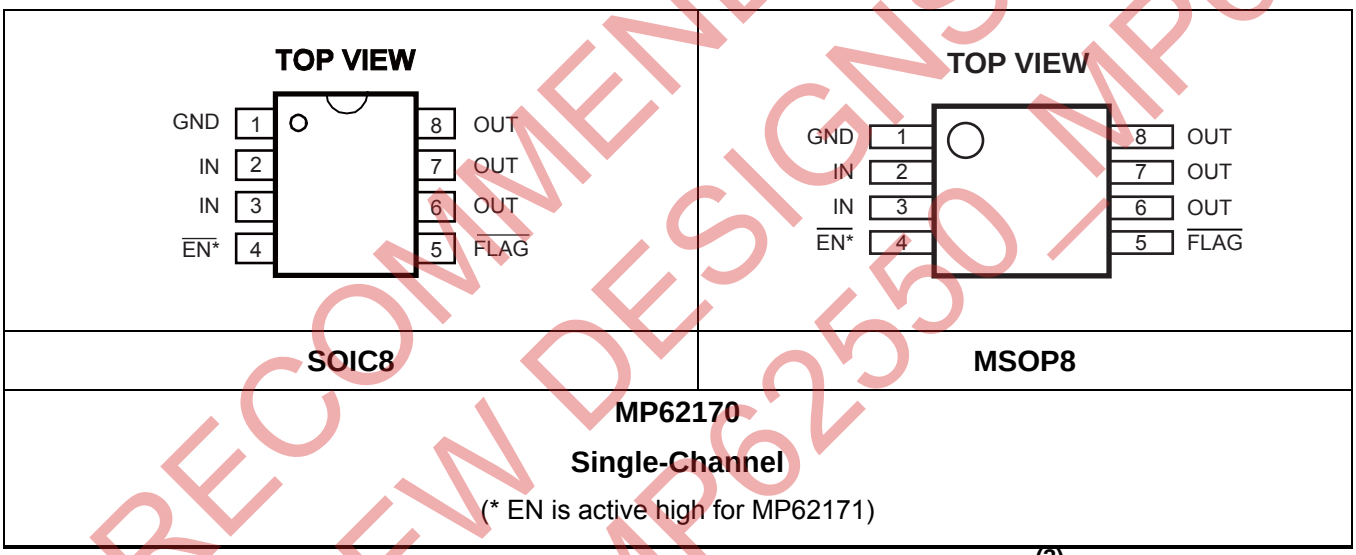
ORDERING INFORMATION

Part Number	Enable	Switch	Maximum Continuous Load Current	Typical Short-Circuit Current @ T_A=25C	Package	Top Marking	Free Air Temperature (T_A)
MP62170ES	Active Low	Single	1.5A	2.3A	SOIC8	62170ES	-20°C to +85°C
MP62170EK					MSOP8	62170EK	
MP62171ES	Active High				SOIC8	62171ES	
MP62171EK					MSOP8	62171EK	

* For Tape & Reel, add suffix –Z (g. MP62170ES–Z).

For RoHS compliant packaging, add suffix –LF (e.g. MP62171ES–LF–Z)

PACKAGE REFERENCE



SOIC8 | **MSOP8**

MP62170

Single-Channel

(* EN is active high for MP62171)

ABSOLUTE MAXIMUM RATINGS (1)

IN .....-0.3V to +6.0V
EN, FLAG, OUT to GND.....-0.3V to +6.0V
Continuous Power Dissipation (T_A = +25°C) (2)
SOIC8.....1.4W
MSOP8.....0.8W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature..... -65°C to +150°C
Operating Junct. Temp (T_J)..... -20°C to +125°C

Thermal Resistance (3)	θ_{JA}	θ_{JC}
SOIC8	90	42 °C/W
MSOP8	150	65 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Measured on JESD51-7，4-layer PCB.

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP62550 _MP62551

MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2010 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS (4)

V_{IN}=5V, T_A=+25°C, unless otherwise noted.

Parameter	Condition	Min	Typ	Max	Units
IN Voltage Range		2.7		5.5	V
Supply Current	EN Enabled, I_{OUT}=0		90	120	μA
Shutdown Current	Device Disable, V_{OUT}=float, V_{IN}=5.5V		1		μA
Off Switch Leakage	Device Disable, V_{IN}=5.5V		1		μA
Current Limit		1.6	2.3	3	A
Trip Current	Current Ramp (slew rate≤100A/s) on Output		2.5	3.3	A
Under-voltage Lockout	Rising Edge	1.95		2.65	V
Under-voltage Hysteresis			250		mV
FET On Resistance	I_{OUT}=100mA (-20°C≤T_A≤+85°C)		75	130	mΩ
EN Input Logic High Voltage		2			V
EN Input Logic Low Voltage				0.8	V
FLAG Output Logic Low Voltage	I_{SINK}=5mA			0.4	V
FLAG Output High Leakage Current	V_{IN}=V_{FLAG}=5.5V			1	μA
Thermal Shutdown			140		°C
Thermal Shutdown Hysteresis			20		°C
V_{OUT} Rising Time, Tr (5)	V_{IN}=5.5V, C_L=1uF, R_L=5.5Ω		0.9		ms
	V_{IN}=2.7V, C_L=1uF, R_L=5.5Ω		1.7		ms
V_{OUT} Falling Time, Tf (6)	V_{IN}=5.5V, C_L=1uF, R_L=5.5Ω			0.5	ms
	V_{IN}=2.7V, C_L=1uF, R_L=5.5Ω			0.5	ms
Turn On Time, Ton (7)	C_L=100μF, RL=5.5Ω			3	ms
Turn Off Time, Toff (8)	C_L=100μF, RL=5.5Ω			10	ms
FLAG Deglitch Time		4	8	15	ms
EN Input Leakage			1		μA
Reverse Leakage Current	V_{OUT} =5.5V, V_{IN} =GND		0.2		μA

Notes:

4) Production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.
5) Measured from 10% to 90% output signal.
6) Measured from 90% to 10% output signal.
7) Measured from 50% EN signal to 90% output signal.
8) Measured from 50% EN signal to 10% output signal.

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP62550 _ MP62551

MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2010 MPS. All Rights Reserved.

PIN FUNCTIONS

SOIC8 MSOP8	Name	Description
1	GND	Ground.
2, 3	IN	Input Voltage. Accepts 2.7V to 5.5V input.
4	$\overline{EN}$	Active High: (MP62171), Active Low: (MP62170).
5	$\overline{FLAG}$	IN-to-OUT Over-current, active-low output flag. Open-Drain.
6, 7, 8	OUT	IN-to-OUT Power-Distribution Output (for all 3 output pins)

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25ºC, unless otherwise noted.

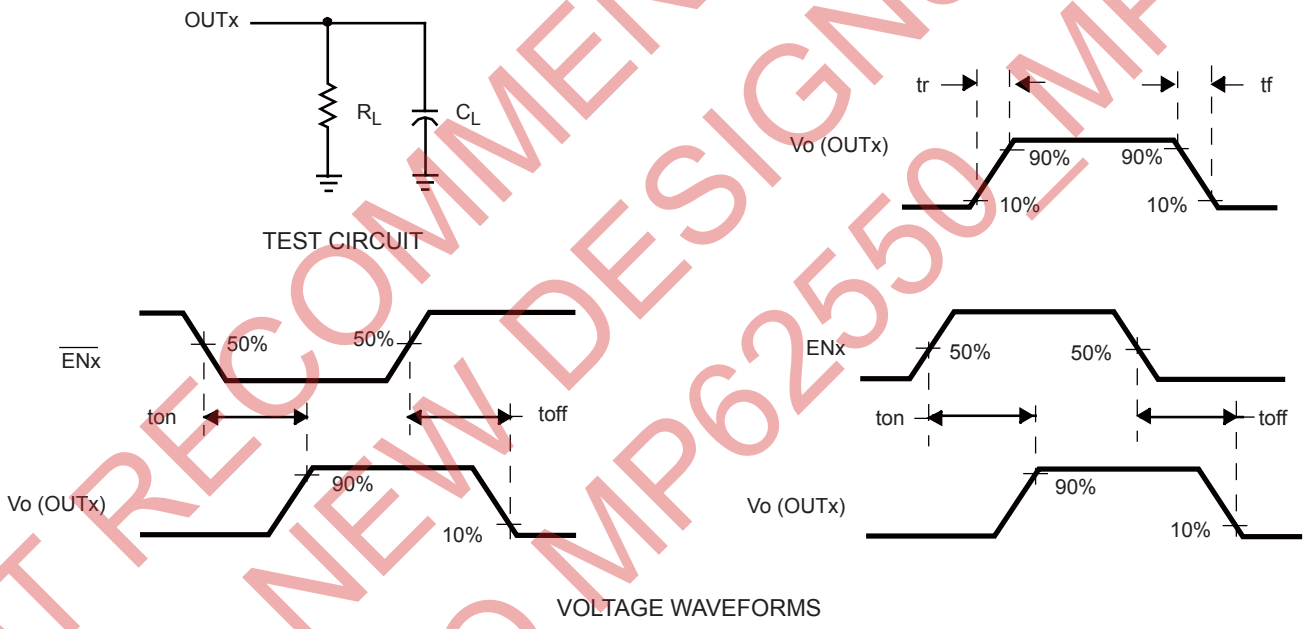


Figure 1—Test Circuit and Voltage Waveforms

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP62550_MP62551

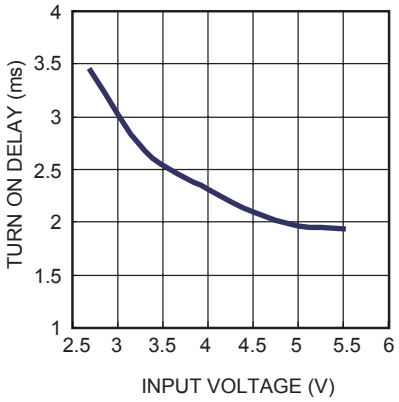
MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2010 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=5V, V_{EN}=0V, V_{CC}=5V, C_L=2.2μF, T_A=25°C, unless otherwise noted.

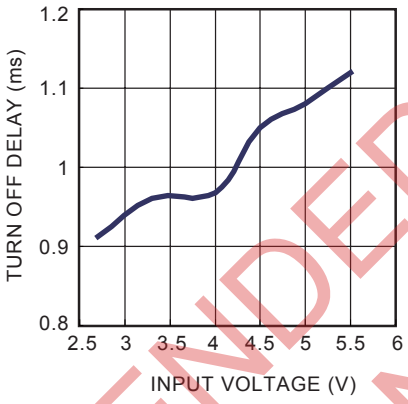
Turn on Delay vs. Input Votage

R_L=3.6Ω, C_L=100uF



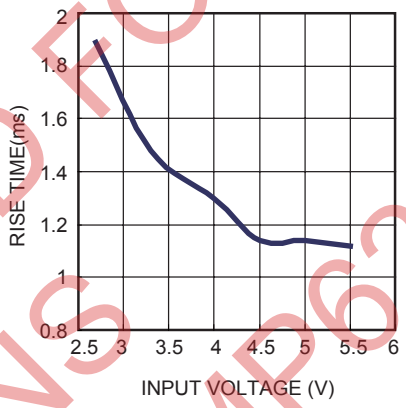
Turn off Delay vs. Input Votage

R_L=3.6Ω, C_L=100uF



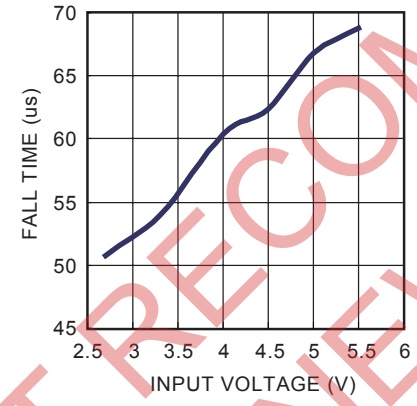
Rise Time vs. Input Votage

R_L=3.6Ω

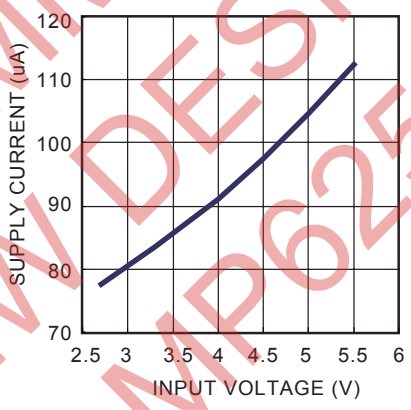


Fall Time vs. Input Votage

R_L=3.6Ω

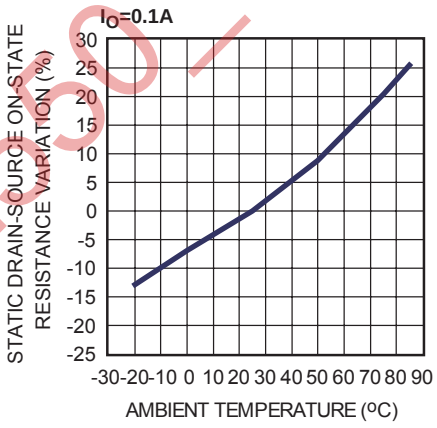


Supply Current, Output Enabled vs.Input Voltage



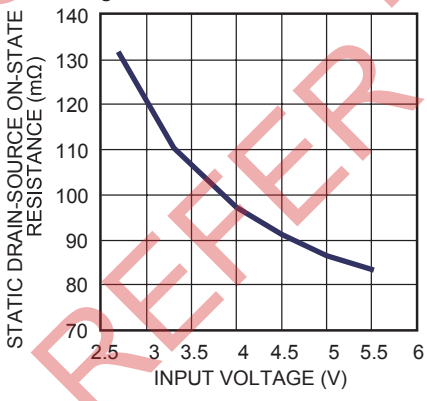
Static Drain-Source On-State Resistance Variation vs. Ambient Temperature

I_O=0.1A

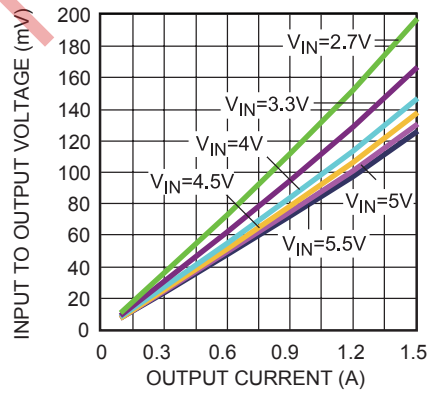


Static Drain-Source On-State Resistance vs. Input Voltage

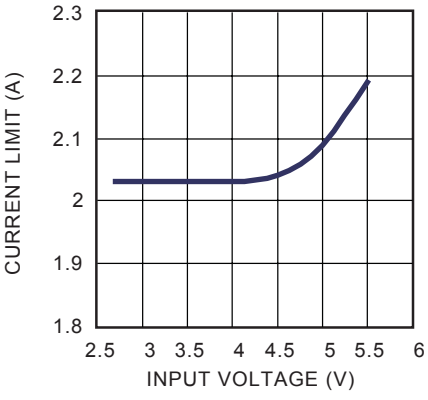
I_O=1.5A



Input to Output Voltage vs. Load Current



Current Limit vs. Input Voltage



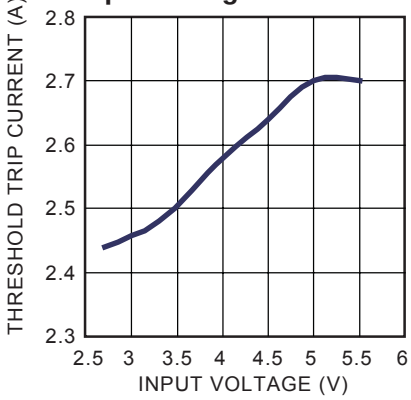
NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP62550 – MP62551

MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2010 MPS. All Rights Reserved.

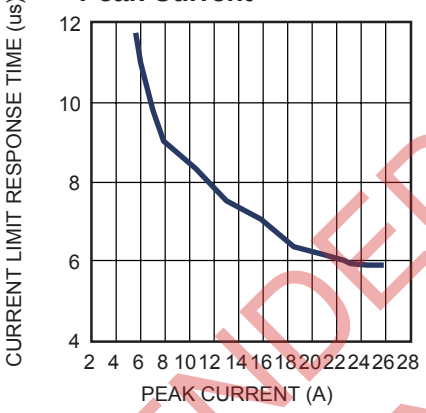
TYPICAL PERFORMANCE CHARACTERISTICS *(CONTINUED)*

V_{IN}=5V, V_{EN}=0V, V_{CC}=5V, C_L=2.2µF, T_A=25°C, unless otherwise noted.

Threshold Trip Current vs. Input Voltage

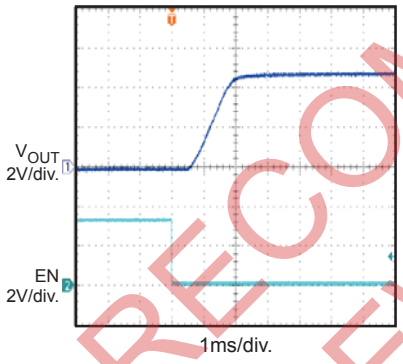


Current Limit Response vs. Peak Current



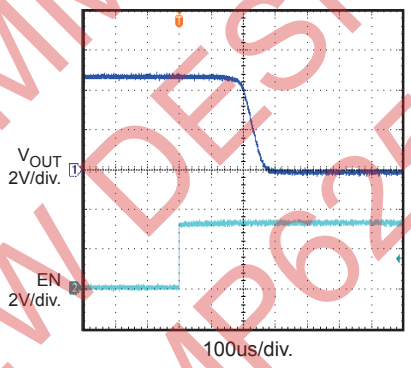
Turn On Delay and Rise Time with 2.2uF Load

R_L=3.3Ω



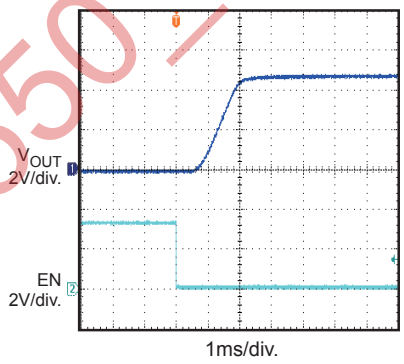
Turn Off Delay and Fall Time with 2.2uF Load

R_L=3.3Ω



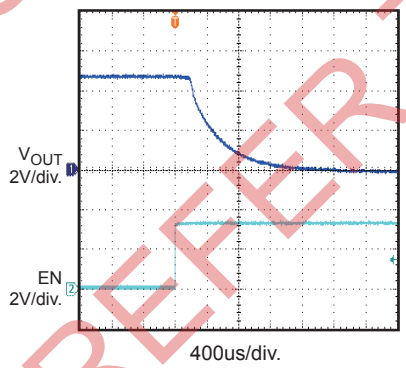
Turn On Delay and Rise Time with 100uF Load

C_L=100uF, R_L=3.3Ω

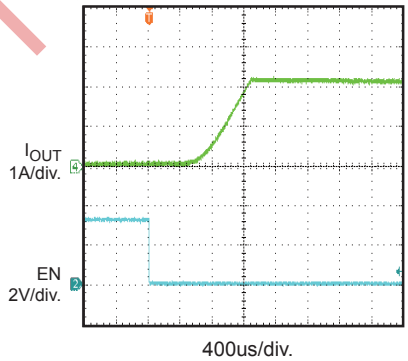


Turn Off Delay and Fall Time with 100uF Load

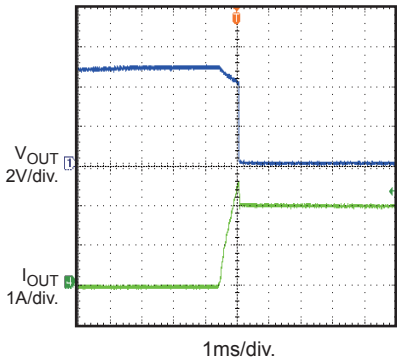
C_L=100uF, R_L=3.3Ω



Short Circuit Current, Device Enabled into Short



Threshold Trip Current with Ramped Load on Enabled Device



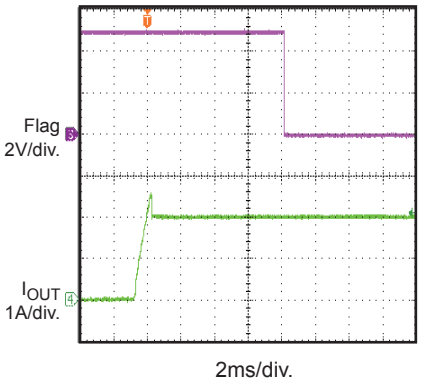
NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP62550 – MP62551

MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2010 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(CONTINUED)*

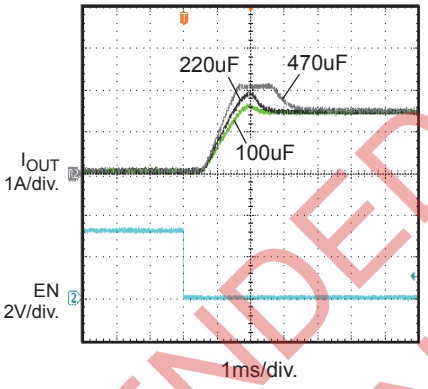
V_{IN}=5V, V_{EN}=0V, V_{CC}=5V, C_L=2.2µF, T_A=25°C, unless otherwise noted.

Ramped Load on Enabled Device

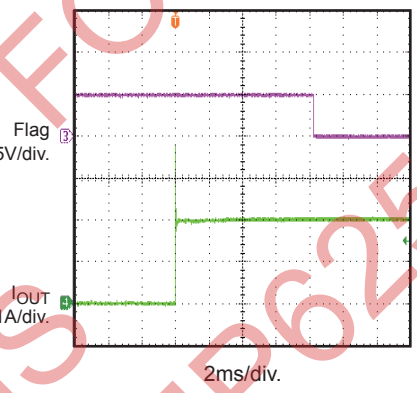


Inrush Current with Different Load Capacitance

I_{OUT} =1.5A



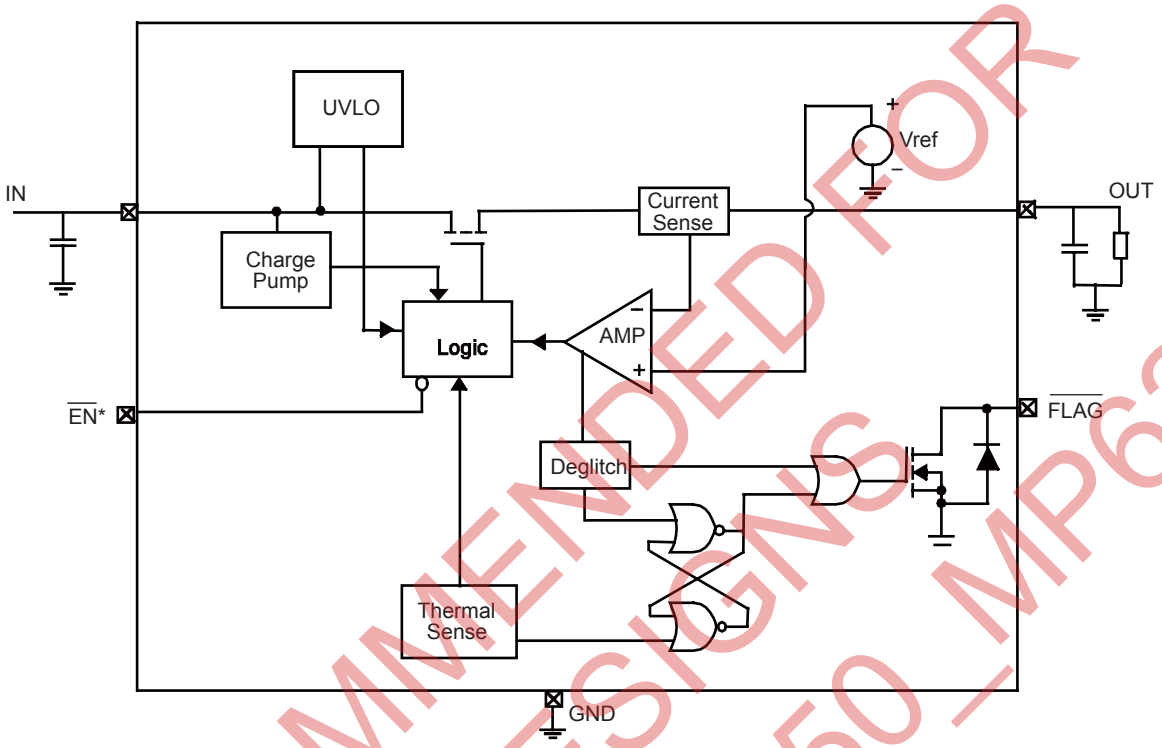
1Ω Load Connected to Enabled Device



NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP62550 _ MP62551

MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2010 MPS. All Rights Reserved.

FUNCTION BLOCK DIAGRAM



* EN is active high for MP62171

Figure 2—Functional Block Diagram

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP62550 _MP62551

MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2010 MPS. All Rights Reserved.

DETAILED DESCRIPTION

Over Current

When the load exceeds trip current (minimum threshold current triggering constant-current mode) or a short is present, MP62170/MP62171 switches into to a constant-current mode (current limit value). MP62170/MP62171 will be shutdown only if the over current condition stays long enough to trigger thermal protection.

Trigger over current protection for different overload conditions occurring in applications:

1) The output has been shorted or overloaded before the device is enabled or input applied. MP62170/MP62171 detects the short or overload and immediately switches into a constant-current mode.
2) A short or an overload occurs after the device is enabled. After the current-limit circuit has been tripped (reached the trip current threshold), the device switches into constant-current mode. However, high current may flow for a short period of time before the current-limit circuit can react.
3) Output current has been gradually increased beyond the recommended operating current. The load current rises until the trip current threshold is reached or until the thermal limit of the device is exceeded. The MP62170/MP62171 is capable of delivering current up to the trip current threshold without damaging the device. Once the trip threshold has been reached, the device switches into its constant-current mode.

Flag Response

The FLAG pin is an open drain configuration. This FAULT will report a fail mode after 8ms deglitch timeout. This is used to ensure that no false fault signals are reported. This internal deglitch circuit eliminates the need for extend components. The FLAG pin is not deglitched during over temperature of voltage lockout.

Thermal Protection

The purpose of thermal protection is to prevent damage in the IC by allowing exceptive current to flow and heating the junction. The die temperature is internally monitored until the thermal limit is reached. Once this temperature is reached, the switch will turn off and allow the chip to cool. The switch has a built-in hysteresis.

Under-voltage Lockout (UVLO)

This circuit is used to monitor the input voltage to ensure that the MP62170/MP62171 is operating correctly. This UVLO circuit also ensures that there is no operation until the input voltage reaches the minimum spec.

Enable

The logic pin disables the chip to reduce the supply current. The device will operate once the enable signal reaches the appropriate level. The input is compatible with both COMS and TTL.

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP62550_MP62551

MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2010 MPS. All Rights Reserved.

APPLICATION INFORMATION

Power-Supply Considerations

Over 10µF capacitor between IN and GND is recommended. This precaution reduces power-supply transients that may cause ringing on the input and improves the immunity of the device to short-circuit transients.

In order to achieve smaller output load transient, placing a high-value electrolytic capacitor on the output pin(s) is recommended when the output load is heavy.

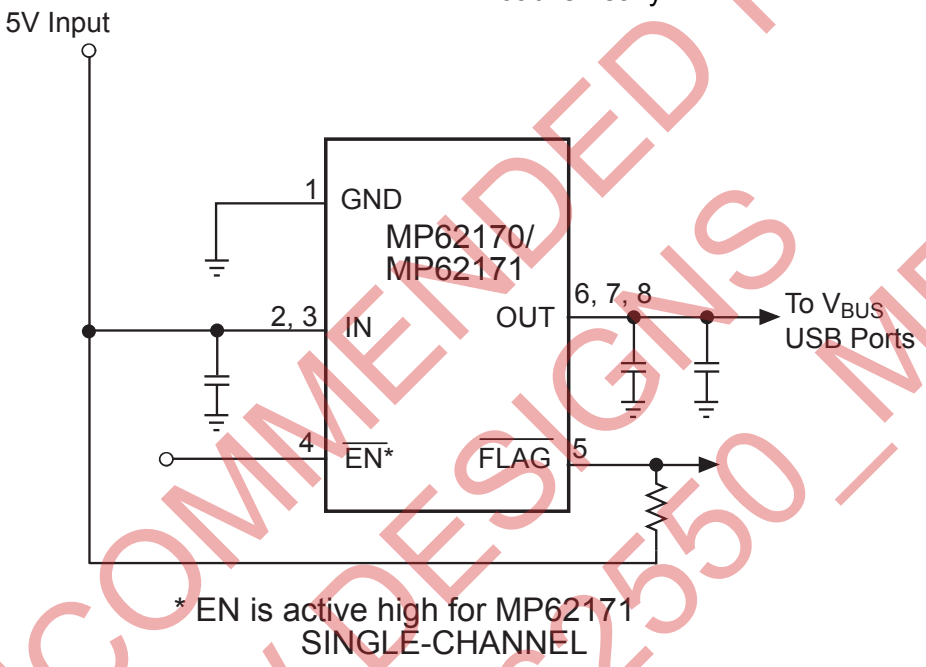


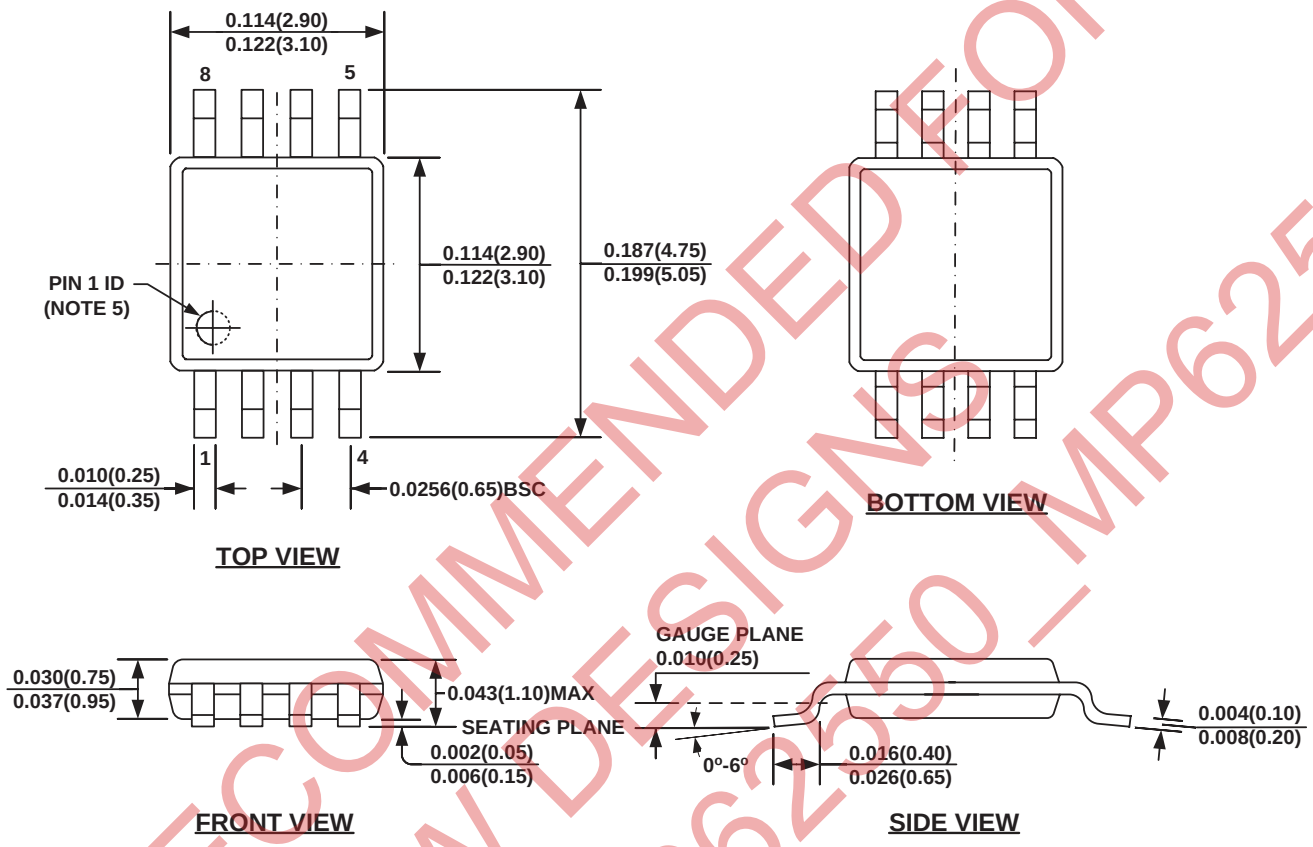
Figure 3—Application Circuit

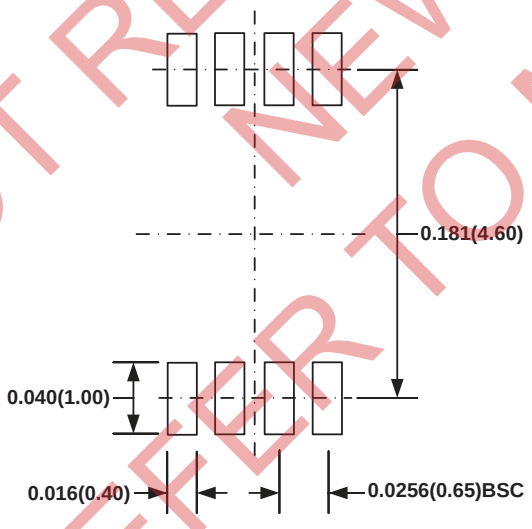
NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP62550 _ MP62551

MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2010 MPS. All Rights Reserved.

PACKAGE INFORMATION

MSOP8





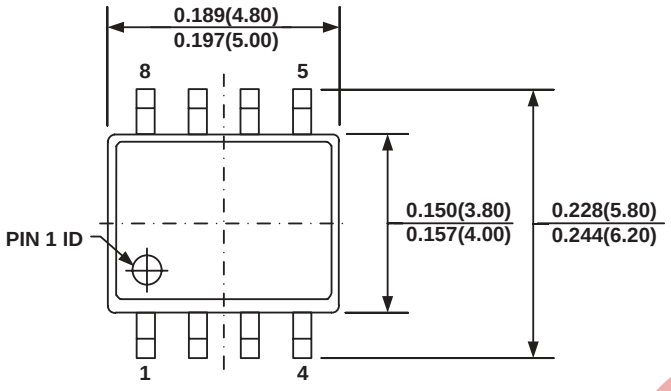
NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) PIN 1 IDENTIFICATION HAS HALF OR FULL CIRCLE OPTION.
6) DRAWING MEETS JEDEC MO-187, VARIATION AA.
7) DRAWING IS NOT TO SCALE.

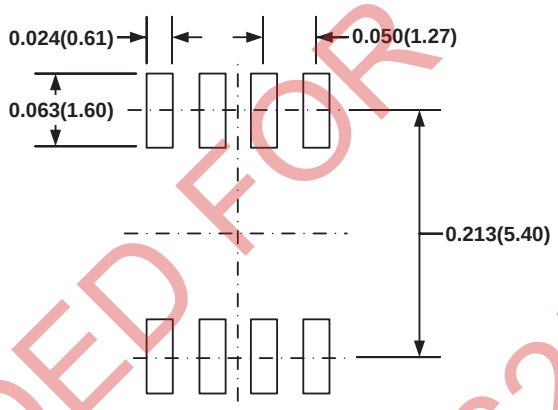
NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP62550_MP62551

MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2010 MPS. All Rights Reserved.

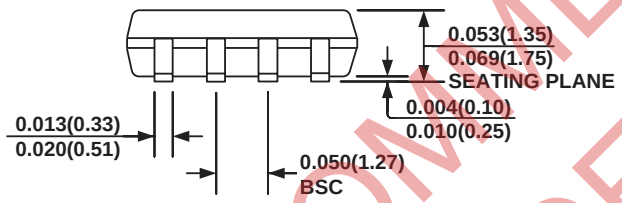
SOIC8



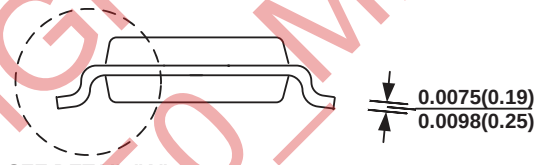
TOP VIEW



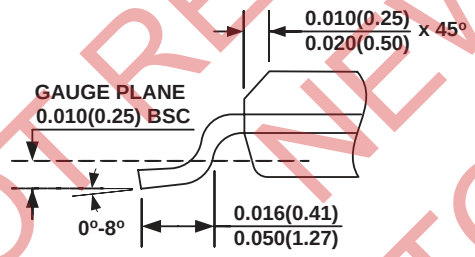
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

NOT RECOMMENDED FOR NEW DESIGNS REFER TO MP62550_MP62551

NOTICE: The information in this document is subject to change without notice. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2010 MPS. All Rights Reserved.