MP6003

Monolithic Flyback/SEPIC DC-DC Converter

The Future of Analog IC Technology

DESCRIPTION

The MP6003 is a monolithic flyback DC-DC converter which includes a 150V power switch and is capable of delivering up to 15W output power. It can also be used for SEPIC boost and Flyback and Forward applications.

The MP6003 uses the fixed-frequency peak current mode primary controller architecture. It has an internal soft-start, auto-retry, and incorporates over current, short circuit, and over-voltage protection. The MP6003 can also skip cycles to maintain zero load regulation.

It has a direct optocoupler interface which bypasses the internal error amplifier when an isolated output is desired.

The MP6003 is ideal for telecom applications, and is available in a compact, thermally enhanced SOIC8 package with an exposed pad.

FEATURES

- Integrated 0.9Ω 150V Power Switch
- Cycle-by-Cycle Current Limiting
- Programmable Switching Frequency
- Duty Cycle Limiting with Line Feed Forward
- Integrated 100V Startup Circuit
- Internal Slope Compensation
- Disable Function
- Built-in Soft-Start
- Line Under Voltage Lockout
- Line Over Voltage Protection
- Auto-Restart for Opened/Shorted Output
- Zero Load Regulation
- Thermal Shutdown

APPLICATIONS

- Telecom Equipment
- VoIP Phones, Power over Ethernet (PoE)
- Distributed Power Conversion

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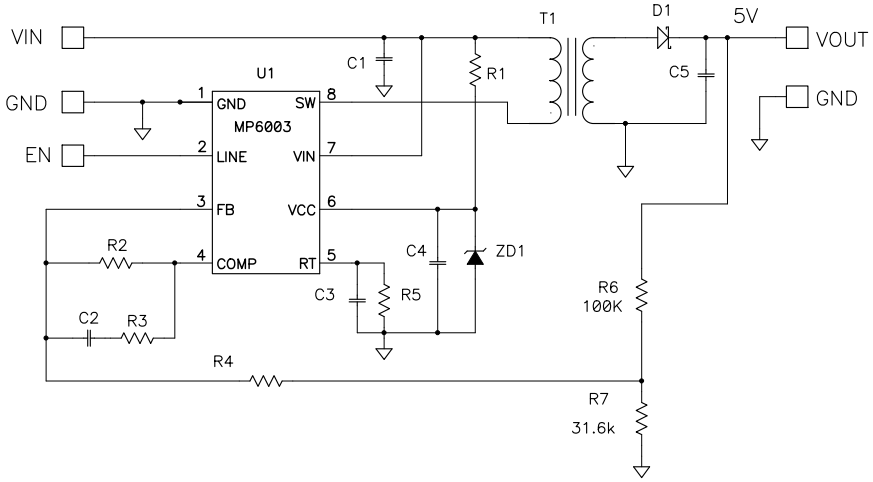
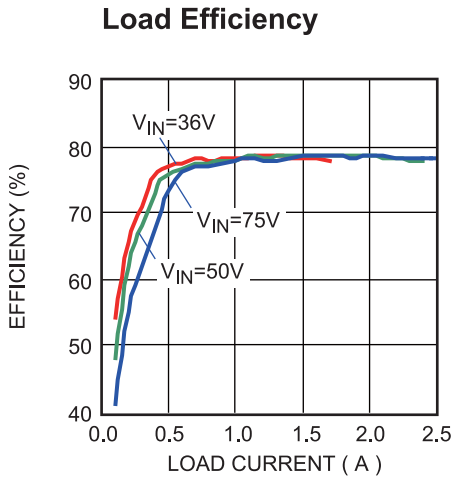
TYPICAL APPLICATION





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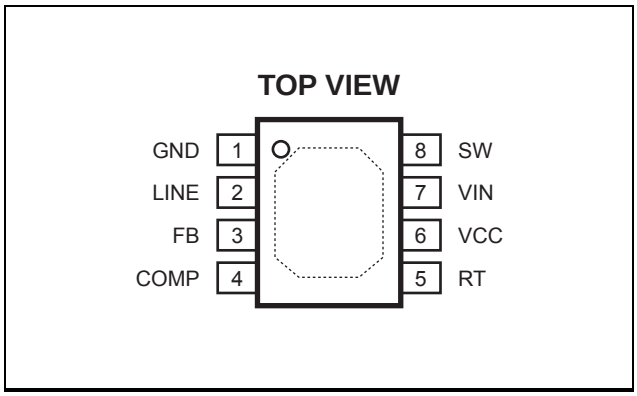
ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature (T_A)
MP6003DN	SOIC8E	MP6003	-40°C to +85°C

* For Tape & Reel, add suffix –Z (eg. MP6003DN–Z).
For RoHS compliant packaging, add suffix –LF (eg. MP6003DN–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

V_{SW} .....-0.5V to +180V
V_{IN} .....-0.3V to +120V
All Other Pins .....-0.3V to +6.5V
Continuous Power Dissipation… (T_A = +25°C) (2)
……..2.5W
Junction Temperature .....150°C
Lead Temperature .....260°C
Storage Temperature..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{CC} .....4.5 V to 6V
Output Voltage V_{SW} .....-0.5V to +150V
Input Voltage V_{IN} .....+10V to +100V
Maximum Junction Temp. (T_J).....+125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

SOIC8E ..... 50 ..... 10... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7 4-layer board.

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ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V, V_{LINE} = 1.8V, RT = 10k, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Quiescent Supply Current	I_{CC}	1.2V < V_{LINE} < 3.2V, V_{FB} = 1.3V		1.0	1.5	mA
Line OV Threshold Voltage		V_{CC} = 5.0V	2.85	3	3.15	V
Line OV Hysteresis		V_{CC} = 5.0V		300		mV
Line UV Threshold Voltage		V_{CC} = 5.0V	1.16	1.21	1.26	V
Line UV Hysteresis		V_{CC} = 5.0V		100		mV
V_{CC} Upper Threshold Voltage			5.7	6.0	6.3	V
V_{CC} Lower Threshold Voltage			4.30	4.50	4.70	V
V_{CC} Over Voltage Threshold Voltage			6.3	6.6	6.9	V
Feedback Voltage	V_{FB}		1.16	1.21	1.26	V
Feedback Input Current	I_{FB}	V_{FB} = 1.2V		50		nA
Error Amplifier Gain Bandwidth (5)	GBW		1			MHz
Error Amplifier DC Gain (5)	A_V		60			dB
Comp Output Source Current	I_{OH}	V_{FB} = 1.0V, V_{COMP} = 0.5V		6.5		mA
Comp Output Sink Current	I_{OL}	V_{FB} = 1.4V, V_{COMP} = 2.5V		3.3		mA
Switch-On Resistance	R_{ON}	V_{SW} = 0.1V		0.9		Ω
Switch Leakage Current	I_{LK}	V_{SW} = 180V			1	μA
Minimum Oscillating Frequency	F_{MIN}	RT = 100k		60		kHz
Maximum Oscillating Frequency	F_{MAX}	RT = 10k		550		kHz
Thermal Shutdown (5)				150		°C
Thermal Shutdown Hysteresis (5)				30		°C
Current Limit (5)	I_{LIM}		550	700		mA
Startup Current	I_{st}	V_{IN} = 20V, V_{CC} = 4.0V		6.5		mA

Note:

5) Guaranteed by design, not production tested.

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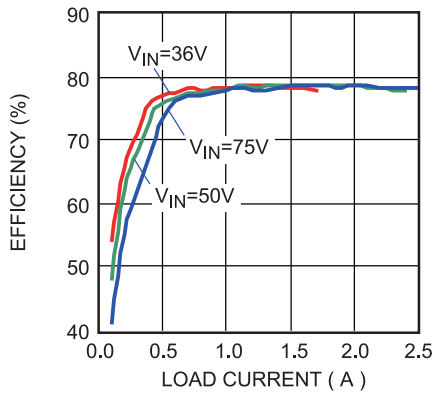
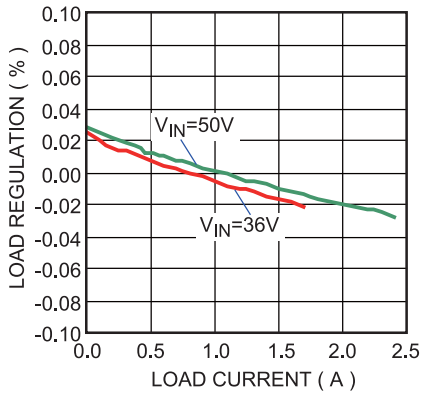
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 36V, V_{OUT} = 5V, I_{OUT} = 1A, T_A = 25ºC, unless otherwise noted.

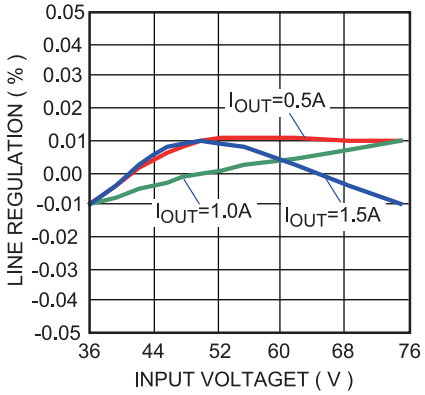
Load Efficiency



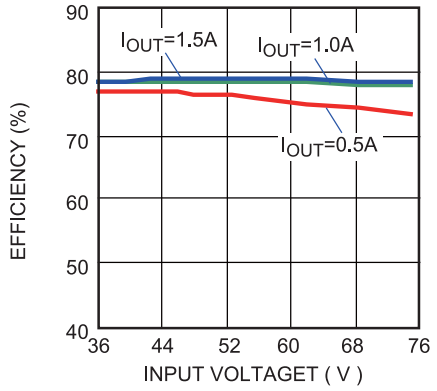
Load Regulation



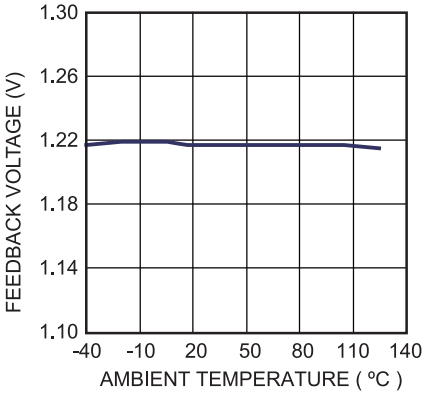
Line Regulation



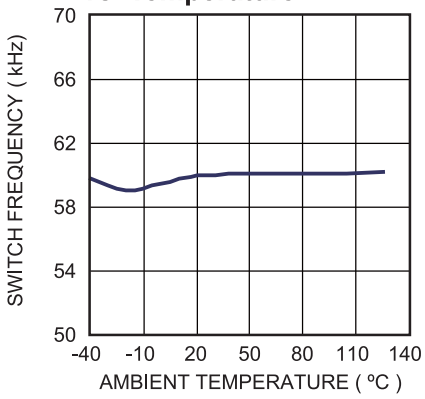
Line Efficiency



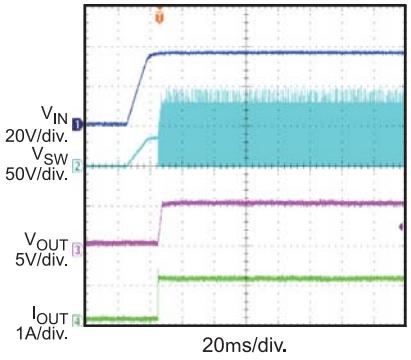
V_{FB} vs. Temperature



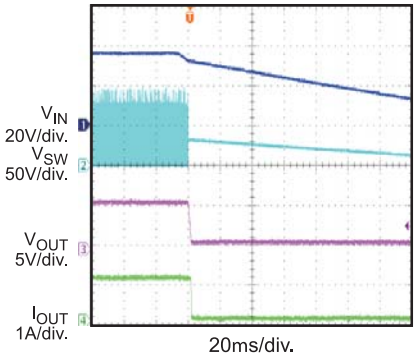
Switch Frequency vs. Temperature



Power Ramp Up

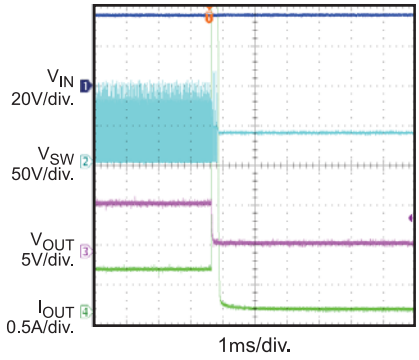


Power Ramp Down



Short Output Protection

I_{OUT} = 0.5A



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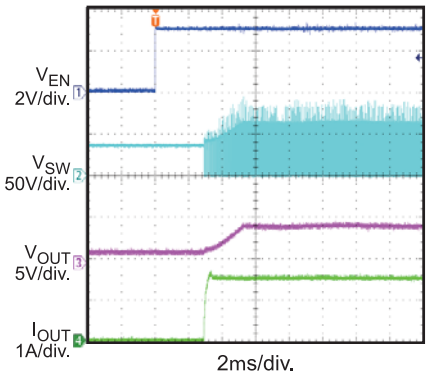
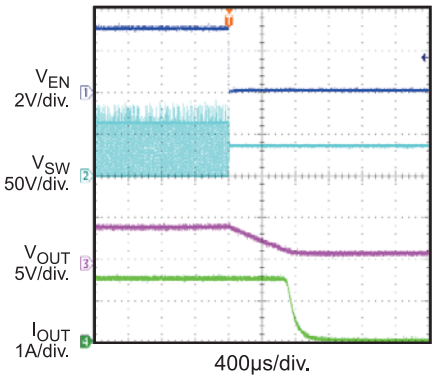
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 36V, V_{OUT} = 5V, I_{OUT} = 1A, T_A = 25ºC, unless otherwise noted.

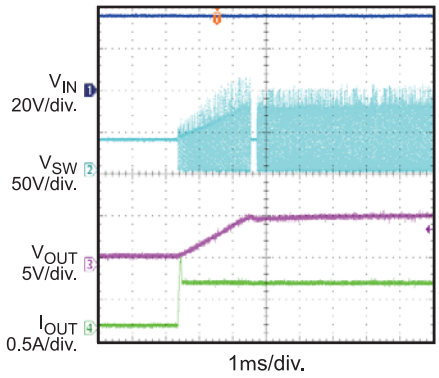
Enable Start Up
I_{OUT}=1.5A



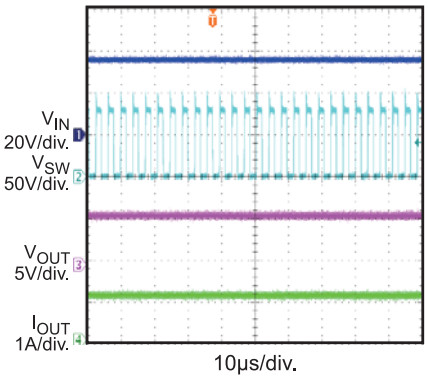
Enable Start Down
I_{OUT}=1.5A



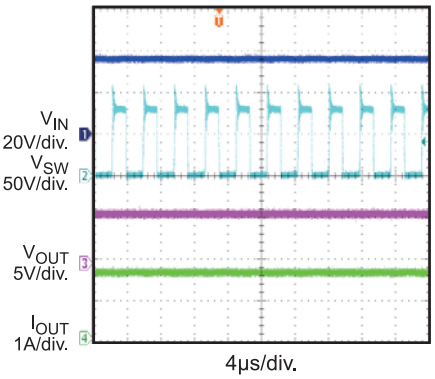
Short Output Recovery
I_{OUT} = 0.5A



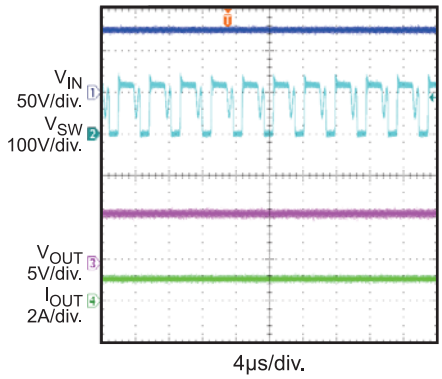
Steady State



Steady State
I_{OUT}=1.5A



Steady State
V_{IN} = 75V



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PIN FUNCTIONS

Pin #	Name	Description
1	GND	Ground. Power return and reference node.
2	LINE	UV/OV Set Point. Short to ground to turn the controller off.
3	FB	Regulation Feedback Input. Inverting input of the error amplifier. The non-inverting is internally connected to 1.2V
4	COMP	Error Amplifier Output.
5	RT	Oscillator Resistor and Synchronous Clock Pin. Connect an external resistor to GND for oscillator frequency setting. It can be used as a synchronous input from external oscillator clock.
6	VCC	Supply Bias Voltage. A capacitor no less than 1uF is recommended to connect between GND.
7	VIN	High Voltage Startup Circuit Supply.
8	SW	Output Switching Node. High voltage power N-Channel MOSFET drain output. The internal start bias current is supplied from this pin.

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OPERATION

The MP6003 uses programmable fixed-frequency, peak current-mode PWM with a single-ended primary architecture to regulate the output voltage. The MP6003 incorporates features such as protection circuitry and an integrated high voltage power switch into a small 8-pin SOIC. This product targets high performance, cost effective DC-DC converter applications.

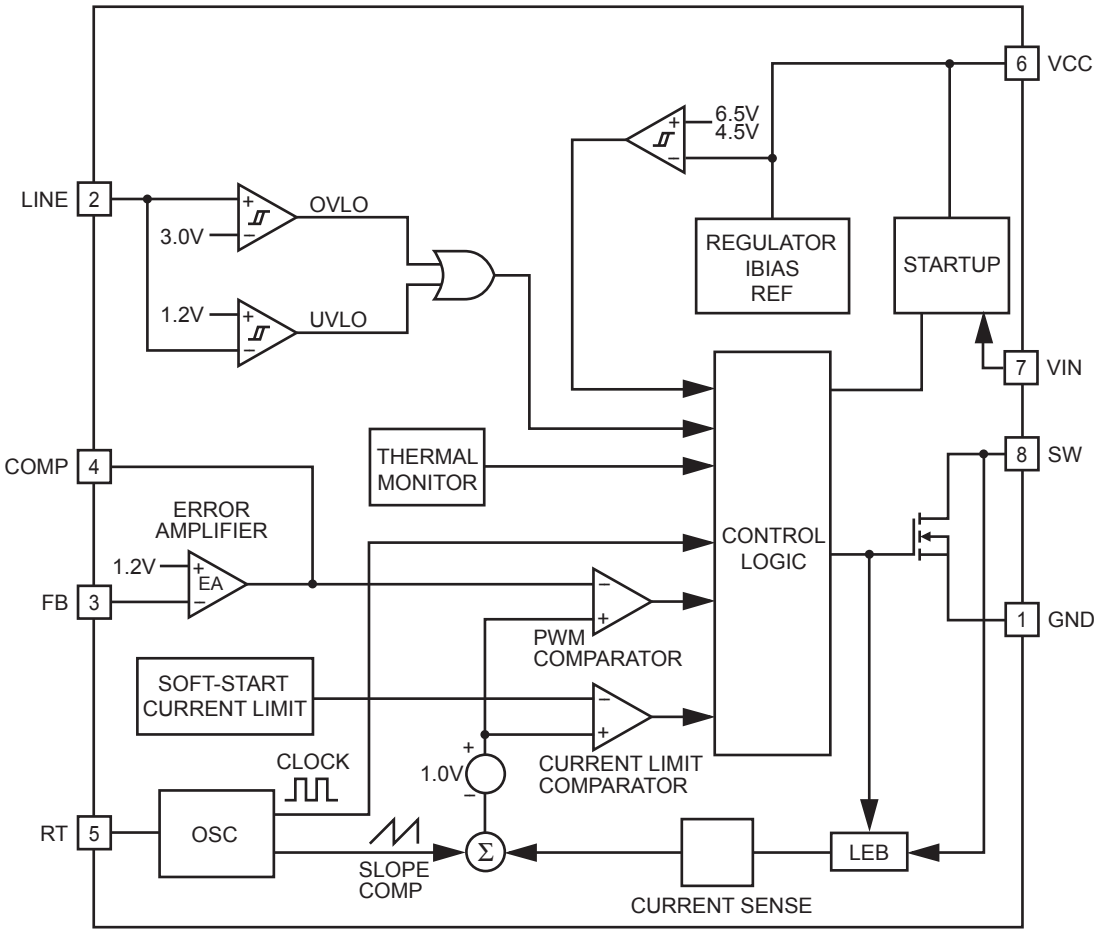

Figure 1—Functional Block Diagram

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High Voltage Startup

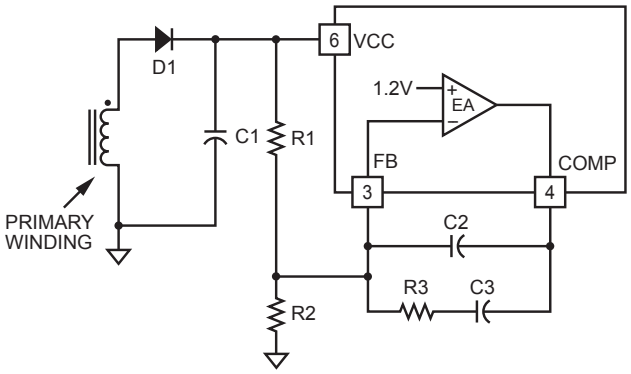
The MP6003 features a 100V startup circuit, see Figure 1. When power is applied, the capacitor at the VCC pin is charged through the VIN pin. When the voltage at the VCC pin crosses 6.0V without fault, the controller is enabled. The VCC pin is then disconnected from the VIN pin and V_{CC} voltage is discharged via the operating current. When V_{CC} drops to 4.5V, the VCC pin is reconnected to the VIN pin and V_{CC} will be recharged. The voltage at the VCC pin repeats this ramp cycle between 4.5V and 6.0V. VIN needs to be higher than 10V in order to keep high voltage startup circuit working properly. This can be guaranteed by setting input UVLO $\geqslant$ 10V. It is also recommended that the capacitor at VCC pin be no less than 1uF to achieve stable operation. The VCC pin can be powered with a voltage higher than 4.5V from an auxiliary winding to reduce the power dissipated in the internal start-up circuit. The VCC pin is internally clamped at 8V.

Under-Voltage and Over-Voltage Detection

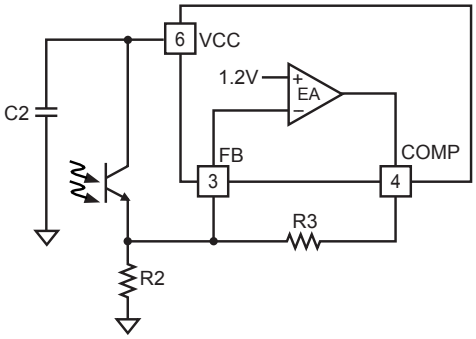
The MP6003 includes a line monitor circuit. Two external resistors form a voltage divider from the input voltage to GND; its tap connects to the LINE pin. The controller is operational when the voltage at the UV/OV pin is between 1.2V and 3V. When the voltage at the UV/OV pin goes out of this operating range, the controller is disabled and goes into standby mode. The LINE pin can also be used as a remote enable. Grounding the UV/OV pin will disable the controller.

Error Amplifier

The MP6003 includes an error amplifier with its non-inverting input connected to internal 1.2V reference voltage. The regulated voltage is fed back through a resistor network or an optocoupler to the FB pin. Figure 2 shows some common error amplifier configurations.



(a) Using Primary winding to provide feedback



(b) Feedback is from Secondary (Common Collector)

Figure 2—Error Amplifier Configurations

Synchronize Programmable Oscillator

The MP6003 oscillating frequency is set by an external resistor from the RT pin to ground. The value of RT can be calculated from:

$$RT = 10k\Omega \times \frac{550kHz}{f_S}$$

The MP6003 can be synchronized to an external clock pulse. The frequency of the clock pulse must be higher than the internal oscillator frequency. The clock pulse width should be within 50ns to 150ns. The external clock can be coupled to the RT pin with a 100pF capacitor and a peak level greater than 3.5V.

Duty Cycle Limiting with Line Feed Forward

The MP6003 has a D_{MAX} (maximum duty cycle) limit at 67.5% when the LINE pin voltage is equal to 1.3V. As V_{LINE} increases, D_{MAX} reduces. Maximum duty cycle can be calculated by:

$$D_{MAX} = \left[\frac{2.7V}{2.7V + V_{LINE}}\right] \times 100\%$$

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Limiting the duty cycle at high line voltage protects against magnetic saturation and minimizes the output sensitivity to line transients.

Auto-Restart

When V_{CC} is biased from an auxiliary winding and an open loop condition occurs, the voltage at the VCC pin increases to 6.5V. When V_{CC} crosses the threshold voltage, the auto-restart circuit turns off the power switch and puts the controller in standby mode. When V_{CC} drops to 4.5V, the startup switch turns on to charge V_{CC} up again. When V_{CC} crosses 6.0V, the switch turns off and the standby current discharges V_{CC} back to 4.5V. After repeating the ramp cycles between the two threshold voltages 15 times, the auto-restart circuit is disabled and the controller begins soft-start.

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APPLICATION INFORMATION

Switching Frequency

The frequency (f_S), has big effects on the selection of the transformer (Tr), the output cap, (C2), and the input cap, (C1). The higher the frequency, the smaller the sizes for Tr, C2, and C1. However, a higher frequency also leads to higher AC power losses in the power switch, control circuitry, transformer, and in the external interconnection. The general rule states that lower the output power, higher the optimum switching frequency. For low current (<10A) applications, f_S is usually 200kHz to 300kHz if synchronous rectifiers are used and 300KHz to 500kHz if Schottky rectifiers are used.

Fundamental Equations

The transformer turns ratio N is defined as:

$$N = \frac{N_P}{N_S}$$

Where N_P and N_S are the number of turns of the primary and secondary side windings, respectively.

The output voltage V_O is estimated to be:

$$V_O = \frac{D}{1-D} \times \frac{V_{IN}}{N}$$

Where D is the duty cycle.

The steady-state drain to source voltage of the primary power switch when it is off is estimated as:

$$V_{DS} = V_{IN} + N \times V_O$$

The steady-state reverse voltage of the Schottky diode D2 is estimated as:

$$V_{D2} = V_O + \frac{V_{IN}}{N}$$

The output current is calculated as:

$$I_O = I_D \times (1-D)$$

Where I_D is the average current through Schottky diode when it is conducting.

The input current is calculated as:

$$I_{IN} = I_S \times D$$

Where I_S is the average current through the primary power switch when it is conducting.

Transformer (Coupled Inductor) Design

1. Transformer Turns Ratio

The transformer turns ratio determines the duty cycle range, selection of the rectifier (D2), primary side peak current, primary snubber loss, and the current as well as voltage stresses on the power switch (S). It also has effects on the selection of C1 and C2. A higher transformer turns ratio (N) means the following:

- Higher Duty Cycle
- Higher voltage stress on S (V_{DS}), but lower voltage stress on D2 (V_{D2}).
- Lower primary side RMS current ($I_{S(RMS)}$), but higher secondary side RMS current ($I_{D2(RMS)}$).
- Use of a smaller input capacitor but bigger output capacitor.
- Lower primary side peak current ($I_{S(PEAK)}$) and lower primary snubber loss.
- Lower main switch (S) turn-on loss

For a 5V power supply design, with V_{IN}=36V~75V, below table shows the voltage stresses of the power switch (S) and the rectifier (D2).

Table 1—Main Switch (S) and Rectifier (D2) Voltage Stress vs. Transformer Turns Ratio

N	D_{MAX}	V_{DS} (V)	V_{DS}/0.9 (V)	V_{D2} (V)	V_{D2}/0.9 (V)
4	0.36	119	132	38	42
5	0.41	125	139	32	36
6	0.45	131	146	28	31
7	0.49	138	153	25	28
8	0.53	144	160	23	26
9	0.56	150	167	21	24
10	0.58	156	174	20	22
11	0.60	163	181	19	21

Note:
The voltage spike due to the leakage inductance of the transformer and device's voltage rating/derating factors were considered. See power switch selection and snubber design for more information.

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2. Ripple Factor of the Magnetizing Current

The conduction loss in S, D2, the transformer, the snubber, and in the ESR of the input/output capacitors will increase as the ripple of the magnetizing current increases. The ripple factor (K_r) is defined as the ratio of the peak-to-peak ripple current vs. the average current as shown in Figure 3.

$$K_r = \frac{\Delta I_M}{I_M}$$

Where I_M can be derived either from input or output current;

$$\overline{I_M} = \frac{I_{IN}}{D} = \frac{I_0}{N \times (1-D)}$$

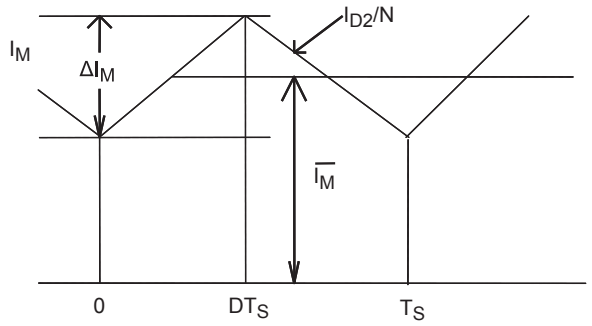

Figure 3—Magnetic Current of Flyback Transformer (Reflected to Primary Side)

The input/output ripple voltage will also increase with a high ripple factor, which makes the filter bigger and more expensive. On the other hand, it can help to minimize the turn-on loss of S and reverse-recovery loss due to D2. With nominal input voltage, K_r can be selected at 60%~120% for most DC-DC converters.

The primary side (or magnetizing) inductance can be determined by:

$$L_F = \frac{V_{IN} \times D \times T_S}{K_r \times \overline{I_M}}$$

3. Core Selection

Pick a core based on experience or through a catalog (Refer to http://www.ferroxcube.com).

Select an ER, EQ, PQ, or RM core to minimize the transformer's leakage inductance.

4. Winding Selection

Solid wire, Litz wire, PCB winding, Flex PCB winding or any combination thereof can be used as transformer winding. For low current applications, solid wire is the most cost effective choice. Consider using several wires in parallel and interleaving the winding structure for better performance of the transformer.

The number of primary turns can be determined by:

$$N_P = \frac{L_F \times I_P}{B_{MAX} \times A_E}$$

Where B_{MAX} is the allowed maximum flux density (usually below 300mT) and A_E is the effective area of the core.

The air gap can be estimated by:

$$Gap = \frac{\mu_o \times N^2 \times A_E}{L_F}$$

5. Right Half Plane Zero

A Flyback converter operating in continuous mode has a right half plane (RHP) zero. In the frequency domain, this RHP zero adds not only a phase lag to the control characteristics but also increases the gain of the circuit. Typical rule of thumb states that the highest usable loop crossover frequency is limited to one third the value of the RHP zero. The expression for the location of the RHP zero in a continuous mode flyback is given by:

$$f_{RHPZ} = R_{LOAD} \times \frac{(1-D)^2}{2\pi \times L_F \times D} \times N^2$$

Where R_{LOAD} is the load resistance, L_F is the magnetizing inductance on transformer primary side, and N is the transformer's turn ratio.

Reducing the primary inductance increases the RHP zero frequency which results in higher crossover frequencies.

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Duty Cycle Range

The duty cycle range is determined once N is selected. In general, the optimum operating duty cycle should be smaller for high input/low output than low input/high output applications. Except for high output voltage or wide input range applications, the maximum D usually does not exceed 60%.

Voltage Stress of the Internal Power Switch & External Schottky Diode

For the internal power switch, the voltage stress is given by:

$$V_{DS} = V_{IN} + V_O \times N + V_P$$

Where V_P is a function of L_{LK} (leakage inductrance), f_S, R, C, C_{DS}, V_{IN}, I_O, etc. Please refer to Figure 4. The lower the L_{LK} and Io, the lower the Vp. Smaller R can reduce Vp, but power loss will increase. See Snubber Design for details.

Typically V_P can be selected as 20~40% of (V_{IN}+NV_O).

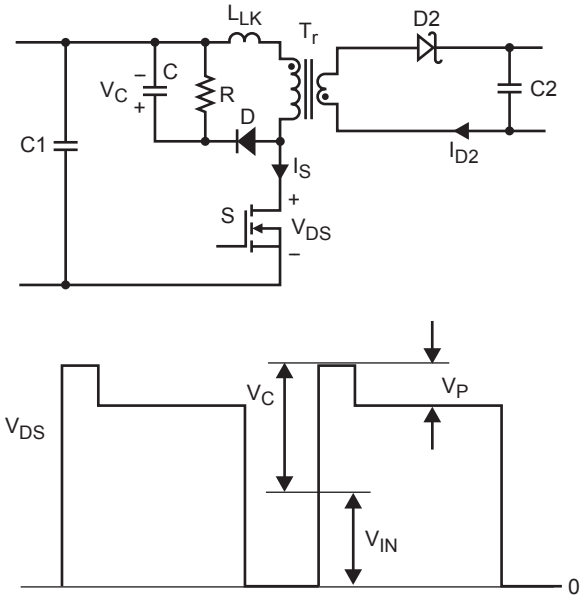

Figure 4—Key Operation Waveform

For the rectifier, D2, the voltage stress is given by:

$$V_{D2} = V_O + \frac{V_{IN}}{N} + V_{PD2}$$

Use of a R-C or R-C-D type snubber circuit for D2 is recommended.

V_{PD2} can be selected as 40~100% of (V_O+V_{IN}/N), thus:

$$V_{DS(MAX)} = K_s \times (V_{IN(MAX)} + NV_0)$$

Where K_S=1.2~1.4, and

$$V_{D2(MAX)} = K_{D2} \cdot (V_0 + \frac{V_{IN(MAX)}}{N})$$

Where K_{D2}=1.4~2.

For example,

$V_{IN(MAX)} = 75V, N = 8, K_S = 1.25, K_{D2} = 1.6, V_O = 5V$

$V_{DS} = 1.25 \times (75V + 8 \times 5V) = 144V$ So

$V_{D2} = 1.6 \times (5V + 75V \div 8) = 23V$

the power switch rating should be higher than 144V, and the rated voltage for the synchronous rectifier or Schottky diode should be higher than 23V.

Snubber Design (Passive)

Snubber for Power Switch

Figure 5 shows four different ways to clamp the voltage on the power device. RCD type of snubber circuit is widely used in many applications.

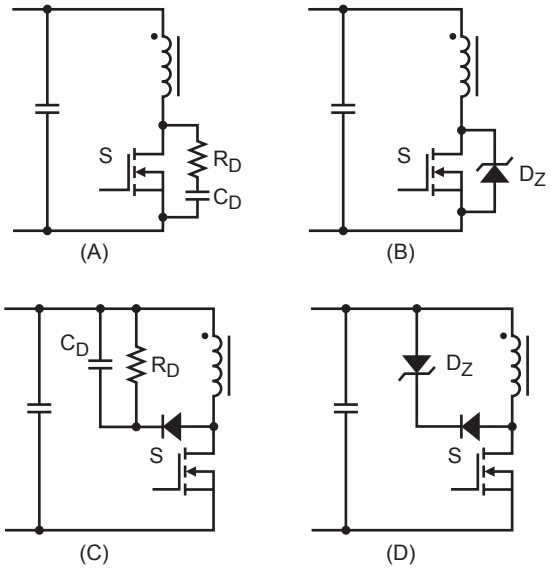

Figure 5—Snubber Designs

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RCD Type of Snubber Design Procedure:

1. Setting V_P

Higher V_P means higher voltage stress on the power switch, but lower power loss. Usually, V_P can be set as 20%~40% of (V_{IN}+ NxV_O).

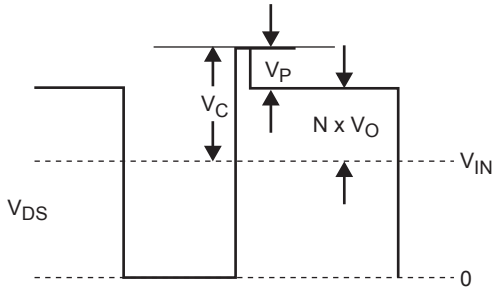

Figure 6—Voltage Waveform of Primary Power Switch Shown in Figure 5(C)

2. Estimated RCD snubber loss is given by:

$$P_{RCD_LOSS} = P_{LK} \times (1 + \frac{N \times V_O}{V_P})$$

Where:

$$P_{LK} = \frac{1}{2} L_{LK} \times I_P{}^2 \times f_C$$

P_{LK} is the energy stored in the leakage inductance (L_{LK}), which carries the peak current at the power switch turn-off.

3. Calculate values of the R_D and C_D of RCD snubber by:

$$R_D = \frac{V_P{}^2}{P_{RCD_LOSS}}$$

$$R_D \times C_D >> \frac{1}{f_S}$$

Input Capacitor

The input capacitors (C1) are chosen based upon the AC voltage ripple on the input capacitors, RMS current ratings, and voltage rating of the input capacitors.

For a given AC ripple voltage, ΔV_{IN_PP}, C1 can be derived from:

$$C1 = \frac{I_{IN} \times (1 - D) \times T_S}{\Delta V_{IN_PP}}$$

ΔV_{IN_PP} may affect the C1 voltage rating and converter stability. C1 RMS current has to be considered:

$$I_{RMS_C1} = I_{IN} \times \sqrt{\frac{(1 - D)}{D}}$$

C1 has to have enough RMS current rating.

Output Filter

The simplest filter is an output capacitor (C2), whose capacitance is determined by the output ripple requirement.

The current waveform in the output capacitor is mostly in rectangular shape. The full load current is drawn from the capacitors during the primary switch on time. The worse case for the output ripple occurs under low line and full load conditions. The ripple voltage can be estimated by:

$$\Delta V_{O-PP-C} = I_O \times \frac{D}{C2 \times f_S}$$

ESR also needs to be specified for the output capacitors. This is due to the step change in D2 current results in a ripple voltage that is proportional to the ESR. Assuming that the D2 current waveform is in rectangular shape, the ESR requirement is then obtained by given the output ripple voltage.

$$\Delta V_{O-PP_R_{ESR}} = \frac{I_O \times ESR}{(1 - D)}$$

The total ripple voltage can be estimated by:

$$\Delta V_{O-PP} = \Delta V_{O-PP-C} + \Delta V_{O-PP_ESR}$$

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Control Design

Generally, some of power supplies require the galvanic isolation between a relatively high input voltage and low output voltages. The most widely used devices to transfer signals across the isolation boundary are pulse transformers and optocouplers.

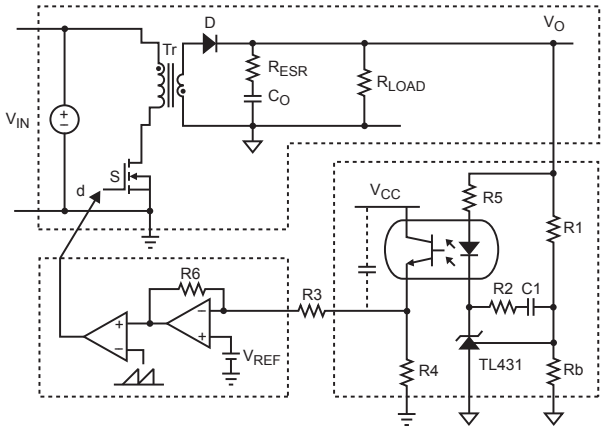

Figure 7—Simplified Circuit of Isolated Power Supply with Optocoupler Feedback

The MP6003 uses current mode control to achieve easy compensation and fast transient response. A type II compensation network which has two poles and one zero is needed to stabilize the system. The practical compensation parameters are provided in the EVQ6003DN datasheet.

Boost Controller Application Design Example 2

The MP6003 can be used as a boost controller as shown in Figure 8.

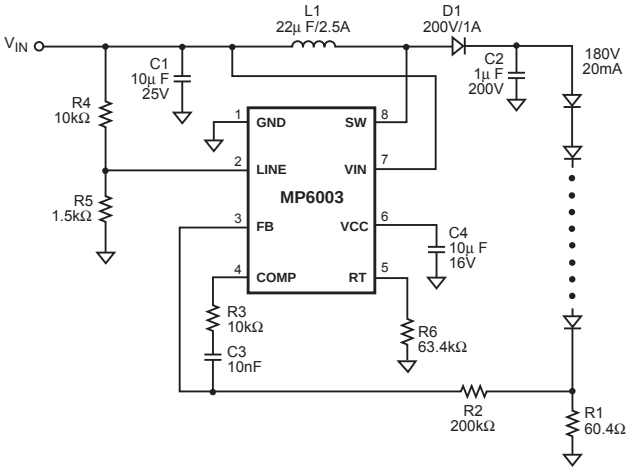

Figure 8—High Voltage LED Boost Controller Circuit

Design Example

This design example shows an flyback topology for industrial application. It has wide input voltage rang from 36V to 80V and 5V output.

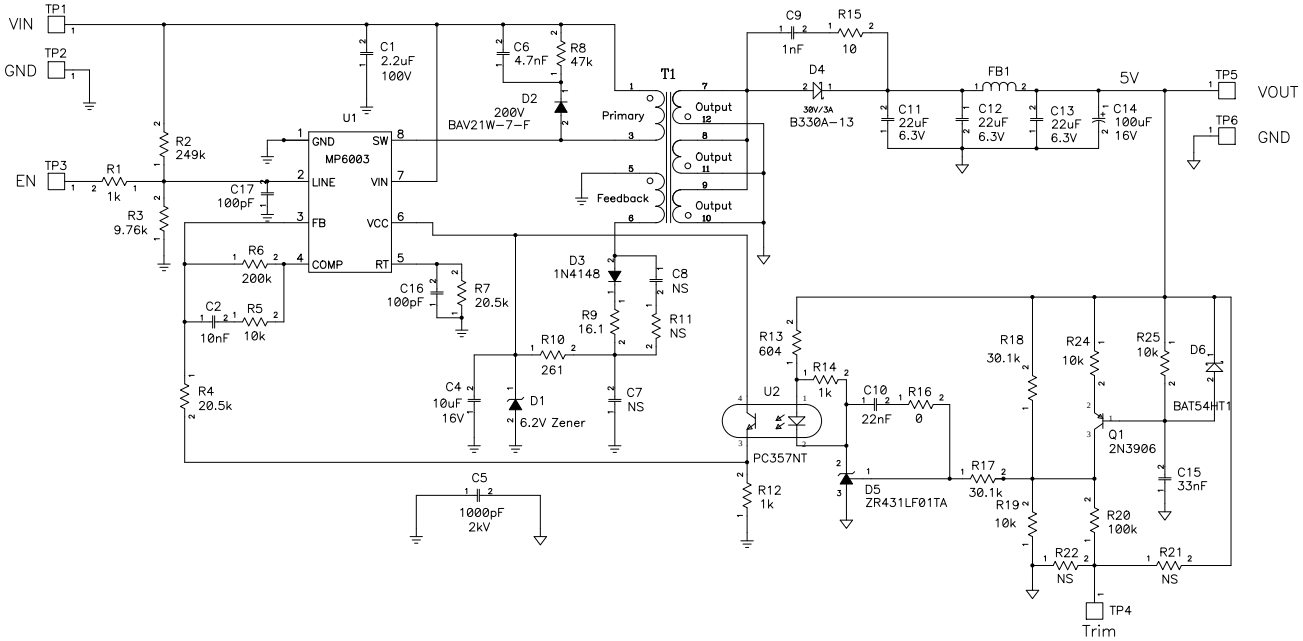

Figure 9—Reference Design Circuit for Flyback Application

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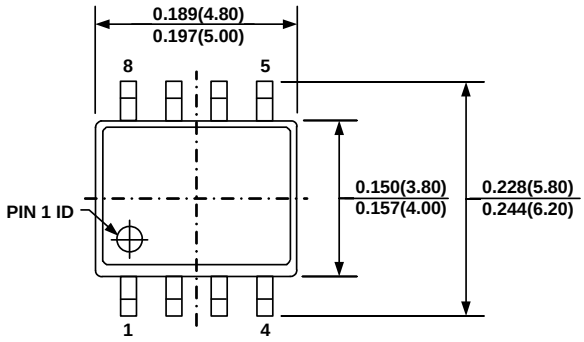
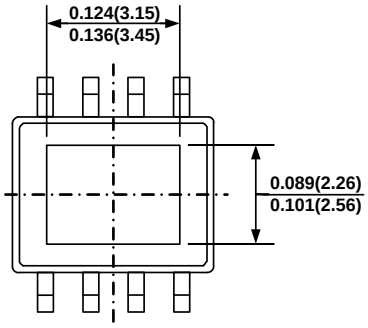
PACKAGE INFORMATION

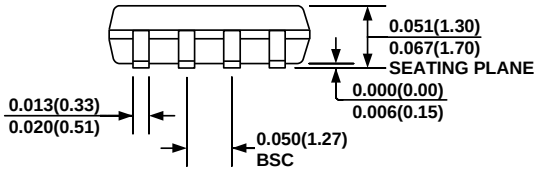
SOIC8E



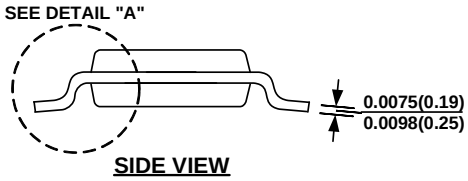
TOP VIEW



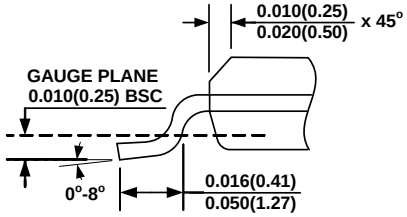
BOTTOM VIEW



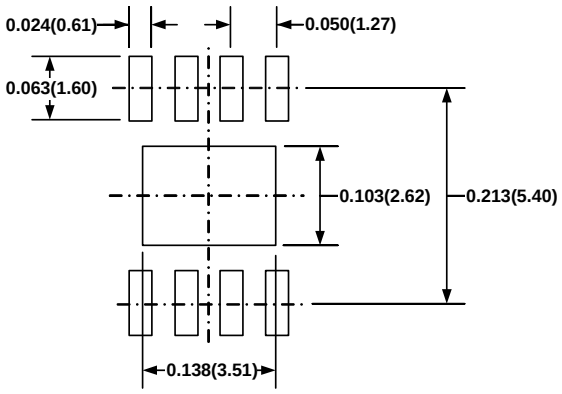
FRONT VIEW



SIDE VIEW



DETAIL "A"



RECOMMENDED LAND PATTERN

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6) DRAWING IS NOT TO SCALE.

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