MP5990

16V, 50A, 1mΩ $R_{DS(ON)}$, Fully Integrated Hot-Swap Solution with PMBus Interface

DESCRIPTION

The MP5990 is a fully integrated, PMBus compatible, compact hot-swap protection device. It contains a hot-swap controller and a high-side power MOSFET (HS-FET), which allow it to operate as a standalone device. The MP5990 can also operate as a hot-swap controller in parallel with the multi-phase MP5991. The device can achieve up to 50A of continuous output current (I_{OUT}) per device at room temperature, and up to 60A of continuous I_{OUT} with airflow.

The device limits the backplane voltage drop by limiting the inrush current to the load while a circuit card is inserted into a live backplane power source. The MP5990 limits the internal MOSFET current (I_{FET}) by controlling the gate voltage (V_{GATE}) via the current limit (I_{LIMIT}) reference input and soft-start ramp.

The MP5990 provides many features to simplify system design, such as an integrated current mirror to monitor I_{OUT} and integrated on-die temperature-sensing. This eliminates the need for an external current-sense power resistor, power MOSFET, and temperature-sense device.

The MP5990 provides rich fault protections, such as input voltage (V_{IN}) over-voltage protection (OVP), I_{OUT} over-current protection (OCP), short-circuit protection (SCP), and over-temperature protection (OTP). The MP5990 detects power MOSFET gate, source, and drain short conditions. The fault status can be indicated with the fault report output (GOK). The MP5990 also provides V_{IN} under-voltage warning (UVW), output over-current warning (D_OC) and power good (PG) indication.

The PMBus interface provides V_{IN}, input current (I_{IN}), input energy (E_{IN}), output voltage (V_{OUT}), I_{OUT}, input power (P_{IN}), and output power (P_{OUT}) telemetry. The MP5990 monitors and reports fault statuses through the PMBus interface.

The MP5990 is available in an LGA-45 (5mmx7mm) package.

FEATURES

- 4V to 16V Operating Input Voltage (V_{IN}) Range
- Maximum 50A of Output Current (I_{OUT})
- Supports 60A of I_{OUT} with Air Flow
- 1mΩ Integrated Power MOSFET
- PMBus/I^2C 1.3 Compatible
- ±1% IMON Reporting Accuracy
- Built-In MOSFET Driver
- Integrated Current-Sense with Sense Output
- Configurable Over-Current Limit
- Configurable Short-Circuit Current Limit
- Built-In Insertion Delay
- Configurable Soft Start (SS)
- Built-In Fuse Health Reporting
- Fault Signal Output (GOK)
- Power Good Indication (PG)
- V_{IN} Under-Voltage Warning (UVW)
- Fault Type Indication (FLT_TYPE)
- Faults Auto-Record to the NVM
- V_{IN} OVP, SCP, OCP, and OTP with Options for No Action, Latch, Retry, or Hiccup Mode
- Intelli-Fuse Junction Temperature Monitoring
- Intelli-Fuse Controller
- Built-in NVM to Store Custom Configurations
- High Precision E_{IN}, P_{IN}, P_{OUT}, and I_{OUT} Reporting
- Configurable TON_DELAY and TOFF_DELAY
- NVM Write Protection
- Available in an LGA-45 (5mmx7mm) Package

APPLICATIONS

- Hot Swaps
- PC Cards
- Disk Drives
- Servers
- 5G Telecom
- Networking
- Laptops

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TYPICAL APPLICATION

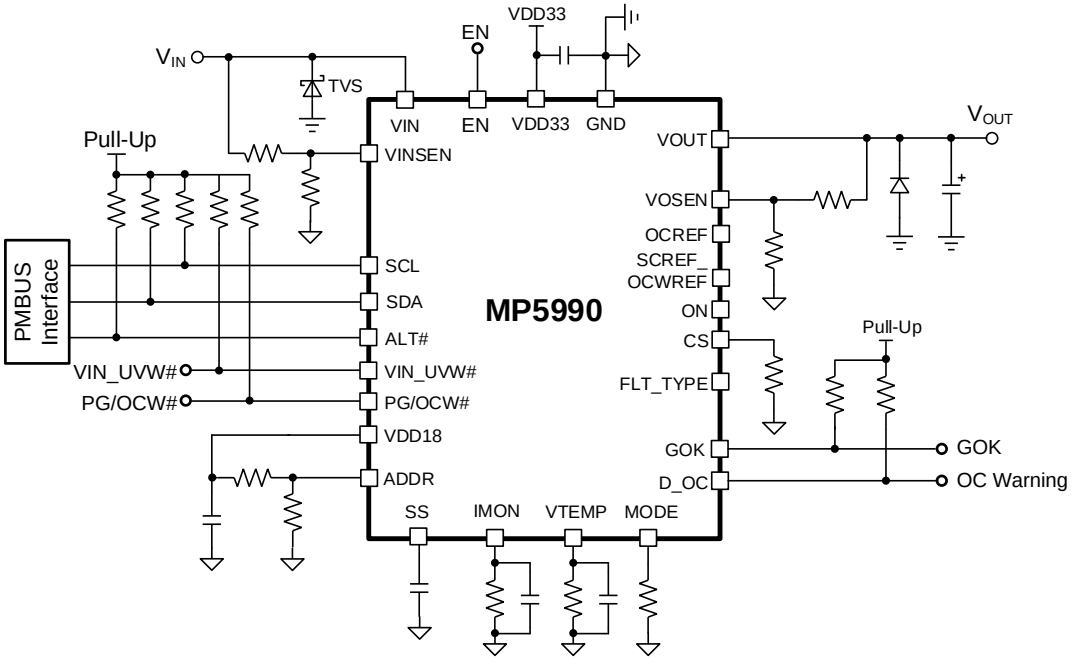

Figure 1: MP5990 Standalone Application Circuit

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TYPICAL APPLICATION *(continued)*

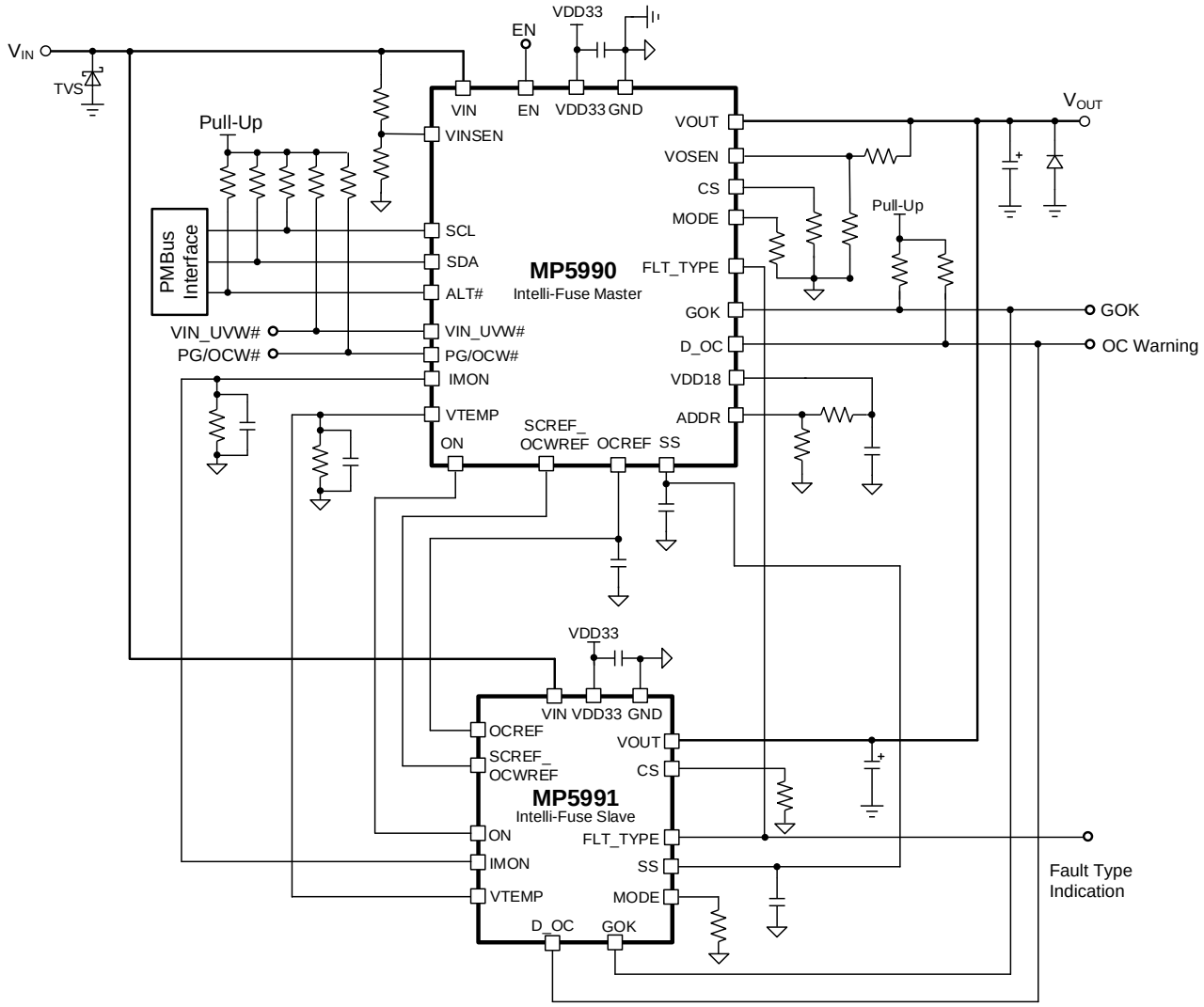

Figure 2: MP5990 (Master) + 1-Phase MP5991 (Slave) – Parallel Operation

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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP5990GMA-xxxx**	LGA-45 (5mmx7mm)	*See Below*	3

* For Tape & Reel, add suffix -Z (e.g. MP5990GMA-xxxx-Z).

** “xxxx” is the configuration code identifier for the register settings stored in the NVM. Each “x” can be a hexadecimal value between 0 & F. Contact an MPS FAE to create this unique number. “-0000” is the universal configuration code with default values.

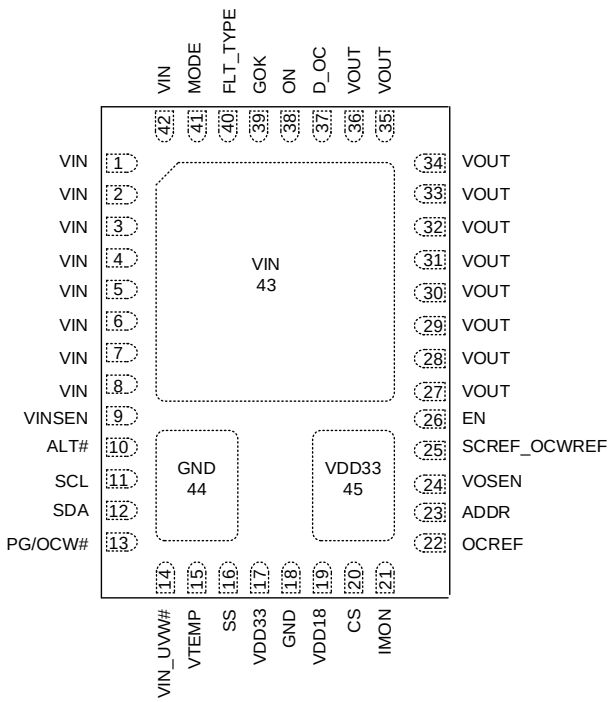
TOP MARKING

MPSYYWW
MP5990
LLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP5990: Part number
LLLLLLL: Lot number

PACKAGE REFERENCE

TOP VIEW



LGA-45 (5mmx7mm)

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PIN FUNCTIONS

Pin #	Name	I/O	Description
1, 2, 3, 4, 5, 6, 7, 8, 42, 43	VIN	A [I]	**System input power supply.** The VIN pin is connected to the drain of the integrated power MOSFET.
9	VINSEN	A [I]	**Input voltage (V_{IN}) sensing.** The VINSEN pin reads back V_{IN} through the internal analog-to-digital converter (ADC). Connect VINSEN to the VIN rail via a resistor divider.
10	ALT#	D [O]	**PMBus alert signal.**
11	SCL	D [I]	**PMBus clock signal.**
12	SDA	D [I/O]	**PMBus data signal.**
13	PG/OCW#	D [O]	**Multi-function pin.** The PG/OCW# pin can be configured for power good (PG) or over-current warning (OCW) indication via register C7h, bit[13]. When this pin is set to PG, this pin is the open-drain PG indicator. If the SS pin's voltage exceeds 340mV and V_{OUT} exceeds the PG setting threshold, PG asserts high. When this pin is set to OCW#, it acts as an open-drain OCW indicator. If the sensed I_{OUT} exceeds the OCW threshold, this pin asserts low.
14	VIN_UVW#	D [O]	**Input under-voltage warning (UVW) open-drain indicator.** If V_{IN} drops below its configured UVW threshold, the VIN_UVW# pin asserts low.
15	VTEMP	A [I]	**Junction temperature (T_J) sense.** Connect all the VTEMP pins of the e-fuse slaves to the MP5990's VTEMP pin. Place a minimum 10kΩ resistor and a maximum 1nF capacitor in parallel from VTEMP to AGND. The MP5990 senses the voltage on the VTEMP pin and reports the maximum T_J of all Intelli-Fuse phases.
16	SS	A [O]	**Soft-start time (t_{SS}) setting.** t_{SS} is set by an external capacitor connected to the SS pin. The internal circuitry controls the V_{OUT} slew rate during start-up.
17, 45	VDD33	Power	**Internal 3.3V LDO output.** Place a 1µF decoupling capacitor close to the VDD33 and GND pins.
18, 44	GND	A	**Ground.**
19	VDD18	Power	**1.8V LDO output.** The VDD18 pin provides the power supply for the internal digital circuit. Connect a 1µF bypass capacitor from VDD18 to AGND.
20	CS	A [O]	**Current-sense output.** The CS pin's voltage (V_{CS}) is compared to V_{OCREF} to determine the Intelli-Fuse over-current (OC) limit. V_{CS} can assert the D_OC pin when it is compared to the OCWREF pin's voltage (V_{OCWREF}). Connect a resistor from the CS pin to GND to generate V_{CS}.
21	IMON	A [I/O]	**Current monitor output.** The IMON pin's output current (I_{OUT}) is proportional to the current flowing through the device. Place a resistor and a 2.2nF to 100nF capacitor in parallel from IMON to AGND. The MP5990 senses the voltage on IMON and converts the voltage into the total I_{OUT} report.
22	OCREF	A [O]	**OC limit reference.** V_{OCREF} is the digital-to-analog converter (DAC) output of the internal OC limit reference. The MP5990 compares V_{OCREF} and V_{CS} to determine the Intelli-Fuse OC limit.
23	ADDR	A [I]	**PMBus address 4 LSB setting.** Connect a resistor divider from the VDD18 to AGND pin to set the 4LSB of the PMBus address based on the ADDR pin's voltage.
24	VOSEN	A [I]	**Output voltage (V_{OUT}) sensing.** The VOSEN pin reads back V_{OUT} through the internal ADC. Connect VOSEN to the rail output via a resistor divider.

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PIN FUNCTIONS *(continued)*

Pin #	Name	I/O	Description
25	SCREF_ OCWREF	A [O]	**Short-circuit current limit reference and over-current warning (OCW) reference.** The SCREF_OCWREF pin is a DAC output that sets the short-circuit current limit and OCW current limit. If V_{SS} > 340mV and ON is high, the pin transits from SCREF to OCWREF.
26	EN	D [I]	**Enable control.** The EN pin is a digital input that turns the MP5990 on and off. Drive EN high to turn on the MP5990; drive it low to turn off the device.
27, 28, 29, 30, 31, 32, 33, 34, 35, 36	VOUT	A [O]	**Output voltage.** The VOUT pin is connected to the source of the integrated power MOSFET.
37	D_OC	D [O]	**OC indication digital output.** The D_OC pin is an open-drain output. If V_{CS} exceeds V_{OCWREF}, D_OC asserts low.
38	ON	D [O]	**Power MOSFET on/off control.** Pull the ON pin above 2V to turn on the e-fuse power MOSFET; pull ON below 0.6V to turn off the e-fuse power MOSFET. The e-fuse power MOSFET cannot be turned off by pulling ON low externally.
39	GOK	D [I/O]	**Intelli-Fuse open-drain fault reporting output, and multi-phase slave fault detection input.** The GOK pin is an open-drain output. If a fault occurs, GOK asserts low and latches. The faults that can trigger GOK include input over-voltage (OV) faults, output OC faults, short-circuit faults, over-temperature (OT) faults, and FET health faults. When the MP5990 operates in parallel with the MP5991, the GOK pin works as the input for the slave phases' (MP5991) fault detections. If GOK is pulled low by the slaves, then the master (MP5990) pulls the ON pin low to disable the output.
40	FLT_TYPE	A [I]	**Intelli-Fuse fault type indication output.** The FLT_TYPE pin reports the fault type. During multi-phase operation, connect the FLT_TYPE pins together to indicate the most serious fault in the system.
41	MODE	A [I]	**Mode selection.** Connect a 120kΩ (±10%) resistor from the MODE pin to GND.

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ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} (DC).....-0.3V to +20V
V_{IN} (1μs)..... 24V
V_{IN} (25ns)..... 29V
V_{OUT}.....-0.3V to +20V
VDD33……..... -0.3V to +4V
VDD18..... -0.3V to +2.2V
IMON, VINSEN, ADDR, FLT_TYPE, VTEMP, VOSEN .....-0.3V to +2.2V
All other pins .....-0.3V to +4V
Continuous power dissipation (T_A = 25°C) (2) 5.46W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings (3)

Human body model (HBM) .....Class 1C
Charged device model (CDM).....Class C2B

Recommended Operating Conditions (4)

Input voltage operating range .....4V to 16V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (5) θ_{JA} θ_{JC}

LGA-45 (5mmx7mm)……..22.9….10.1...°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Followed ANSI/ESDA/JEDEC JS-001 for HBM and ANSI/ESDA/JEDEC JS-002 for CDM.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, EN = high, R_{CS} = 2kΩ, R_{IMON} = 2kΩ, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Quiescent current	I_{QIN}	EN is low, low-power mode		1.2	2.5	mA
		EN is low, regular power mode		11	22.5	mA
		Both EN and ON are high, no load		11.2	22.7	mA
		Fault latch off		11	22.4	mA
VDD33 Regulator and Under-Voltage Lockout (UVLO)						
VDD33 regulator output voltage	VDD33	I_{VDD33} = 0mA	3.22	3.32	3.42	V
VDD33 regulator load capability	Δ_{VDD33}	I_{VDD33} = 25mA			2	%
		I_{VDD33} = 40mA			3.5	%
VDD33 UVLO rising threshold	$VDD33_{VTH}$		2.55	2.7	2.85	V
VDD33 UVLO falling threshold	$VDD33_{VTL}$		2.15	2.3	2.45	V
VDD33 UVLO hysteresis	$VDD33_{HYS}$			400		mV
VDD18 Regulator						
1.8V regulator output voltage			1.78	1.8	1.82	V
1.8V regulator load capability	Δ_{VDD18}	I_{VDD18} = 30mA			2	%
V_{IN} Under-Voltage Protection (UVP) and Over-Voltage Protection (OVP)						
V_{IN} analog UVLO rising threshold	$V_{IN_VTHR_ANA}$	Disable digital V_{IN} UVLO (C4h, bit[7] = 0)	3.05	3.2	3.35	V
V_{IN} analog UVLO falling threshold	$V_{IN_VTHF_ANA}$		2.55	2.7	2.95	V
V_{IN} digital on/off threshold configurable range (6)	$V_{IN_ON_OFF_DGTL}$	Set by 35h, bits[6:0] and 36h, bits[6:0]		0 to 63.5		V
V_{IN} analog OVP threshold	$V_{IN_OVP_ANA}$	Set the digital OVP threshold to 20V via 55h, bits[6:0]	17	18.5	20	V
V_{IN} analog OVP hysteresis	$V_{IN_OVP_ANA_HYS}$	Auto-retry mode, set the digital OVP threshold to 20V via 55h, bits[6:0]		1.2		V
V_{IN} digital OV configurable range (6)	$V_{IN_OVP_DGTL}$	Set by 55h, bits[6:0]		0 to 63.5		V
Enable (EN)						
EN rising threshold	V_{EN_ON}			1.2		V
EN falling threshold	V_{EN_OFF}			0.83		V
EN high leakage	$I_{IH(EN)}$	EN = 3.3V		3.6		µA
Enable delay	t_{DLY_LP}	Low-power mode, EN high to ON high, TON_DELAY = 0		130		µs
	t_{DLY_RP}	Regular power mode, EN high to ON high, TON_DELAY = 0		0.5	10	µs
Power MOSFET						
On resistance	$R_{DS(ON)}$	T_J = 25°C, I_{FET} = 2A		1	1.25	mΩ
		T_J = 125°C, I_{FET} = 2A (6)		1.35	1.7	
Off-state leakage current	I_{OFF}	V_{IN} = 16V, power MOSFET off			1	µA

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, EN = high, R_{CS} = 2kΩ, R_{IMON} = 2kΩ, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
ON						
ON output low voltage	V_{OLON}				0.6	V
ON output high voltage	V_{OHON}		2			V
ON output at no power	V_{ONINI}	VDD33 < UVLO threshold, EN = 0, sink current = 100μA			0.6	V
FET on insertion delay time	t_{DLY_ON}	V_{IN} and VDD33 > UVLO threshold	0.8	1.3	1.8	ms
ON blanking time	$t_{ONBLANK}$	ON reset from fault status, high level trig mode	0.7	1	1.5	ms
Analog-to-Digital Converter (ADC)						
Voltage range (6)	FS_{ADC}			0 to 1.6		V
Reference voltage			-0.5%	1.6	+0.5%	V
ADC resolution (6)				10		bits
DNL(6)				1		LSB
INL (6)				1		LSB
Sample rate (6)				780		kHz
Current Monitor Output (IMON)						
IMON sense gain		I_{OUT} > 4A	9.9	10	10.1	μA/A
IMON sense offset		I_{OUT} > 4A	-1		+1	μA
Current-Sense (CS) Output for Over-Current Protection (OCP)						
CS gain	I_{CS} / I_{OUT}	I_{OUT} > 4A	9.6	10	10.4	μA/A
CS gain offset		I_{OUT} > 4A	-1		+1	μA
Over-Current Limit Reference (OCREF)						
OCREF internal max current limit clamp	V_{OCREF_CLAMP}	V_{BE} at V_{OUT} < 80% of V_{IN}, T_J = 25°C	570	635	699	mV
		V_{BE} at V_{OUT} < 80% of V_{IN}, T_J = 125°C (6)	370	440	570	mV
		V_{OUT} ≥ 80% of V_{IN}	1.9	2	2.1	V
OCREF over-current (OC) regulation timer	t_{OC_REG}	V_{OUT} ≥ 90% of V_{IN}, V_{OCREF} ≥ 0.3V		220		μs
OCREF DAC operating range (6)	$FS_{DACOCREF}$			0 to 1.8		V
DAC reference	$V_{OCREFREF}$		1.74	1.76	1.78	V
Resolution (6)	Resolution			6		bit
	Δ_{DAC_OCREF}			28		mV
OCREF DAC buffer sink ability	Δ_{OCREF_SI}	I_{SINK} = 200μA, V_{OCREF} = 0.31V		6		%
		I_{SINK} = 200μA , V_{OCREF} = 1.76V		1		%
OCREF DAC buffer source ability	Δ_{OCREF_SO}	I_{SOURCE} = 200μA, V_{OCREF} = 0.31V		-4		%
		I_{SOURCE} = 200μA, V_{OCREF} = 1.76V		-1		%
Short Circuit Current Limit Reference (SCREF)						
SCREF voltage range for short-circuit current limit	$V_{SCLIMIT}$	SC limit = 40A		0	0.16	V
		SC limit = 60A	0.24	0.3	0.36	V
		SC limit = 80A	0.48	0.6	0.72	V
		SC limit = 120A	0.96	1.2	1.44	V
		SC limit = 100A	1.68			V
Short-circuit current limit accuracy (6)	$I_{LIMITSC}$	V_{SCREF} > 1.68V		100		A

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, EN = high, R_{CS} = 2kΩ, R_{IMON} = 2kΩ, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Short-circuit protection response time (6)	t_{SC}			200		ns
Short-circuit start-up protection timer	t_{SC_TIMER}	V_{OUT} < 1/8 of V_{IN}, MOSFET current is regulated by V_{BE}		2.1	3.2	ms
SCREF DAC voltage range (6)	$FS_{DAC\ SCREF}$			0 to 1.8		V
SCREF DAC reference	$V_{SCREF\ REF}$		1.74	1.76	1.78	V
Resolution (6)	Resolution			6		bits
	$\Delta_{DAC\ OCREF}$			28		mV
SCREF DAC buffer sink ability	Δ_{SCREF_SI}	I_{SINK} = 200μA, V_{SCREF} = 0.31V		6		%
		I_{SINK} = 200μA, V_{SCREF} = 1.76V		1		%
SCREF DAC buffer source ability	Δ_{SCREF_SO}	I_{SOURCE} = 200μA, V_{SCREF} = 0.31V		-2		%
		I_{SOURCE} = 200μA, V_{SCREF} = 1.76V		-1		%
Soft Start (SS)						
SS pull-up current	I_{SS}	V_{IN} = 12V, R_{SS} = 0.8MΩ	13	15	17	μA
SS pull low voltage	V_{OL_SS}	Sink current = 10mA			0.2	V
SS MOSFET off-state leakage current	I_{LKG_SS}	ON = 0, V_{SS} = 3.3V			1	μA
SS internal comparator threshold	$V_{SS\ TH}$	Transit from SCREF to OCWREF		340		mV
GOK Output and Comparator						
Output low voltage	V_{OL_GOK}	Sink current = 10mA			0.3	V
GOK off-state leakage current	I_{LKG_GOK}	V_{GOK} = 3.3V			3	μA
GOK internal pull-up resistor (6)	R_{GOK_INT}			370		kΩ
GOK comparator low threshold	V_{GOK_TH}	Fault status	1.05	1.16	1.3	V
GOK comparator hysteresis	$V_{GOK\ HYS}$			900		mV
GOK fault delay time				10	15	μs
D_OC Output						
Output low voltage	V_{OL_DOC}	Sink current 10mA			0.3	V
D_OC bar off-state leakage current	I_{LKG_DOC}	V_{DOC} = 3.3V			1	μA
D_OC high to low threshold	V_{DOC_TH}	V_{OUT} ≥ 90% of V_{IN}, 0.3V ≤ V_{OCWREF} ≤ 1.8V, R_{MODE} = 120kΩ	95%	100%	105%	V_{OCWREF}
OCW Output						
OCW low voltage	V_{OLGOK}	Sink current = 10mA			0.3	V
OCW high leakage current	IL_{GOK}	V_{OCW} = 3.3V		1.5	2.3	μA
FET Short Detection						
FET drain-to-source short analog entry threshold	V_{OUT_DSTH}		85%	90%	95%	V_{IN}
FET drain-to-source short analog recovery threshold	V_{OUT_FAULTH}		65%	70%	75%	V_{IN}
GS short protection delay time (6)	t_{GS_ST}	V_{SS} > VDD33 - 0.7	200	250	300	ms

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, EN = high, R_{CS} = 2kΩ, R_{IMON} = 2kΩ, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Fault Type Indication Output (FLT_TYPE) Total 6 Types						
FLT_TYPE voltage during SCP (6)	V_{FLT_TYPESC}	Short-circuit fault		1.5		V
FLT_TYPE voltage during OCP	V_{FLT_TYPEOC}	OC fault during normal operation and soft start	1.16	1.2	1.24	V
FLT_TYPE voltage during OTP and V_{IN} OVP	V_{FLT_TYPEOT}	Ove-temperature (OT) fault, V_{IN} over-voltage (OV) fault	0.865	0.9	0.935	V
FLT_TYPE voltage during FET GS and DS short	$V_{FLT_TYPEDSS}$	FET DS and GS short event	0.57	0.6	0.63	V
FLT_TYPE voltage during GOK fault	$V_{FLT_TYPEGSS}$	GOK fault event	0.275	0.3	0.325	V
FLT_TYPE voltage at other faults	$V_{FLT_TYPEOTHER}$		0.08	0.1	0.12	V
MODE						
MODE source current	I_{MODE}		9	10	11	μA
MODE voltage setting window	V_{MODE}	R_{MODE} = 120kΩ	0.96	1.2	1.44	V
VTEMP						
VTEMP sense gain (6)				8.7		mV/°C
VTEMP sense output (6)		T_J = 25°C		370		mV
Thermal Shutdown						
OT threshold (6)	T_{J_OTP}			145		°C
PMBus Timing Characteristics (1MHz) (6) (7)						
Operating frequency range			10		1000	kHz
Bus free time		Between a stop and start condition	0.5			μs
Hold time			0.26			μs
Repeated start condition set-up time			0.26			μs
Stop condition setup time			0.26			μs
Data hold time			0			ns
Data set-up time			50			ns
Clock low timeout			25		35	ms
Clock low period			0.5			μs
Clock high period			0.26		50	μs
Clock/data falling time					120	ns
Clock/data rising time					120	ns

Note:

6) Guaranteed by design or characterization data. Not tested in production.
7) The device supports 100kHz, 400kHz, and 1MHz bus speeds. The PMBus timing parameters in this table are for operation at 1MHz. If the PMBus operating frequency is 100kHz or 400kHz, refer to the SMBus specifications for timing parameters.

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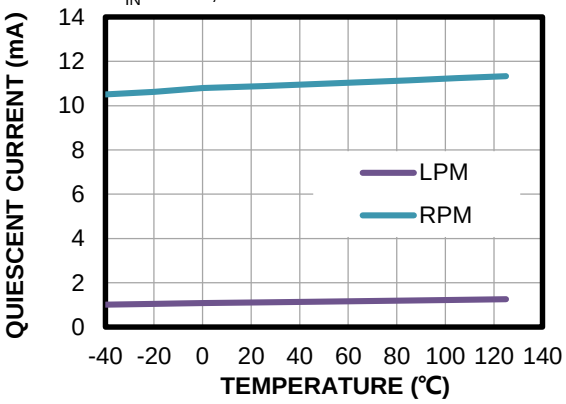
TYPICAL CHARACTERISTICS

V_{IN} = 12V, C_{OUT} = 330µF, R_{CS} = R_{IMON} = 2kΩ, T_A = 25°C, unless otherwise noted.

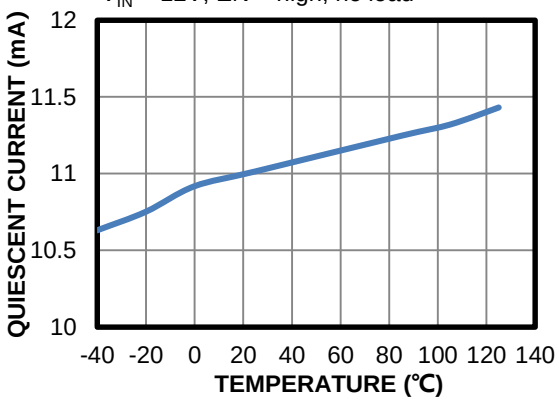
Quiescent Current vs. Temperature

V_{IN} = 12V, EN = low

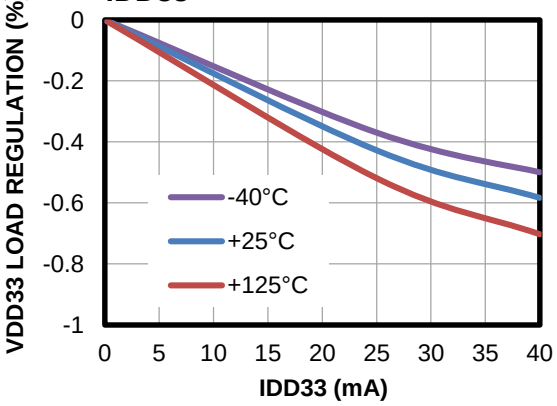


Quiescent Current vs. Temperature

V_{IN} = 12V, EN = high, no load

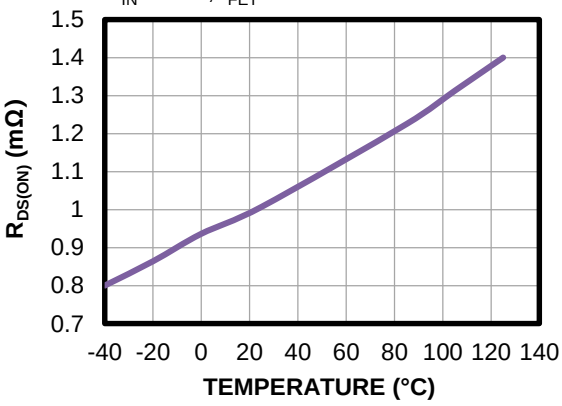


VDD33 Load Regulation vs. IDD33

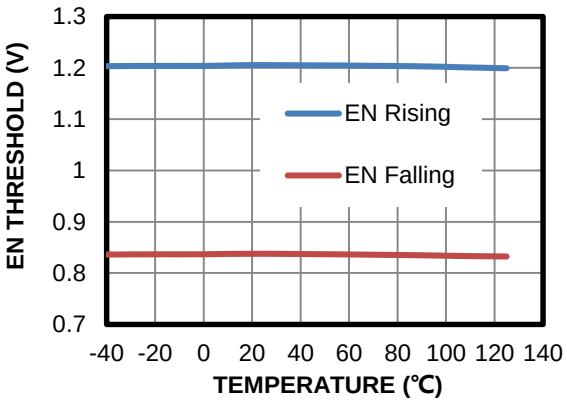


$R_{DS(ON)}$ vs. Temperature

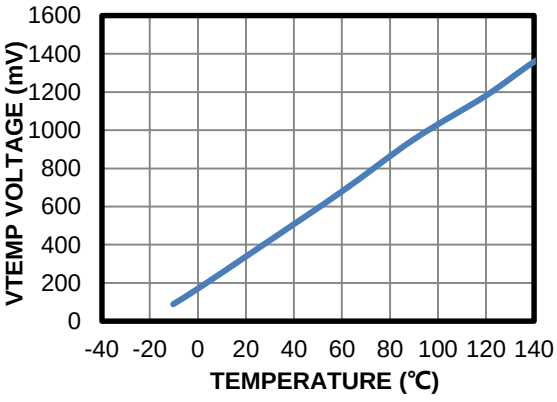
V_{IN} = 12V, I_{FET} = 2A



EN Threshold vs. Temperature



VTEMP Voltage vs. Temperature



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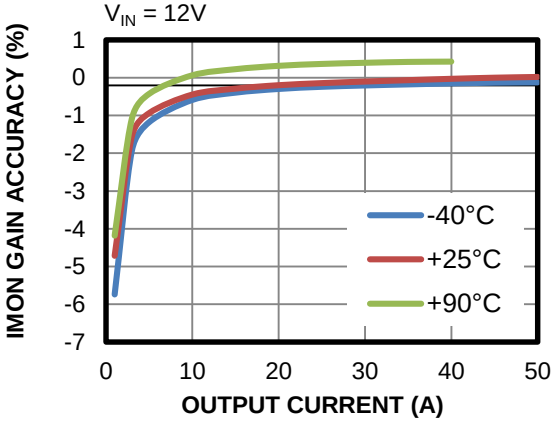
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, C_{OUT} = 330µF, R_{CS} = R_{IMON} = 2kΩ, T_A = 25°C, unless otherwise noted.

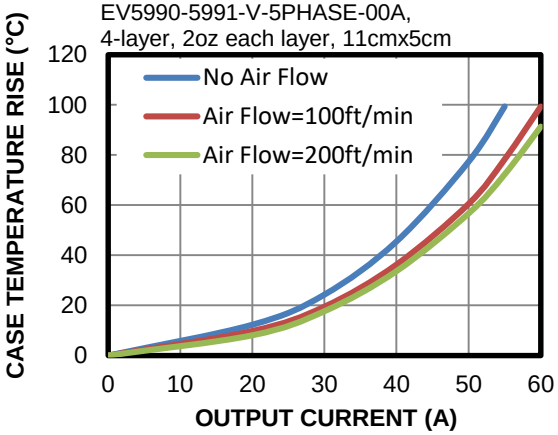
IMON Gain Accuracy vs. Output Current

V_{IN} = 12V



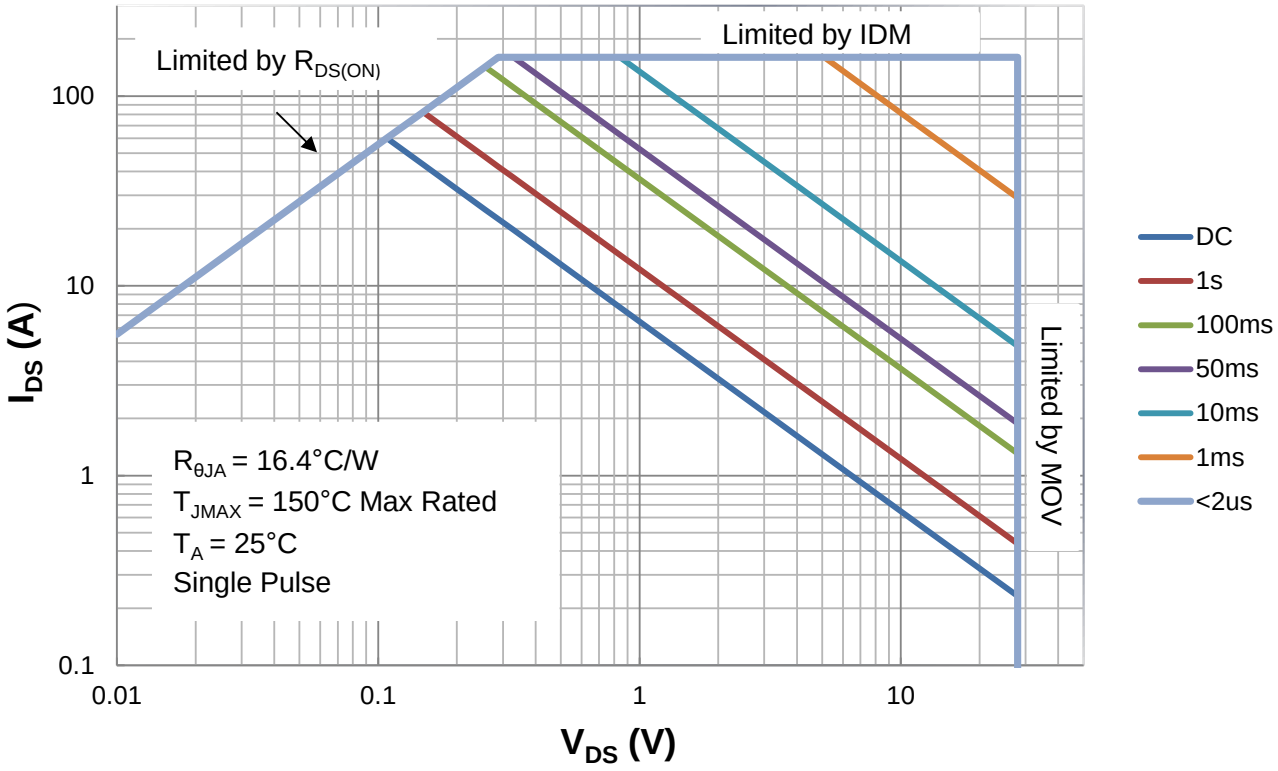
Case Temperature Rise vs. Output Current

EV5990-5991-V-5PHASE-00A,
4-layer, 2oz each layer, 11cmx5cm



Safe Operation Area (SOA)

Tested on the EV5990-5991-V-5PHASE-00A, 4-layer (2oz per layer), 11cmx15cm



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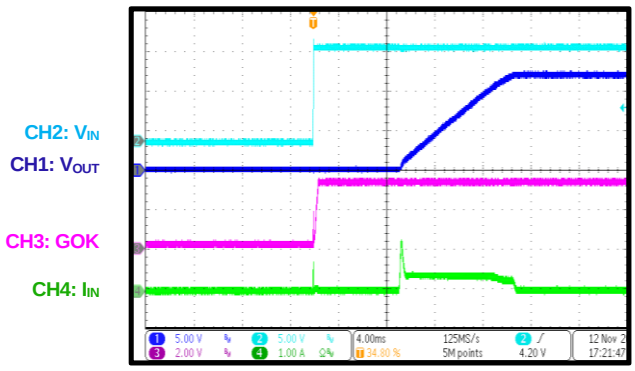
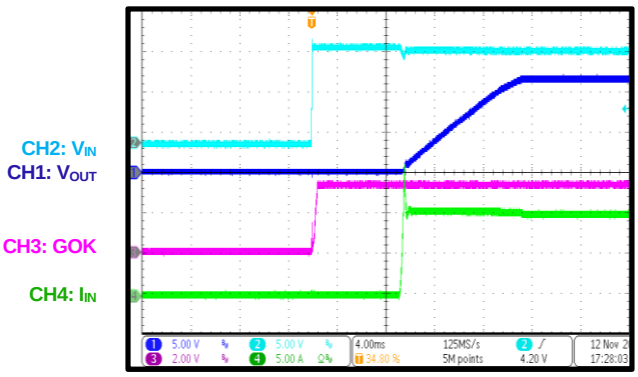
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, C_{OUT} = 330µF, R_{CS} = R_{IMON} = 2kΩ, T_A = 25°C, unless otherwise noted.

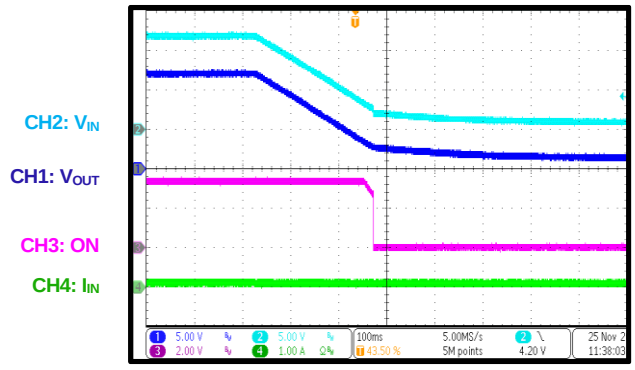
VIN Hot Plug
I_{OUT} = 0A



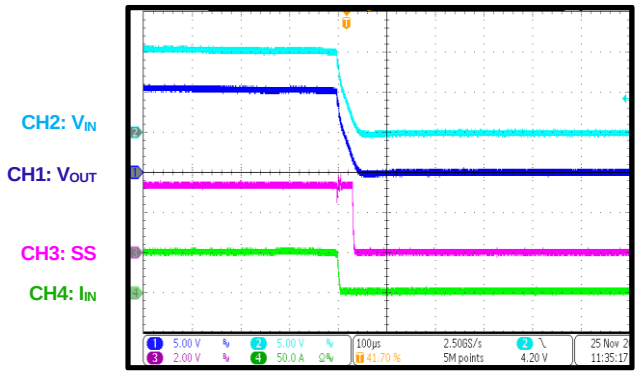
VIN Hot Plug
I_{OUT} = 10A



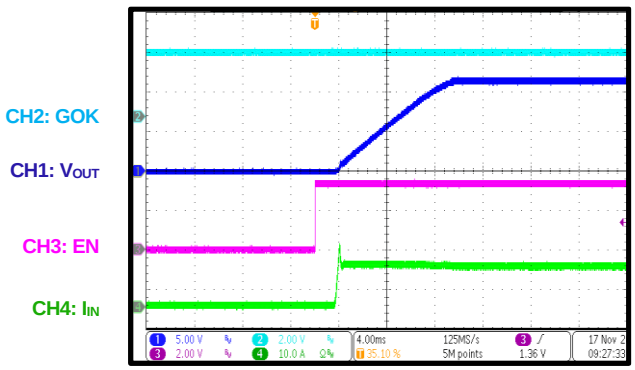
Shutdown through VIN
I_{OUT} = 0A



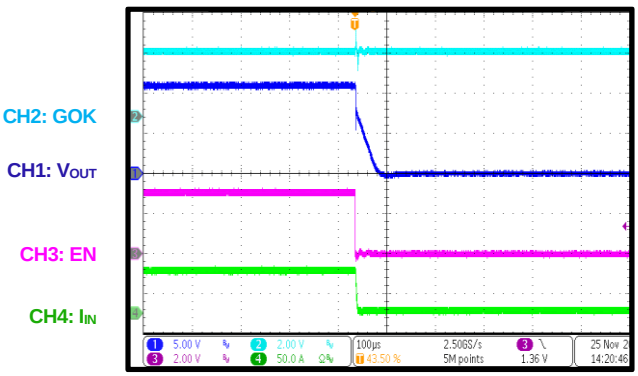
Shutdown through VIN
I_{OUT} = 50A



Start-Up through EN
I_{OUT} = 10A



Shutdown through EN
I_{OUT} = 50A



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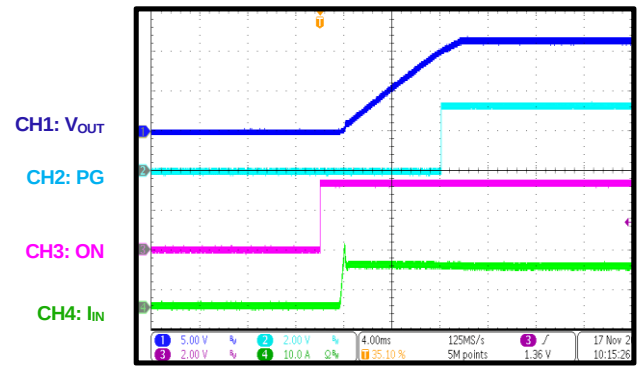
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, C_{OUT} = 330µF, R_{CS} = R_{IMON} = 2kΩ, T_A = 25°C, unless otherwise noted.

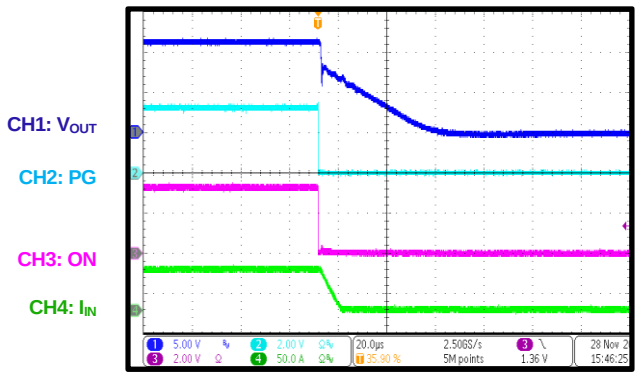
Start-Up via On Command

I_{OUT} = 10A, PG on = 10V



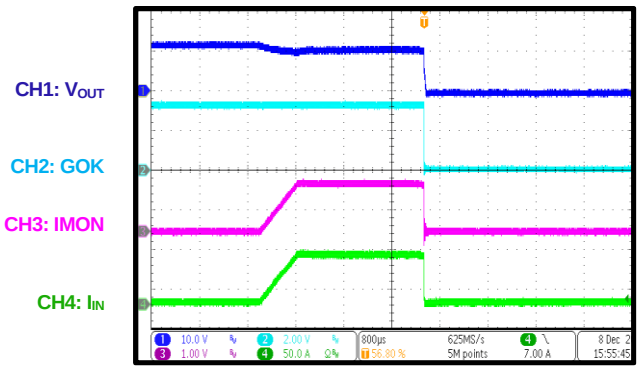
Shutdown via On Command

I_{OUT} = 50A



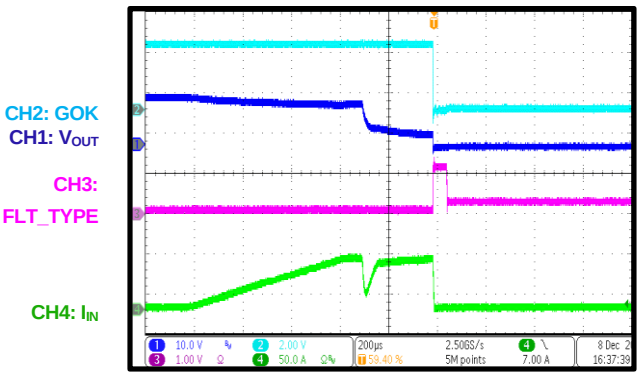
Total OCP

Total OCP limit = 55A, fault timer = 2ms, latch-off mode



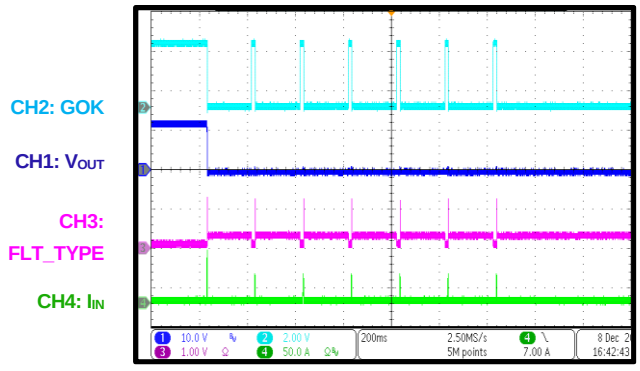
Per-Phase OCP

Per-phase OCP limit = 60A, latch-off mode



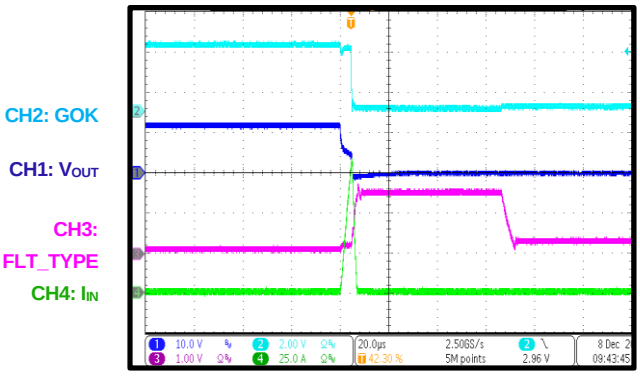
Per-Phase OCP

Per-phase OCP limit = 60A, retry 6 times mode, auto retry time = 200ms



SCP

I_{LIMIT} = 80A, latch-off mode



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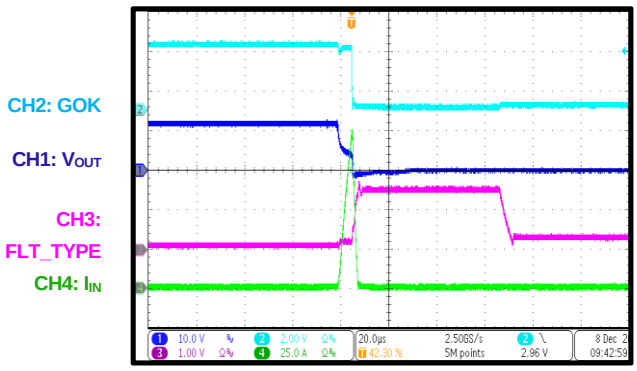
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

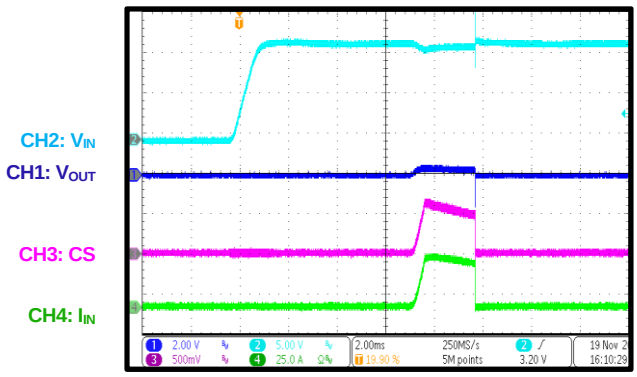
V_{IN} = 12V, C_{OUT} = 330µF, R_{CS} = R_{IMON} = 2kΩ, T_A = 25°C, unless otherwise noted.

SCP

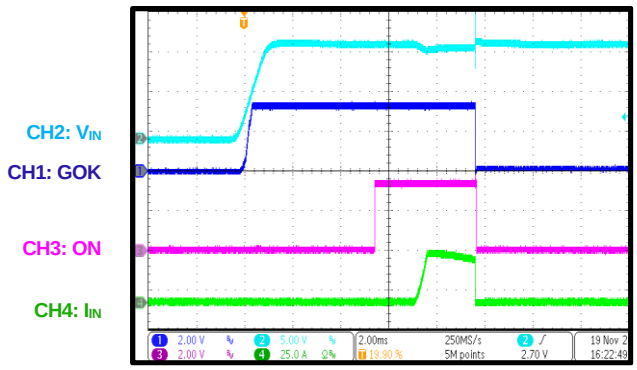
I_{LIMIT} = 100A, latch-off mode



Short-Circuit Start-Up

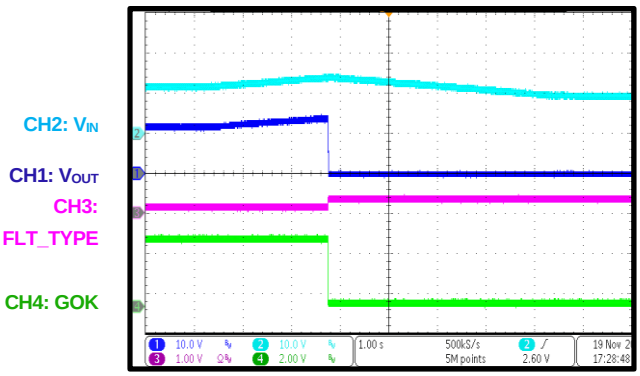


Short Circuit Start-Up



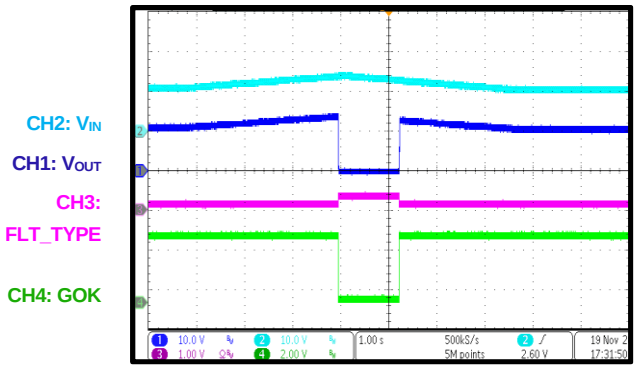
V_{IN} OVP in Latch-Off Mode

OV rising = 14V, OV falling = 13V, apply 14V to VIN, then reduce V_{IN}



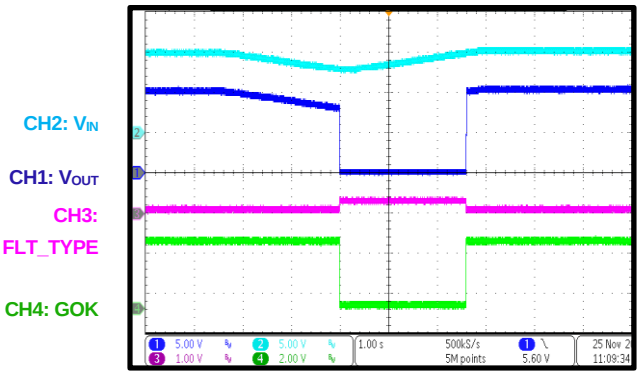
VIN OVP in Hiccup Mode

OV rising = 14V, OV falling = 13V, apply 14V to VIN, then reduce V_{IN}



VIN UVP

UV rising = 10V, UV falling = 8V, reduce VIN, then increase V_{IN}



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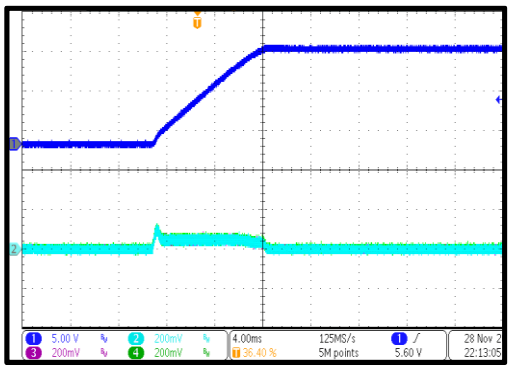
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, C_{OUT} = 330µF, R_{CS} = R_{IMON} = 2kΩ, T_A = 25°C, unless otherwise noted.

Current Balance during Start-Up while Paralleling

1 MP5990 and 2 MP5991s work in parallel, R_{IMON} = R_{CS} per device, I_{OUT} = 0A

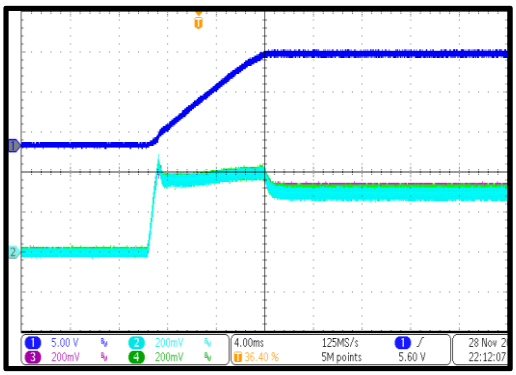
CH1: V_{OUT}
CH2: MP5990-CS
CH3: MP5991-CS1
CH4: MP5991-CS2



Current Balance during Start-Up while Paralleling

1 MP5990 and 2 MP5991s work in parallel, R_{IMON} = R_{CS} per device, I_{OUT} = 45A

CH1: V_{OUT}
CH2: MP5990-CS
CH3: MP5991-CS1
CH4: MP5991-CS2



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FUNCTIONAL BLOCK DIAGRAM

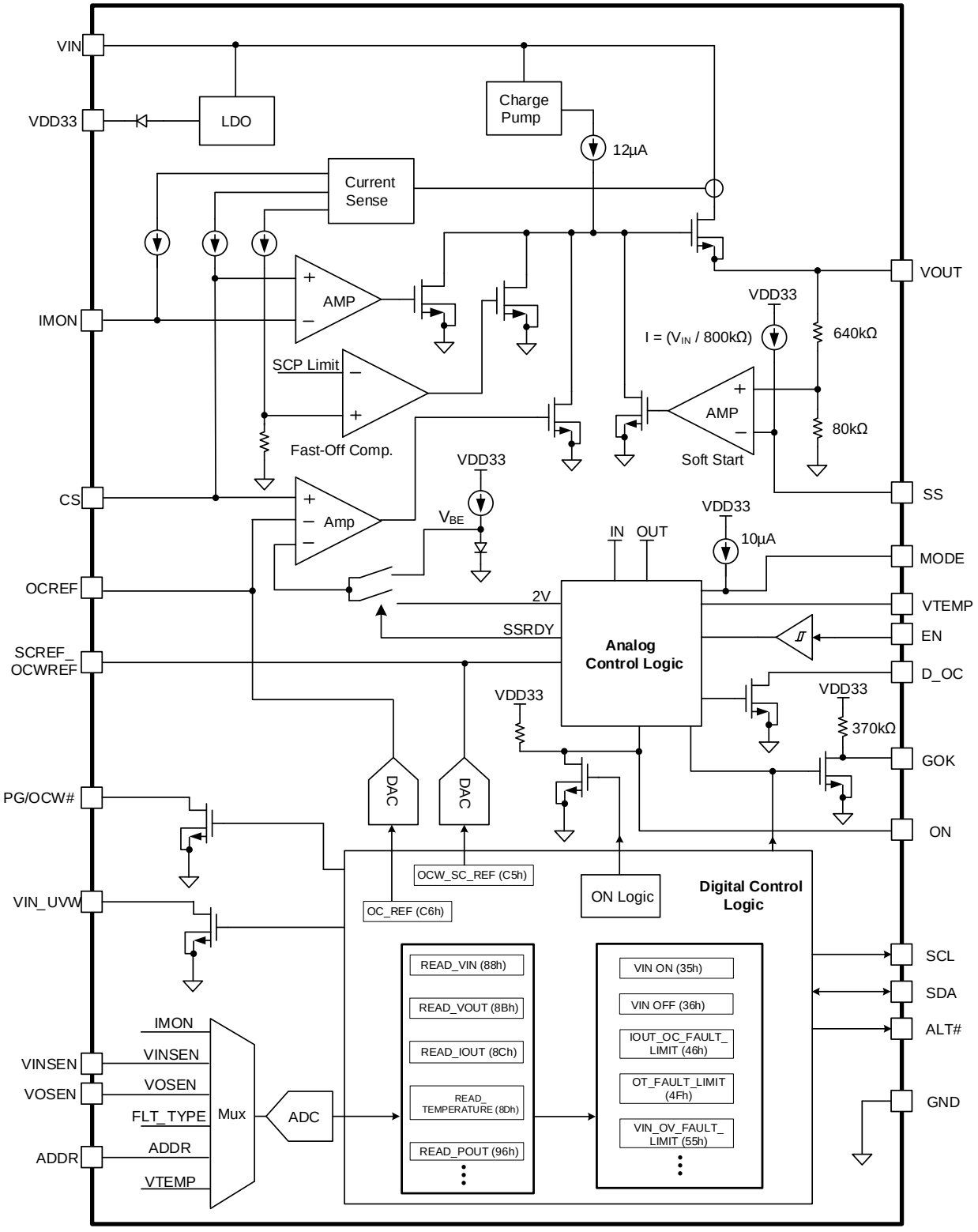

Figure 3: Functional Block Diagram

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OPERATION

The MP5990 is a fully integrated, PMBus compatible, compact hot-swap protection device. It contains a hot-swap controller and a high-side power MOSFET (HS-FET), which allow it to operate as a standalone device. The MP5990 can also operate as a hot-swap controller that works in parallel with the multi-phase MP5991. The device can achieve up to 50A of continuous output current (I_{OUT}) per device at room temperature, and up to 60A of continuous I_{OUT} with airflow.

The device limits the backplane voltage drop by limiting the inrush current to the load while a circuit card is inserted into a live backplane power source. The MP5990 limits the internal MOSFET current (I_{FET}) by controlling the gate voltage (V_{GATE}) via the current limit (I_{LIMIT}) reference input and soft-start ramp.

The MP5990 provides rich fault protections, such as input voltage (V_{IN}) over-voltage protection (OVP), I_{OUT} over-current protection (OCP), short-circuit protection (SCP), and over-temperature protection (OTP). The MP5990 detects power MOSFET gate, source, and drain short conditions. The fault status can be indicated with fault report output (GOK). The MP5990 also provides V_{IN} under-voltage warning (UVW), output over-current warning (D_OC) and power good (PG) indication.

Enable (EN) Control and Low-Power Mode

The EN pin controls the MP5990's on/off state. When V_{IN} exceeds its rising threshold, VDD33 is generated, regardless of the EN pin's status. The MP5990 provides regular power mode and low-power mode (LPM). In regular power mode, the PMBus interface, access to the non-volatile memory (NVM), and control circuitries are all live, even when EN is low. EN controls the output of the ON pin, which turns the MOSFET on and off. When EN is low, the quiescent current (I_{QIN}) is about 11mA in regular power mode.

When LPM is enabled (ADVANCE_CTRL (F1h), bit[12] = 1) and EN is low, most of the control circuitries are disabled to reduce the power consumption to 1.2mA. The PMBus interface and NVM are still accessible when the MP5990 is disabled. Connect EN to VDD33 for automatic start-up via VIN.

MOSFET On/Off Control (ON)

The ON pin is an output signal that turns the MOSFET on and off. In standalone operation, the MP5990 drives ON above 2V to turn on the power MOSFET. The MP5990 internally pulls ON below 0.6V to turn it off.

In multi-phase applications, the ON pins of the e-fuse slaves are connected to the MP5990's ON pin. Then the MP5990 works as a master to control the system's on/off sequence.

Soft Start (SS)

The MP5990 limits the inrush current with a controlled output voltage (V_{OUT}) ramp-up slew rate. The SS capacitor (C_{SS}) determines the soft-start time (t_{SS}). When ON is pulled high and the insertion delay time ends, a constant current source proportional to V_{IN} charges C_{SS}. V_{OUT} rises at a similar slew rate to V_{SS}. C_{SS} can be calculated with Equation (1):

$$C_{SS} = \frac{9 \times t_{SS}}{R_{SS}} \quad (1)$$

Where R_{SS} is 0.8MΩ.

For example, a 100nF capacitor sets t_{SS} to 8.9ms. If the load capacitance is extremely large, the current required to maintain the preset t_{SS} exceeds the start-up current limit. In this scenario, the rising time is limited by the load capacitor and the start-up current limit (I_{LIMIT_SU}). Float the SS pin to generate a fast ramp-up voltage. A current source (12μA) pulls up the MOSFET gate. The gate charge current controls the V_{OUT} rising time. Meanwhile, t_{SS} is about 1.5ms, which is the minimum soft-start time.

Start-Up Sequence

Figure 4 on page 20 shows the start-up sequence in regular power mode.

t0 to t1: At t0, V_{IN} rises immediately once the MP5990 is hot plugged into a live backplane. After V_{IN} exceeds its UVLO threshold, VDD33 starts ramping up. At t1, VDD33 reaches its UVLO rising threshold. Once the VDD33 power is ready, the GOK pin is high by default.

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t1 to t2: The power-on reset (POR) signal waits for all power supplies to be stable. After POR, the data in the multiple-time programmable (MTP) memory starts loading into the operating registers to initialize system configuration. After MTP copying ends, the system initialization delay (configured via D0h) starts. All analog-to-digital converter (ADC) channels start except for the ADDR channel. ON is low during this stage to keep the MOSFET off.

t2 to t3: Once the system initialization delay ends, the OCREF and SCREF_OCWREF pins output their limit settings.

The PMBus address is set by detecting the ADDR pin voltage. Once the ADDR sample is obtained, the PMBus starts communication. If the MP5990 is configured for LPM, the device enters LPM once the system initialization delay ends.

t3 to t4: At t3, EN asserts high. If OPERATION (01h) is set to 0x80 (its default value) before t3, TON_DELAY starts counting. TON_DELAY does not start if an ON command is not received.

t4 to t5: When the TON_DELAY time expires, ON pulls high to initiate the power MOSFET insertion delay time.

t5 to t6: At t5, the insertion delay time ends and the gate current source starts to charge the power MOSFET's gate. Once the MOSFET's gate voltage exceeds the turn-on threshold, the MP5990 starts to turn on the MOSFET with the controlled V_{OUT} slew rate to limit the inrush current.

t6 to t7: When the MP5990 detects that V_{SS} exceeds 340mV and ON is high, the output of SCREF_OCWREF transitions from the SCP limit (SCREF) to the over-current warning limit (OCWREF). The SCREF and OCWREF levels can be set via register OCW_SC_REF (C5h). If V_{OUT} reaches the PG high threshold and the PG/OCW pin is selected to be PG, then PG asserts high.

t7 to t8: At t8, soft start ends. At this point, the MOSFET is fully enhanced and can deliver energy to the output.

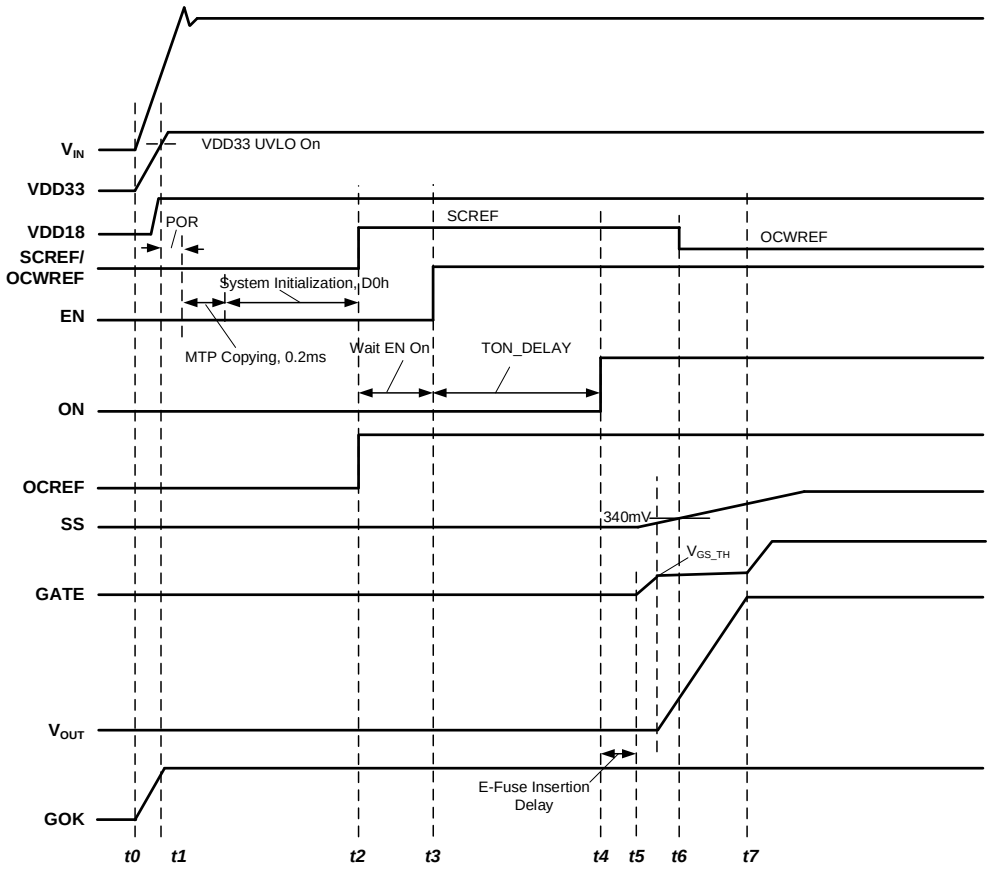

Figure 4: Start-Up Sequence in Regular Power Mode

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Figure 5 shows the start-up sequence in LPM. In LPM, ADVANCE_CTRL (F1h), bit[13] selects whether the device should enter the optional MTP copying mode or initiate the system initialization delay time after EN pulls high. If bit[13] is set to 0, then the MP5990 starts TON_DELAY after EN goes high. This sequence is different from regular power mode.

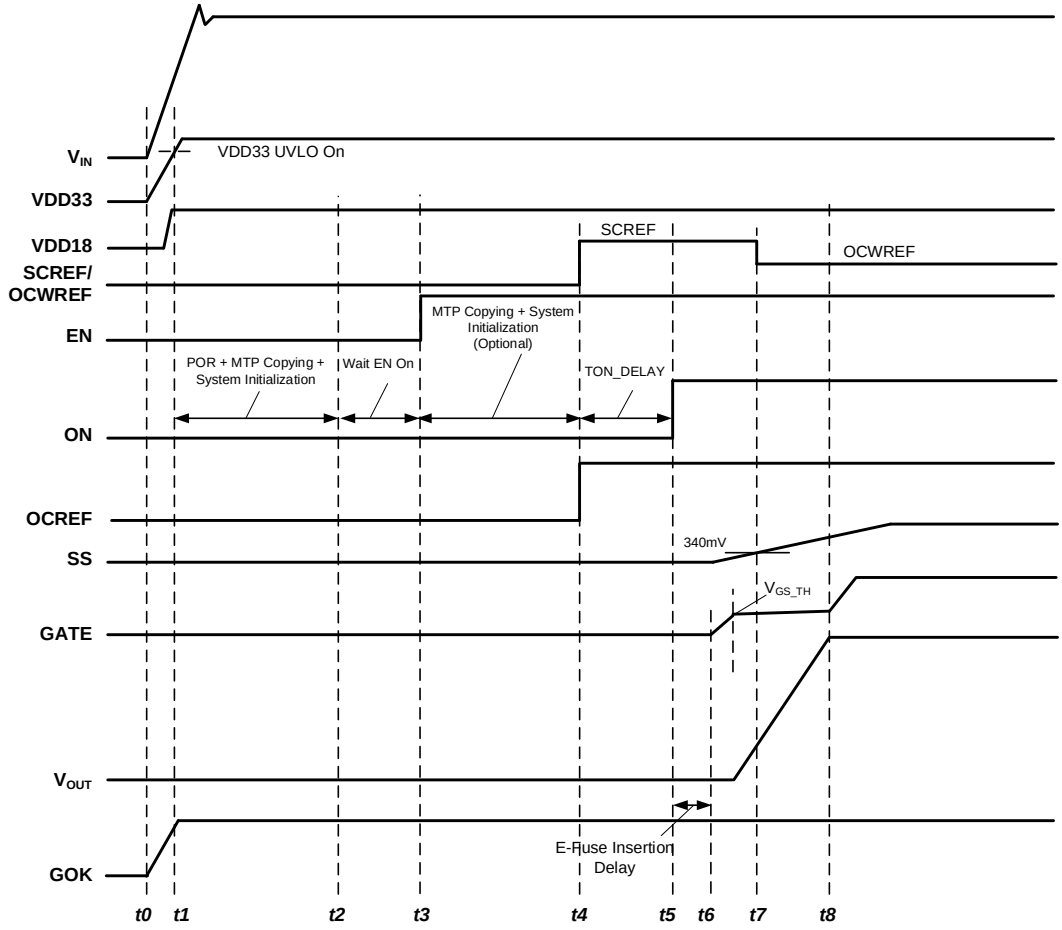

Figure 5: Start-Up Sequence in Low-Power Mode

Current-Sense Output (CS)

The CS pin provides a current proportional to I_{OUT} flowing through the device. V_{CS} is used for over-current (OC) limiting, OC warning indication, and parallel operation with start-up current balancing. The current-sense gain is 10μA/A while the MOSFET is fully on. A resistor (R_{CS}) on the CS pin generates V_{CS}. I_{CS} can be estimated with Equation (2):

$$I_{CS} = I_{OUT} \times 10\mu A/A \quad (2)$$

V_{CS} can be calculated with Equation (3):

$$V_{CS} = I_{CS} \times R_{CS} \quad (3)$$

Once V_{CS} reaches V_{OCREF}, the internal circuit regulates V_{GATE} to maintain a constant I_{FET}.

Output Current Monitor (IMON)

The MP5990 provides a high-accuracy MOSFET current monitor output (IMON). The current monitor gain is 10μA/A. Connect a resistor (R_{IMON}) between the IMON and GND pins. The recommended IMON voltage (V_{IMON}) range is 0V to 1.6V, which is also within the internal ADC-sensing limit. IMON can be estimated with Equation (4):

$$I_{IMON} = I_{OUT} \times 10\mu A/A \quad (4)$$

V_{IMON} can be calculated with Equation (5):

$$V_{IMON} = I_{IMON} \times R_{IMON} \quad (5)$$

If there is no bandwidth requirement, place a 2.2nF to 100nF capacitor from IMON to GND to smooth the indicator voltage.

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The MP5990 can operate in parallel with multiple MP5991s or other devices for high-current applications. The current-balance loop balances the start-up current for each active channel. Connect the IMON pins of all devices together for current balancing. The sensed current from each active IMON pin is summed, then divided by the number of active channels. The resulting average load current (I_{LOAD}) provides a value for the total I_{LOAD}.

Start-up current balancing is essential to achieve the thermal advantages of parallel operation. Current sharing/balancing can aid power loss by dissipating the heat across the devices and the large area.

The MP5991's current balance is achieved by comparing the sensed CS current (I_{CS}) of each device to the average current. This creates an appropriate V_{GATE} adjustment for each Intelli-Fuse during start-up. The equivalent average R_{IMON} (R_{IMON_AVG}) can be calculated with Equation (6):

$$R_{IMON_AVG} = R_{CS} / N \quad (6)$$

Where N is the number of active devices.

Over-Current Limit Reference (OCREF)

The OCREF pin is a DAC output that sets the over-current reference (V_{OCREF}), which can be configured to be between 0V and 1.76V via register OC_REF (C6h).

The MP5990's I_{LOAD} is limited by V_{OCREF} and the external current-sense resistor (R_{CS}). To regulate V_{GATE}, V_{CS} is compared to V_{OCREF} through an amplifier. This prevents the Intelli-Fuse current from exceeding the current limit set by V_{OCREF}.

To protect the MP5990 from overheating during start-up, the OCREF pin has an internal clamp voltage (V_{OCREF_CLAMP}) that depends on V_{IN} and V_{OUT} (see Figure 6). If V_{OUT} is below 80% of V_{IN}, then V_{OCREF_CLAMP} is V_{BE} (about 635mV with a negative temperature coefficient). If V_{OUT} exceeds 80% of V_{IN}, then V_{OCREF_CLAMP} is released to 2V.

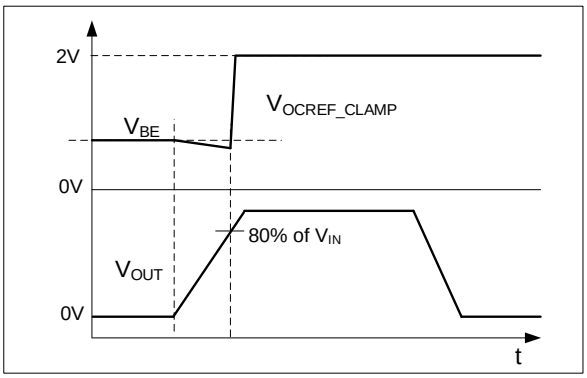

Figure 6: OCREF Internal Clamp Voltage

If V_{OCREF} is below V_{OCREF_CLAMP}, the actual current-limit reference voltage is determined by V_{OCREF}. If V_{OCREF} exceeds V_{OCREF_CLAMP}, the actual current-limit reference voltage is determined by V_{OCREF_CLAMP}.

Over-Current Protection (OCP)

The MP5990 provides two types of OCP: V_{IMON}-based total OCP and V_{CS}-based OCP on the Intelli-Fuse.

In multi-phase applications, Intelli-Fuse OCP can set the per-phase OCP limit. The total OCP limit can set the system's total OC limit.

The Intelli-Fuse over-current limit (I_{LIMIT}) is a function of the CS resistor (R_{CS}), current-sense gain (G_{CS}), and V_{OCREF}. I_{LIMIT} can be calculated with Equation (7):

$$I_{LIMIT} = \frac{V_{OCREF}}{G_{CS} \times R_{CS}} \quad (7)$$

The MP5990's current limit can exceed the normal maximum load current, allowing for tolerances in the current-sense value.

Intelli-Fuse OCP during Start-Up

If V_{CS} exceeds V_{OCREF} during SS, V_{GATE} is regulated to maintain a constant I_{FET}. If V_{OUT} is below 1/8 of V_{IN} and the MOSFET current is regulated by V_{OCREF} for 2.1ms, then the MOSFET turns off as a faulty latch condition and GOK is pulled low (see Figure 7 on page 23).

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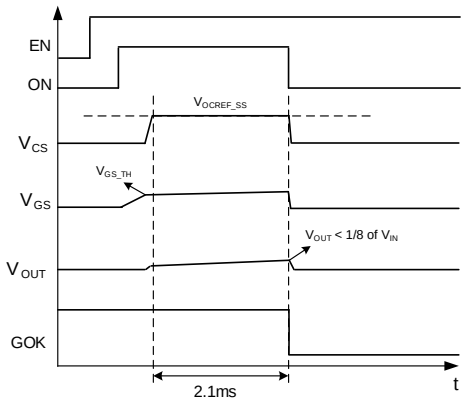

Figure 7: Failed Start-Up with Output Hard Short

Intelli-Fuse OCP at Normal Operation

If V_{OUT} exceeds 80% of V_{IN}, then the internal clamp voltage (V_{OCREF_CLAMP}) is released to 2V and V_{GATE} is close to the internal charge pump voltage. Once SS finishes, the MP5990 begins normal operation.

Once V_{CS} (configured via an external resistor) exceeds V_{OCREF}, the internal circuitry regulates V_{GATE} to maintain a constant current on the MOSFET. To limit I_{OUT}, the MOSFET's gate-to-source (GS) voltage (V_{GS}) is regulated from 3.3V to 1V. The response time is about 14µs. I_{OUT} may have a small overshoot during this response time.

If I_{OUT} exceeds the current limit (I_{LIMIT}), then the internal fault timer (220µs) starts. If I_{OUT} drops below I_{LIMIT} within the fault timer period, then the device resumes normal operation. If I_{OUT} exceeds I_{LIMIT} for 220µs, then the MOSFET latches off and GOK pulls low (see Figure 8).

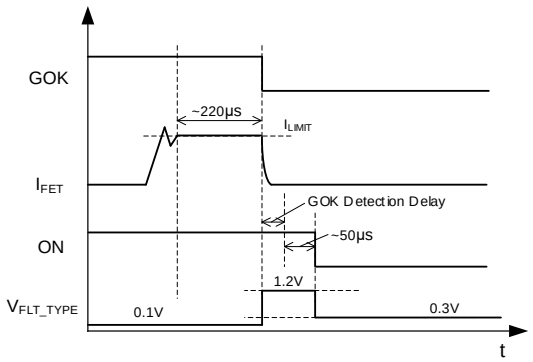

Figure 8: Intelli-Fuse OCP Behavior

If an Intelli-Fuse OC fault occurs, FLT_TYPE outputs 1.2V for about 50µs to indicate an OCP_FUSE fault. Then FLT_TYPE releases to 0.3V since ON is pulled low internally. The MP5990 samples the FLT_TYPE voltage during the 50µs hold time, then stores the detailed fault types to FAh, bits[2:0].

In latch-off mode, FLT_TYPE can be reset to 0.1V by cycling the power on VIN, VDD33, or EN, or by sending an ON command. Then the MOSFET turns on with soft start.

In hiccup mode, the MOSFET tries to soft start automatically and GOK is released high after the retry delay time ends. FLT_TYPE reset back to 0.1V after the retry delay time expires.

Total OCP

The MP5990 senses the total output current (I_{TTL}) through V_{IMON}. The sensed ADC value is converted into a direct I_{OUT}. R_{IMON} can be configured via IOUT_CAL_GAIN (38h) and stored in the NVM. The sensed I_{OUT} can be used for I_{OUT} reporting, OCW, and OCP. The total phase number should be configured via IOUT_GAIN_PHASE (4Dh) and stored in the NVM.

The total over-current limit (I_{TTL_LIMIT}) is configured via IOUT_OC_FAULT_LIMIT (46h), and the total OC delay time (t_{TTL_DELAY}) is configured by register PRT_DELAY (E8h). Total OCP can be configured for different protection modes via RETRY_TIMES (F4h) and PROTECT_CFG (E6h). These modes include no action, latch-off, retry (1 time to 14 times), and hiccup mode.

If the total current exceeds I_{TTL_LIMIT} for the total OCP fault timer, then the MP5990 pulls ON low to turn off all the paralleled devices. Then GOK pulls low to indicate that the fault event occurred. Meanwhile, the PG and SS pins pull low and the FLT_TYPE pin pulls to 0.3V (see Figure 9).

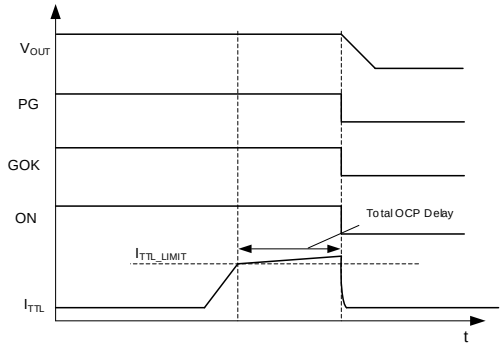

Figure 9: Total OCP Behavior

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Short-Circuit Current Limit (SCREF)

If the load current increases rapidly due to a short circuit, the current may exceed I_{LIMIT} before the hot-swap OC control loop can respond. If the Intelli-Fuse current reaches the short-circuit current limit (I_{LIMIT_SC}), a fast turn-off circuit in the Intelli-Fuse is enabled to turn the MOSFET off. The total short-circuit response time is about 200ns. If a short-circuit event occurs, the ON and GOK pins pull low.

To determine I_{LIMIT_SC}, the MP5990 samples the SCREF voltage during the insertion delay time after ON exceeds its UVLO threshold (see Figure 10). The short-circuit current limit is held once the insertion delay time ends. Changing the SCREF voltage after the insertion delay time does not affect the short-circuit current. To select a new short-circuit current limit, the user must initiate the next insertion delay.

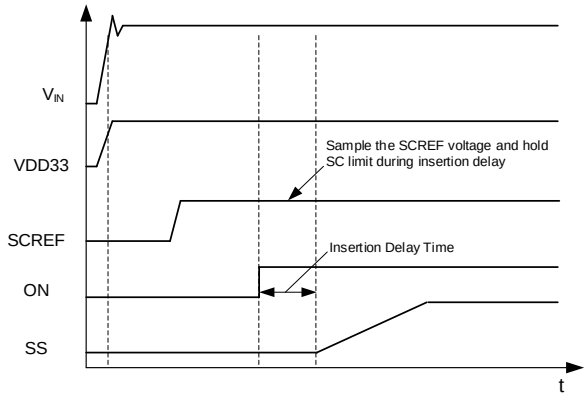

Figure 10: SCREF Samples and Holds the Short-Circuit Limit

The MP5990 provides five short-circuit levels. The level is selected by the SCREF voltage, which can be configured via OCW_SC_REF (C5h) and stored in the NVM. Table 1 shows the short-circuit current limit at different SCREF voltages.

Table1: SCP Limit Selection Table

V_{SCREF} (V)	SCP Limit (A)
<0.16	40
0.24 to 0.36	60
0.48 to 0.72	80
0.96 to 1.44	120
>1.68	100

The MP5990 provides short-circuit protection (SCP) to protect the part from a severe OC events, such as an output hard short to ground.

If the MOSFET current exceeds I_{LIMIT_SC}, the MOSFET turns off immediately, and GOK and SS pull low. FLT_TYPE indicates 1.5V for about 50µs to indicate SCP has occurred, then the ON pin is pulled low internally (see Figure 11).

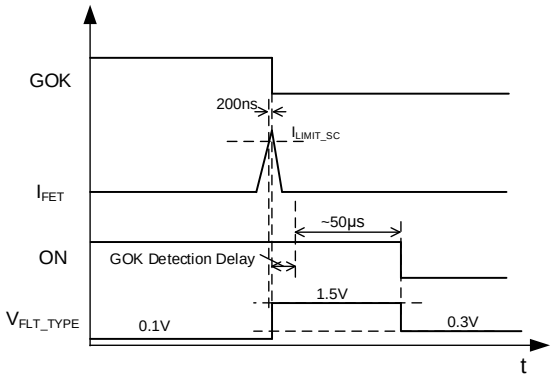

Figure 11: SCP Behavior

When a fault is cleared in latch-off mode, FLT_TYPE can be reset to 0.1V by cycling the power on VIN, VDD33, or EN, or by sending an ON command. Then the power MOSFET turns on with soft start.

In hiccup mode, the MOSFET tries to SS automatically, and GOK pulls high after the retry delay time ends. FLT_TYPE resets back to 0.1V after the retry delay time expires.

Input Voltage Sensing (VINSEN)

The MP5990 senses V_{IN} through the VINSEN pin. A resistor divider is connected from VIN to GND and tapped to VINSEN. Figure 12 shows the V_{IN} sense connection.

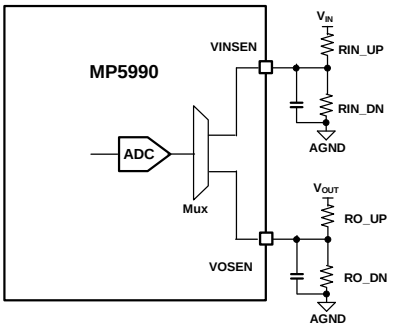

Figure 12: V_{IN} and V_{OUT} Sensing

The recommended top resistance for VINSEN is 75kΩ, and the recommended bottom resistance is 4.99kΩ. Place a 10nF capacitor in parallel with the bottom resistor.

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The sensed ADC value is converted into a direct V_{IN} value. The VINSEN divider ratio can be configured via VIN_SCALE (E4h) and stored in the NVM. The sensed V_{IN} is used for V_{IN} reporting, P_{IN} reporting, E_{IN} reporting, power MOSFET drain-to-source short detection, V_{IN} UVW alerts, and V_{IN} OVP.

Output Voltage Sensing (VOSEN)

The MP5990 senses V_{OUT} through the VOSEN pin. A resistor divider is connected from VOUT to GND and tapped to VOSEN. Figure 12 on page 24 shows the V_{OUT} sense connection. The recommended top resistor for VOSEN is 75kΩ, and the bottom resistor is 4.99kΩ. Place a 10nF capacitor in parallel with the bottom resistor.

The sensed ADC value is converted into a direct V_{OUT} value. The VOSEN divider ratio can be configured via VOUT_SCALE_LOOP (29h) and stored in the NVM. The sensed V_{OUT} is used for V_{OUT} reporting, P_{OUT} reporting, MOSFET drain-to-source short detection, and PG indication.

Temperature Sensing (VTEMP)

The MP5990 senses the on-die temperature and reports this value to the PMBus. When VDD33 exceeds its UVLO threshold and the MP5990 is in active mode, the VTEMP pin outputs a voltage proportional to T_J. The VTEMP output voltage (V_{TEMP}) is 8.7mV/°C with a 152.5mV offset. V_{TEMP} can be calculated with Equation (8):

$$V_{TEMP} = T_J \times 8.7mV + 152.5mV \quad (8)$$

For example, if T_J is 100°C, then V_{TEMP} is about 1.022V. If V_{TEMP} is 0V, then T_J is about -18°C. The total temperature sense range is -18°C to +140°C. When T_J is below -18°C, VTEMP remains at 0V.

In multi-phase applications, the VTEMP pins of each Intelli-Fuse can be connected to the MP5990's VTEMP pin (see Figure 13). VTEMP indicates the highest T_J of all the Intelli-Fuses. The MP5990 senses the voltage on VTEMP and reports the maximum temperature to the PMBus. The sensed temperature is used for system temperature monitoring, over-temperature warning (OTW), and OTP. Place a maximum 1nF capacitor and a minimum 10kΩ resistor on the VTEMP pin to filter noise.

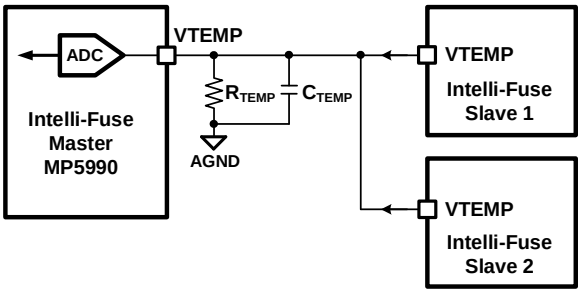

Figure 13: Multi-Fuse Temperature-Sense in Parallel Operation

Power Good (PG) Indicator

The PG/OCW# pin can be configured to PG or OCW# via ON_HICCUP_DLY (C7h), bit[13]. When this pin is set as PG, PG stays low until all of the following conditions are met:

- The ON pin is high
- V_{SS} > 340mV
- V_{OUT} > the PG rising threshold, which is configured via POWER_GOOD_ON (5Eh)
- No DS short event is occurring

PG pulls low if any of the following events occur:

- Shutdown events: EN turns off, V_{IN} UVLO, VDD33 UVLO, or an off command is received
- Fault events: DS short, total OCP, V_{IN} OVP, OTP, or GOK fault (slave fault). If any of the above fault events are detected, PG de-asserts low immediately
- V_{OUT} < PG falling threshold, which is configured via POWER_GOOD_OFF (5Fh)
- V_{SS} < 340mV, which is enabled when EFUSE_CFG (C4h), bit[11] is set to 1

GOK Report

The GOK pin is an open drain with an internal, weak pull-up, active-low signal that reports Intelli-Fuse faults. If a fault occurs, GOK pulls low.

Pull GOK up to the VDD33 via a 10kΩ to 100kΩ resistor. During start-up, the GOK voltage (V_{GOK}) rises according to V_{DD33}.

In multi-phase applications, the GOK pins of each Intelli-Fuse are connected together. The MP5990 provides a comparator on the GOK pin

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for control during parallel operation. If the GOK voltage is below 1.5V, the MP5990 registers a system fault and pulls ON low to turn off all paralleled devices. If any of the paralleled devices has fault event, the system shuts down.

D_OC and OCW# Reporting

The MP5990 provides two OCW indicators: D_OC and OCW#.

The D_OC pin is an open-drain, active-low output that reports an OCW condition when V_{OUT} ≥ 90% of V_{IN}. If V_{CS} exceeds the OCWREF voltage (V_{OCWREF}), D_OC is driven low. Once V_{CS} drops below V_{OCWREF} (the typical hysteresis voltage is 25mV), D_OC is released high again. Pull D_OC up to the VDD33 pin via a 10kΩ to 100kΩ resistor.

If PG/OCW# is set as OCW# and I_{TTL} exceeds the total OCW threshold, then OCW# pulls low immediately to indicate a total OCW event. Once I_{TTL} drops below the total OCW threshold, OCW# is released high again. The total OCW limit can be configured via IOUT_OC_WARN_LIMIT (4Ah).

VIN_UVW# Reporting

The VIN_UVW# pin is an open-drain, active-low output. Once V_{IN} drops below the V_{IN} under-voltage warning (UVW) threshold, VIN_UVW# pulls low immediately. When V_{IN} rises above the V_{IN} UVW threshold, VIN_UVW# is released high again. The V_{IN} UVW threshold can be configured via VIN_UV_WARN_LIMIT (58h).

Pull VIN_UVW# up to the VDD33 voltage via a 10kΩ to 100kΩ resistor.

Fault Type Indication (FLT_TYPE)

The MP5990 reports the fault type via the FLT_TYPE pin's voltage. Table 3 shows the FLT_TYPE voltage (V_{FLT_TYPE}) for each fault condition.

Table 2: Fault Type Indication

Fault Type	V_{FLT_TYPE}
SCP	1.5V
Intelli-Fuse OCP	1.2V
OTP (absolute 145°C limit), V_{IN} OVP (absolute 18.5V limit)	0.9V
DS/GS/GD short	0.6V
GOK fault	0.3V
No fault	0.1V

In multi-phase applications, the FLT_TYPE pin of each Intelli-Fuse can be connected to the MP5990's FLT_TYPE pin to indicate the most serious fault event in the system. The voltage indicates the associated value when the fault is real and the MOSFET has turned off. For example, if Intelli-Fuse OCP occurs, FLT_TYPE outputs 1.2V when the 220µs hold time ends and the MOSFET starts to turn off. If multiple faults occur simultaneously, the higher voltage has higher priority. For example, if an Intelli-Fuse OCP and OTP (absolute 145°C limit is triggered) fault occur simultaneously, FLT_TYPE is set to 1.2V. Figure 14 shows FLY_TYPE indication based on Table 2.

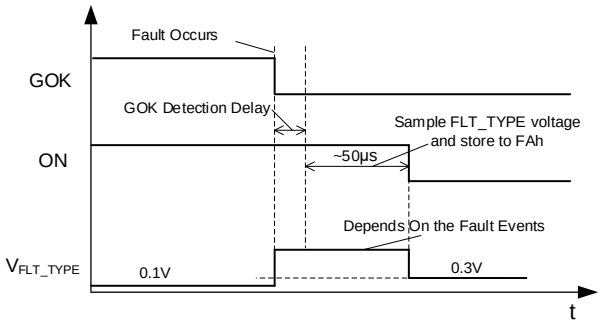

Figure 14: FLT_TYPE Indication

If any of the fault events listed in Table 2 occur, GOK pulls low immediately and the FLT_TYPE pin outputs the corresponding voltage (see Figure 14). The ON pin pulls low after a delay time, which includes the GOK detection delay time (0µs to 15µs, as set by register E8h) plus a 50µs sample delay time. The FLT_TYPE pin voltage is sampled and stored to the register FAh. Once the delay time ends, the FLT_TYPE pin voltage is released to 0.3V.

If a fault not mentioned in Table 2 occurs (e.g. total OCP or V_{TEMP}-sensed OTP), then the GOK, ON and SS pins pull low immediately, and FLT_TYPE indicates 0.3V (see Figure 15 on page 27).

If CFG_EXT (F5h), bit[5] is set to 1, the MP5990 does not sample the FLT_TYPE voltage when the faults not listed in Table 2 occur.

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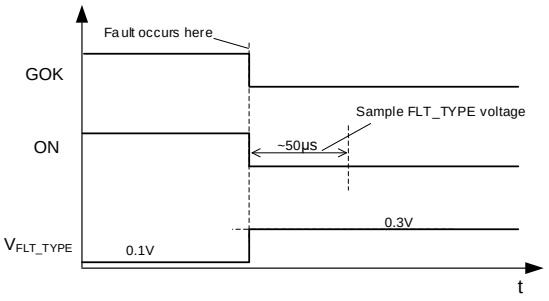

Figure 15: FLT_TYPE Indication of Other Faults

Do not connect a resistor from the FLT_TYPE pin to GND. Never short the FLT_TYPE pin to ground.

Additional Protections

The MP5990 provides additional protections, described below.

Over-Temperature Protection (OTP)

The MP5990 provides three types of OTP: MOSFET (Intelli-Fuse) on-die temperature protection, controller on-die temperature protection, and V_{TEMP}-sensed OTP.

The MP5990 senses T_J internally on the MOSFET. If T_J exceeds the 145°C threshold, the MOSFET turns off, and GOK and SS pull low. If there is no higher-priority fault, FLT_TYPE outputs 0.9V for about 50µs to indicate an OT fault, then ON is pulled low internally.

The MP5990 senses the MOSFET temperature via the VTEMP pin. The ADC-sensed value is converted into a direct temperature for the MOSFET. If the sensed temperature exceeds the OT threshold, the MP5990 pulls ON low to turn off the MOSFET. Meanwhile, GOK and SS are pulled low immediately. The V_{TEMP}-sensed OT threshold can be configured via OT_FAULT_LIMIT (4Fh). The protection mode can be set via RETRY_TIMES (F4h).

If the temperature drops below the falling threshold in latch-off mode, the MOSFET does not turn on again and soft start is not initiated until power is cycled on VIN, VDD33, or EN, or an ON command is received.

In hiccup mode, the retry delay time initiates when T_J falls below the falling threshold. Once the retry delay time expires, the MOSFET tries to soft start automatically and GOK is released high. The retry delay time can be configured via ON_HICCUP_DELAY (C7h). FLT_TYPE resets back to 0.1V after the retry delay time expires.

The MP5990 also monitors the controller's on-die temperature. Once the on-die temperature exceeds 165°C, the MOSFET turns off immediately. Controller on-die OTP provides latch-off and hiccup mode.

V_{IN} Over-Voltage Protection (V_{IN} OVP)

The MP5990 monitors V_{IN} via the VINSEN pin. The V_{IN} over-voltage (OV) rising threshold can be configured via VIN_OV_FAULT_LIMIT (55h). If V_{IN} exceeds the OV rising threshold, the ON, GOK, and SS pins are pulled low immediately.

The MP5990 has an absolute 18.5V input OVP limit, which works when VIN_OV_FAULT_LIMIT (55h) is set above 18.5V. If V_{IN} exceeds 18.5V and there is no other high-priority fault, the MOSFET turns off and FLT_TYPE indicates 0.9V for 50µs to indicate an OV event.

If the 18.5V V_{IN} OVP is triggered in latch-off mode, once V_{IN} drops below its falling threshold (17.3V), there are a few methods to reset FLT_TYPE to 0.1V and turn on the MOSFET with a soft start:

- Power is cycled on VIN, VDD33, or EN
- An ON command is received

If the 18.5V V_{IN} OVP is triggered in hiccup mode, then the retry delay time initiates when VIN falls below 17.3V. Once the retry delay time expires, the MOSFET tries to soft start automatically and GOK is released high. FLT_TYPE resets to 0.1V after the retry delay time expires.

Damaged Intelli-Fuse MOSFET Detection

The MP5990 can detect a shorted power MOSFET during start-up. Once VDD33 exceeds 2.7V and ON exceeds 1.4V, the MP5990 recognizes the condition that V_{OUT} exceeds 90% of V_{IN} before the insertion delay finishes as a shorted MOSFET. If V_{OUT} exceeds 90% of V_{IN} during start-up, GOK pulls low and FLT_TYPE indicates 0.6V for 50µs to indicate a DS/GS/GD fault.

If V_{OUT} drops below 70% of V_{IN}, the MOSFET does not turn on again and soft start is not initiated until power is cycled on VIN, VDD33, or EN, or an ON command is received.

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Power MOSFET Not Fully On

After the MP5990 is enabled and V_{OUT} begins ramping, the device recognizes a MOSFET not fully on fault event if all of the following conditions are met:

- V_{SS} > VDD33 - 0.7V
- V_{GS} < V_{CP} - 0.7V
- No OC event has occurred
- No SC event has occurred

When these conditions are met, this indicates that the MOSFET is not fully on. The MP5990 stops regulating the gate voltage and turns off the MOSFET after a 250ms delay. Meanwhile, GOK and SS pull low (see Figure 16). FLT_TYPE indicates 0.6V for 50μs to indicate a DS/GS/GD fault. Then FLT_TYPE is released to 0.3V.

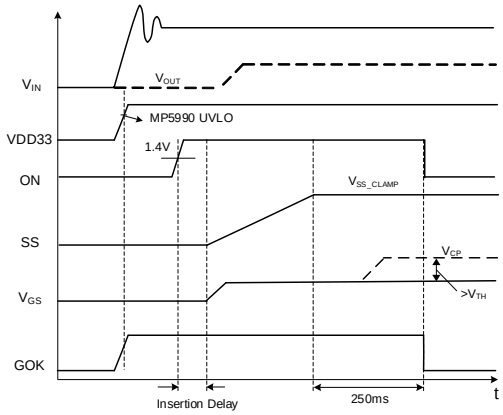

Figure 16: Power MOSFET Not Fully On Fault in Latch-Off Mode

In latch-off mode, the MOSFET does not turn on again and soft start is not initiated until power is cycled on VIN, VDD33, or EN, or an ON command is received.

In hiccup mode, the MOSFET tries to soft start automatically and GOK pulls high after a retry delay time.

Maximum SS Fault

The MP5990 detects the voltage of SS pin (V_{SS}) to check whether the MOSFET is fully enhanced. The maximum SS timer starts counting when ON exceeds its rising threshold. If V_{SS} is below 340mV when the maximum SS timer finishes, then ON, GOK, and SS pull low. The maximum SS fault protection mode can be configured to latch-off or hiccup mode via EFUSE_CFG (C4h), bit[13]. The maximum SS fault timer can be configured via MAX_SS_TIMER (C7h). The maximum fault timer is 600ms.

GOK Fault

A comparator on the GOK pin controls parallel operation. If the GOK voltage is below 1.5V, FLT_TYPE indicates 0.3V. Then the MP5990 registers a system fault and turns off the MOSFET with a 50μs delay time.

The GOK fault can be configured to latch-off or hiccup mode via RETRY_TIMES (F4h).

In latch-off mode, the MOSFET does not turn on again and soft start is not initiated until power is cycled on VIN, VDD33, or EN, or an ON command is received.

In hiccup mode, the MOSFET tries to soft start automatically and GOK pulls high after a retry delay time.

For standalone operation, GOK has an internal 370kΩ pull-up resistor to avoid falsely triggering a GOK fault when there is no external pull-up resistor.

Under-Voltage Lockout (UVLO) Protection

The MP5990 has two V_{IN} UVLO protections. The first is an absolute V_{IN} UVLO protection, with a fixed 3.2V rising threshold and 2.9V falling threshold. The second is a PMBus-configurable V_{IN} UVLO. The rising and falling thresholds can be configured via VIN_ON (35h) and VIN_OFF (36h). The PMBus-configurable V_{IN} UVLO protection can be disabled via VIN_PROTECT_EN (E6h), bit[0]. The protection mode can be configured via EFUSE_CFG (C4h), bit[7].

The MP5990 can start up only when both VDD33 and V_{IN} exceed their respective UVLO rising thresholds. The actual V_{IN} UVLO rising threshold that the MP5990 responds to is the larger value between VIN_ON (35h) and 3.2V.

The MP5990 shuts down when either the VDD33 drops below its UVLO falling threshold (typically 2.3V) or V_{IN} drops below its UVLO falling threshold.

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The actual V_{IN} UVLO falling threshold that the MP5990 responds to is the larger value between VIN_OFF (36h) and 2.9V.

These UVLO protections cannot be set to latch-off mode.

Input and Output Transient Protection

The hot-swap system experiences positive transients on the input during a hot plug or rapid turn-off with a high current due to parasitic inductance in the input circuit. For input transient protection, place a transient voltage suppressor (TVS) diode on the input to limit transient voltages below the absolute maximum ratings.

The output may experience negative transients during rapid turn-off with high current due to inductance in the output circuit. If a transient makes V_{OUT} more negative, the MOSFET may not turn off properly. Place an output voltage clamp diode on the output to limit negative transients. It is recommended to use a Schottky diode with a low forward voltage.

Parallel Operation

The MP5990 can be used in parallel operation with the Intelli-Fuse (MP5991) to support higher currents with a maximum 20-phase limit. The MP5990 works as a master to control the system's start-up/shutdown sequences.

The following connections are required for multiple fuses in parallel operation (see the Typical Application section on page 3 for more details):

1. Connect the VIN pins to the same input bus.
2. Connect the VOUT pins to the same output bus.
3. Tie the ON pins together for start-up sequence control.
4. Tie the SS pins together for soft start sequence control.
5. Tie the GOK pins together for system fault control.
6. Design the CS resistor (R_{CS}) with the same resistance for each phase.
7. Tie the IMON pins together and design the total system IMON resistor (R_{IMON}) as R_{CS} / N, where N is the phase count. This helps to achieve soft start current balance control.
8. Tie the OCREF pins together.
9. Connect a 120kΩ resistor to each MODE pin.
10. Tie the VTEMP pins together so that VTEMP always reports the highest T_J of all phases.
11. When applicable, connect all the FLT_TYPE pins together to indicate the most serious fault event in the system.

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PMBUS/I²C COMMUNICATION

General Description

The power management bus (PMBus) is an open-standard power management protocol that defines a means of communicating with power conversion and other devices. It is a two-wire, bidirectional serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are externally pulled to a bus voltage when they are idle. Connecting to the line, a master device generates the SCL signal and device address, then arranges the communication sequence. This is based on the I²C operation principles.

The MP5990 supports 100kHz, 400kHz, and 1MHz bus timing requirements. The timing and electrical characteristics of the PMBus can be found in the Electrical Characteristics section on page 11 or in the PMBus Power System Management Protocol Specification, part 1, revision 1.3, available at http://PMBus.org.

PMBus/I²C Address

To support multiple devices using the same PMBus/I²C interface, the MP5990 provides a configurable PMBus address via the ADDR pin or register ADDR_PMBUS (D2h).

The device address is a 7-bit code that ranges between 0x00 and 0x7F. The 3MSB (most significant bits) are set by D2h, bits[6:4]. The 4LSB (least significant bits) can be set by either D2h or the ADDR pin.

The device's 4LSB address configuration mode can be selected by D2h, bit[7]. When bit[7] = 1, the 4LSB are determined by the lower 4 bits in D2h. When bit[7] = 0, the ADDR voltage determines the 4LSB.

The ADDR voltage is configured by the resistor divider from VDD18 to GND. Figure 19 on page 31 shows the recommended connections for the pin. Table 3 shows the resistor values for the different device address.

The address 00h is reserved as the all call address. Do not set 00h as the MP5990's unique device address.

Table 3: PMBus 4LSB Address Setting from ADDR

PMBus Address Bits[3:0]	ADDR Voltage (V)	R_{TOP} (kΩ) 1%	R_{BOT} (kΩ) 1%
0h	0	-	0
1h	0.038	3.32	0.0715
2h	0.065	3.32	0.124
3h	0.090	3.32	0.174
4h	0.116	3.32	0.226
5h	0.156	3.32	0.316
6h	0.205	3.32	0.43
7h	0.266	3.32	0.576
8h	0.340	3.32	0.768
9h	0.430	3.32	1.05
Ah	0.540	3.32	1.43
Bh	0.675	3.32	2
Ch	0.844	3.32	2.94
Dh	1.048	3.32	4.64
Eh	1.301	3.32	8.66
Fh	1.500	3.32	16.5

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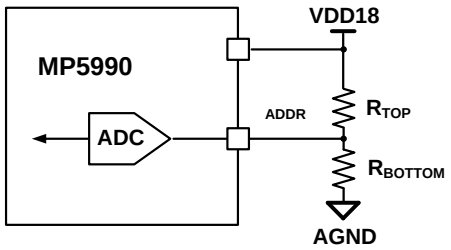

Figure 19: Recommended Circuit Design for PMBus Address Pin Set

PMBus Communication Failure

A data transmission fault occurs when data is not properly transferred between devices. There are several data transmission faults, listed below.

- Sending too little data
- Reading too little data
- The host sends too many bytes
- Reading too many bytes
- Improperly set read bit in the address byte
- Unsupported command code

The communication failure is recorded into STATUS_CML (7Eh). The CLEAR_FAULTS (03h) command can clear the fault record.

PMBus/I²C Transmission Structure

The MP5990 supports 5 kinds of transmission structures with or without packet error checking (PEC):

1. Send command only
2. Write byte
3. Write word
4. Read byte
5. Read word

The MP5990 supports the PEC mechanism, which can improve reliability and make communication more robust. The PEC is a CRC-8 error checking byte, calculated on all the message bytes (including addresses and read/write bits). The MP5990 only processes the message if the PEC is correct. If the PEC byte sent to the MP5990 is incorrect, then 7Eh, bit[5] is set and latched. The ALT# pin does not indicate low when the PEC byte is incorrect.

The PEC is calculated in CRC-8, calculated with the polynomial in Equation (8):

$$C(x) = x^8 + x^2 + x^1 + 1 \quad (8)$$

Figure 20 shows the supported PMBus/I²C transmission structure without PEC.

Figure 21 on page 32 shows the supported PMBus/I²C transmission structure with PEC.

To read or write to the MP5990's registers, the PMBus/I²C command must be compliant with the byte number of the registers in the register map.

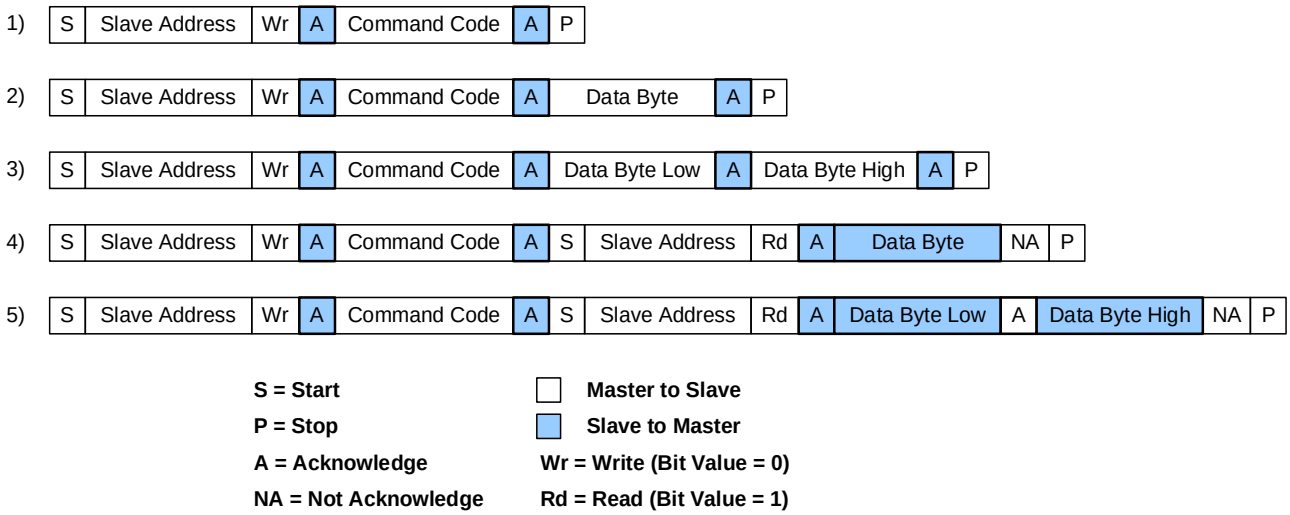

Figure 20: Supported PMBus/I²C Transmission Structure without PEC

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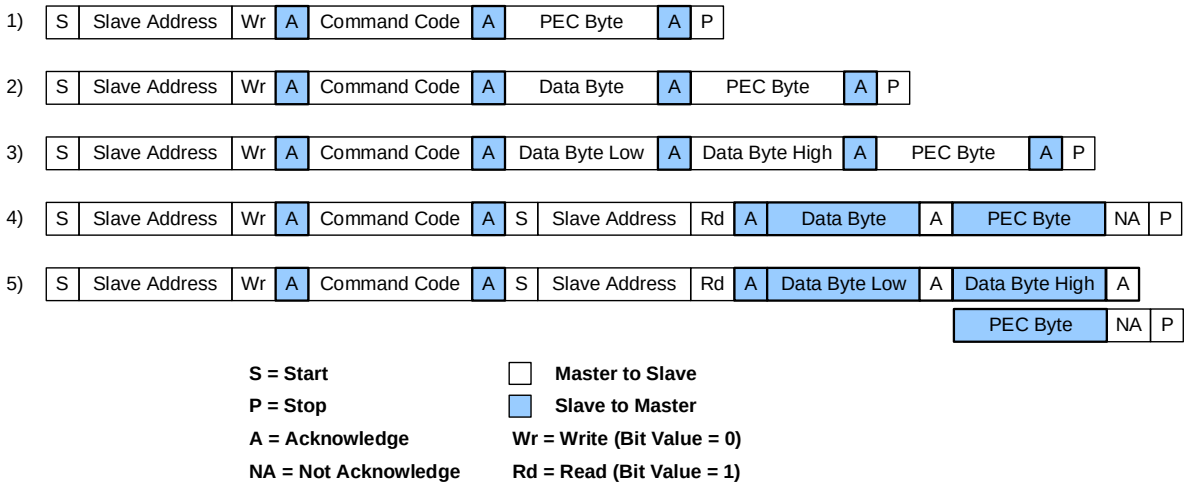

Figure 21: Supported PMBus/I²C Transmission Structure with PEC

PMBus Reporting and Status Monitoring

The MP5990 supports real-time monitoring of the e-fuse operation parameters and statuses via the PMBus interface.

Table 4 lists the monitored parameters.

Table 4: PMBus-Monitored Parameters

Parameter	Resolution	Register
Input energy	1J/LSB	86h
V_{IN}	31.25mV/LSB	88h
V_{OUT}	31.25mV/LSB	8Bh
I_{OUT}	62.5mA/LSB	8Ch
Temperature	1°C/LSB	8Dh
P_{OUT}	1W/LSB	96h
P_{IN}	1W/LSB	97h
PG	-	79h, bit[11]
Total OC fault	-	79h, bit[4]; 7Bh, bit[7]
Total OC warning	-	7Bh, bit[5]
OP warning	-	7Bh, bit[0]
OT fault	-	7Dh, bit[7]
OT warning	-	7Dh, bit[6]
V_{IN} UVLO	-	79h, bit[3]; 7Ch, bit[4]
V_{IN} UV warning	-	7Ch, bit[5]
V_{IN} OVP	-	7Ch, bit[7]
Slave fault	-	79h, bit[9]
CML fault	-	7Eh

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SUPPORTED PMBUS COMMAND LIST

Command Name	Code	Type	Bytes	Default Value for the 4-Digit "-0000" Code
OPERATION	01h	R/W	1	80h
CLEAR_FAULT	03h	Send byte	0	-
CLEAR_LAST_FAULT	08h	Send byte	0	-
LAST_FAULT_RESTORE	0Ch	Send byte	0	-
POWER_CYCLE	0Fh	Send byte	0	-
WRITE_PROTECTION	10h	R/W	1	00h
STORE_ALL	15h	Send byte	0	-
RESTORE_ALL	16h	Send byte	0	-
CAPABILITY	19h	R	1	D0h
VOUT_SCALE_LOOP	29h	R/W	2	0140h
VIN_ON	35h	R/W	2	0023h
VIN_OFF	36h	R/W	2	0020h
IOUT_CAL_GAIN	38h	R/W	2	0280h
IOUT_CAL_OFFSET	39h	R/W	2	0000h
IOUT_OC_FAULT_LIMIT	46h	R/W	2	0037h
IOUT_OC_WARN_LIMIT	4Ah	R/W	2	0034h
IOUT_GAIN_PHASE	4Dh	R/W	2	0002h
OT_FAULT_LIMIT	4Fh	R/W	2	007Dh
OT_WARN_LIMIT	51h	R/W	2	006Eh
VIN_OV_FAULT_LIMIT	55h	R/W	2	0048h
VIN_OV_WARN_LIMIT	57h	R/W	2	0044h
VIN_UV_WARN_LIMIT	58h	R/W	2	0022h
POWER_GOOD_ON	5Eh	R/W	2	0080h
POWER_GOOD_OFF	5Fh	R/W	2	0070h
TON_DELAY	60h	R/W	2	0064h
TOFF_DELAY	64h	R/W	2	0000h
OP_WARN_LIMIT	6Ah	R/W	2	00A1h
STATUS_BYTE	78h	R	1	0
STATUS_WORD	79h	R	2	0
STATUS_IOUT	7Bh	R	1	0
STATUS_INPUT	7Ch	R	1	0
STATUS_TEMPERATURE	7Dh	R	1	0
STATUS_CML	7Eh	R	1	0
REV_ID	80h	R	1	0
READ_EIN	86h	R	6	0
READ_VIN	88h	R	2	0
READ_VOUT	8Bh	R	2	0
READ_IOUT	8Ch	R	2	0
READ_TEMPERATURE	8Dh	R	2	0
READ_POUT	96h	R	2	0

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SUPPORTED PMBUS COMMAND LIST *(continued)*

Command Name	Code	Type	Bytes	Default Value for the 4-Digit "-0000" Code
READ_PIN	97h	R	2	0
PMBUS_REV_CONST	98h	R	1	33h
VENDOR_ID	99h	R	3	4D5053h
PRODUCT_ID	9Ah	R	6	4D5035393930h
REV_CONST	9Bh	R	1	0
READ_VIN_PEAK	A1h	R	2	0
READ_PIN_PEAK	A3h	R	2	0
READ_VOUT_PEAK	A5h	R	2	0
READ_IOUT_PEAK	A6h	R	2	0
READ_TEMP_PEAK	AFh	R	2	0
CONFIG_ID	C0h	R/W	2	0000h
CONFIG_CODE_REV	C1h	R/W	2	0002h
PRODUCT_REV_USER	C2h	R/W	2	0000h
REV_CONST_CFG	C3h	R/W	1	00h
EFUSE_CFG	C4h	R/W	2	6888h
OCW_SC_REF	C5h	R/W	2	0FE5h
OC_REF	C6h	R/W	1	2Bh
ON_HICCUP_DLY	C7h	R/W	2	1019h
SYS_INITIAL_DELAY	D0h	R/W	2	0005h
ADDR_PMBUS	D2h	R/W	2	0040h
VIN_CFG	E3h	R/W	2	0000h
VIN_SCALE	E4h	R/W	2	0140h
TEMP_TUNE	E5h	R/W	2	CF5Ch
PROTECT_CFG	E6h	R/W	2	55EBh
VIN_PROTECT_LEVEL	E7h	R/W	2	00A0h
PRT_DELAY	E8h	R/W	2	5555h
SMBALERT_MASK	E9h	R/W	2	8000h
LEVEL_SEL	EBh	R/W	2	0401h
ADVANCE_CTRL	F1h	R/W	2	0D60h
RETRY_TIMES	F4h	R/W	2	0000h
CFG_EXT	F5h	R/W	2	0000h
CHECK_SUM_FUNC	F8h	R	2	0
FAULT_RECORD	FAh	R	2	0
FAULT_RECORD_LAST	FBh	R	2	0
CLEAR_MTP_FAULT	FEh	Send byte	0	-

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REGISTER MAP

OPERATION (01h)

The OPERATION command controls the power MOSFET, which provides another way to control the hot-swap on/off function via the PMBus. This command can turn the power MOSFET on and off under host control and re-enable the power MOSFET after a fault-triggered shutdown.

Command	OPERATION							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function		X	X	X	X	X	X	X

Bits	Bit Name	Description
7	ON_OFF_STATE	1'b0: Turn off the power MOSFET 1'b1: Turn on the power MOSFET
6:0	RESERVED	Always write into 6'b 00 0000.

CLEAR_FAULT (03h)

The CLEAR_FAULT command clears all the status faults of the read-only STATUS registers (78h~7Eh). This command is write-only. There is no byte for this command.

CLEAR_LAST_FAULT (08h)

The CLEAR_LAST_FAULT command clears the last fault stored in NVM, and can clear the last faults stored in FBh (this function is optional). The information stored in FBh is cleared if F5h, bit[6] is set to 1. This command is write-only. There is no byte for this command.

LAST_FAULT_RESTORE (0Ch)

The LAST_FAULT_RESTORE command restores the latest fault information in the NVM to register FBh. This command is write-only. There is no byte for this command.

POWER_CYCLE (0Fh)

The POWER_CYCLE command turns the power MOSFET off for approximately 5 seconds. Then the power MOSFET restarts automatically. This command is write-only. There is no byte for this command.

WRITE_PROTECTION (10h)

The WRITE_PROTECTION command controls writing to the PMBus device. This provides protection against accidental changes. This command is not intended to provide protection against deliberate changes to a device's configuration or operation. All supported commands can have their parameters read, regardless of the WRITE_PROTECTION settings.

Command	WRITE_PROTECTION							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	WRITE_PROTECTION							

Bits	Bit Name	Description
7:0	WRITE_PROTECTION	8'b0000 0000: Enable writes to all commands 8'b01x0 0000: Disable all writes except to the PAGE, OPERATION, WRITE_PROTECTION 8'b1000 0000: Disable all writes except to the WRITE_PROTECTION commands Others: No action. Keep the previous setting

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STORE_ALL (15h)

The STORE_ALL command stores all registers to the NVM. It can be configured by F5h, bit[3] to select whether to store the fault information from FAh to the NVM after sending a 15h command. If F5h, bit[3] is set to 0, all registers are stored to the NVM, including FAh. If F5h, bit[3] is set to 1, all registers besides FAh are stored to the NVM. This command is write-only. There is no byte for this command.

RESTORE_ALL (16h)

The RESTORE_ALL command restores all registers from the NVM. This command is write-only. There is no byte for this command.

CAPABILITY (19h)

The CAPABILITY command provides 1 byte to return the key capabilities that the PMBus device can support. The MP5990 always return 0xD0.

Command	CAPABILITY							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function		MAX_BUS_SPEED					X	X

Bits	Bit Name	Description
7	PEC_SUPPORT	1'b1: Packet error checking (PEC) is supported
6:5	MAX_BUS_SPEED	2'b10: The maximum supported bus speed is 1MHz
4	SMBALERT_SUPPORT	1'b1: The device does have an SMBALERT# pin and does support the SMBus alert response protocol
3	NUMERIC_FORMAT	1'b0: Numeric data is in Linear11, ULinear16, SLinear16, or direct format
2	AVSBUS_SUPPORT	1'b0: The AVSBus is not supported
1:0	RESERVED	1'bx: Reserved

VOUT_SCALE_LOOP (29h)

The VOUT_SCALE_LOOP command sets the V_{OUT} divider ratio (see Figure 22).

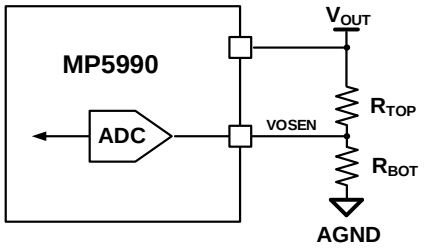

Figure 22: Output Voltage Sense Circuit Design

Command	VOUT_SCALE_LOOP															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	VOUT_SCALE_LOOP										

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates writes are ignored and reads are always 0.

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10:0	VOUT_SCALE_LOOP	Sets VOUT_SCALE_LOOP, calculated with the following equation: VOUT_SCALE_LOOP = 5120 x R_{BOT} / (R_{TOP} + R_{BOT}).

VIN_ON (35h)

The VIN_ON command sets the V_{IN} under-voltage lockout (UVLO) rising threshold.

Command	VIN_ON															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X	X	VIN_ON						

Bits	Bit Name	Description
15:7	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
6:0	VIN_ON	Sets the V_{IN} UVLO rising threshold, calculated with the following equation: Rising threshold = (VIN_ON + 1) x Resolution. Where VIN_ON is bits[6:0] of this command, and Resolution is determined by C4h, bit[6] and E7h, bit[7]. 500mV/LSB when C4h, bit[6] = 0 and E7h, bit[7] = 0; supports up to 64V 250mV/LSB when C4h, bit[6] = 0 and E7h, bit[7] = 1; supports up to 32V 125mV/LSB when C4h, bit[6] = 1; supports up to 16V

VIN_OFF (36h)

The VIN_OFF command sets the V_{IN} under-voltage lockout (UVLO) falling threshold.

Command	VIN_OFF															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X	X	VIN_OFF						

Bits	Bit Name	Description
15:7	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
6:0	VIN_OFF	Sets the V_{IN} UVLO falling threshold, calculated with the following equation: Falling threshold = VIN_OFF x Resolution Where the VIN_OFF is bits[6:0] of this command and Resolution is determined by C4h, bit[6] and E7h, bit[7]. 500mV/LSB when C4h, bit[6] = 0 and E7h, bit[7] = 0; supports up to 64V 250mV/LSB when C4h, bit[6] = 0 and E7h, bit[7] = 1; supports up to 32V 125mV/LSB when C4h, bit[6] = 1; supports up to 16V

IOUT_CAL_GAIN (38h)

The IOUT_CAL_GAIN command sets the I_{OUT} report gain. The reported I_{OUT} is returned via PMBus command READ_IOUT (8Ch).

Command	IOUT_CAL_GAIN															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	IOUT_CAL_GAIN										

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Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10:0	IOUT_CAL_GAIN	Sets the I_{OUT} calculation gain, calculated with the following equation: IOUT_CAL_GAIN = 12.8 / (G_{IMON} x R_{IMON} x N), Where G_{IMON} is 10μA/A, R_{IMON} is the equivalent resistor of the IMON pin, and N is phase count in parallel operation.

IOUT_CAL_OFFSET (39h)

The IOUT_CAL_OFFSET sets any offsets in the I_{OUT} sense circuit. Typically, this command is used with IOUT_CAL_GAIN (38h) to minimize the current-sense circuit error.

Command	IOUT_CAL_OFFSET															
Format	Two's complement															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	IOUT_CAL_OFFSET								

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	IOUT_CAL_OFFSET	Sets the I_{OUT} calculation offset. It is in two's complement format. Bit[8] is the signed bit. The current list below shows the binary data and the real-world current values. 8'b 0000 0000: 0 8'b 0000 0001: (+1 x 0.0625) A 8'b 0111 1111: (+127 x 0.0625) A 8'b 1000 0000: (-128 x 0.0625) A 8'b 1000 0001: (-127 x 0.0625) A 8'b 1111 1111: (-1 x 0.0625) A

IOUT_OC_FAULT_LIMIT (46h)

The IOUT_OC_FAULT_LIMIT command sets the limit for the V_{IMON}-based total over-current protection (OCP).

Command	IOUT_OC_FAULT_LIMIT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	IOUT_OC_FAULT_LIMIT									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	IOUT_OC_FAULT_LIMIT	Sets the limit for the V_{IMON}-based total OCP. 1A/LSB.

IOUT_OC_WARN_LIMIT (4Ah)

The IOUT_OC_WARN_LIMIT command sets the warning limit for the V_{IMON}-based total OCP.

Command	IOUT_OC_WARN_LIMIT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	IOUT_OC_WARN_LIMIT									

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Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	IOUT_OC_WARN_LIMIT	Sets the warning limit for V_{IMON}-based total OCP. 1A/LSB.

IOUT_GAIN_PHASE (4Dh)

The IOUT_GAIN_PHASE command sets the paralleled phase count.

Command	IOUT_GAIN_PHASE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	IOUT_GAIN_PHASE									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	IOUT_GAIN_PHASE	Sets the e-fuse phase count for the I_{OUT} PMBus report, calculated with the following equation: IOUT_GAIN_PHASE = 2 x N Where N is the e-fuse phase count.

OT_FAULT_LIMIT (4Fh)

The OT_FAULT_LIMIT command sets the over-temperature (OT) fault limit for a V_{TEMP}-based OT fault.

Command	OT_FAULT_LIMIT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X	OT_FAULT_LIMIT							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	OT_FAULT_LIMIT	Sets the OT fault limit for a V_{TEMP}-based OT fault. 1°C/LSB.

OT_WARN_LIMIT (51h)

The OT_WARN_LIMIT command sets the warning limit for a V_{TEMP}-based over-temperature (OT) fault.

Command	OT_WARN_LIMIT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X	OT_WARN_LIMIT							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	OT_WARN_LIMIT	Sets the OT warning limit for a V_{TEMP}-based OT fault. 1°C/LSB.

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VIN_OV_FAULT_LIMIT (55h)

The VIN_OV_FAULT_LIMIT command sets the V_{IN} over-voltage (OV) fault limit.

Command	VIN_OV_FAULT_LIMIT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X	X	VIN_OV_FAULT_LIMIT						

Bits	Bit Name	Description
15:7	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
6:0	VIN_OV_FAULT_LIMIT	Sets the V_{IN} OV fault threshold, calculated with the following equation: V_{IN} OV threshold = VIN_OV_FAULT_LIMIT x Resolution Where VIN_OV_FAULT_LIMIT is bits[6:0] of this command and Resolution is determined by C4h, bit[6] and E7h, bit[7]. 500mV/LSB when C4h, bit[6] = 0 and E7h, bit[7] = 0; supports up to 64V 250mV/LSB when C4h, bit[6] = 0 and E7h, bit[7] = 1; supports up to 32V 125mV/LSB when C4h, bit[6] = 1; supports up to 16V

VIN_OV_WARN_LIMIT (57h)

The VIN_OV_WARN_LIMIT command sets the V_{IN} over-voltage (OV) warning limit.

Command	VIN_OV_WARN_LIMIT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X	X	VIN_OV_WARN_LIMIT						

Bits	Bit Name	Description
15:7	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
6:0	VIN_OV_WARN_LIMIT	Set the V_{IN} OV warning threshold, calculated with the following equation: V_{IN} OV warning = VIN_OV_WARN_LIMIT x Resolution. Where VIN_OV_WARN_LIMIT is bits[6:0] of this command and Resolution is determined by C4h, bit[6] and E7h, bit[7]. 500mV/LSB when C4h, bit[6] = 0 and E7h, bit[7] = 0; supports up to 64V 250mV/LSB when C4h, bit[6] = 0 and E7h, bit[7] = 1; supports up to 32V 125mV/LSB when C4h, bit[6] = 1; supports up to 16V

VIN_UV_WARN_LIMIT (58h)

The VIN_UV_WARN_LIMIT command sets the V_{IN} under-voltage warning (UVW) limit.

Command	VIN_UV_WARN_LIMIT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X	X	VIN_UV_WARN_LIMIT						

Bits	Bit Name	Description
15:7	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.

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6:0	VIN_UV_WARN_LIMIT	Set the V_{IN} UVW threshold, calculated with the following equation: V_{IN} UVW threshold = VIN_UV_WARN_LIMIT x Resolution. Where VIN_UV_WARN_LIMIT is bits[6:0] of this command and Resolution is determined by C4h, bit[6] and E7h, bit[7]. 500mV/LSB when C4h, bit[6] = 0 and E7h, bit[7] = 0; supports up to 64V 250mV/LSB when C4h, bit[6] = 0 and E7h, bit[7] = 1; supports up to 32V 125mV/LSB when C4h, bit[6] = 1; supports up to 16V

POWER_GOOD_ON (5Eh)

The POWER_GOOD_ON command sets the power good (PG) rising threshold.

Command	POWER_GOOD_ON															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	POWER_GOOD_ON									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	POWER_GOOD_ON	Sets the voltage at which PG pulls high. 62.5mV/LSB.

POWER_GOOD_OFF (5Fh)

The POWER_GOOD_OFF command sets the power good (PG) falling threshold.

Command	POWER_GOOD_OFF															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	POWER_GOOD_OFF									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates writes are ignored and reads are always 0.
9:0	POWER_GOOD_OFF	Sets the voltage at which PG pulls low. 62.5mV/LSB.

TON_DELAY (60h)

The TON_DELAY command sets the turn-on delay between EN and ON.

Command	TON_DELAY															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X	TON_DELAY							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates writes are ignored and reads are always 0.
7:0	TON_DELAY	Sets the delay from when EN asserts high to when the ON signal starts to rise. 0.1ms/LSB.

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TOFF_DELAY (64h)

The TOFF_DELAY command sets the turn-off delay between EN and ON.

Command	TOFF_DELAY															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X	TOFF_DELAY							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	TOFF_DELAY	Set the delay from when EN de-asserts to when the ON signal drops low. 0.1ms/LSB.

OP_WARN_LIMIT (6Ah)

The OP_WARN_LIMIT command sets the input over-power (OP) warning limit.

Command	OP_WARN_LIMIT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	OP_WARN_LIMIT													

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
13:0	OP_WARN_LIMIT	Sets the input OP warning limit. 4W/LSB.

STATUS_BYTE (78h)

The STATUS_BYTE command returns 1 byte of information with a summary of the most critical statuses and faults.

Command	STATUS_BYTE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function			X					

Bits	Bit Name	Description
7	NVM_BUSY	Indicates whether the NVM is busy. 1'b0: NVM access is idle 1'b1: The NVM is busy. The NVM cannot be accessed and PMBus writes are ignored
6	OFF	Indicates whether the output is off. VOUT may be off due to a protection, EN going low, or a command. 1'b0: VOUT is on 1'b1: VOUT is off
5	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.

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4	IOUT_OC_FAULT	Indicates whether an I_{OUT} over-current (OC) fault has occurred. If V_{IMON}-based total OCP occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No I_{OUT} OC fault has occurred 1'b1: An I_{OUT} OC fault has occurred
3	VIN_UV_FAULT	Indicates whether a V_{IN} under-voltage (UV) fault has occurred. If a V_{IN} UV fault occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{IN} UV fault has occurred 1'b1: A V_{IN} UV fault has occurred
2	TEMPERATURE	Indicates whether an over-temperature (OT) fault or warning has occurred. If a V_{TEMP}-based OT fault or warning has occurred, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No OT fault or warning has occurred 1'b1: An OT fault or warning has occurred
1	CML	Indicates whether a PMBus communication fault has occurred. If a PMBus communication related fault occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No CML fault has occurred 1'b1: A CML fault has occurred
0	MAX_SS_FAULT	Indicates whether the slave experiences a maximum SS fault. If V_{SS} is below 340mV when the maximum soft start time ends, this bit is set. 1'b0: No maximum SS fault has occurred 1'b1: A maximum SS fault has occurred

STATUS_WORD (79h)

The STATUS_WORD command returns 2 bytes of information with a summary of the device fault/warning condition. The higher byte gives more detailed information of the fault conditions. The lower byte shares this information with register STATUS_BYTE (78h).

Command	STATUS_WORD															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function				X		X					X					

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14	IOUT_POUT	Indicates whether an I_{OUT}/P_{OUT} fault or warning has occurred. If an I_{OUT} fault and warning or P_{OUT} warning occurs, this bit is set and latched. The CLEAR_FAULTS command (03h) can reset this bit. 1'b0: No I_{OUT}/P_{OUT} fault and warning 1'b1: An I_{OUT}/P_{OUT} fault or warning has occurred
13	INPUT	Indicates whether an input voltage, current, or power fault/warning has occurred. If any of these input faults/warnings occur, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No input fault/warning has occurred 1'b1: An input fault/warning has occurred
12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.

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11	PG	Indicates the power good (PG status). 1'b0: PG is high 1'b1: PG is low
10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9	SLAVE_FAULT	Indicates whether a slave fault has occurred. If an e-fuse slave has a fault or the fault from Table 2 on page 26 occurs, GOK is pulled low and this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No slave faults have occurred 1'b1: Slave faults have occurred
8	WATCH_DOG	Indicates whether the watchdog timer from the monitor block has overflowed. The monitor value calculation has a watchdog timer. If the timer overflows, the monitor value calculation state machine and the timer are reset. Meanwhile, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: The watchdog timer has not overflowed 1'b1: The watchdog timer has overflowed
7	NVM_BUSY	Indicates whether the NVM is busy. 1'b0: NVM access is idle 1'b1: The NVM is busy. The NVM cannot be accessed and PMBus writes are ignored
6	OFF	Indicates whether the output is off. VOUT may be off due to a protection, EN going low, or a command. 1'b0: VOUT is on 1'b1: VOUT is off
5	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
4	IOUT_OC_FAULT	Indicates whether an I_{OUT} over-current (OC) fault has occurred. If V_{IMON}-based total OCP occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No I_{OUT} OC fault has occurred 1'b1: An I_{OUT} OC fault has occurred
3	VIN_UV_FAULT	Indicates whether a V_{IN} under-voltage (UV) fault has occurred. If a V_{IN} UV fault occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{IN} UV fault has occurred 1'b1: A V_{IN} UV fault has occurred
2	TEMPERATURE	Indicates whether an over-temperature (OT) fault or warning has occurred. If a V_{TEMP}-based OT fault or warning has occurred, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No OT fault or warning has occurred 1'b1: An OT fault or warning has occurred
1	CML	Indicates whether a PMBus communication fault has occurred. If a PMBus communication related fault occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No CML fault has occurred 1'b1: A CML fault has occurred
0	MAX_SS_FAULT	Indicates whether the slave experiences a maximum SS fault. If V_{SS} is below 340mV when the maximum soft start time ends, this bit is set. 1'b0: No maximum SS fault has occurred 1'b1: A maximum SS fault has occurred

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STATUS_IOUT (7Bh)

The STATUS_IOUT command returns 1 data byte with the detailed I_{OUT} fault and warning status.

Command	STATUS_IOUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function		X		X	X	X	X	

Bits	Bit Name	Description
7	IOUT_OC_FAULT	Indicates whether an I_{OUT} over-current (OC) fault has occurred. If V_{IMON}-based total OCP occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No I_{OUT} OC fault has occurred 1'b1: An I_{OUT} OC fault has occurred
6	RESERVED	Unused. X indicates writes are ignored and reads are always 0.
5	IOUT_OC_WARNING	Indicates whether an I_{OUT} over-current (OC) warning has occurred. If V_{IMON}-based total OC warning occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No I_{OUT} OC warning has occurred 1'b1: An I_{OUT} OC warning has occurred
4:1	RESERVED	Unused. X indicates writes are ignored and reads are always 0.
0	POUT_OP_WARN	Indicates whether an output over-power (OP) warning has occurred. If an output OP warning occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No output OP warning has occurred 1'b1: An output OP warning has occurred

STATUS_INPUT (7Ch)

The STATUS_INPUT command returns 1 data byte with input fault or warning messages.

Command	STATUS_INPUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function						X	X	X

Bits	Bit Name	Description
7	VIN_OV_FAULT	Indicates whether a V_{IN} over-voltage (OV) fault has occurred. If V_{IN} exceeds the value set by VIN_OV_FAULT_LIMIT (55h), this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{IN} OV fault has occurred 1'b1: A V_{IN} OV fault has occurred
6	VIN_OV_WARNING	Indicates whether a V_{IN} over-voltage (OV) warning has occurred. If V_{IN} exceeds the value set by VIN_OV_WARN_LIMIT (57h), this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{IN} OV warning has occurred 1'b1: A V_{IN} OV warning has occurred

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5	VIN_UV_WARNING	Indicates whether a V_{IN} under-voltage (UV) warning has occurred. If V_{IN} falls below the value set by VIN_UV_WARN_LIMIT (58h), this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{IN} OV fault has occurred 1'b1: A V_{IN} OV fault has occurred
4	VIN_UV_FAULT	Indicates whether a V_{IN} under-voltage (UV) fault has occurred. If V_{IN} falls below the value set by VIN_OFF (36h), this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{IN} UV fault has occurred 1'b1: A V_{IN} UV fault has occurred
3	VIN_UVLO	Indicates whether V_{IN} under-voltage lockout (UVLO) has occurred. If V_{IN} falls below the value set by VIN_OFF (36h), this bit is set regardless of EN. This bit is live. 1'b0: No V_{IN} UVLO fault has occurred 1'b1: V_{IN} UVLO fault has occurred
2:0	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.

STATUS_TEMPERATURE (7Dh)

The STATUS_TEMPERATURE command returns 1 data byte with temperature fault or warning messages.

Command	STATUS_TEMPERATURE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function			X	X	X	X	X	

Bits	Bit Name	Description
7	OT_SENSED_FAULT	Indicates whether a sensed over-temperature (OT) fault has occurred. If the V_{TEMP}-sensed temperature exceeds the OT fault limit set by OT_FAULT_LIMIT (4Fh), this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{TEMP}-sensed OT fault has occurred 1'b1: A V_{TEMP}-sensed OT fault has occurred
6	OT_SENSED_WARN	Indicates whether a sensed over-temperature (OT) warning has occurred. If the V_{TEMP}-sensed temperature exceeds the OT warning limit set by OT_WARN_LIMIT (51h), this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{TEMP}-sensed OT warning has occurred 1'b1: A V_{TEMP}-sensed OT warning has occurred
5:1	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
0	OT_CONTROLLER_FAULT	Indicates whether the controller experiences an over-temperature (OT) fault. If the controller's temperature exceeds its OT threshold, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No controller OT fault has occurred 1'b1: A controller OT fault has occurred

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STATUS_CML (7Eh)

The STATUS_CML command returns 1 data byte with the memory and communication fault messages.

Command	STATUS_CML							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function					X	X		

Bits	Bit Name	Description
7	INVALID_CMD	Indicates whether an invalid PMBus command was received. If the MP5990 receives an unsupported command code, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No invalid PMBus command has been received 1'b1: An invalid PMBus command has been received
6	INVALID_DATA	Indicates whether invalid PMBus data was received. If the MP5990 receives unsupported data, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No invalid PMBus data has been received 1'b1: Invalid PMBus data has been received
5	PEC_FAILED	Indicates whether a PMBus packet error checking (PEC) fault has occurred. The PMBus interface supports the use of the PEC byte that is defined in the SMBus standard. The PEC byte is transmitted by the MP5990 during a read transaction or sent to the MP5990 during a write transaction. If the PEC byte sent to the MP5990 during a write transaction is incorrect, the command is not executed and this bit is set and latched. Send a CLEAR_FAULTS (03h) to reset this bit. 1'b0: No PEC fault has been detected 1'b1: A PEC fault has been detected
4	NVM_CRC_FAULT	Indicates whether a CRC fault has occurred. While storing operating memory data to the NVM, the MP5990 calculates a CRC code for each bit and saves the final CRC code to the NVM. While restoring the NVM data to the operating memory, the MP5990 recalculates the CRC code with each bit. The MP5990 checks the CRC results when the restoring process is done. If the CRC result does not match what is stored during the storing process, the e-fuse shuts down and this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No NVM CRC fault has been detected 1'b1: An NVM CRC fault has been detected
3:2	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
1	COMMU_OTHER_ FAULT	If a start or stop condition interrupts the data transmission, this bit is set. This bit is in latch-off mode. Send a CLEAR_FAULTS (03h) command to reset this bit.
0	NVM_SIG_FAULT	While restoring data from the NVM to the memory, the device checks the signature register in address 00h of the NVM first. If the signature register is 0x1234, the restoration process stops immediately and this bit is set and latched. Send a CLEAR_FAULTS (03h) command to clear this bit. 1'b0: No NVM signature fault has occurred 1'b1: An NVM signature fault has occurred

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REV_ID (80h)

The REV_ID commands returns the silicon revision number and can express the version of silicon when the metal changes. This value is fixed in the analog design.

Command	REV_ID							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	REV_ID							

Bits	Bit Name	Description
7:0	REV_ID	Returns the silicon revision number.

READ_EIN (86h)

The READ_EIN command returns the input energy (E_{IN}). The calculation method follows PMBus requirement.

Byte	Byte Name	Description
6	RESERVED	Unused. X indicates writes are ignored and reads are always 0.
5	SAMPLE_COUNT_HIGH	Counts the sample numbers, which is 24 bits in total. 100μs/LSB.
4	SAMPLE_COUNT_MID	Counts the sample numbers, which is 24 bits in total. 100μs/LSB.
3	SAMPLE_COUNT_LOW	Counts the sample numbers, which is 24 bits in total. 100μs/LSB.
2	ACCU_ROLL_COUNT	Counts the input energy (E_{IN}) accumulator roll counters.
1	EIN_ACCU_HIGH	Counts the E_{IN} counter, which is 16 bits in total. The MSB is the signed bit. 1W/LSB.
0	EIN_ACCU_LOW	Counts the E_{IN} counter, which is 16 bits in total. The MSB is the signed bit. 1W/LSB.

READ_VIN (88h)

The READ_VIN command returns the sensed V_{IN}.

Command	READ_VIN															
Format	Linear11															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	READ_VIN															

Bits	Bit Name	Description
15:0	READ_VIN	These bits are configured by register C4h, bit[9] to select linear mode or direct mode. In linear mode, bits[15:11] are the signed two's complement value for the exponent (bits[15:11] = N), while bits[10:0] are the signed two's complement mantissa (bits[10:0] = Y). The reported V_{IN} can be calculated with the following equation: Reported V_{IN} = Y x 2 ^ N In direct mode, bits[15:11] are always 0000, while bits[10:0] are the actual calculated bits. 31.25mV/LSB.

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READ_VOUT (8Bh)

The READ_VOUT command returns the sensed V_{OUT}.

Command	READ_VOUT															
Format	Linear11															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	READ_VOUT															

Bits	Bit Name	Description
15:0	READ_VOUT	These bits are configured by register C4h, bit[9] to select linear mode or direct mode. In linear mode, bits[15:11] are the signed two's complement value for the exponent (bits[15:11] = N), while bits[10:0] are the signed two's complement mantissa (bits[10:0] = Y). The reported V_{OUT} can be calculated with the following equation: Reported V_{OUT} = Y x 2 ^ N In direct mode, bits[15:11] are always 0000, while bits[10:0] are the actual calculated bits. 31.25mV/LSB.

READ_IOUT (8Ch)

The READ_IOUT command returns the measured I_{OUT}.

Command	READ_IOUT															
Format	Linear11															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	READ_IOUT															

Bits	Bit Name	Description
15:0	READ_IOUT	These bits are configured by register C4h, bit[9] to select linear mode or direct mode. In linear mode, bits[15:11] are the signed two's complement value for the exponent (bits[15:11] = N), while bits[10:0] are the signed two's complement mantissa (bits[10:0] = Y). The reported I_{OUT} can be calculated with the following equation: Reported I_{OUT} = Y x 2 ^ N In direct mode, bits[15:14] are always 0000, while bits[13:0] are the actual calculated bits. 62.5mA/LSB.

READ_TEMPERATURE (8Dh)

The READ_TEMPERATURE command returns the measured temperature.

Command	READ_TEMPERATURE															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	X	X	READ_TEMPERATURE							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates writes are ignored and reads are always 0.
7:0	READ_TEMPERATURE	Returns the temperature sensed on the VTEMP pin. 1°C/LSB.

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READ_POUT (96h)

The READ_POUT command reports the output power (P_{OUT}).

Command	READ_POUT															
Format	Linear11															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	READ_POUT															

Bits	Bit Name	Description
15:0	READ_POUT	These bits are configured by register C4h, bit[9] to select linear mode or direct mode. In linear mode, bits[15:11] are the signed two's complement value for the exponent (bits[15:11] = N), while bits[10:0] are the signed two's complement mantissa (bits[10:0] = Y). The reported P_{OUT} can be calculated with the following equation: Reported P_{OUT} = Y x 2 ^ N In direct mode, bits[15:0] is the actual calculated bits. 1W/LSB.

READ_PIN (97h)

The READ_PIN command reports the input power (P_{IN}).

Command	READ_PIN															
Format	Linear11															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	READ_PIN															

Bits	Bit Name	Description
15:0	READ_PIN	These bits are configured by register C4h, bit[9] to select linear mode or direct mode. In linear mode, bits[15:11] are the signed two's complement value for the exponent (bits[15:11] = N), while bits[10:0] are the signed two's complement mantissa (bits[10:0] = Y). The reported P_{IN} can be calculated with the following equation: Reported P_{IN} = Y x 2 ^ N In direct mode, bits[15:0] is the actual calculated bits.1W/LSB.

PMBUS_REVISION (98h)

The PMBUS_REVISION command reads the PMBus revision to which the device is compliant. It is read-only.

Command	PMBUS_REVISION							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	PMBUS_REVISION							

Bits	Bit Name	Description
7:0	PMBUS_REVISION	The default value is 33h, which means Part I Revision is 1.3, and the Part II Revision is 1.3.

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VENDOR_ID (99h)

The VENDOR_ID command returns company identification. It is block read.

PRODUCT_ID (9Ah)

The PRODUCT_ID command returns the part name. It is block read.

REV_CONST (9Bh)

The REV_CONST command returns the manufacturer's revision number. It is read only.

Command	REV_CONST							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	X	

Bits	Bit Name	Description
7:1	RESERVED	Unused. X indicates writes are ignored and reads are always 0.
0	REV_CONST	Returns the manufacturer's revision number. This value can be configured via REV_CONST_CFG (C3h).

READ_VIN_PEAK (A1h)

The READ_VIN_PEAK command returns the peak V_{IN} sample value. It is read-clear data. The peak value is the maximum value between the two read commands.

Command	READ_VIN_PEAK															
Format	Linear11															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	READ_VIN_PEAK															

Bits	Bit Name	Description
15:0	READ_VIN_PEAK	These bits are configured by register C4h, bit[9] to select linear mode or direct mode. In linear mode, bits[15:11] are the signed two's complement value for the exponent (bits[15:11] = N), while bits[10:0] are the signed two's complement mantissa (bits[10:0] = Y). The peak V_{IN} can be calculated with the following equation: Peak V_{IN} = Y x 2 ^ N At direct mode, bits[15:11] is always 0000, bit[10:0] is the actual calculated bits. 31.25mV/LSB.

READ_PIN_PEAK (A3h)

The READ_PIN_PEAK command returns the peak P_{IN} sample value. It is read-clear data. The peak value is the maximum value between the two read commands.

Command	READ_PIN_PEAK															
Format	Linear11															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	READ_PIN_PEAK															

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Bits	Bit Name	Description
15:0	READ_PIN_PEAK	These bits are configured by register C4h, bit[9] to select linear mode or direct mode. In linear mode, bits[15:11] are the signed two's complement value for the exponent (bits[15:11] = N), while bits[10:0] are the signed two's complement mantissa (bits[10:0] = Y). The peak P_{IN} can be calculated with the following equation: Peak P_{IN} = Y x 2 ^ N In direct mode, bits[15:0] is the actual calculated bits. 1W/LSB.

READ_VOUT_PEAK (A5h)

The READ_VOUT_PEAK command returns the peak V_{OUT} sample value. It is read-clear data. The peak value is the maximum value between the two read commands.

Command	READ_VOUT_PEAK															
Format	Linear11															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	READ_VOUT_PEAK															

Bits	Bit Name	Description
15:0	READ_VOUT_PEAK	These bits are configured by register C4h, bit[9] to select linear mode or direct mode. In linear mode, bits[15:11] are the signed two's complement value for the exponent (bits[15:11] = N), while bits[10:0] are the signed two's complement mantissa (bits[10:0] = Y). The peak V_{OUT} can be calculated with the following equation: Peak V_{OUT} = Y x 2 ^ N In direct mode, bits[15:11] is always 0000, bits[10:0] is the actual calculated bits. 31.25mV/LSB.

READ_IOUT_PEAK (A6h)

The READ_IOUT_PEAK command returns the peak I_{OUT} sample value. It is read-clear data. The peak value is the maximum value between the two read commands.

Command	READ_IOUT_PEAK															
Format	Linear11															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function																

Bits	Bit Name	Description
15:0	READ_IOUT_PEAK	These bits are configured by register C4h, bit[9] to select linear mode or direct mode. In linear mode, bits[15:11] are the signed two's complement value for the exponent (bits[15:11] = N), while bits[10:0] are the signed two's complement mantissa (bits[10:0] = Y). The peak V_{OUT} can be calculated with the following equation: Peak I_{OUT} = Y x 2 ^ N In direct mode, bits[15:14] is always 0000, while bits[13:0] is the actual calculated bits. 62.5mA/LSB.

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READ_TEMP_PEAK (AFh)

The READ_TEMP_PEAK is used to read TEMP peak sample value. It is read-clear data. The peak value is the maximum value between the two read commands.

Command	READ_TEMP_PEAK															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X	X	X	X	X	X	X	X	READ_TEMP_PEAK							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	READ_TEMP_PEAK	No negative value. 1°C/LSB.

CONFIG_ID (C0h)

The CONFIG_ID command sets the 4-digit part number.

Command	CONFIG_ID															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	CONFIG_ID															

Bits	Bit Name	Description
15:0	CONFIG_ID	Sets the 4-digit part number.

CONFIG_CODE_REV (C1h)

The CONFIG_CODE_REV command sets the configuration code revision.

Command	CONFIG_CODE_REV															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	CONFIG_CODE_REV															

Bits	Bit Name	Description
15:0	CONFIG_CODE_REV	Sets the configuration code revision.

PRODUCT_REV_USER (C2h)

The PRODUCT_REV_USER command provides 2 bytes to set the product revision for the user.

Command	PRODUCT_REV_USER															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15:0	PRODUCT_REV_USER	Sets the production revision.

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REV_CONST_CFG (C3h)

The REV_CONST_CFG stores the silicon revision number, which can also be read via 9Bh.

Command	REV_CONST_CFG							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	REV_CONST_CFG							

Bits	Bit Name	Description
7:0	REV_CONST_CFG	Stores the silicon revision number.

EFUSE_CFG (C4h)

The EFUSE_CFG command configures functions related to the MP5990.

Command	EFUSE_CFG															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X			X							X	X	X	X	X	X

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14	CONTROLLER_OTP_CFG	Configures the controller's over-temperature protection (OTP fault protection mode. 1'b0: Hiccup mode 1'b1: Latch-off mode
13	SLAVE_MAX_SS_CFG	Configures the maximum SS fault protection mode. 1'b0: Hiccup mode 1'b1: Latch-off mode
12	RESERVED	Always set to 0.
11	SLAVE_SS_FLT_EN	Enables slave fault detection by monitoring the SS pin. If this function is enabled, the MP5990 indicates that the slave is experiencing a fault when the EN/ON/PG pins are all high, and the SS pin is pulled low by the e-fuse slave. 1'b0: Disabled 1'b1: Enabled
10	SS_CFG	Enables the device to pull the SS pin low if a fault occurs. 1'b0: Do not pull the SS pin low if a fault occurs 1'b1: Pull the SS pin low if a fault occurs
9	RPT_FORMAT	Configures the report format of the MP5990. 1'b0: Direct mode 1'b1: Linear mode When selecting linear mode, the device tunes the exponent automatically. For the voltage-related reports (e.g. V_{IN} and V_{OUT}), the device has a 31.25mV/62.5mV resolution, up to 64V. For current-related reports (e.g. I_{OUT}), the device has a 0.0625A/0.125A/0.25A/0.5A/1A resolution, up to 1023A. For power-related reports (e.g. P_{IN} and P_{OUT}), the device has 1W/2W/4W/8W/16W/32W/64W, up to 6.5535kW.

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8	VIN_OVP_MODE	Sets the V_{IN} over-voltage protection (OVP) mode. 1'b0: Latch-off mode 1'b1: Hiccup mode
7	VIN_UVLO_FAULT	If V_{IN} under-voltage lockout (UVLO) is enabled by E6h, bits[0], this bit can configure the V_{IN} UVLO response. The V_{IN} UVLO thresholds are set by registers 35h and 36h. If the response is set to no action, UVLO does not set the corresponding bits in FAh, and the ON, GOK, SS, and PG pins do not pull low. 1'b0: No action 1'b1: Action
6	VIN_PRT_RESO	Combine this bit with VIN_PRT_SEL (E7h), bit[7]) to configure V_{IN}-related protection resolutions (e.g. VIN_ON, VIN_OFF, and VIN_OV). 500mV when VIN_PRT_RESO = 0, and VIN_PRT_SEL = 0. 250mV when VIN_PRT_RESO = 0, and VIN_PRT_SEL = 1 125mV when VIN_PRT_RESO = 1, and VIN_PRT_SEL = 0 or 1
5:0	RESERVED	Always set to 6b'00 1000.

OCW_SC_REF (C5h)

The OCW_SC_REF command sets the OCWREF and SCREF voltage levels for slave devices.

Command	OCW_SC_REF															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	SCREF						OCWREF					

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:6	SCREF	Sets the SCREF voltage level, which selects the short-circuit protection (SCP) level at 40A, 60A, 80A, 100A, and 120A. 28mV/LSB.
5:0	OCWREF	Sets the OCWREF voltage level. If the CS voltage (V_{CS}) exceeds V_{OCWREF}, D_OC asserts. 28mV/LSB.

OC_REF (C6h)

The OC_REF command set the OCREF voltage for the slaves.

Command	OC_REF							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	OCREF					

Bits	Bit Name	Description
7:6	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
5:0	OCREF	Sets the OCREF voltage for V_{CS}-based over-current protection (OCP). 28mV/LSB.

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ON_HICCUP_DLY (C7h)

The ON_HICCUP_DLY command sets the ON signal timeout and hiccup delay time.

Command	ON_HICCUP_DLY															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X		MAX_SS_TIME				HICCUP_DLY								

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates writes are ignored and reads are always 0.
13	PG_MUX	Sets pin 13 to have the power good (PG) or over-current warning (OCW) output. 1'b0: PG 1'b1: OCW
12:9	MAX_SS_TIME	Sets the maximum soft start (SS) time. The maximum SS timer starts counting when the ON pin exceeds its rising threshold. If V_{SS} is below 340mV when the timer finishes, ON and GOK are pulled low. 40ms/LSB with a maximum of 600ms.
8:0	HICCUP_DLY	Sets the hiccup delay time. 20ms/LSB with a maximum of 10.22s. Do not set the hiccup delay time to 0ms, regardless of whether latch-off mode or hiccup mode is selected.

SYS_INITIAL_DELAY (D0h)

The SYS_INITIAL_DELAY command sets the system initialization delay time.

Command	SYS_INITIAL_DELAY															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X	X	X	X	X	DELAY_MASTER			

Bits	Bit Name	Description
15:4	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
3:0	DELAY_MASTER	Sets the controller system initialization delay time. The timer starts when NVM copying ends. When the system initialization delay is over, the MP5990 starts to detect if EN is high. 10ms/LSB.

ADDR_PMBUS (D2h)

The ADDR_PMBUS command configures the device address, including pin configurations and register configurations.

Command	ADDR_PMBUS															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X											

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.

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10:8	I2C_TIMEOUT_CFG	Configures the I²C timeout function. Bit[10] sets whether an I²C timeout resets the I²C state machine. 1'b0: Do not reset 1'b1: Reset Bits[9:8] determine whether SDA and SCL are used for a timeout. 2'b00: The timeout is always counted 2'b01: The timeout starts to count while SCL is pulled low 2'b10: The timeout starts to count while SDA is pulled low 2'b11: The timeout starts to count while both SCL and SDA are pulled low
7	ADDR_CFG	Selects the PMBus address configuration mode. 1'b0: The PMBus address is configured by the ADDR pin. The final PMBus address is set by bits[6:4] of this command and the 4LSB set via the ADDR pin 1'b1: The PMBus address is configured by the register. The final PMBus address is set by bits[6:4] and bits[3:0] of this command
6:4	ADDR_PMBUS_3MSB	Sets the 3MSB of the PMBus address.
3:0	ADDR_PMBUS_4LSB	Sets the 4LSB of the PMBus address. When bit [7] of register ADDR_PMBUS (D2h) is 0, the PMBus address 4-LSB is set by the ADDR pin. ADDR_PMBUS_4LSB returns the 4-LSB. When bit [7] of register ADDR_PMBUS (D2h) is 1, the 4-LSB of the PMBus address is set by ADDR_PMBUS_4LSB.

VIN_CFG (E3h)

The VIN_CFG command sets the V_{IN} sense offset.

Command	VIN_CFG															
Format	Two's complement															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X	X	X	X	X	VIN_TUNE			

Bits	Bit Name	Description
15:4	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
3:0	VIN_TUNE	Trims the V_{IN} sense with the gain and offset. Tune the offset with 1 ADC value/LSB. It is two's complement format.

VIN_SCALE (E4h)

The VIN_SCALE command sets the V_{IN} sense scale loop.

Command	VIN_SCALE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	VIN_SCALE										

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10:0	VIN_SCALE	Sets the V_{IN} scale, calculated with the following equation: $VIN_SCALE = 5120 \times R_{BOT} / (R_{TOP} + R_{BOT})$

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Figure 23 shows the V_{IN} sense circuit.

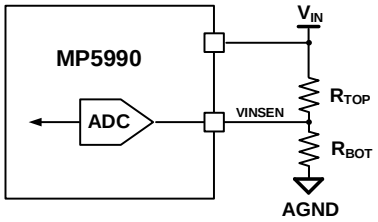

Figure 23: V_{IN} Sense Circuit Design

TEMP_TUNE (E5h)

The TEMP_TUNE command sets the temperature-sense gain and offset. The temperature can be calculated with Equation (9):

$$\text{Real Temperature (1°C/LSB)} = (\text{VTEMP (V)} \times 320 + \text{TEMP_OFFSET_TUNE}) \times \text{GAIN_TUNE} / 256 \quad (9)$$

Command	TEMP_TUNE															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	TEMP_OFFSET_TUNE								GAIN_TUNE							

Bits	Bit Name	Description
15:8	TEMP_OFFSET_TUNE	Sets the temperature-sense offset. It is in two's complement format. Bit[15] is the signed bit. The offset can be calculated with the following equation: TEMP_OFFSET_TUNE= -VTEMP_OFFSET x 320 Where VTEMP_OFFSET is 152.5mV.
7:0	GAIN_TUNE	Sets the temperature-sense gain, calculated with the following equation: GAIN_TUNE = 256 / (320 x VTEMP_GAIN) Where VTEMP_GAIN is 8.7mV/°C.

PROTECT_CFG (E6h)

The PROTECT_CFG command configures e-fuse protection.

Command	PROTECT_CFG															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X		X		X		X			X		X		X		

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14	OTP_ CONTROLLER_EN	Enable the controller's over-temperature protection (OTP). 1'b0: Disabled 1'b1: Enabled
13	RESERVED	Always set to 0.
12	PROTECT_ASSERT	Configures whether a protection can be asserted during NVM fault recording. 1'b0: Assert at any time 1'b1: Assert when not storing to the NVM
11	RESERVED	Always set to 0.

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10	MAX_SS_FAULT_EN	Enables maximum SS fault protection. 1'b0: Disabled 1'b1: Enabled
9	RESERVED	Always set to 0.
8	PROTECT_RECORD	Enables the device to store the fault register (FAh) to the NVM. 1'b0: Disabled 1'b1: Enabled
7	FLT_TYPE_EN	Enables the device to detect the e-fuse slave fault type by the FLT_TYPE pin. 1'b0: Disabled 1'b1: Enabled
6	RESERVED	Always set to 0.
5	OCP_TOTAL_EN	Enables the e-fuse controller's total over-current protection (OCP). 1'b0: Disabled 1'b1: Enabled
4	RESERVED	Always set to 0.
3	SLAVE_GOK_FAULT_EN	Enables slave fault detection by monitoring the GOK pin. 1'b0: Disable slave fault detection 1'b1: Enable slave fault detection by monitoring the GOK pin. If GOK pulls low due to the e-fuse slave, the MP5990 recognizes a slave fault status
2	RESERVED	Always set to 0.
1	OTP_PWR_EN	Enables over-temperature protection (OTP) by sensing the VTEMP voltage. 1'b0: Disabled 1'b1: Enabled
0	VIN_PROTECT_EN	Enables V_{IN} related protections, including over-voltage protection (OVP) and under-voltage protection (UVP). 1'b0: Disabled 1'b1: Enabled

VIN_PROTECT_LEVEL (E7h)

The VIN_CFG command configures V_{IN} reporting and protection-related functions.

Command	VIN_PROTECT_LEVEL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X		VIN_OVP_HYS			X	X	X	X

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates writes are ignored and reads are always 0.
7	VIN_PRT_SEL	Combine this bit with VIN_PRT_RESO (C4h, bit[6]) to configure V_{IN}-related protection resolutions (VIN_ON, VIN_OFF, and VIN_OV). 500mV when VIN_PRT_RESO = 0 and VIN_PRT_SEL = 0 250mV when VIN_PRT_RESO = 0 and VIN_PRT_SEL = 1 125mV when VIN_PRT_RESO = 1 and VIN_PRT_SEL = 0 or 1.

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6:4	VIN_OVP_HYS	Sets the V_{IN} over-voltage protection (OVP) hysteresis. 3'b000: 7LSB 3'b001: 6LSB 3'b010: 5LSB 3'b011: 4LSB 3'b100: 3LSB 3'b101: 2LSB 3'b110: 1LSB 3'b111: 0LSB The V_{IN} OV falling threshold is configured via VIN_OV_FAULT_LIMIT (55h), calculated with the following equation: V_{IN} OV falling threshold = (VIN_OV_FAULT_LIMIT - VIN_OVP_HYS) x Resolution Where Resolution is determined by C4h, bit[6] and E7h, bit[7]. 500mV/LSB when C4h, bit[6] = 0 and E7h, bit[7] = 0; supports up to 64V 250mV/LSB when C4h, bit[6] = 0 and E7h, bit[7] = 1; supports up to 32V 125mV/LSB when C4h, bit[6] = 1; supports up to 16V
3:0	RESERVED	Always returns 0.

PRT_DELAY (E8h)

The PRT_DELAY is used to set the delay time of slave fault (GOK) and total OCP fault.

Command	PRT_DELAY															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X					X	X	X	X	OCP_DELAY			

Bits	Bit Name	Description
15:12	RESERVED	Always set to 5.
11:8	SLAVE_GOK_ FAULT_DELAY	Sets the slave GOK fault detection delay time. 1μs/LSB with a maximum of 15μs.
7:4	RESERVED	Always set to 5.
3:0	OCP_DELAY	Sets the over-current protection (OCP) delay. The resolution can be configured via F5h, bit[4] . 500μs/LSB when F5h, bit[4] = 0, up to 7.5ms 100μs/LSB when F5h, bit[4] = 1, up to 1.5ms

SMBALERT_MASK (E9h)

The SMBALERT_MASK command masks the faults and warnings to assert ALT#.

Command	SMBALERT_MASK															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function																

Bits	Bit Name	Description
15	INVALID_CMD	1'b0: No mask 1'b1: If an PMBus invalid command is received, ALT# does not assert
14	INVALID_DATA	1'b0: No mask 1'b1: If invalid PMBus data is received, ALT# does not assert

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13	PEC_FAILED	1’b0: No mask 1’b1: If a PMBus packet error check failure is received, ALT# does not assert
12	NVM_SIG_FAULT	1’b0: No mask 1’b1: If the NVM has a signature fault, ALT# does not assert
11	COMM_OTHER	1’b0: No mask 1’b1: If a different communication fault is received, ALT# does not assert
10	SLAVE_GOK_FAULT	1’b0: No mask 1’b1: If a slave GOK fault is received, ALT# does not assert
9	SLAVE_MAX_SS	1’b0: No mask 1’b1: If a slave’s maximum SS fault is received, ALT# does not assert
8	TOTAL_OC_FAULT	1’b0: No mask 1’b1: If total input over-current protection (OCP) occurs, ALT# does not assert
7	OP_WARN	1’b0: No mask 1’b1: If an input over-power warning is received, ALT# does not assert
6	VIN_OV_FAULT	1’b0: No mask 1’b1: If an input over-voltage (OV) fault is received, ALT# does not assert
5	VIN_UVLO	1’b0: No mask 1’b1: If input UVLO occurs, ALT# does not assert
4	OT_SENSED_FAULT	1’b0: No mask 1’b1: If a V_{TEMP}-sensed over-temperature (OT) fault is received, ALT# does not assert
3	UV_WARN	1’b0: No mask 1’b1: If an input under-voltage (UV) warning is received, ALT# does not assert
2	OC_WARN	1’b0: No mask 1’b1: If an input OC warning is received, ALT# does not assert
1	VIN_OV_WARN	1’b0: No mask 1’b1: If an input OV warning is received, ALT# does not assert
0	OT_SEN_WARN	1’b0: No mask 1’b1: If a V_{TEMP}-sensed OT warning is received, ALT# does not assert

LEVEL_SEL (EBh)

The LEVEL_SEL command sets the over-temperature protection (OTP) hysteresis for the V_{TEMP}-based OTP.

Command	LEVEL_SEL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X	X	X	X	X	X	X	OTP_HYS	

Bits	Bit Name	Description
15:2	RESERVED	Always write to 0.
1:0	OTP_HYS	Select V_{TEMP} based on OTP hysteresis. 2’b00: 20°C 2’b01: 25°C 2’b10: 30°C 2’b11: 35°C

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ADVANCE_CTRL (F1h)

The ADVANCE_CTRL command configures some advanced functions for the MP5990.

Command	ADVANCE_CTRL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function						X			X			GATECLK_CFG				

Bits	Bit Name	Description
15	I2C_VOL_SET	Sets the I^2C voltage. 1'b1: 1.8V 1'b0: 3.3V
14	COMM_INITIAL	Configures the PMBus communication behavior during the system initialization state or a NVW storing/restoring state. 1'b0: Acknowledge (ACK) the PMBus address, but do not acknowledge (NACK) PMBus commands 1'b1: NACK PMBus address
13	LPM_COPY_CFG	Configure whether MP5990 enters system initial delay and NVM copy again when exit low power mode, 1'b0: Disabled 1'b1: Enabled
12	LPM_EN_CFG	Enables low-power mode (LPM). 1'b0: Disabled 1'b1: Enabled
11	CLR_NVM_LAST_FAULT_EN	Enables the last faults recorded to the NVM to be cleared by the 08h command. 1'b0: Disabled 1'b1: Enabled
10	RESERVED	Always set to 0.
9	NVM_COPY_EN	Enables the device to restore the NVM after EN turns on or an on command is received. 1'b0: Disabled 1'b1: Enabled
8	CRC_PROTECT_EN	Enables the NVM CRC function. 1'b0: Disabled 1'b1: Enabled
7	RESERVED	Always set to 0.
6	CAL_WATCH_DOG_EN	Enables the calculation for the watchdog function. This can prevent the calculation state machine from running out of control. If this function is enabled, the calculation state machine is reset when the state is unchanged for more than 700μs. 1'b0: Disabled 1'b1: Enabled
5	BG_CHOP_EN	Enables the bandgap chop function, which can reduce amplifier's input offset voltage. 1'b0: Disabled 1'b1: Enabled

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4:0	GATECLK_CFG	Configures the gate clock function. Enable this function to reduce the controller's power loss. Bit[4] is reserved and always set to 0. Bit[3] enables NVM operation. 1'b0: Disabled. The gate clock for NVM operation always works 1'b1: Enabled. The gate clock only works after sending 15h and 16h commands Bit[2] enables register writing. 1'b0: Disabled. The gate clock of the write command always works 1'b1: Enabled. The gate clock only works when sending a write command Bit[1] is reserved and always set to 0. Bit[0] enables PMBus communication. 1'b0: Disabled 1'b1: Enabled

RETRY_TIMES (F4h)

The RETRY_TIMES command sets the protection mode, including latch-off, retry, hiccup mode. If a new protection mode is selected, it must be activated by cycling the VIN, VDD33, or EN signal.

Command	RETRY_TIMES															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	OTP_RETRY_TIMES				X	X	X	X					OCP_RETRY_TIMES			

Bits	Bit Name	Description
15:12	OTP_RETRY_TIMES	Sets the V_{TEMP}-based over-temperature protection (OTP) mode. 4'b0000: Latch-off mode 4'b0001~4'h1110: Retry mode. The retry times are set by bits bits[15:12] 4'b1111: Hiccup mode
11:8	RESERVED	Always set to 0.
7:4	SLAVE_GOK_ FAULT_RETRY_TIMES	Set slave faults (GOK) protection mode. 4'b0000: Latch-off mode 4'b0001~4'h1110: retry mode, and retry times is the value of bits[7:4] 4'b1111: Hiccup mode
3:0	OCP_RETRY_TIMES	Sets the total over-current protection (OCP) mode. 4'b0000: Latch-off mode 4'b0001~4'h1110: retry mode, and retry times is the value of bits[3:0] 4'b1111: Hiccup mode

CFG_EXT (F5h)

The CFG_EXT command configures the MP5990's extended functions.

Command	CFG_EXT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X	X	X	X	X	X	X	X							X	X

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Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7	OCW_EN	Enables over-current warning (OCW). 1'b0: Disabled 1'b1: Enabled
6	CLR_FAULT_CFG	Configures whether to clear the FBh register value after sending a 08h command to clear the NVM's latest fault. 1'b0: Do not clear the FBh value 1'b1: Clear the FBh value
5	FAULT_DET_CFG	Configures the fault conditions under which the MP5990 detects the FLT_TYPE pin voltage. Slave faults are detected when GOK or SS goes low. 1'b0: Any fault 1'b1: Slave faults
4	OCP_TIME_SEL	Selects the resolution of the total over-current protection (OCP) timer. 1'b0: 500μs /LSB 1'b1: 100μs /LSB
3:2	NVM_RCD_CFG	Configure the NVM storing mode. Bit[3] selects whether to store protection information when sending a 15h command. 1'b0: Store all protection information 1'b1: Do not store any protection information Bit[2] selects whether to store a section or just the protection word when the protection recording function is enabled. 1'b0: Store section 1'b1: Just protection
1:0	RESERVED	Always write to 2'b00.

CHECK_SUM_FUNC (F8h)

The CHECK_SUM_USER_CODE command provides 2 bytes to return the check sum code (CRC code) for the user code. When the MP5990 sends the 15h command to store configuration information to the NVM, this command returns a CRC code for the user code, which are stored to the NVM. When the MP5990 sends 16h command or starts NVM copying after VDD33 starts up, this command returns a CRC code for the user code, which is exported from the NVM. This is read-only register.

Command	CHECK_SUM_FUNC															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function																

Bits	Bit Name	Description
15:0	CHECK_SUM_FUNC	These bits are read-only.

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FAULT_RECORD (FAh)

The FAULT_RECORD command stores all the current fault bits of system. The related bit is set to 1 if a fault occurs.

Command	FAULT_RECORD															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X			X			X		X							

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14	NVM_CRC_FAULT	Indicates whether a CRC fault has occurred. While storing the operating memory data to the NVM, the MP5990 calculates a CRC code for each bit and saves the final CRC code to the NVM. When restoring the NVM data to the operating memory, the MP5990 recalculates the CRC code for each bit. The MP5990 checks the CRC results when the restoration process is complete. If the CRC result does not match what is stored in the storing process, the VR shuts down and this bit is set. 1'b0: No NVM CRC fault has been detected 1'b1: An NVM CRC fault has been detected
13	NVM_SIG_FAULT	While restoring data from the NVM to the memory, the device checks the signature register in address 00h of the NVM first. If the signature register is 0x1234, the restoration process stops immediately and this bit is set. 1'b0: No NVM signature fault has occurred 1'b1: An NVM signature fault has occurred
12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11	OTP_CONTROLLER_FAULT	Indicates whether the controller experiences an over-temperature (OT) fault. Once the controller's temperature exceeds its OT threshold, this bit is set. 1'b0: No controller OT fault has occurred 1'b1: A controller OT fault has occurred
10	MAX_SS_FAULT	Indicates whether the slave experiences a maximum SS fault. If the SS pin is still low when the maximum soft start time ends, this bit is set. 1'b0: No maximum SS fault has occurred 1'b1: A maximum SS fault has occurred
9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8	VIN_OV_FAULT	V_{IN} over-voltage (OV) fault indicator. Once the sensed V_{IN} exceeds the V_{IN} OV fault limit, this bit is set. 1'b0: No V_{IN} OV fault has occurred 1'b1: A V_{IN} OV fault has occurred
7	RESERVED	Unused. X indicates writes are ignored and reads are always 0.
6	SLAVE_GOK_FAULT	Indicates whether a slave GOK fault has occurred. If a slave has faults, GOK pulls low and this bit is set. 1'b0: No slave faults have occurred 1'b1: A slave fault has occurred

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5	IOUT_OC_FAULT	Indicates whether an I_{OUT} over-current (OC) fault has occurred. If I_{OUT} OCP occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No I_{OUT} OC fault has occurred 1'b1: An I_{OUT} OC fault has occurred
4	VIN_UVLO_FAULT	Indicates whether a V_{IN} under-voltage (UV) fault indicator. C4h, bit[7] selects whether to report this fault. If the sensed V_{IN} falls below the V_{IN} falling threshold after EN pulls high, this bit is set. 1'b0: No V_{IN} UV fault has occurred 1'b1: A V_{IN} UV fault has occurred
3	OT_SENSED_FAULT	Indicates whether an over-temperature (OT) fault has occurred. If the temperature sensed via VTEMP exceeds the OT fault limit set by OT_FAULT_LIMIT (4Fh), this bit is set. 1'b0: No sensed OT fault has occurred 1'b1: A sensed OT fault has occurred
2:0	FAULT_TYPE	Indicates whether a fault type detected by FAULT_TYPE has occurred. 3'b00x: No fault has occurred 3'b010: A GOK fault has occurred 3'b011: A FET DS/GS short fault has occurred 3'b100: An over-temperature fault (145°C limit) or OV fault (18.5V limit) has occurred 3'b101: An OC fault based on V_{CS} has occurred 3'b110: Short-circuit fault

FAULT_RECORD_LAST (FBh)

The FAULT_RECORD_LAST stores the last system fault. The related bit is set to 1 if the fault has occurred, and it can be cleared by sending an 08h command after being stored to the NVM.

Command	FAULT_RECORD_LAST															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X			X			X		X							

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates writes are ignored and reads are always 0.
14	NVM_CRC_FAULT	Indicates whether a CRC fault has occurred. While storing the operating memory data to the NVM, the MP5990 calculates a CRC code for each bit and saves the final CRC code to the NVM. When restoring the NVM data to the operating memory, the MP5990 recalculates the CRC code for each bit. The MP5990 checks the CRC results when the restoration process is complete. If the CRC result does not match what is stored in the storing process, the VR shuts down and this bit is set. 1'b0: No NVM CRC fault has been detected 1'b1: An NVM CRC fault has been detected
13	NVM_SIG_FAULT	While restoring data from the NVM to the memory, the device checks the signature register in address 00h of the NVM first. If the signature register is 0x1234, the restoration process stops immediately and this bit is set. 1'b0: No NVM signature fault has occurred 1'b1: An NVM signature fault has occurred

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12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11	OTP_CONTROLLER_FAULT	Indicates whether the controller experiences an over-temperature (OT) fault. Once the controller's temperature exceeds its OT threshold, this bit is set. 1'b0: No controller OT fault has occurred 1'b1: A controller OT fault has occurred
10	MAX_SS_FAULT	Indicates whether the slave experiences a maximum SS fault. If the SS pin is still low when the maximum soft start time ends, this bit is set. 1'b0: No maximum SS fault has occurred 1'b1: A maximum SS fault has occurred
9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8	VIN_OV_FAULT	V_{IN} over-voltage (OV) fault indicator. If the sensed V_{IN} exceeds the V_{IN} OV fault limit, this bit is set. 1'b0: No V_{IN} OV fault has occurred 1'b1: A V_{IN} OV fault has occurred
7	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
6	SLAVE_GOK_FAULT	Indicates whether a slave GOK fault has occurred. If a slave has faults, GOK pulls low and this bit is set. 1'b0: No slave faults have occurred 1'b1: A slave fault has occurred
5	IOUT_OC_FAULT	Indicates whether an I_{OUT} over-current (OC) fault has occurred. If I_{OUT} OCP occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No I_{OUT} OC fault has occurred 1'b1: An I_{OUT} OC fault has occurred
4	VIN_UVLO_FAULT	Indicates whether a V_{IN} under-voltage (UV) fault has occurred. C4h, bit[7] selects whether to report this fault. If the sensed V_{IN} falls below the V_{IN} falling threshold after EN pulls high, this bit is set. 1'b0: No V_{IN} UV fault has occurred 1'b1: A V_{IN} UV fault has occurred
3	OT_SENSED_FAULT	Indicates whether an over-temperature (OT) fault has occurred. If the temperature sensed via VTEMP exceeds the OT fault limit set by OT_FAULT_LIMIT (4Fh), this bit is set. 1'b0: No sensed OT fault has occurred 1'b1: A sensed OT fault has occurred
2:0	FAULT_TYPE	FAULT_TYPE has six types: 3'b00x: No fault 3'b010: GOK fault 3'b011: FET DS/GS short fault 3'b100: Over-temperature fault (145°C limit) or OV fault (18.5V OV limit) 3'b101: V_{CS} based on OC fault 3'b110: Short-circuit fault

CLEAR_MTP_FAULT (FEh)

The CLEAR_MTP_FAULT command clears the NVM fault. The NVM fault contains the signature fault and CRC fault. When restoring information from the NVM, there may be an NVM signature fault or a CRC fault. If this command is sent, the device ignores any faults and the system operates normally.

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APPLICATION INFORMATION

Selecting the Current Limit Resistor (R_{CS})

The MP5990's normal current limit should exceed the normal maximum load current to allow for tolerances in the current-sense value. The current limit (I_{LIMIT}) can be calculated with Equation (9):

$$I_{LIMIT} = \frac{V_{OCREF}}{R_{CS}} \times 10^5 \ (A) \qquad (9)$$

Where V_{OCREF} is the current limit reference voltage when the MOSFET works in linear mode, and R_{CS} is the resistor from CS to ground (in Ω).

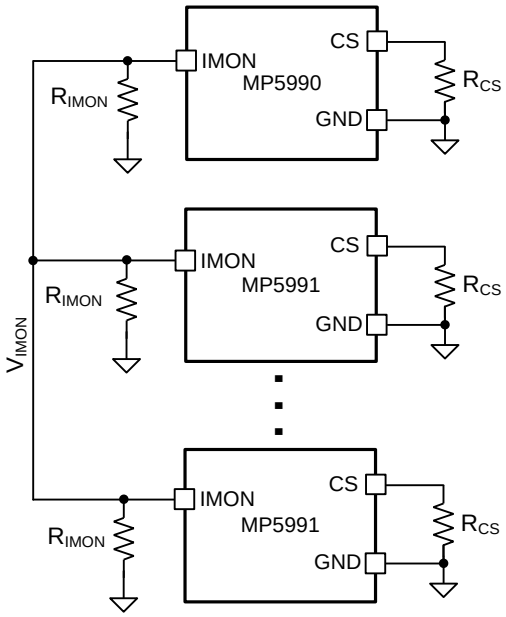
If R_{CS} is set to 3kΩ, and V_{OCREF} is 1.2V, then the optimal current limit is about 40A. When V_{OCREF} is 0.3V, the current limit is about 10A.

Setting the Current Monitor (IMON)

The MP5990 provides a MOSFET current-monitoring function. Connect a resistor to ground to set the I_{OUT} gain.

In standalone applications with the MP5990, the IMON resistor should exceed the value of the CS resistor.

To achieve current balancing during start-up when the MP5990 and MP5991 are used in a multi-phase parallel application, connect IMON and CS (see Figure 24).



$$R_{IMON} = R_{CS}$$

$$R_{IMON_AVG} = \frac{R_{CS}}{N}$$

Figure 24: IMON and CS Connection with MP5990 and Multiple MP5991s in Parallel Application

The equivalent average IMON resistor (R_{IMON_AVG}) can be calculated with R_{CS} / N, where N is the active parallel number.

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PCB Layout Guidelines

Efficient PCB layout is critical for optimal IC performance. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 25 and follow the guidelines below:

1. Place the MP5990 close to the board's input connector to minimize trace inductance.
2. Place a small capacitor (C_{IN}, about 100nF) close to VIN and GND to minimize transients, which may occur on the input supply line. Note that transients of several volts can occur when the load current is shut off.
3. Place a 1µF capacitor as close to VDD33 as possible.
4. Keep the high-current path from the board's input to the load, and the return path, close to one other (and in parallel) to minimize loop inductance.
5. Place an analog signal ground (AGND) plane locally in the MP5990 and connect it to the PCB power ground planes at a single point.
6. Add vias to improve thermal performance.
7. Place a minimum of 9 vias on the bottom VIN pad.
8. Place a minimum of 12 vias close to the MP5990's VIN pads at the IC edge.
9. Place a minimum of 9 vias close to the MP5990's VOUT pads.

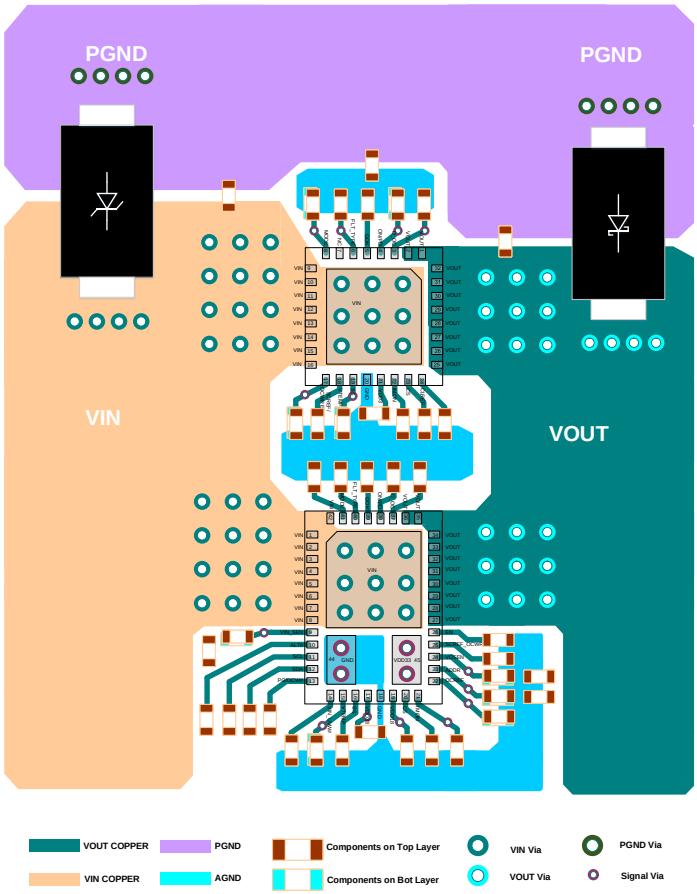

Figure 25: Recommended PCB Layout (Placement and Top Layer PCB)

VIN TVS Diode: SMDJ13A

VOUT Diode: MBRA340T3G for single MP5990, MBRS540T3G for parallel operation

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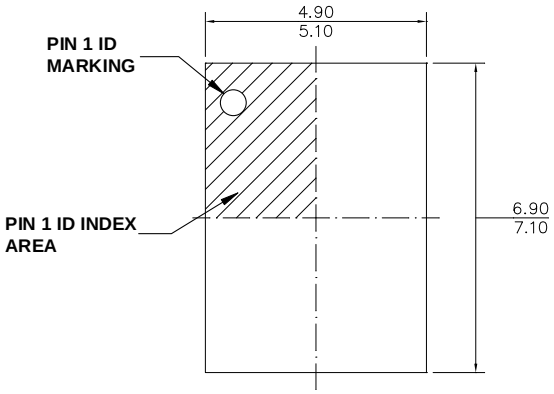
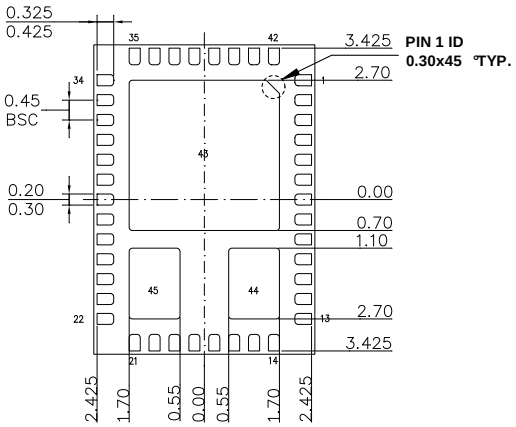
PACKAGE INFORMATION

LGA-45 (5mmx7mm)

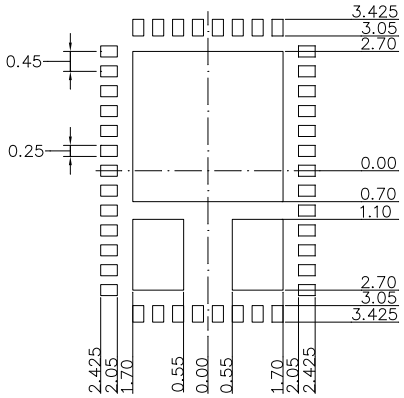


TOP VIEW



BOTTOM VIEW

SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-303.
4) DRAWING IS NOT TO SCALE.

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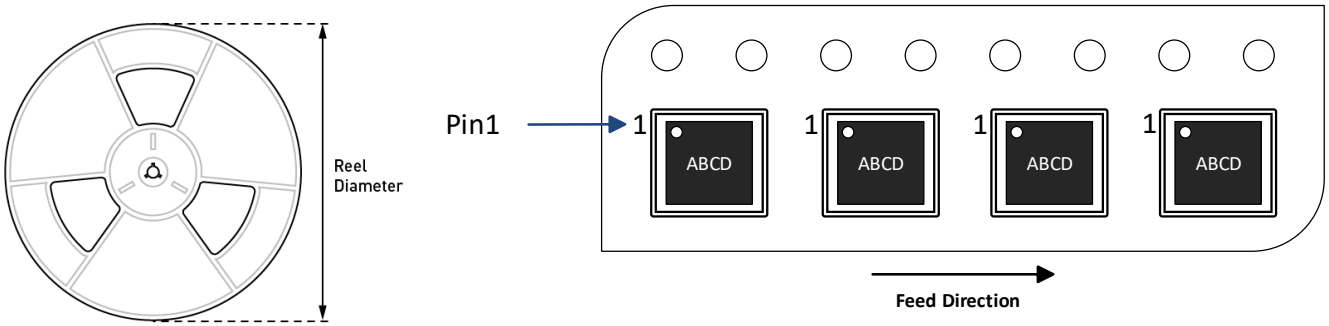
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP5990GMA-xxxx-Z	LGA-45 (5mmx7mm)	5000	N/A	N/A	13in	16mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	5/18/2022	Initial Release	-
1.1	4/19/2024	Updated Figure 5: Changed SS voltage from “250mV” to “340mV”	21
		Updated the PMBus/I^{2}C Transmission Structure section: Added description of the register and ALT# pin behavior if the PEC is incorrect	31
		Updated IOUT_CAL_OFFSET (39h) format to two’s complement	38
		Updated STATUS_CML (7Eh), bit[5]: Changed “If the PEC byte sent to the controller during…” to “If the PEC byte sent to the MP5990 during...”	47
		• Updated READ_VOUT (8Bh) to Linear11 format • Updated READ_TEMPERATURE (8Dh) to direct format	49
		• Updated REV_CONST (9Bh) to unsigned binary format • Updated READ_VIN_PEAK (A1h) to Linear11 format	51
		Updated READ_IOUT_PEAK (A6h) to Linear11 format	52
		Updated READ_TEMP_PEAK (AFh) to direct format	53
		Added to ON_HICCUP_DLY (C7h), bits[8:0]: “Do not set the hiccup delay time to 0ms, regardless of whether latch-off mode or hiccup mode is selected.”	56
		Updated CFG_EXT (F5h) description from “MP5900” to “MP5990”	63
		Updated CLEAR_MTP_FAULT (FEh): Changed “The CLEAR_NVM_FAULT command...” to “The CLEAR_MTP_FAULT command…”	67
1.11	1/15/2026	Updated the data in Table 3. Changed the ADDR voltage and R_{BOT} values from 1h~3h.	30

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