The Future of Analog IC Technology

MP5600

Compact Multiple-Output Power Supply for TV-LCD panel

DESCRIPTION

The MP5600 represents an integrated power supply for large size LCD panel. It contains a buck regulator to generate the logic supply rail, a boost regulator to generate the source driver supply, two charge-pump controllers to generate a positive output and negative output respectively, and a programmable delay gate pulse management switch. Each regulator features adjustable output, internal soft-start, and timer-delayed fault protection.

With the input range from 9V to 18V, the buck regulator can adjust output from 1.5V to 5V; the boost regulator can adjust output from Vin to 19.5V. Both the buck and boost regulators use an external-selectable fixed-frequency (450 kHz or 675 kHz).

With external diode, two regulated charge pump controller could afford voltage up to 3X boost output and low to negative boost output. Gate pulse management provides TFT positive gate driver voltage with two operation mode and programmable delay.

The MP5600 has a 5V linear regulator, a 1.227V reference output, adjustable power up sequences, and over temperature protection.

The MP5600 is available in a 40 pins, 5mm x 5mm, thin QFN package. The device operates over the -20°C to +85°C temperature range.

FEATURES

- 9V to 18V Input Voltage Range
- 450kHz or 675kHz Selectable Frequency
- 7.5V Input Under-Voltage Lockout
- High Efficiency
- Internal Soft-start

Buck Regulator

- Peak Current-Mode, Fast Transient Response
- Integrated 20V, 5A, 60mΩ N-MOSFET
- Internal Fixed 3.3V or Adjustable Output Voltage
- Power Good Signal
- Short Circuit Protection with Switching Frequency Fold-Back

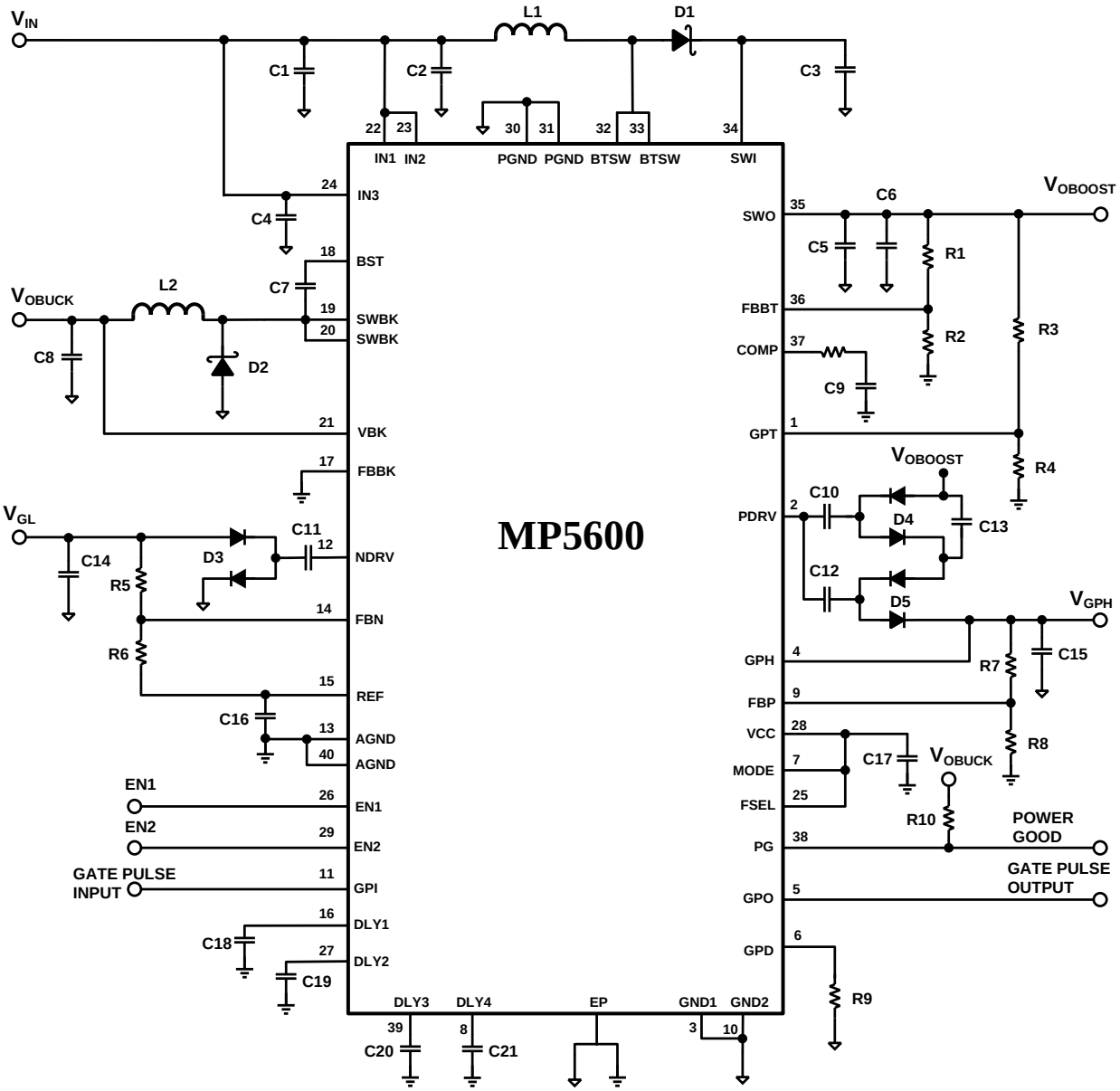
Boost Regulator

- Peak Current-Mode Control
- Integrated 20V, 5A, 60mΩ N-MOSFET
- 19.5V Over Voltage Protection
- Full Isolation Between VIN and Load
- 100mΩ MOSFET Output Isolation Switch
- Adjustable Positive Charge Pump and Negative Charge Pump regulator with 120mA Max Load
- Adjustable GPI and GPO Delay Time
- Dual Mode, Logic-Controlled, High-Voltage Switch with Programmable Delay
- Internal Timer-Delay Fault Protection
- 150°C Thermal Shutdown
- 40-Pin, 5mm x 5mm, Thin QFN Package

APPLICATIONS

- LCD TV Panel
- LCD Monitor

TYPICAL APPLICATION

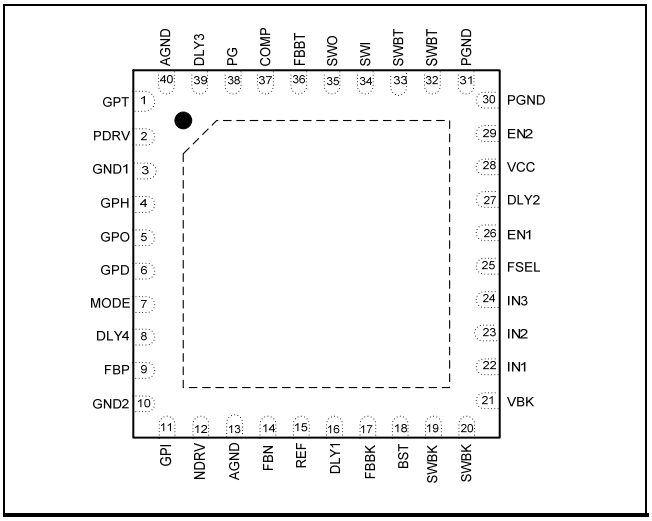


ORDERING INFORMATION

Part Number*	Package	Top Marking	Temperature
MP5600EU	5mm×5mm Thin QFN	5600EUT	–20°C to +85°C

* For Tape & Reel, add suffix –Z (e.g. MP5600EU–Z).
For RoHS compliant packaging, add suffix –LF (e.g. MP5600EU–LF–Z)

PACKAGE REFERENCE



Not affect IC operation if all N.C pin is connected to ground on the PCB.

ABSOLUTE MAXIMUM RATINGS (1)

IN1, IN2, IN3, EN1, EN2, FSEL, PG to AGND .....-0.3V to +24V
GND1, GND2, PGND to AGND ..... ±0.3V
VBK, MODE, GPI, GPT, DLY1, DLY2, DLY3, DLY4, VCC to AGND -0.3V to +7.0V
REF, FBP, FBN, FBBK, FBBT, COMP to AGND -0.3V to (VCC + 0.3V)
SWI, SWO to AGND .....-0.3V to +24V
SWBT to PGND .....-0.3V to +24V
SWI to SWO .....-0.3V to +24V
NDRV to GND2, PDRV to GND1 ....-0.3V to (VSWI + 0.3V)
SWBK to AGND ..... -0.3V to (VIN+ 0.3V)
BST to SWBK .....-0.3V to +6.5V
GPH to AGND.....-0.3V to +45V
GPO, GPD to AGND.....-0.3V to (VGPH + 0.3V)
GPO to GPD .....-0.3V to +45V
Continuous Power Dissipation (T_A = +25°C) (2) 3.4W
Junction Temperature.....150°C
Lead Temperature ..... 260°C
Storage Temperature..... -65°C to +150°C

Recommended Operating Conditions (2)

Supply Voltage V_{IN} .....9V to 18V
Operating Temperature..... –20°C to +85°C

Thermal Resistance (3)

	θ_{JA}	θ_{JC}	
5x5 TQFN40	36	8	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN}=12V, V_{OBUCK}=3.3V, V_{OBOOST}=16V, T_A=25°C unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
POWER SUPPLY						
Input Voltage Range			9	12	18	V
Quiescent Current	I_Q	No SW (EN1=EN2=VCC,FSEL=0 V_{FBBK}=V_{FBBT}=V_{FBP}=1.5V,V_{FBN}=0)		3.5		mA
V_{IN} Under-Voltage Lockout	V_{UVLO}	IN rising, 200mV hysteresis	TBD	7.5	8.5	V
Shutdown Supply Current	I_{ST}	EN1=EN2=AGND		1200		µA
VCC REGULATOR						
VCC Output Voltage	V_{CC}	All regulators ready	4.8	5	5.2	V
VCC Source Current	I_{CC}				50	mA
VCC UVLO	V_{CCUVLO}	VCC rising, 200mV hysteresis	TBD	3.3	3.6	V
VREFERENCE						
Reference Voltage	V_{REF}	No load	1.214	1.227	1.241	V
VREF Load Regulation		0µA<I_{Load}<40µA			10	mV
VREF Max Source Current		External		40		µA
VREF Max Sink Current		External		10		µA
VREF UVLO	V_{R-UVLO}	Rising edge		1.0		V
INTERNAL OSCILLATOR						
Operating Frequency	f_{SW}	FSEL=GND	360	450	540	kHz
		FSEL = IN	540	675	810	
Oscillator Maximum Duty Cycle	D_{MAX}	FSEL= GND	85			%
		FSEL = IN	85			
FSEL Logic Low Voltage	V_{FSELL}				0.8	V
FSEL Logic High Voltage	V_{FSELH}		2.2			V
FSEL Sink Current				10		µA
BOOST REGULATOR						
Output Voltage Range					19.5	V
Min Turn-on Time	t_{ON-MIN}			100		nS
FBBT Regulation Voltage	V_{FBBT}		1.214	1.227	1.241	V
FBBT Fault Threshold	V_{FBBT-L}	Falling edge		1.0		V
FBBT Output Bias Current	I_{FBBT}	V_{FB} = 1.2V		1	100	nA
FBBT Trans-conductance		ΔI = +/-2.5µA at COMP	150	320	560	µS
FBBT Voltage Gain		FBBT to COMP		1400		V/V
SWBT On-Resistance	R_{ON-BT}	I_{SWBT} = 500mA		60	100	m Ω
SWBT Leakage Current	I_{LKG-BT}	V_{SWBT} =20V		0.1	5	µA
SWBT Current Limit	$I_{LIMIT-BT}$			5		A
Current-Sense Trans-resistance				0.2		V/A
Soft-Start Time	t_{SS-BT}	FSEL=GND		4		ms
OVP	V_{OVP}		19.2	19.5	19.8	V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN}=12V, V_{OBUCK}=3.3V V_{OBOOST}=16V, T_A=25°C unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
BOOST REGULATOR SWITCH						
SWI Supply Range	V_{SWI}		9		20	V
SWI-SWO Switch Resistance	R_{DS-SW}	Fully turn on		100		mΩ
SWI-SWO Current Limit	$I_{LIMIT-SW}$	SWI to SWO=11V		280		mA
BUCK REGULATOR						
Fixed Mode OUT Supply Voltage		FBBK=GND, no load	3.25	3.3	3.35	V
FBBK Adjustable-Mode Threshold		Dual mode comparator		0.2		V
FBBK Regulation Voltage in Adjustable-Mode	V_{FBBK}	Adjustable-Mode, V_{OUT}=3.3V, no load	1.214	1.227	1.241	V
FBBK Fault Trip Level	V_{FBBK-L}	Falling edge	0.85	0.9	0.95	V
FBBK Output Bias Current	I_{FB}	V_{FBBK}=1.2V		1	100	nA
SWBK to IN On-Resistance	R_{HDS-BK}	I_{LOAD} = 500mA		60	120	mΩ
SWBK to GND On-Resistance	R_{LDS-BK}	I_{LOAD} = 500mA		15		Ω
BST to SWBK Regulation Voltage		V_{IN}=12V, V_{OUT}=3.3V, I_{LOAD}=1A		5		V
SWBK Leakage Current	I_{LKG-BK}	V_{IN}=20V, V_{SWBK}= 0V		0.1	5	μA
SWBK Current Limit	$I_{LIMIT-BK}$			5		A
Current-Sense Trans-resistance			0.10	0.16	0.26	Ω
Low-Frequency Operation Output Ratio		Buck, Vout falling edge		50		%
Low-Frequency Operation Switching Frequency	f_{SW-L}	FSEL=GND		28		kHz
		FSEL=IN		42		
Soft-Start Time	t_{SS-BK}	FSEL=GND		1		ms
POWER-GOOD BLOCK						
FBBK Power Good Threshold	V_{TH-PG}	FBBK rising	0.85	0.9	0.95	V
FBBK Threshold Hysetersis				100		mV
PG to AGND Resistance	R_{DS-PG}	I_{PG}=1mA		900		Ω
PG Leakage Current	I_{LKG-PG}	V_{PG}=3.3V		0.1	1	μA
NEGATIVE CHARGE PUMP CONTROLLER						
External Load Driving Capability				120		mA
FBN Regulation Voltage	V_{FBN}		0.19	0.2	0.21	V
FBN output Bias Current	I_{LKG-N}	V_{FBN} = 0.2V		10	100	nA
FBN Fault Trip Level	V_{FBN-L}	Rising edge	0.3	0.4	0.5	V
High-Side Driver On Resistance	R_{HDS-N}	I_{LOAD}=20mA		5	8	Ω
Low-Side Driver Sink Current	I_{SINK-L}			1.2		A

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN}=12V, V_{OBUCK}=3.3V V_{OBOOST}=16V, T_A=25°C unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Soft-Start Time	t_{SS-N}	FSEL=GND		1		ms
POSITIVE CHARGE PUMP CONTROLLER						
External load Driving Capability				120		mA
FBP Regulation Voltage	V_{FBP}		1.20	1.227	1.25	V
FBP output Bias Current	I_{FBP}	V_{FBP} = 1.2V		10	100	nA
FBP Fault Trip Level	V_{FBP-L}	Falling edge	0.96	1.0	1.04	V
High-side Driver On resistance	R_{HDS-P}	I_{LOAD}=20mA		5	8	Ω
Low-side Driver Sink Current	I_{SINK-L}			1.2		A
Soft-Start time	t_{SS-P}	FSEL=GND		4		ms
GATE PULSE DRIVER AND CONTROL SWITCHES						
GPH Input Voltage Range				35	45	V
GPH Input Current	I_{GPH}	MODE = DLY4 = GPI = VCC		300	600	µA
GPI Input Low Voltage	V_{PGI-L}				0.6	V
GPI Input High Voltage	V_{PGI-H}		2.2			V
GPI Input Leakage Current	$I_{LKG-GPH}$	GPI = GND or VCC			10	nA
GPI-to-GPH Propagation Delay		1kOhm from GPD to GND,GPI = GND to VL step, no load on GPO, Measure V_{GPI}=2V to GPO=20%		60		ns
		1kOhm from GPD to GND,GPI = VL to GND step, no load on GPO, Measure V_{GPI}=0.6V to GPO=80%		60		ns
GPH-to-GPO Switch On-Resistance	R_{DS-GPH}	DLY4 = GPI =VCC		6	10	Ω
GPH-to-GPO Switch Saturation Current	I_{ST-GPH}	(V_{GPH}-V_{GPO})>6V	150	390		mA
GPD-to-GPO Switch On-Resistance	R_{DS-GPD}	DLY4 = VCC, GPI =GND		8	15	Ω
GPD-to-GPO Switch Saturation Current	I_{ST-GPD}	(V_{GPO}-V_{GPD})>6V	75	180		mA
GPO-to-PGND Switch On-Resistance	R_{DS-GPO}	DLY4 = 0, V_{GPO} = 5V	3	5	8	kΩ
MODE Switch On-Resistance	$R_{DS-MODE}$	DLY4 = 0, V_{GPO} = 5V		1250		Ω
MODE 1 Voltage Threshold	V_{TH-M1}	MODE rising edge		4	4.5	V
MODE Capacitor Charge Current	I_{MODE}	Mode 2,V_{MODE}<V_{VL}/4	40	50	60	µA
MODE 2 Voltage Threshold for Enabling GPD switch	V_{TH-M2}	MODE rising edge	1.2	1.25	1.3	V

ELECTRICAL CHARACTERISTICS *(continued)*

(Vin=12v, AVDD=16V, others see typical application diagram. Typical is at 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
MODE Current-Source Stop Voltage Threshold	$V_{LIMIT-M}$	MODE rising edge		2.5		V
DLY4 Turn-On Threshold	$V_{TH-DLY4}$			1.2		V
GPT-to-GPO Voltage Gain		V_{GPO} = 12V, V_{GPT} = 1.2V	9	10	11	V/V
SEQUENCE CONTROL						
EN1, EN2 Input H2L Voltage	V_{ENL}				0.6	V
EN1, EN2 Input L2H Voltage	V_{ENH}		2.2			V
EN1, EN2 Pull Down Current	I_{DOWN}			10		µA
DLY1, DLY2, DLY3, DLY4 Charge Current	I_{DLY}	$V_{DLY1~4}$ =1V		6		µA
DLY1, DLY2, DLY3, DLY4 Turn-on Threshold	V_{TH-DLY}		1.166	1.227	1.288	V
DLY1, DLY2, DLY3, DLY4 Discharge Resistance	R_{DLY}	EN1=GND or fault tripped		50		Ω
FAULT PROTECTION						
Duration to Trigger Fault				32		ms
Duration to Restart After Fault				130		ms
Number of Restart Attempts		Optional			5	
Thermal Shutdown,	T_{SD}	Temperature rising		150		°C
Thermal Shutdown Hysteresis				20		°C

PIN FUNCTIONS

Pin #	Name	Description
1	GPT	Gate Pulse Output (GPO) Low Level Threshold Set Input. Connect a resistor divider between boost output and GND. Tie GPT pin to the center of a resistive divider to set the GPO discharging low level. The low level is 10 times of GPT voltage.
2	PDRV	Driver Output pin of Positive Charge Pump. Connect charge pump capacitor to this pin.
3	GND1	Power Ground. Ground for GPM block.
4	GPH	Gate Pulse High Level Input. This pin is the output of the positive charge pump regulator.
5	GPO	Gate Pulse Output Pin. It is the common terminal of the internal High-Voltage MOSFET Switch.
6	GPD	Gate Pulse Low Level Discharge Pin. Connect a resistor from this pin to GND to set the GPO discharge speed.
7	MODE	Gate Pulse Block Mode Selection. See the High-Voltage Switch Control section for details.
8	DLY4	Gate Pulse Block Delay or Enable Pin. The Gate Pulse Block enables when positive charge pump regulator is ready and DLY4 voltage reaches 1.2V.
9	FBP	Positive Charge Pump Regulator Feedback Pin. Connect this pin to a resistor divider between the positive charge pump regulator output (GPH) and GND, which sets the positive charge pump regulator output voltage. Place the resister divider to FBP pin as close as possible.
10	GND2	Power Ground. It is refer to charge pump and buck regulator.
11	GPI	Gate Pulse Signal Input Pin.
12	NDRV	Negative Charge Pump Driver Output. Connect the negative charge pump flying capacitor to this pin.
13	AGND	Analog Ground
14	FBN	Negative Charge Pump Regulator Feedback Pin. Connect this pin to the center of a resistor divider between the negative output and REF to set the negative charge-pump regulator output voltage. Place the resister divider to FBP pin as close as possible.
15	REF	Internal Reference Output. Connect a decoupled capacitor from REF to GND. A 0.22μF ceramic capacitor is enough for most case.
16	DLY1	Negative Charge-Pump Delay Pin. Connect a capacitor from this pin to GND to set the delay time between the buck output and the negative charge pump output.
17	FBBK	Buck Regulator Feedback Pin. Connect this pin to GND to select the buck internal fixed 3.3V output. Connect FBBK to the center of a resistor divider between the buck regulator output and GND to set the buck regulator output voltage for adjustable output.

PIN FUNCTIONS *(continued)*

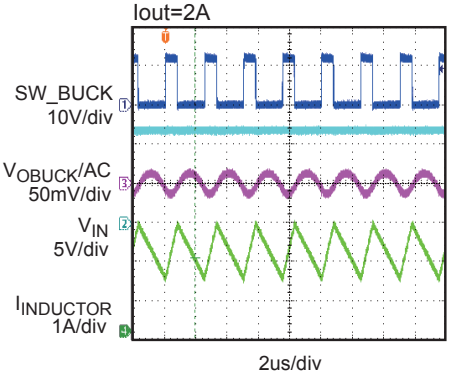
Pin #	Name	Description
18	BST	Buck Regulator Bootstrap Pin. Connect a capacitor between this pin and SWBK to form a floating supply to drive the internal MOSFET. 0.1μF is recommended for most application.
19.20	SWBK	Buck Regulator Switching Output. SWBK is the source of the internal N-channel MOSFET. Connect the inductor and schottky diode to SWBK pin.
21	VBK	Buck Regulator Output Pin. Connect buck regulator output to this pin.
22,23	IN1,IN2	Buck Regulator Power Input Pin. Drain of the internal N-channel MOSFET.
24	IN3	Input Pin for powering internal 5V regulator and logic circuitry. Bypass this pin to GND with a capacitor. A 0.22μF is enough for most application.
25	FSEL	Switching Frequency Select Pin. If FSEL is connected to GND, the switching frequency is set to 450kHz, if FSEL is connected to VCC, the switching frequency is set to 675kHz.
26	EN1	Buck and Negative Charge Pump Regulator Enable Pin. High level enables buck regulator, Low level disables buck regulator.
27	DLY2	Positive Charge Pump Delay Pin. Connect a capacitor from DLY2 and GND to set the delay time between the boost startup and the startup of positive charge pump regulator.
28	VCC	5V Internal Regulator Output Pin. Bypass VCC to GND with 1μF ceramic capacitor. It provides power for the internal reference, logic and driving circuit.
29	EN2	Boost and Positive Charge Pump Regulator Enable Pin. High level enables boost regulator, Low level disables boost regulator. EN2 is not effective before EN1 is high.
30,31	PGND	Power Ground. It is refer to boost regulator.
32,33	SWBT	Boost Regulator Power Switching Output. SWBT is the drain of the internal MOSFET. Connect the inductor and Schottky to both SWBT pins.
34	SWI	Boost Regulator Internal N-Channel MOSFET Pass Switch Input. It is the drain of internal isolation MOSFET. Connect the cathode of Schottky to SWI.
35	SWO	Boost Regulator Internal N-Channel MOSFET Pass Switch Output. It is the source of internal isolation MOSFET. SWO is the real boost regulator output.
36	FBBT	Boost Regulator Feedback Pin. Connect FBBT to the center of a resistor divider between the boost regulator output and GND to set the boost regulator output voltage.
37	COMP	Boost Regulator Compensation Pin. This pin is used to compensate the regulator control loop. Connect a capacitor or a series RC network from COMP pin to GND.
38	PG	Power Good Pin. Open-Drain Power Good Output indicator for buck regulator.
39	DLY3	Power Good Delay Pin. Connect a capacitor from DLY3 to GND to set the delay time between buck regulator and PG indication signal.
40	AGND	Analog Ground
EP	GND	Exposed Paddle (GND)

TYPICAL PERFORMANCE CHARACTERISTICS

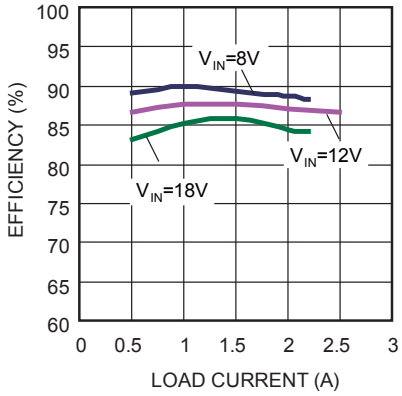
V_{IN} =12V, V_{OBUCK}=3.3V, V_{OBOOST}=16V, V_{GL}=-6V, V_{GPH}=35V, unless otherwise noted.

Buck Regulator Steady State Operation

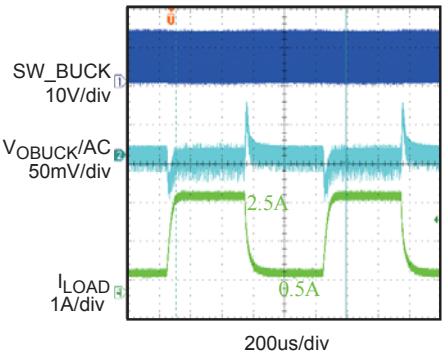
Iout=2A



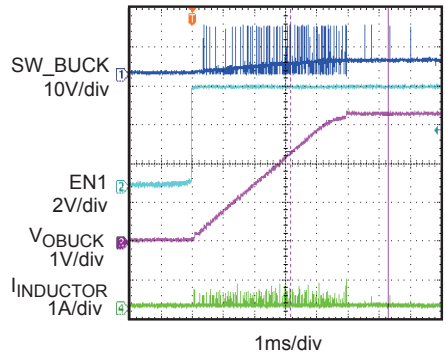
Buck Regulator Efficiency vs. Load Current



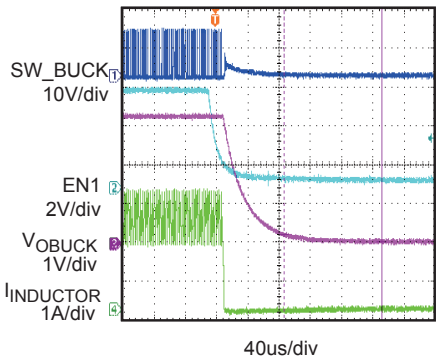
Buck Regulator Load Transient



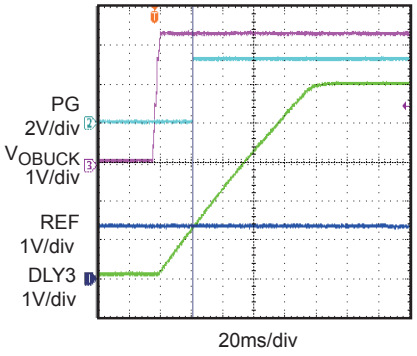
Buck Regulator Start Up



Buck Regulator Shut Down

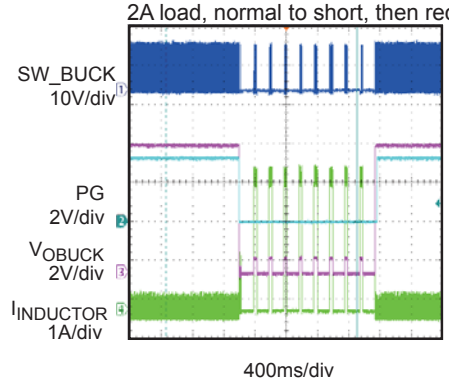


Buck Regulator Power Good Signal



Buck Regulator Short Circuit Protection

2A load, normal to short, then recovery

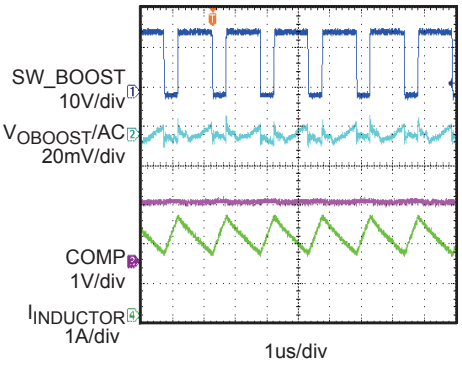


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

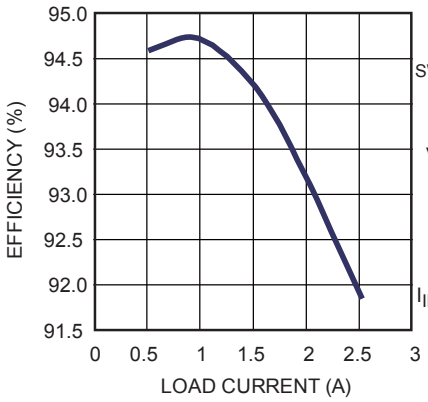
V_{IN} =12V, V_{OBUCK}=3.3V, V_{OBOOST}=16V, V_{GL}=-6V, V_{GPH}=35V, unless otherwise noted.

Boost Regulator Steady State Operation

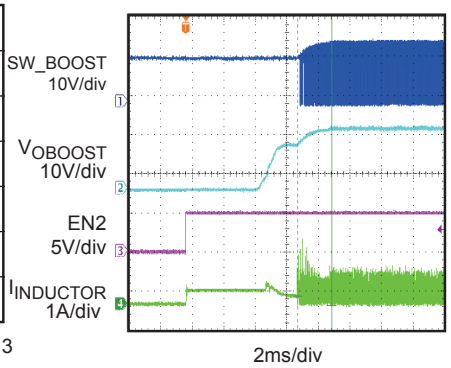
Iavdd=1.5A



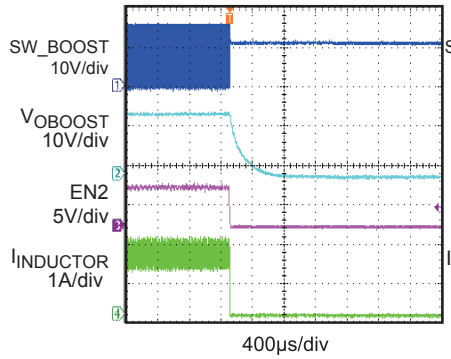
Boost Regulator Efficiency vs. Load Current



Boost Regulator EN2 Start Up

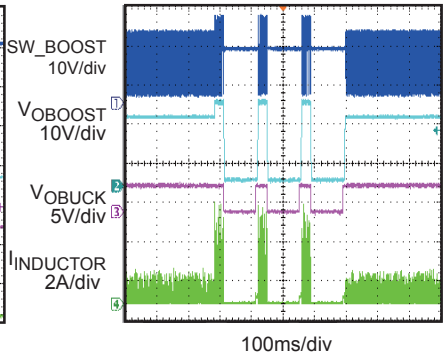


Boost Regulator EN2 Shut Down

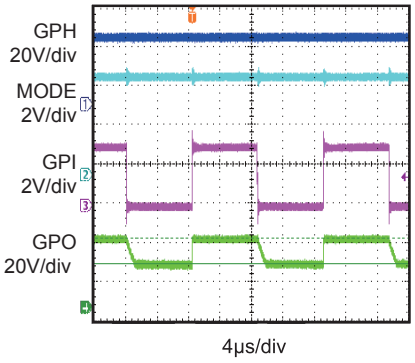


Boost Regulator OVP and Recovery

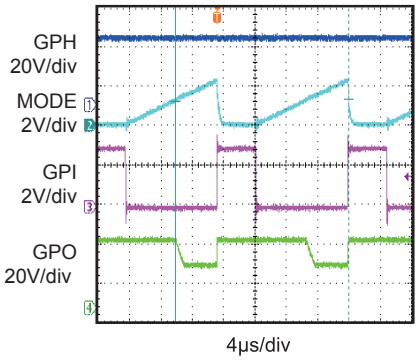
short R2, then recovery



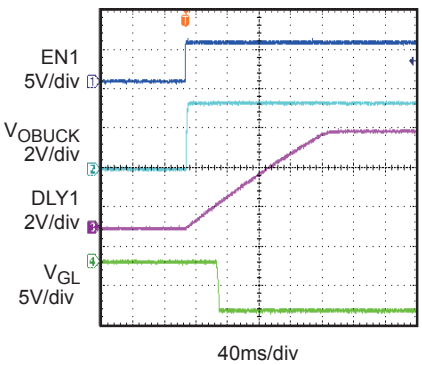
Gate Pulse Management MODE1



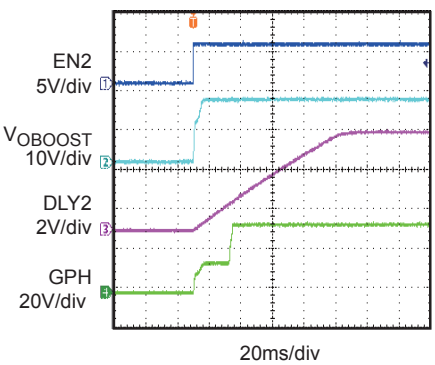
Gate Pulse Management MODE2



Power On Sequence



Power On Sequence



FUNCTION DIAGRAM

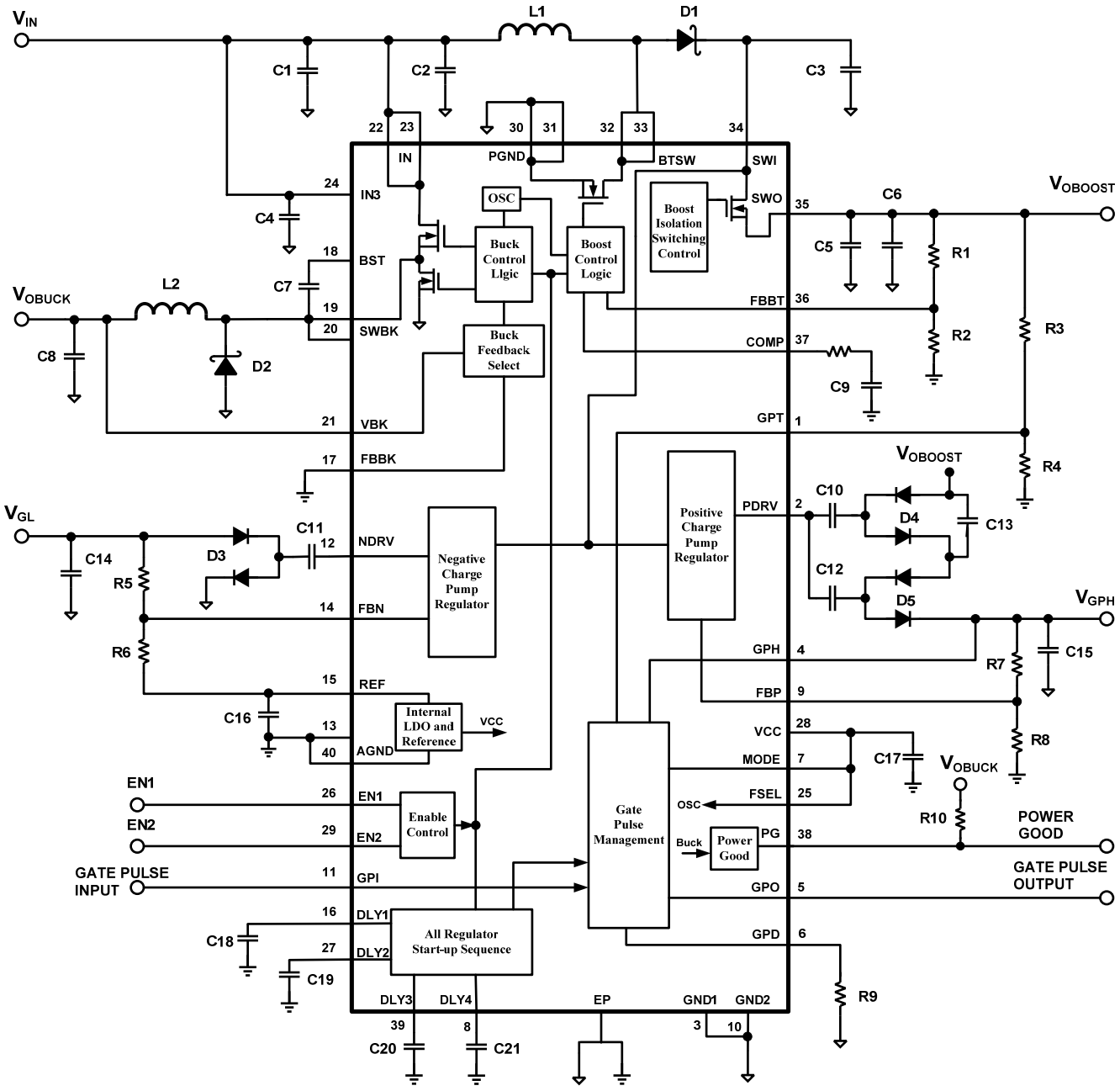


Figure 1—Functional Block Diagram

OPERATION

The MP5600 is a power supply designed for TFT LCD panels used in TVs and Monitors. It contains a buck switching regulator to generate the logic supply rail, a boost switching regulator to generate the source driver supply, and two charge-pump regulators to generate the gate driver supplies. Each regulator features adjustable output voltage, internal soft-start, and timer-delayed fault protection. Figure 1 shows the total functional block diagram.

Buck Regulator

The buck regulator employs fixed switching frequency, peak current mode architecture to obtain the quick response. It uses an internal N-channel MOSFET to step down the input voltage to the regulated output voltage. A bootstrap capacitor connected between SWBK and BST is required to drive the high-side MOSFET. See the figure2.

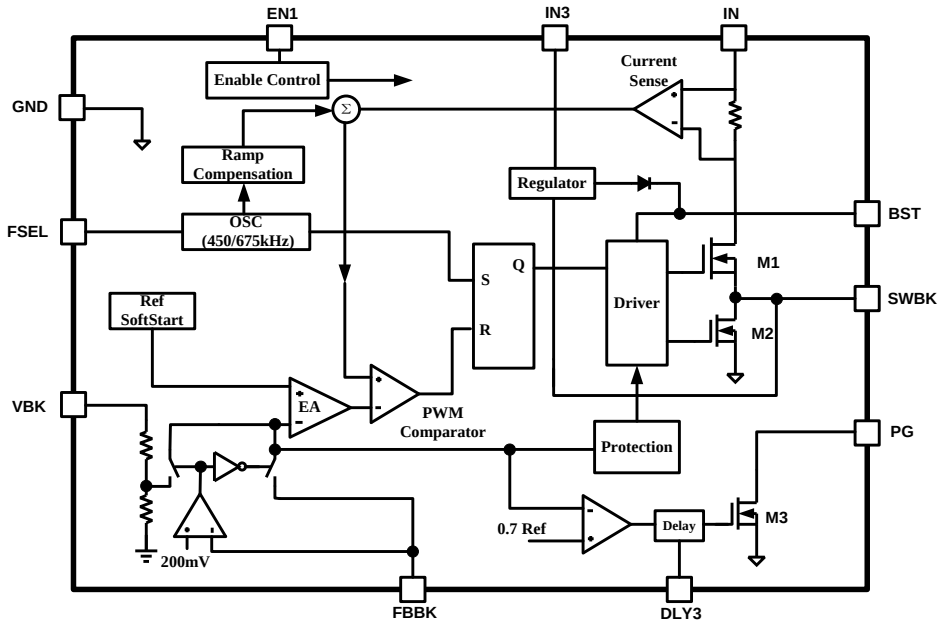


Figure 2 —Buck Regulator Block Diagram

At the beginning of a cycle, M1 is off. The EA output voltage is higher than the current sense amplifier output, and the current comparator's output is low. The rising edge of the oscillator signal sets the RS Flip-Flop. Its output turns on M1 thus connecting the SWBK pin and inductor to the input supply. The increasing inductor current is sensed and amplified by the Current Sense Amplifier. Ramp compensation is summed to the Current Sense Amplifier output and compared to the Error Amplifier output by the PWM Comparator. When the sum of the Current Sense Amplifier output and the Slope Compensation signal exceeds the EA output voltage, the RS Flip-Flop is reset and M1 is turned off. The external schottky rectifier diode conducts the inductor current. If the sum of the Current Sense Amplifier output and the Slope Compensation signal does not exceed the EA output for a whole cycle, then the falling edge of the CLK resets the Flip-Flop. The output of the Error Amplifier integrates the voltage difference between the feedback and the reference. The polarity is such that a FBBK pin voltage is lower than reference increases the EA output voltage. Since the EA output voltage is proportional to the peak inductor current, an increase in its voltage also increases current delivered to the output.

With dual mode feedback feature, the buck regulator supports both fixed and adjustable output voltages. Connect FBBT to GND to enable the 3.3V fixed output voltage. Connect a resistive voltage-divider between V_{OBUCK} and GND with the center point connected to FBBT to set the output voltage.

The buck regulator also includes a 15Ω low side MOSFET M2, this switch is used to charge the bootstrap capacitor during startup and reduce the

SW ring to improve the EMI performance at light load.

The buck regulator includes a 7-bit soft-start DAC that steps its internal reference voltage from 0 to 1.2V in 128 steps. The soft-start period is 1ms (fsw=450kHz)and FBBK fault detection is disabled during this period. The soft-start feature effectively minimizes the inrush current at startup

The MP5600 contains a power good output signal. When buck output voltage reaches the 70% threshold, the internal MOSFET M3 with open drain turns off. The power good signal delay time is determined by external capacitor on DLY3 pin.

The buck regulator provides the under voltage lockout, over current protection and short circuit protection. When short output to GND,MP5600 shuts down after it runs for 32ms. It restarts after 130ms until the fault is removed.

Boost Regulator

The boost regulator also uses a constant frequency, peak current mode architecture to regulate the feedback voltage. The output voltage can be set from V_{IN} to 19.5V with an external resistive voltage-divider. It can be understood by referring to the block diagram of the figure 3.

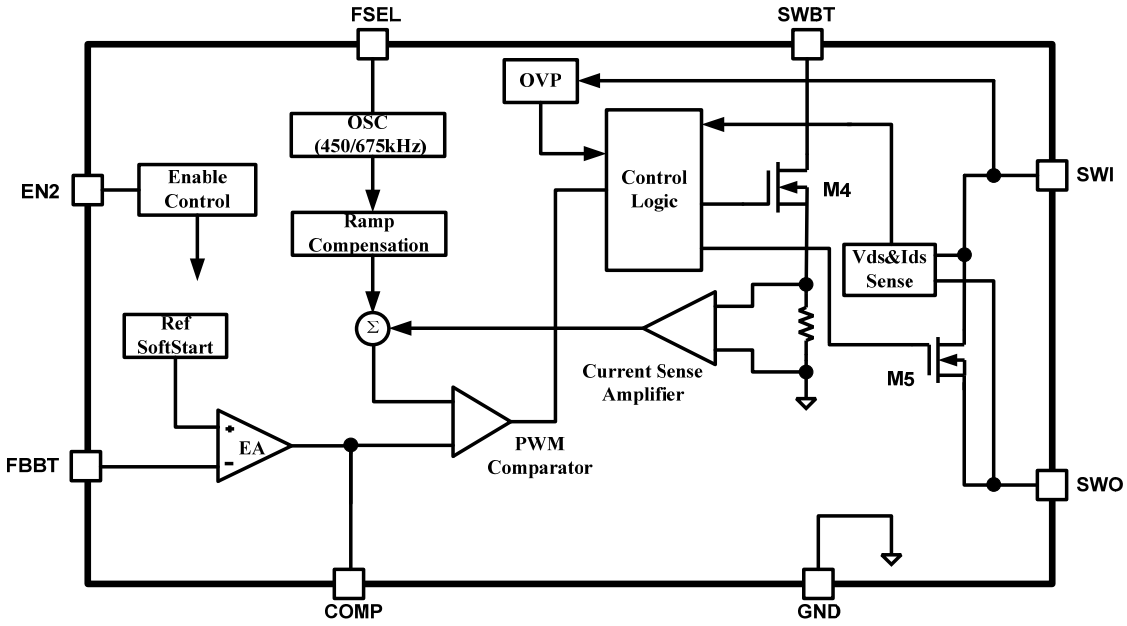


Figure 3 —Boost Regulator Block Diagram

At the beginning of each cycle, the N-Channel MOSFET switch M4 is turned on, forcing the inductor current to rise. The current at the source of the switch is internally measured and converted to a voltage by the current sense amplifier. That voltage is compared to the error voltage at COMP. The voltage at the output of the error amplifier is an amplified version of the difference between the reference voltage and the feedback voltage. When these two voltages are equal, the PWM comparator turns off the switch forcing the inductor current to the output capacitor through the external rectifier. This causes the inductor current to decrease. The peak inductor current is controlled by the voltage at COMP, which is controlled by the output voltage. Thus the output voltage controls the inductor current to satisfy the load.

The boost regulator includes a 7-bit soft-start DAC that steps its internal reference voltage from 0 to 1.2V in 128 steps. The soft-start period is 4ms (fsw=450kHz) and FBBT fault detection is disabled during this period. The soft-start feature effectively limits the inrush current during startup.

Boost Regulator Internal N-Channel MOSFET Pass Switch

The MP5600 contains an integrated 100mΩ high-voltage N-channel MOSFET pass switch M5 between SWI pin and SWO pin to achieve true disconnection of the boost regulator output (V_{OBOOST}) from input. This switch is connected in series between the boost regulator's schottky diode and its output capacitors. This switch also controls the startup inrush current into the boost regulator's output capacitors. See figure 3.

When EN2 is low, N-channel isolation MOSFET gate is pulled down to GND to make it turn off. Once EN2 is high, the MP5600 starts pulling up N-channel MOSFET Gate with variable current limit which clamp drain current. The internal N-channel MOSFET turns on and connects the cathode of the boost regulator schottky diode to the output capacitors, when N-channel MOSFET Drain-source voltage drops lower than 1V, the boost regulator begins to soft-start.

The boost regulator includes over voltage protection and short circuit protection. When output voltage exceeds the OVP threshold, the boost regulator shuts down. It restarts when output voltage is below OVP threshold. When short circuit occurs, the output current will be limited to about 300mA by internal isolated MOSFET to protect IC from damage.

Negative Charge-Pump Regulator

The negative charge-pump regulator provides the negative supply rail for the TFT LCD gate driver ICs. Connect a flying capacitor on NDRV pin. Tie an external resistor divider between negative charge pump output and REF. Connect the midpoint of resistor divider to FBN. The feedback divider determines the output of the negative charge-pump regulator. See figure 4.

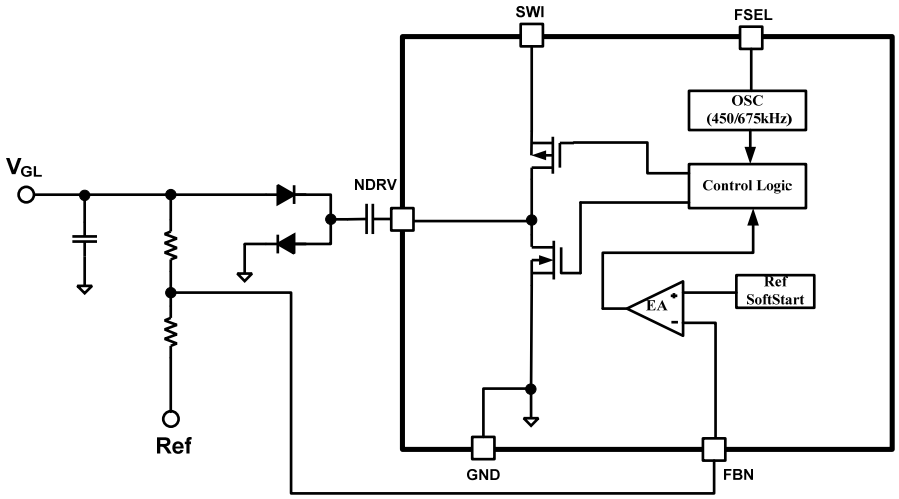


Figure 4 Negative Charge Pump Block Diagram

When EN1 is logic-high, An internal 6uA current source begins to charge the DLY1 capacitance, Negative charge pump will be enabled when the voltage on the capacitor exceeds 1.2V. Each time when it is enabled, the negative charge-pump regulator goes through a soft-start routine by ramping down its internal reference voltage from 1.20V to 200mV in 128 steps. The soft-start period is 1ms (fsw=450kHz) and FBN fault detection is disabled during this period.

Positive Charge-Pump Regulator

The positive charge-pump regulator provides the positive supply rail for the LCD gate driver ICs. Connect the flying capacitor to PDRV pin. Tie an external resistor divider between positive charge pump output and GND. Connect the midpoint of resistor divider to FBN. The feedback divider determines the output voltage of the positive charge-pump regulator. See figure 5.

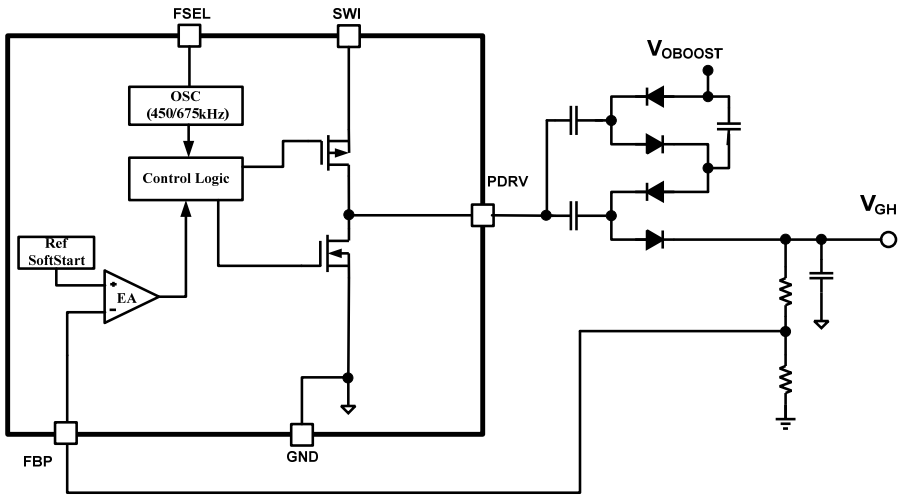


Figure 5 Positive Charge Pump Block Diagram

When EN2 is logic-high, An internal 6uA current source begins to charge the DLY2 capacitance, positive charge pump will be enabled when the voltage on the capacitor is higher than 1.2V. Each time when it is enabled, the positive charge-pump regulator goes through a soft-start routine by ramping up its internal reference voltage from 0 to 1.2V in 128 steps. The soft-start period is 4ms (fsw=450kHz) and FBP fault detection is disabled during this period.

Gate Pulse Management

Gate pulse management section consists of P-channel MOSFET: M6 is between GPH pin and GPO pin. M7 is between GPO pin and GPD pin. The GPM section is enabled when V_{DLY4} exceeds 1.2V. There are two different operation modes: mode 1 and mode 2. See figure 6.

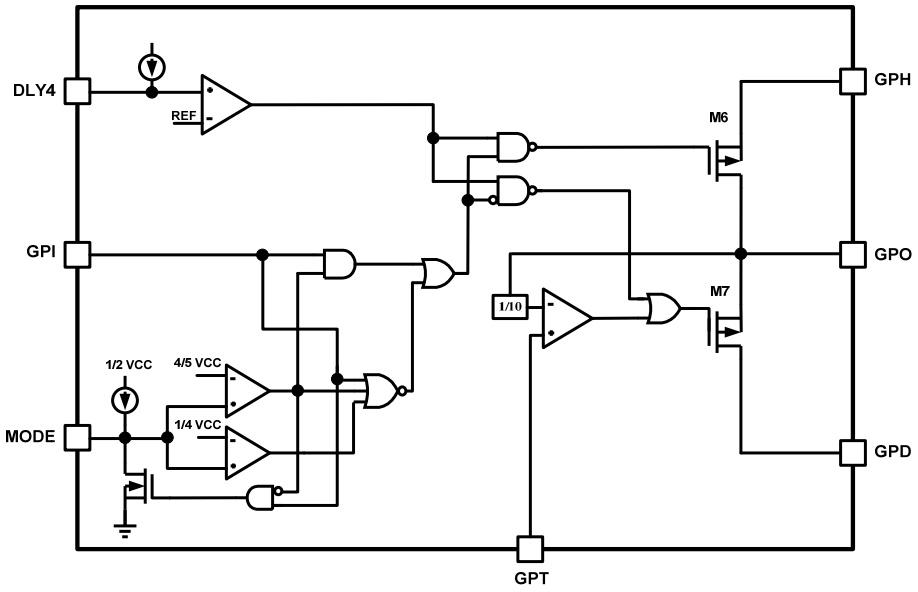


Figure 6 Gate Pulse Management Block Diagram

Mode 1 is selected by connecting the MODE pin to VCC. When GPI is high, GPO is connected to GPH through M6. When GPI is low, GPO is connected to GPD through M7. Then GPO is discharged through a resistor connected between GPD and GND. And the discharging of GPO is stop when V_{GPO} reaches 10 times of the voltage on GPT pin programmed by the external resistive divider. See figure 7.

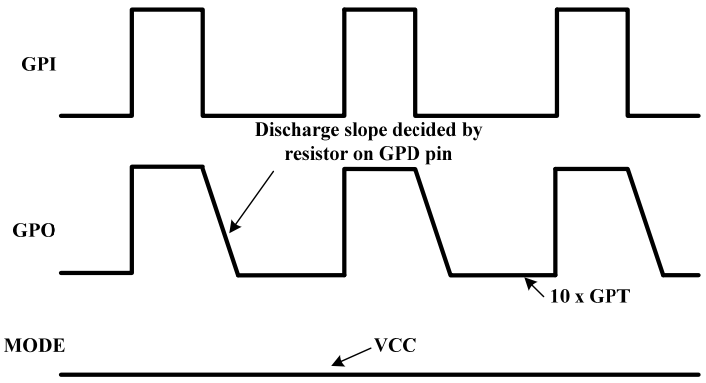


Figure 7 Gate Pulse Management at Mode 1

Mode 2 is selected by connecting a capacitor between MODE pin and GND. When the voltage of MODE pin is less than 4/5 VCC, it works in the mode 2. The rising edge of GPI signal makes GPO connect to GPH through M6. An internal switch meantime discharges the external capacitor between MODE and GND. The falling edge of GPI signal turns on an internal 50μA current source to start charging the MODE capacitor. Once MODE voltage exceeds 1/4 VCC, GPO will be connected to GPD through M7. Then GPO can be discharged through a resistor connected between GPD and GND or AVDD. And the discharging of GPO is stop when V_{GPO} reaches 10 times the voltage on GPT. See figure 8. The switch control function is disabled and DLY4 is held in low level when EN1 or EN2 is low or the IC is in a fault state.

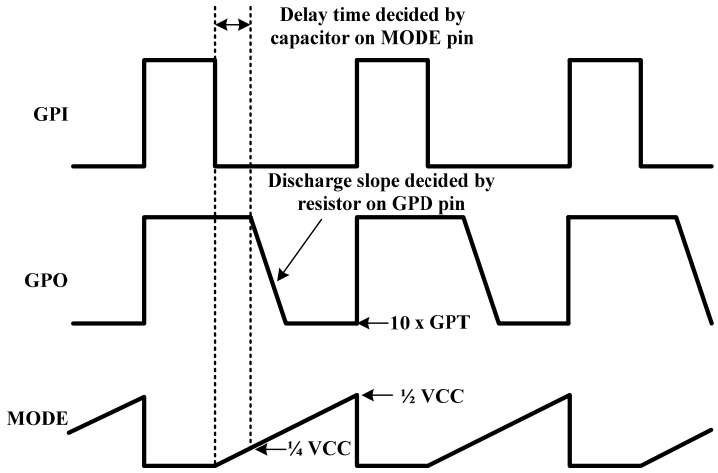


Figure 8 Gate Pulse Management at Mode 2

Linear Regulator (VCC)

The MP5600 contains an internal 5V linear regulator. V_{IN} is the input of the linear regulator. The input voltage range is from 9V to 18V. The regulator provides the power for the internal MOSFET drivers, PWM controllers, charge-pump regulators, and logic circuitry. Bypass VCC to GND with a ceramic capacitor.

Reference Voltage (REF)

The reference output is 1.2V. VCC is the input of the internal reference block. Bypass REF with a ceramic capacitor connected between REF and GND.

Power-On Sequence

The power-on sequence consists of 8 steps. See figure 9.

1. VCC is active whenever VIN is above under voltage lockout threshold (7.5V).

2. When the MP5600 internal reference voltage is above it's under voltage lockout threshold and EN1 is logic-high. The buck regulator starts up and a 6μA current source charges C_{DLY1} linearly. The FBBK fault-detection circuit disable in the soft-start period.
3. Once the buck regulator reaches 70% regulated value, the power good signal will be sent to indicate that the buck regulator is ready with some delay time programmed by the capacitance on DLY3 pin. See figure 10.
4. The negative charge-pump regulator soft-starts when DLY1 voltage reaches 1.2V (In despite of voltage on C_{DLY1} is over 1.2V, negative charge pump is not enabled if the buck regulator does not reach regulated voltage). FBN fault detection is enabled once the soft-start of the negative charge-pump is done.
5. The N-channel MOSFET pass switch begin to turn on when EN2 is logic-high. A 6μA current source at DLY2 pin charges C_{DLY2} linearly.
6. When the N-channel MOSFET pass switch Drain-Source voltage drop lower than 1V. The boost regulator begins to soft-start. FBBT fault detection is enabled once the positive charge-pump soft-start is done.
7. The positive charge-pump regulator soft-starts when DLY2 pin Voltage reaches 1.2V. FBP fault detection is enabled once the soft-start of the positive charge-pump is done.
8. A 6μA current source charges C_{DLY4} linearly. The gate pulse management is enabled and GPO can be controlled by GPI when V_{DLY4} reaches 1.2V.

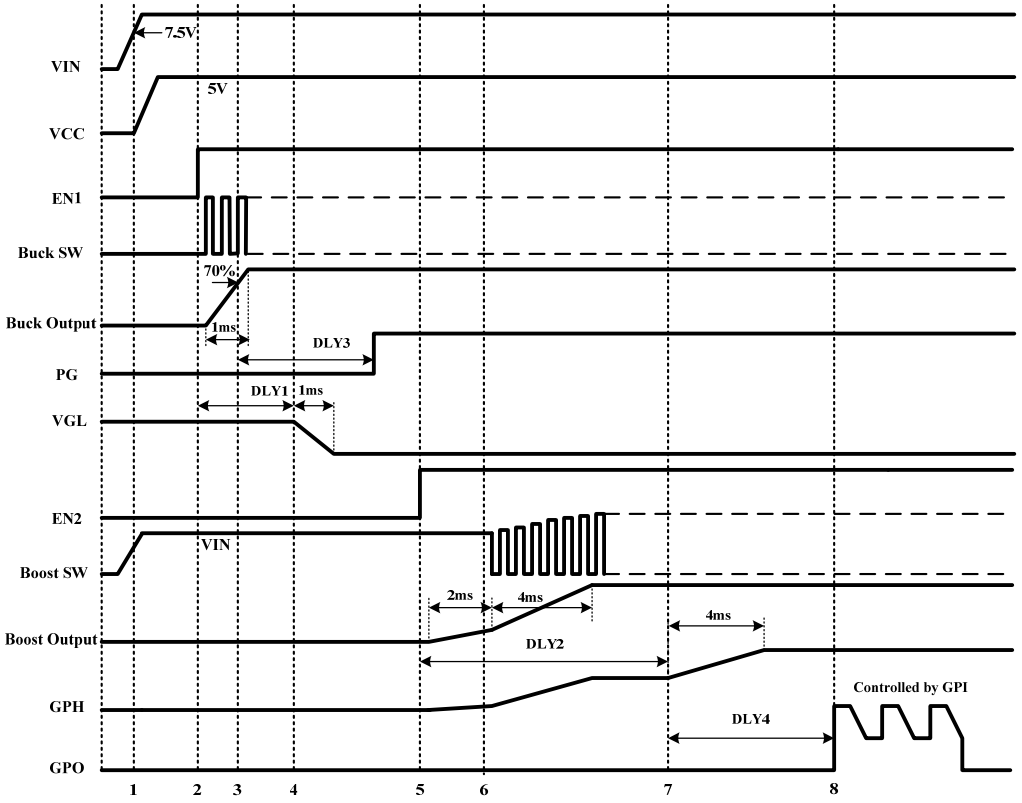


Figure 9—Power-On Sequence

Power-Off Control

The MP5600 disables the boost regulator, positive charge pump regulator, N-channel isolation pass switch, DLY2 delay block, and gate pulse management block when EN2 is logic-low, or when the fault latch is set. The buck regulator and negative charge-pump regulator are disabled only when EN1 is logic-low or when the fault latch is set.

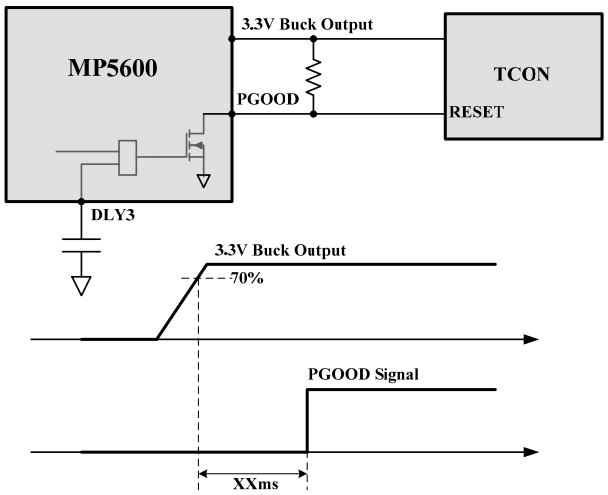


Figure 10—Open Drain Output of Power Good Signal

Fault Protection

During steady-state operation, if any output of the four regulators (buck regulator, boost regulator, positive charge-pump regulator, and negative charge-pump regulator) does not exceed its respective fault-detection threshold, the MP5600 activates an internal fault timer. If any condition or the combination of conditions indicates a continuous fault for the fault timer duration (32ms), the MP5600 triggers a non-latching output fault. After triggering, the MP5600 turns off for 130ms and then restarts according to the EN1 and EN2 logic states. If another 32ms fault timeout occurs after restarting, the MP5600 shuts down for 130ms again. It repeats until the fault is removed.

Thermal-Overload Protection

Whenever the temperature of MP5600 exceeds T_J = 150°C, It will shut down immediately. During shutdown there would be no output except VREF. It will work again after it cool down by 20 °C

APPLICATION INFORMATION

Frequency Selection (FSEL)

The buck regulator and boost regulator use the same internal oscillator. The FSEL input selects the switching frequency. Set the FSEL to high level for high switching frequency. High-frequency 675kHz operation optimizes the application for the smallest component size, trading off efficiency due to higher switching losses. Set the FSEL to low level for low switching frequency. Low-frequency 450kHz operation offers the best overall efficiency at the expense of component size and board space.

Buck Regulator

Setting the Output Voltage

If the FBBK pin is connected to GND, the output voltage is fixed to 3.3V.

The output voltage can also be programmed by using an external resistive voltage divider from the output voltage to GND pin by the equation:

$$V_{OBUCK} = V_{FBBK} \times (1 + \frac{R_H}{R_L})$$

Where, V_{OBUCK} is the output voltage. V_{FBBK} is the FBBK voltage. R_H is the high side divided resistor; R_L is the low side divided resistor, and it is recommended to range R_L from 5kΩ to 50kΩ.

Selecting the Inductor

The inductor is required to supply constant current to the output load while being driven by the switched input voltage. A larger value inductor will result in less ripple current that will result in lower output ripple voltage. However, the larger value inductor will have a larger physical size, higher series resistance, and/or lower saturation current.

A good rule for determining the inductance to use is to allow the peak-to-peak ripple current in the inductor to be approximately 30% of the maximum switch current limit. Also, make sure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by:

$$L = \frac{V_{OBUCK}}{f_S \times \Delta I_L} \times \left(1 - \frac{V_{OBUCK}}{V_{IN}}\right)$$

Where VIN is the input voltage, fs is the switching frequency, and ΔIL is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated by:

$$I_{LP} = I_{LOAD} + \frac{V_{OBUCK}}{2 \times f_S \times L} \times \left(1 - \frac{V_{OBUCK}}{V_{IN}}\right)$$

Where, I_{LOAD} is the buck regulator load current.

Selecting the Input Capacitor

The input current of the buck converter is discontinuous, therefore a capacitor is required to supply the AC current of the buck converter while maintaining the DC input voltage. Low ESR capacitors should be used to get high performance. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors may also suffice.

Since the input capacitor (C1) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OBUCK}}{V_{IN}} \times \left(1 - \frac{V_{OBUCK}}{V_{IN}}\right)}$$

The worse case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{C1} = \frac{I_{LOAD}}{2}$$

For simplification, choose the input capacitor whose RMS current rating is greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. when electrolytic or tantalum capacitors are used, a small and high quality ceramic capacitor should be placed as close to the IC as possible, usually, 0.1μF is enough for most application. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OBUCK}}{V_{IN}} \times \left(1 - \frac{V_{OBUCK}}{V_{IN}}\right)$$

Selecting the Output Capacitor

The output capacitor (C8) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to reduce the output voltage ripple. The output voltage ripple can be estimated by:

$$\Delta V_{OBUCK} = \frac{V_{OBUCK}}{f_S \times L} \times \left(1 - \frac{V_{OBUCK}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C8}\right)$$

Where L is the inductance of the inductor and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OBUCK} = \frac{V_{OBUCK}}{8 \times f_S^{\,2} \times L \times C8} \times \left(1 - \frac{V_{OBUCK}}{V_{IN}}\right)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated by:

$$\Delta V_{OBUCK} = \frac{V_{OBUCK}}{f_S \times L} \times \left(1 - \frac{V_{OBUCK}}{V_{IN}}\right) \times R_{ESR}$$

Selecting the Diode

The output rectifier diode supplies the current to the inductor when the high-side switch is off. To reduce losses due to the diode forward voltage and recovery times, Schottky diode is preferred.

Choose a diode whose maximum reverse voltage rating is greater than the maximum input voltage, and whose current rating is greater than the maximum load current.

Boost Regulator

Setting the Output Voltage

Set the output voltage by selecting the resistive voltage divider ratio. The R2 is low-side resistor of the voltage divider. Determine the high-side resistor R1 by the equation:

$$R1 = \frac{R2(V_{OBOOST} - V_{FB})}{V_{FB}}$$

Where V_{OBOOST} is the output voltage of the boost regulator.

Selecting the Inductor

The inductor is required to force the higher output voltage while being driven by the input voltage. A larger value inductor results in less ripple current that results in lower peak inductor current, reducing stress on the internal N-Channel switch. However, the larger value inductor has a larger physical size, higher series resistance, and/or lower saturation current.

The inductance value can be exactly calculated. A good rule of thumb is to allow the peak-to-peak ripple current to be approximately 30-50% of the maximum input current. Make sure that the peak inductor current is below 75% of the current limit value at the operating duty cycle to prevent loss of regulation due to the current limit. Also make sure that the inductor does not saturate under the worst-case load transient and startup conditions. Calculate the required inductance value by the equation:

$$L = \frac{V_{IN} \times (V_{OBOOST} - V_{IN})}{V_{OBOOST} \times f_S \times \Delta I}$$

$$I_{IN(MAX)} = \frac{V_{OBOOST} \times I_{LOAD(MAX)}}{V_{IN} \times \eta}$$

$$\Delta I = (30\% - 50\%) I_{IN(MAX)}$$

Where $I_{LOAD(MAX)}$ is the maximum load current, ΔI is the peak-to-peak inductor ripple current, and η is efficiency.

Selecting the Input Capacitor

An input capacitor is required to supply the AC ripple current of the inductor, while limiting noise at the input source. A low ESR capacitor is required minimize the noise of the IC. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors may also suffice.

The capacitance of the input capacitor should be greater than 4.7μF. The capacitor can be electrolytic, tantalum or ceramic. However since it absorbs the input switching current, it requires an adequate ripple current rating. Use a capacitor with RMS current rating which is greater than the inductor ripple current.

Place the input capacitor as close to the IC as possible to reduce the noise. Alternately a smaller and high quality ceramic capacitor should be placed closer to the IC if the larger capacitor

is placed further away, usually 0.1μF is enough for most application. If using this technique, it is recommended that the larger capacitor will be tantalum or electrolytic type. All ceramic capacitors should be placed close to the MP5600.

Selecting the Output Capacitor

The output capacitor is required to maintain the DC output voltage. Low ESR capacitors are preferred to minimize the output voltage ripple. The characteristic of the output capacitor also affects the stability of the regulation control system. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. In the case of ceramic capacitors, the impedance of the capacitor at the switching frequency is dominated by the capacitance, and so the output voltage ripple is mostly independent of the ESR. The output voltage ripple is estimated to be:

$$V_{RIPPLE} \approx \frac{\left(1 - \frac{V_{IN}}{V_{OBOOST}}\right) \times I_{LOAD}}{C5 \times f_S}$$

Where V_{RIPPLE} is the output ripple voltage, V_{OBOOST} is the output voltage, I_{LOAD} is the load current, f_S is the switching frequency, and C5 is the capacitance of the output capacitor.

In the case of tantalum or low-ESR electrolytic capacitors, the ESR dominates the impedance at the switching frequency, and so the output ripple is calculated as:

$$V_{RIPPLE} \approx \frac{(1 - \frac{V_{IN}}{V_{OBOOSTT}}) \times I_{LOAD}}{C5 \times f_S} + \frac{I_{LOAD} \times R_{ESR} \times V_{OBOOSTT}}{V_{IN}}$$

Where, R_{ESR} is the equivalent series resistance of the output capacitors.

Selecting the Diode

The output rectifier diode supplies current to the inductor when the internal MOSFET is off. To reduce losses due to diode forward voltage and recovery time, Schottky diode should be used. The diode should be rated with a reverse voltage equal to or greater than the output voltage. The average current rating should be greater than the maximum load current expected, and the peak current rating should be greater than the peak inductor current.

Compensation

The output of the trans-conductance error amplifier (COMP) is used to compensate the regulation control system. The external RC network connected to COMP pin can maintain loop stability and adjust the system response performance. A high capacitor value and low resistor value can be used to increase system stability. A low capacitor value and high resistor value can be used to improve the transient response. A single 22nF capacitor on COMP pin is usually sufficient for most application.

Charge Pump Regulator

Selecting the Number of Charge-Pump Stages

For highest efficiency, always choose the lowest number of charge-pump stages that meet the output requirement. The number of positive charge-pump stages is given by:

$$N_P = \frac{V_{GPH} + V_{DROP} - V_{OBOOST}}{V_{SWI} - 2 \times V_D}$$

Where N_P is the number of positive charge-pump stages, V_{GPH} is the output of the positive charge-pump regulator, V_{SWI} is the supply voltage of the charge pump regulators, V_D is the forward voltage drop of the charge-pump diode, and V_{DROP} is the dropout margin for the regulator. Use V_{DROP} = 300mV.

The number of negative charge-pump stages is given by:

$$N_N = \frac{-V_{GL} + V_{DROP}}{V_{SWI} - 2 \times V_D}$$

Where N_N is the number of negative charge-pump stages and V_{GL} is the output of the negative charge pump regulator.

The above equations are derived based on the assumption that the first stage of the positive charge pump is connected to V_{OBOOST} and the first stage of the negative charge pump is connected to ground. Sometimes fractional stages are more desirable for better efficiency. This can be done by connecting the first stage to V_{OBUCK} or another available supply. If the first charge-pump stage is powered from V_{OBUCK}, then the above equations become:

$$N_P = \frac{V_{GPH} + V_{DROP} - V_{OBUCK}}{V_{SWI} - 2 \times V_D}$$

$$N_N = \frac{-V_{GL} + V_{DROP} + V_{OBUCK}}{V_{SWI} - 2 \times V_D}$$

Selecting Flying Capacitors

Increasing the flying capacitors (connected to NDRV and PDRV) value lowers the effective source impedance and increases the output-current capability. Increasing the capacitance indefinitely has a negligible effect on output-current capability because the internal switch resistance and the diode impedance place a lower limit on the source impedance. A 0.1μF ceramic capacitor works well in most low-current applications. The flying capacitor's voltage rating must exceed the following:

$$V_C = N \times V_{SWI}$$

Where N is the stage number in which the flying capacitor appears.

Setting the Output Voltage

Increasing the output capacitance or decreasing the ESR reduces the output ripple voltage and the peak to peak transient voltage. With ceramic capacitors, the output voltage ripple is dominated by the capacitance value. Use the following equation to approximate the required capacitor value:

$$C_{CP\text{-}OUT} \geq \frac{I_{LOAD}}{2 \times f_S \times V_{RIPPLE}}$$

Where $C_{CP\text{-}OUT}$ is the output capacitor of the charge pump, I_{LOAD} is the load current of the charge pump, and V_{RIPPLE} is the peak-to-peak value of the output ripple. Adjust the positive charge-pump regulator's output voltage by connecting a resistive voltage-divider from the GPH output to GND with the center tap connected to FBP. Select the lower resistor of divider R8 in the 10kΩ to 30kΩ range. Calculate the upper resistor, R7, with the following equation:

$$R_7 = R_8 \times (\frac{V_{GPH}}{V_{FBP}} - 1)$$

Where V_{FBP} = 1.25V

Adjust the negative charge-pump regulator's output voltage by connecting a resistive voltage-divider from V_{GL} to REF with the center tap connected to FBN. Select R6 in the 20kΩ to 50kΩ range. Calculate R5 with the following equation:

$$R_5 = R_6 \times \frac{V_{FBN} - V_{GL}}{V_{REF} - V_{FBN}}$$

Where V_{FBN} = 200mV, VREF = 1.25V.

LAYOUT CONSIDERATION

Careful attention must be paid to the PCB board layout and components placement. Proper layout of the high frequency switching path is critical to prevent noise and electromagnetic interference problems. Please follow these guidelines and take EV board for reference.

1) Keep the path of switching current short and minimize the loop of high frequency pulse current. For buck converter, the loop formed by input capacitor, internal high-side MOSFET and external Schottky diode should be as short as possible. For boost converter, the loop formed by output capacitor, internal low-side MOSFET and external Schottky diode should be minimized.
2) Bypass ceramic capacitors connected to Vin pin, VCC pin and REF pin, capacitors adjusted delay time on DLY1~4 pin should be placed as close to IC as possible.
3) Ensure all feedback connections are short and direct. Place all feedback resistors and compensation components as close to the chip as possible.
4) Route SWBK, SWBT away from sensitive analog areas such as FBBK, FBBT, FBN and FBP.
5) Minimize the length and maximize the width of power trace with large current for best transient responses and efficiency, such as the traces between input capacitor, internal MOSFET, inductor, external Schottky and output capacitor.
6) Isolate the power ground (PGND) and analog ground (AGND), and connect PGND and AGND at single point.

   For buck regulator, create a power ground including input and output capacitor ground and diode ground. Connect all these together with short, wide trace to GND2 pin.

   For boost regulator, create a power ground (PGND), consisting of the input and output capacitor grounds and connect all these together with short, wide trace to PGND pin.

   For the positive, negative charge pump regulators and Gate Pulse Management, create a power ground (GND1 and GND2), consisting of SWI and output (GPH, VGL)

capacitor grounds, and negative charge-pump diode ground. Connect them to GND1 and GND2 pins.

Connect all ground planes together with wide traces. Maximizing the width of the power ground traces can improve efficiency and reduce output voltage ripple and noise.

Create an analog ground plane (AGND) including all the feedback divider ground connections, the COMP and DLY capacitor ground, AGND pin and the device's exposed backside pad. Connect AGND and PGND by connecting the two ground pins directly to the exposed backside pad.

TYPICAL APPLICATION CIRCUIT

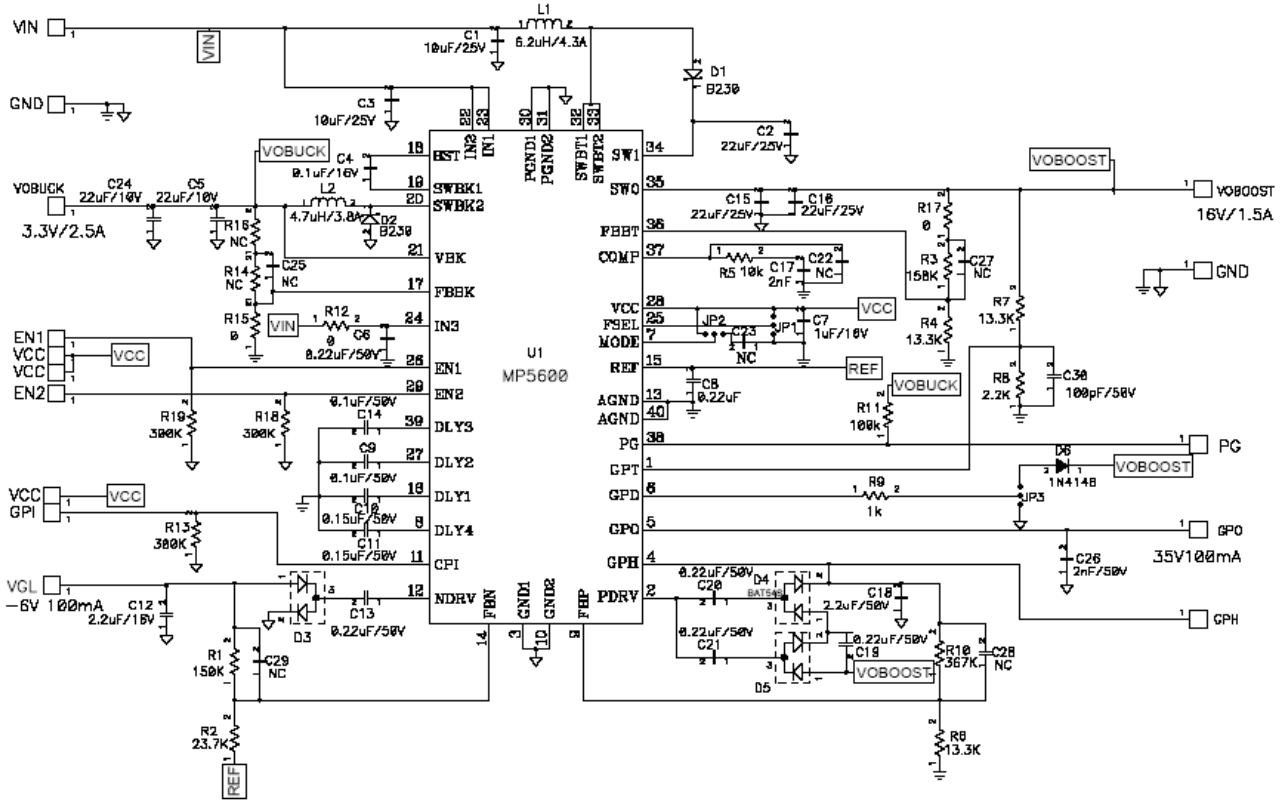
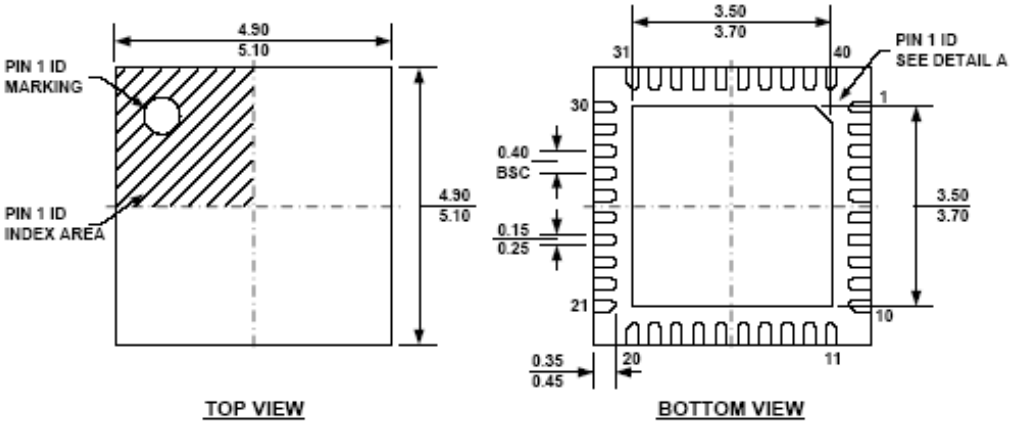
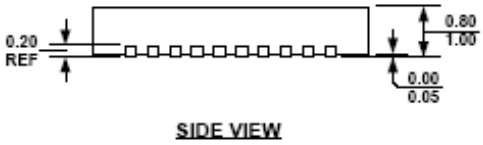


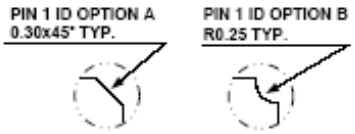
Figure 11—Multiple-Output, Low-Profile LCD TV Power Supply

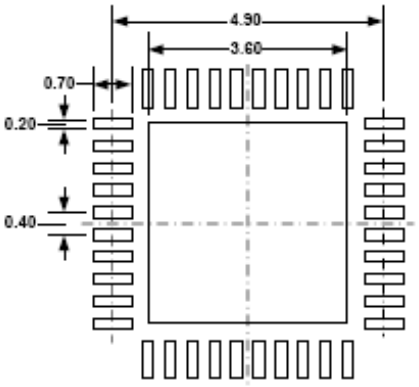
PACKAGE INFORMATION

QFN40 (5mm x 5mm)









NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFIRMS TO JEDEC MO-220, VARIATION VHHC-2.
5) DRAWING IS NOT TO SCALE.