# MP5507E

## 7V, 3A, High-Efficiency, Energy Management IC for Power Backup

The Future of Analog IC Technology

## DESCRIPTION

The MP5507E is an integrated power management IC that provides a power backup function for solid-state drive and hard-disk drive applications. The MP5507E provides an efficient and compact system solution with an integrated, programmable, input-current limit switch, energy storage, and a backup function.

The MP5507E applies MPS' patented energy storage and release management technology to minimize the required storage components, system solution size, and cost. The MP5507E boosts up the input voltage to a higher storage voltage in normal condition and releases the energy to the system when an input outage occurs. The internal input current limit block with DVDT control prevents inrush current during system start-up and provides reverse current blocking during the backup period. The system voltage start-up slew rate can be programmable. The storage voltage and release voltage are both programmable for different system applications.

The MP5507E requires a minimal number of readily available, standard, external components and is available in a QFN-16 (2.5mmx3.2mm) package.

## FEATURES

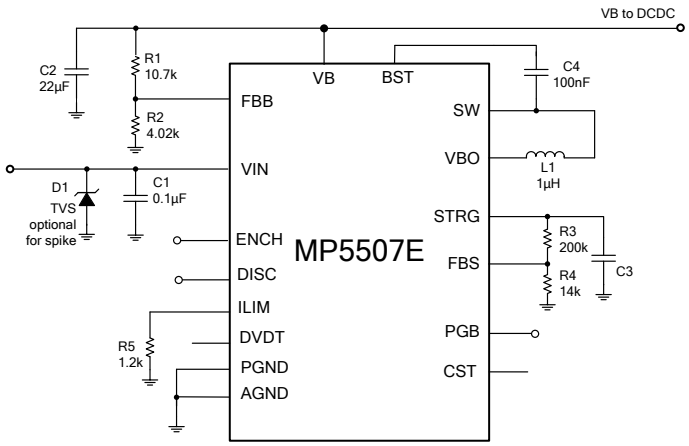
- Small 2.5mmx3.2mm QFN-16 Package
- Wide 2.7V to 7V Operating Input Range
- Programmable Storage Voltage up to 30V
- Up to 4.6A Programmable Input Current Limit
- Up to 3A Buck Release Current Capability
- Reverse Current Block of Input Switch
- 6V Bus Clamping Voltage
- Adjustable DVDT Slew Rate for VB Start-Up
- Bus Power Good Indicator
- 1.2MHz Buck Release Mode Switching Frequency
- Internal 60mΩ Hot-Swap Switch
- Internal 100mΩ and 80mΩ Power Switches for Energy Storage and Release Management Circuits
- Thermal Protection

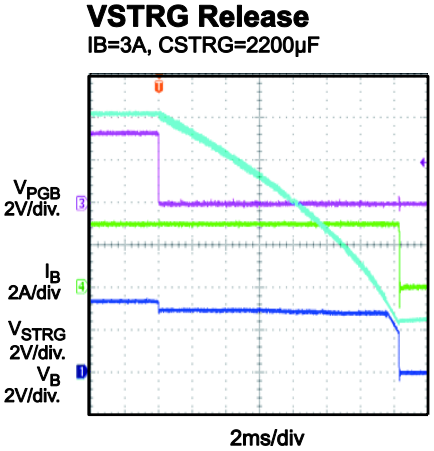
## APPLICATIONS

- Solid-State Drives
- Hard-Disk Drives
- Power Back-Up Systems



## TYPICAL APPLICATION



## ORDERING INFORMATION

| Part Number* | Package | Top Marking |
|---|---|---|
| MP5507EGRG | QFN-16 (2.5mmx3.2mm) | *See Below* |

* For Tape & Reel, add suffix –Z (e.g. MP5507EGRG–Z)

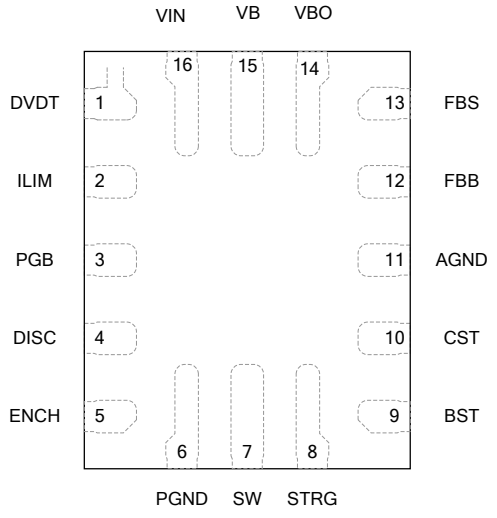
## TOP MARKING

AVU
YWW
LLL

AVU: Product code of MP5507E
Y: Year code
WW: Week code
LLL: Lot number

## PACKAGE REFERENCE

**TOP VIEW**




**QFN-16 (2.5mmx3.2mm)**

## ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage ($V_{IN}$) ..... 8.0V
$V_{STRG}$ ..... -0.3V to 35V
$V_{SW}$ ..... -0.3V to $V_{STRG}$ + 0.3V
$V_{BST}$ ..... -0.3V to $V_{STRG}$ + 6.5V
$V_{CST}$ ..... -0.3V to 40V
All other pins ..... -0.3V to 6.5V
Continuous power dissipation ($T_A$ = +25°C) (2) ..... 2.08W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Operating temperature ..... -40°C to +85°C

## *Recommended Operating Conditions* (3)

Supply voltage ($V_{IN}$) ..... 2.7V to 7V
Bus voltage ($V_B$) ..... 2.7V to 6V
Storage voltage ($V_{STRG}$) ..... $V_{IN}$ to 30V
Max. input current ..... 4.6A
Max. buck release current ..... 3A
Operating junction temp. ($T_J$). .. -40°C to +125°C

## *Thermal Resistance* (4) $\theta_{JA}$ $\theta_{JC}$

| | | |
|---|---|---|
| QFN-16 (2.5mmx3.2mm) | 60 | 14 °C/W |

**NOTES:**

1) Exceeding these ratings may damage the device.
2) The maximum power dissipation is a function of the maximum junction temperature $T_J$ (MAX), the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature $T_A$. The maximum continuous power dissipation at any ambient temperature is calculated by $P_D$ (MAX) = ($T_J$ (MAX)-$T_A$)/$\theta_{JA}$. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

**$V_{IN}$ = 5.0V, $T_A$ = 25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Input supply voltage range | $V_{IN}$ | | 2.7 | | 7 | V |
| Supply current (quiescent) | $I_Q$ | $V_{ENCH}$ = 2V, $V_{FBB/FBS}$ = 1V | | | 2 | mA |
| VIN under-voltage lockout threshold rising | $INUV_R$ | | | 2.5 | 2.7 | V |
| VIN under-voltage lockout threshold hysteresis | $INUV_{HYS}$ | | 0.3 | 0.4 | 0.5 | V |
| ENCH high threshold rising | $ENCH_R$ | | | | 1.2 | V |
| ENCH low threshold falling | $ENCH_F$ | | 0.4 | | | V |
| DISC high threshold rising | $DISC_R$ | | | | 1.2 | V |
| DISC low threshold falling | $DISC_F$ | | 0.4 | | | V |
| VIN to VB current limit FET on resistance | $R_{DS(ON)}$ | | | 60 | | mΩ |
| Continuous current limit | $I_{LIM}$ | $R_{ILIM}$ = 1.4kΩ | 3.24 | 3.6 | 3.96 | A |
| Off-state leakage current | $I_{LEAK}$ | $V_{IN}$ = 6V, $V_B$ = 0V or $V_B$ = 6V, $V_{IN}$ = 0V | | | 2 | μA |
| VB clamping voltage | $V_{CLAMP}$ | $V_{IN}$ = 7V | 5.5 | 6 | 6.5 | V |
| Rise time (DVDT) | $T_R$ | DVDT floating | | 0.8 | | ms |
| | | Connect a capacitor to DVDT, test DVDT charge current | | 2 | | μA |
| Internal reset delay time | $T_D$ | Power on to VB rise delay | | 1.1 | | ms |
| Pre-charge current | $I_{CH-PRE}$ | | | 130 | | mA |
| Charge peak current in boost mode | $I_{CH}$ | | | 500 | | mA |
| Boost disconnect switch $R_{on}$ | $R_{dison}$ | | | 25 | | mΩ |
| Energy management HS $R_{on}$ | $R_{Hon}$ | | | 100 | | mΩ |
| Energy management LS $R_{on}$ | $R_{Lon}$ | | | 80 | | mΩ |
| Feedback voltage | $V_{FBB}$, $V_{FBS}$ | | 0.782 | 0.79 | 0.81 | V |
| Feedback current | $I_{FBB}$ | $V_{FBB}$ = $V_{FBS}$ = 0.79V | | | 50 | nA |
| PGB high threshold | $PG_{H\_B}$ | | | 1.03 | | $V_{FBB}$ |
| PGB low threshold | $PG_{L\_B}$ | | | 1 | | $V_{FBB}$ |
| PGB delay | $PG_{D\_B}$ | Falling | | 0.5 | | μs |
| PGB sink current capability | | Sink 4mA | | | 0.3 | V |
| PGB leakage current | | $V_{PGB}$ = 3.3V | | | 120 | nA |
| Buck-mode dumping peak current limit | $I_{DUMP}$ | | | 5 | | A |
| Release-buck switching frequency | $f_{s\_RLS}$ | | | 1.2 | | MHz |

## ELECTRICAL CHARACTERISTICS *(continued)*

**$V_{IN}$ = 5.0V, $T_A$ = 25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| VB under-voltage lockout threshold rising (5) | INUVBR | | 1.8 | 2.2 | 2.5 | V |
| VB under-voltage lockout threshold hysteresis (5) | $INUVB_{HYS}$ | | 0.15 | 0.25 | 0.35 | V |
| Thermal shutdown (6) | $T_{SD}$ | | | 150 | | °C |
| Thermal shutdown hysteresis (6) | $T_{HYS}$ | | | 30 | | °C |

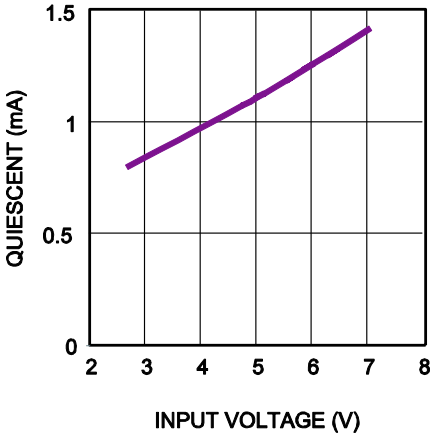
**NOTES:**

5) VB UVLO is applied to energy storage and release circuitry.
6) Guaranteed by characterization, not tested in production.

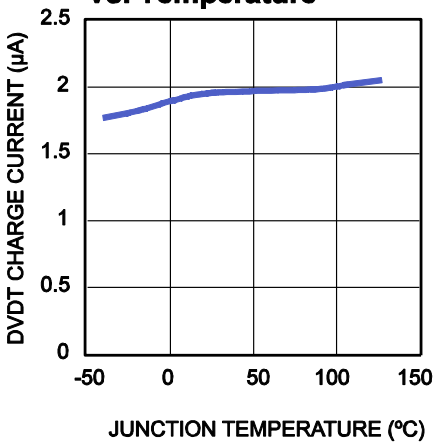
## TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{IN}$ = 3.3V, $V_{STRG}$ = 12V, $V_{RLS}$ = 2.9V, L = 1µH, $T_A$ = 25°C, unless otherwise noted.**

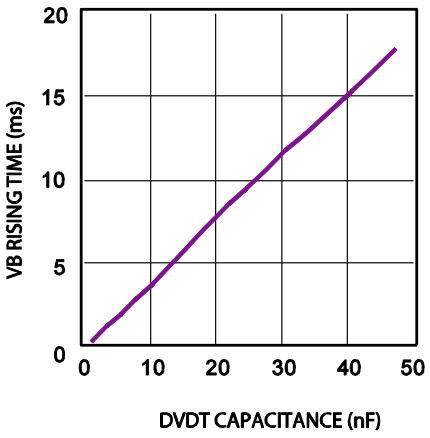
**Quiescent Current Vs. Input Voltage**



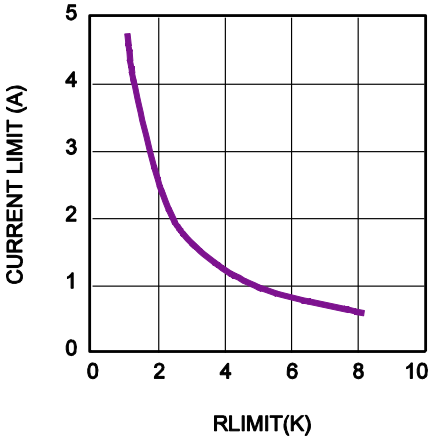

**DVDT Charge Current Vs. Temperature**



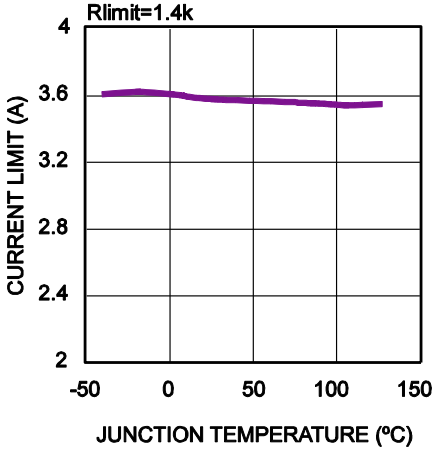

**VB Rising Time Vs. DVDT Capacitance**



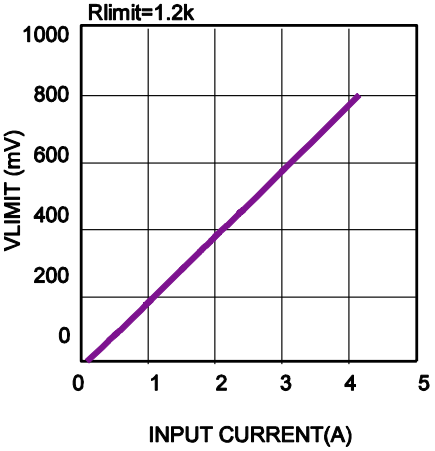

**VIN to VB Current limit Vs. Limit Resistor**




**VIN to VB Current limit Vs. Temperature**



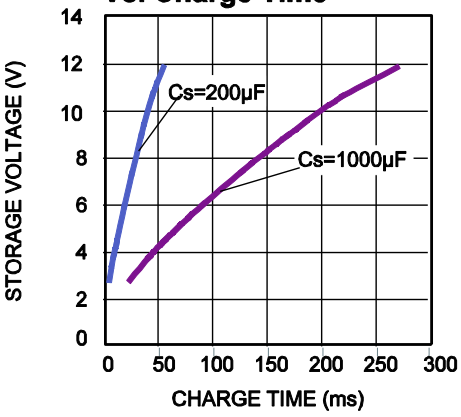

**ILIM Monitor Voltage Vs. Input Current**



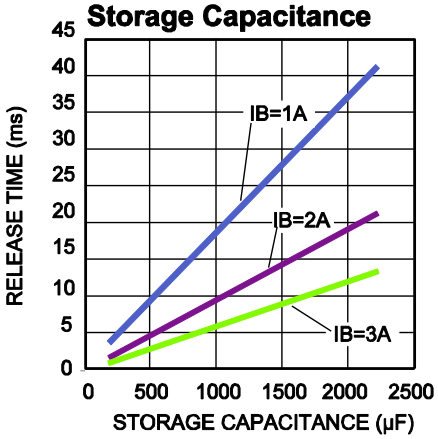
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**Performance waveforms are tested on the evaluation board of the Design Example section.**
**$V_{IN}$ = 3.3V, $V_{STRG}$ = 12V, $V_{RLS}$ = 2.9V, L = 1μH, $T_A$ = 25°C, unless otherwise noted.**

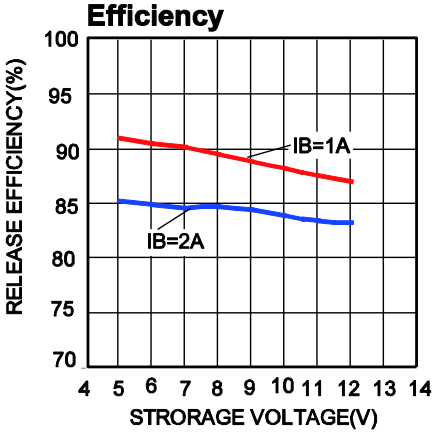
**Storage-Charge Voltage Vs. Charge Time**




**Release Time Vs. Storage Capacitance**

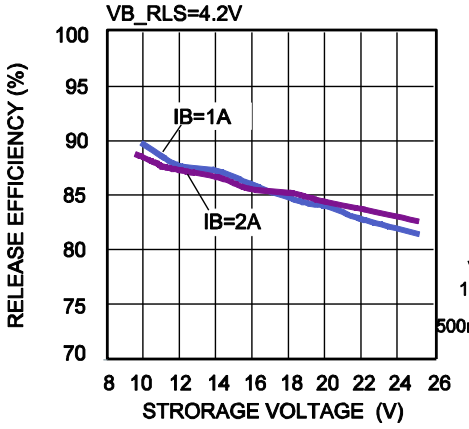



**Buck-Release Efficiency**

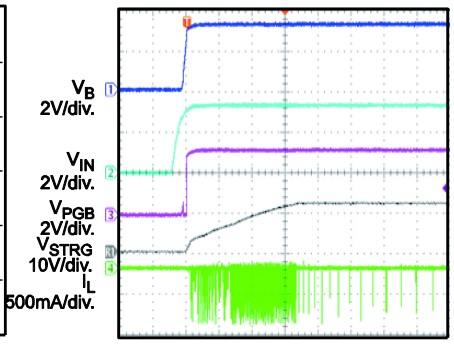



**Buck-Release Efficiency**

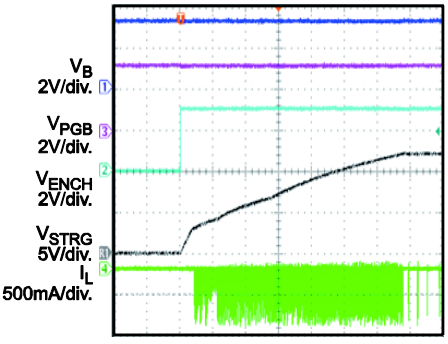
VB_RLS=4.2V




**$V_{IN}$ Power On**

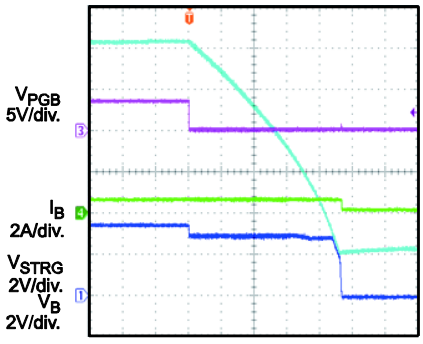



**ENCH Power On**



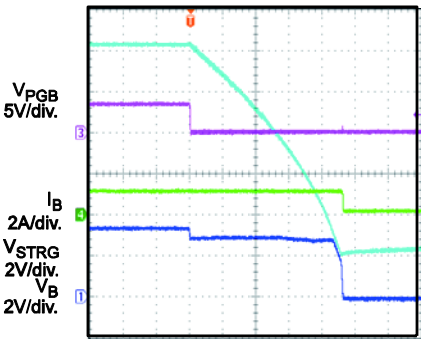

**VSTRG Release**

IB=0.5A, CSTRG=200μF



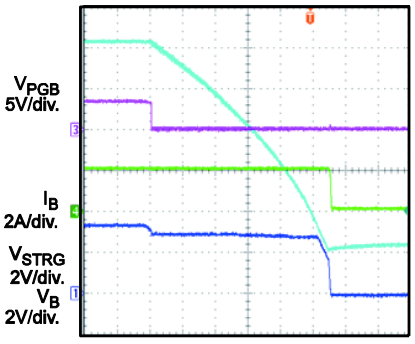

**VSTRG Release**

IB=1A, CSTRG=200μF




**VSTRG Release**

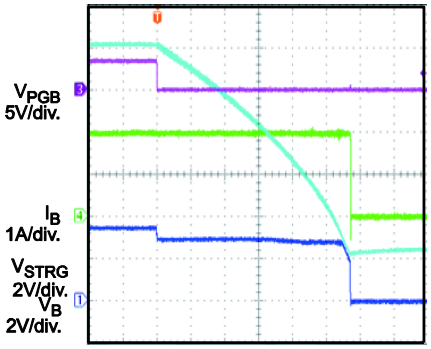
IB=2A, CSTRG=200μF



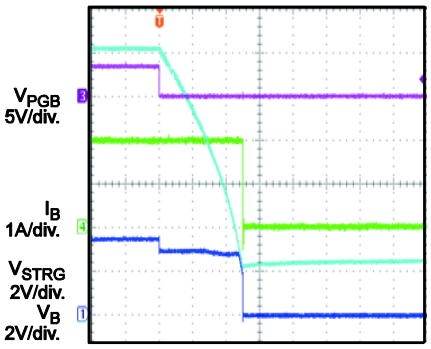
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**Performance waveforms are tested on the evaluation board of the Design Example section.**
**$V_{IN}$ = 3.3V, $V_{STRG}$ = 12V, $V_{RLS}$ = 2.9V, L = 1μH, $T_A$ = 25°C, unless otherwise noted.**

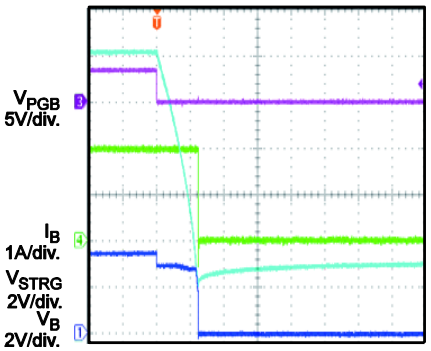
**VSTRG Release**
IB=2A, CSTRG=2200μF



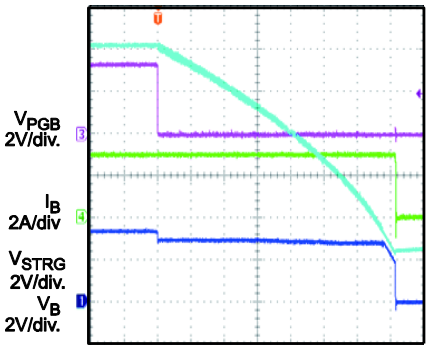

**VSTRG Release**
IB=2A, CSTRG=1000μF



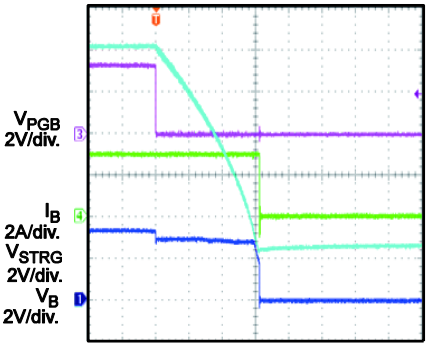

**VSTRG Release**
IB=2A, CSTRG=470μF



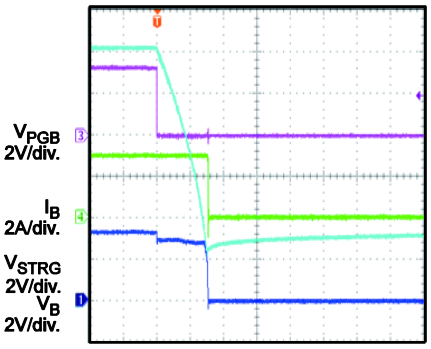

**VSTRG Release**
IB=3A, CSTRG=2200μF




**VSTRG Release**
IB=3A, CSTRG=1000μF




**VSTRG Release**
IB=3A, CSTRG=470μF



## PIN FUNCTIONS

| QFN-16 Pin # | Name | Description |
|---|---|---|
| 1 | DVDT | **VB voltage slew-rate control.** Connect a capacitor from DVDT to AGND to program the VB charge-up slew rate. Leave DVDT floating for the default soft-start time (around 0.8ms from 0V to 5V). |
| 2 | ILIM | **Input current limit setting.** Connect a resistor between ILIM and AGND to adjust the DC limit from VIN to VB. ILIM cannot be left floating. Pull ILIM higher than 1V to turn off the VIN-to-VB MOSFET. Do not pull ILIM up to a voltage source higher than the maximum of VIN and VB. |
| 3 | PGB | **VB power good indicator.** PGB is an open-drain output. PGB goes high if the FBB voltage exceeds $1.03xV_{FBB}$ (typically 0.813V). PGB goes low if the FBB voltage drops below $1.0xV_{FBB}$ (0.79V). |
| 4 | DISC | **On/off control for the VIN-to-VB isolation FET.** When DISC is pulled down, the VIN-to-VB isolation FET is turned off. When DISC is pulled high, the VIN-to-VB isolation FET is turned on. It is recommended to pull DISC up to VIN through a 100k resistor for automatic start-up. |
| 5 | ENCH | **On/off control for the charge/release circuitry.** When ENCH is pulled down, the charge/release circuitry is disabled. ENCH must be kept high to achieve energy release. |
| 6 | PGND | **Power ground.** |
| 7 | SW | **Switch output for the charge/release circuitry.** Connect a small inductor between SW and VBO. |
| 8 | STRG | **Storage voltage.** Connect the appropriate storage capacitors for energy storage and release operation. |
| 9 | BST | **Bootstrap for the charge/release circuitry.** The internal bidirectional switcher requires a bootstrap capacitor (typically 100nF) from BST to SW to supply high-side switch-driver voltage during release. |
| 10 | CST | **High-side switch driving voltage storage.** CST is charged by the storage power when the storage voltage is high and supports driver voltage when the storage voltage drops close to the VB regulated voltage. |
| 11 | AGND | **IC signal ground.** |
| 12 | FBB | **Bus voltage feedback sense.** FBB sets the bus release voltage. |
| 13 | FBS | **Storage voltage feedback sense.** FBS sets the storage voltage. |
| 14 | VBO | **Source of internal isolation FET.** Connect the inductor between SW and VBO for boost and buck operation. |
| 15 | VB | **Bus voltage.** A 22µF to 47µF ceramic capacitor is required as close to VB as possible. |
| 16 | VIN | **Input supply voltage.** The MP5507E operates from an unregulated 2.7V to 7V input. Place a ceramic capacitor 0.1µF or larger as close to VIN as possible. A TVS diode at the input is necessary if the VIN voltage spike is high. Refer to the Selecting the Input Capacitor and TVS section on page 14 for additional details. |

## BLOCK DIAGRAM

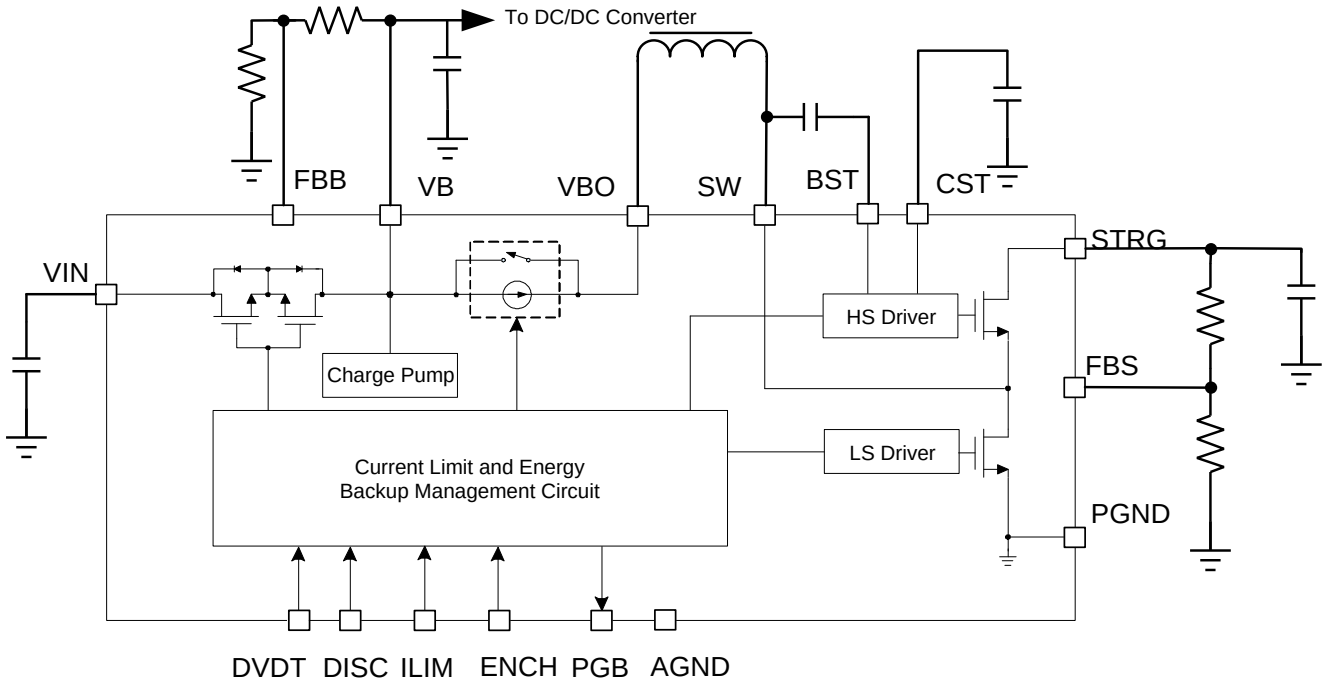



**Figure 1: Functional Block Diagram**

## OPERATION

The MP5507E is an energy storage and management unit in a QFN-16 (2.5mmx3.2mm) package. The MP5507E provides a very compact and efficient power backup solution for typical solid-state drive applications. MPS' patented lossless energy storage and release management circuits use a bidirectional buck/boost converter to achieve optimal energy transfer and provide a cost-effective energy storage solution.

The MP5507E's built-in boost converter charges the bulk storage capacitors to a programmed voltage when the system is powered up. If an input power outage occurs, the MP5507E indicates a VB bus power failure, disconnects the input switch, and transfers the energy from the storage capacitor to VB through the built-in buck converter, holding the bus voltage to a regulated voltage when the system consumes energy for data backup. The buck converter can work in 100% duty cycle operation to deplete the stored energy completely. Depending on different power backup times and storage components from different applications, the MP5507E can provide a compact solution with a programmable storage voltage setting.

### Start-Up

When VIN starts up, the VB bus voltage is charged from 0 to VIN. The VB rising slew rate is controlled by the DVDT capacitance. This function prevents input inrush current and provides protection to the downstream system.

EHCH is used to enable and disable the storage charge and release circuitry. The storage charge circuitry operate in two modes: pre-charge mode (the STRG voltage is charged to the VB voltage from 0V using a current source) and boost mode (the STRG voltage is charged to set the voltage). The pre-charge mode charges the STRG voltage up to the VB voltage using a near-constant current source (around 130mA). When the STRG voltage is close to VB, and the VB voltage is higher than a certain threshold (where PGB rises high), boost mode is initiated.

If ENCH is already high before VIN rises to the UVLO threshold, the storage charge circuitry starts a linear charge automatically when VIN is higher than the UVLO threshold (typically 2.5V), switches to boost switching mode when the storage voltage is charged close to VB, and PGB rises high. If ENCH rises high after VB, DVDT elapses and PGB has raised high, pre-charge begins, followed by boost switching.

Boost mode charges the STRG voltage to the target voltage. The charging build-up process when ENCH is high before VB starts up is shown in Figure 2.

It is strongly recommended to enable ENCH after VB has settled (see Figure 3). Because the release mode is triggered when the FBB voltage is lower than 0.79V (although there is a 23mV hysteresis between boost mode and release mode), the VB voltage may be pulled back low and accidently enter release mode. To prevent this, enable ENCH after VB settles if the system I/O can be used to control ENCH. The charging build-up process when ENCH is enabled after VB settles is shown in Figure 3.

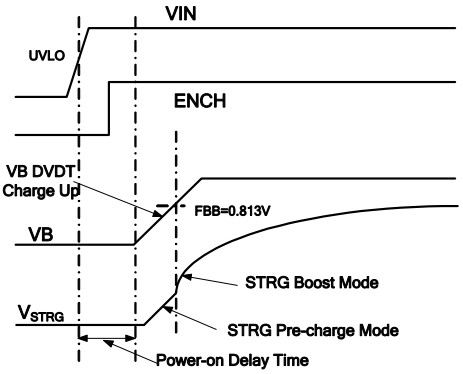



**Figure 2: Charging Process**

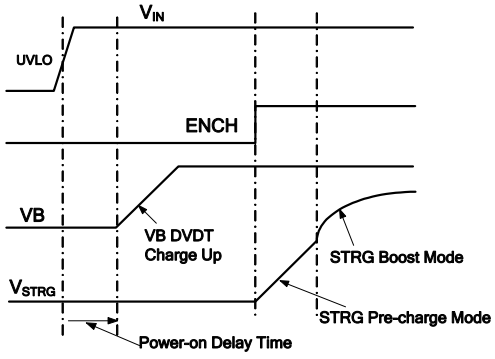



**Figure 3: Charging Process when ENCH is Enabled after VB Settles**

### Storage Voltage

After the storage voltage charges up, the internal boost converter regulates it to the regulated voltage automatically. The MP5507E uses burst mode to minimize the converter's power loss. When the storage voltage drops below the set voltage, burst mode is initiated and charges the storage capacitor. During the burst period, the current limit and the low-side MOSFET (LS-FET) control the switching. When the LS-FET turns on, then the inductor current increases until it reaches the current limit (about 500mA). After reaching the current limit, the LS-FET turns off for the set minimum off time. At the end of this minimum off time, if the feedback voltage remains below the 0.79V internal reference, the LS-FET turns on again. Otherwise, the MP5507E waits until the voltage drops below the threshold before turning on the LS-FET. During boost mode, the HS-FET is turned off, and the body diode of the HS-FET conducts the current.

### Release

The MP5507E monitors the input voltage and bus voltage continuously. Once the bus voltage drops below the release voltage (mostly due to the input voltage outage), the internal boost converter stops charging and works in buck-release mode. In buck mode, the part transfers energy from the high-voltage storage capacitor to the low-voltage bus capacitor. Determine the release voltage by selecting resistor values for the bus resistor divider.

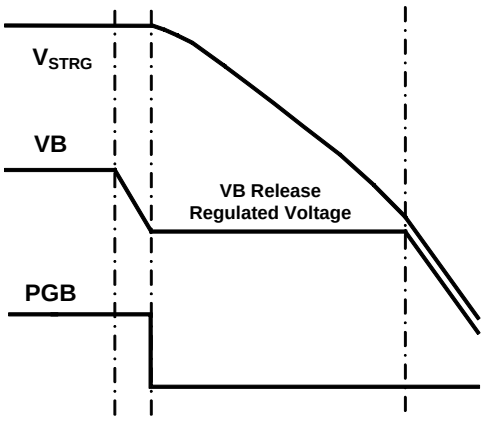



**Figure 4: Release Times**

The released buck applies the fixed-frequency constant-on-time (COT) control and enables a fast transition between the charge and release modes. The buck converter works at 100% duty cycle until the storage capacitor voltage approaches the bus voltage. Then the storage and VB voltages drop until they reach the DC/DC converter's UVLO threshold (see Figure 4).

### Input Current Limit Switch

The input current limit switch controls the input inrush current of the internal hot-swap MOSFET to prevent an inrush current from the input to the VB capacitor. A capacitor connected to DVDT sets the VB rising soft-start time. Despite the soft-start process, ILIM can limit the steady-state current. Connect a resistor between ILIM and GND to set the current limit.

### Reverse-Current Protection

The hot-swap circuit uses reverse-current protection to prevent the storage energy from transferring back to the input when energy is released from the storage capacitors to the bus. The hot-swap MOSFET turns on when the input voltage exceeds the VIN UVLO threshold during start-up or when the input voltage is about 0.2V higher than the VB voltage during VIN power recovery. The hot-swap MOSFET turns off when the input voltage falls below the VB voltage during release or when PGB drops.

### DVDT

Connect a capacitor across DVDT to program the soft-start time. Depending on the system inrush current requirement, different DVDT capacitors can be selected to program the inrush current during system start-up.

### VIN-to-VB Switch Off Control (DISC)

When DISC is pulled low, the VIN-to-VB MOSFET switches off directly. If ENCH is high, the MP5507E enters buck mode once VB drops to the VB regulation threshold (see Figure 5). The VIN-to-VB switch cannot turn on until DISC is high. Pull DISC up to VIN through a 100k resistor for automatic start-up.

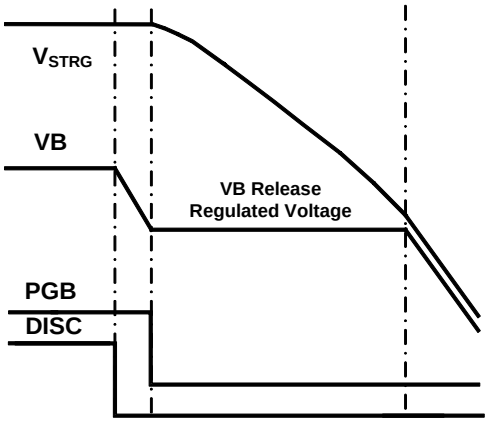



**Figure 5: DISC Off**

### Bus Power-Good Indicator (PGB)

When the voltage on FBB (bus feedback) falls below $1.0xV_{FBB}$, the MP5507E pulls PGB low to indicate the release status. When the FBB voltage rises above $1.03xV_{FBB}$, the MP5507E pulls PGB high to indicate the input power good status.

### Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from thermal damage. When the silicon die temperature is higher than its upper threshold, the entire chip shuts down. When the temperature is below its lower threshold, the chip turns on again if VIN power is available. However, if thermal shutdown occurs in buck mode without VIN power, the chip will not turn on again, even if STRG has a power supply.

# APPLICATION INFORMATION

### Selecting the Input Capacitor and TVS

Capacitors at VIN are recommended to absorb possible voltage spikes during input power turn-on, input switch hard-off (during power-off), or other special conditions. The application determines the capacitor. For example, if the input power trace is too long (with a higher parasitic inductance) during the input switch hard-off period, more energy is pumped into the input. This means that more input capacitors are needed to ensure that the input voltage spike remains in a safe range. Use a capacitor 0.1µF or larger based on the spike condition.

Consider inrush current requirements when selecting an input capacitor. Typically, more input capacitors result in a higher input inrush current during hot-plugging. A smaller input capacitor is needed for a smaller inrush current. The MP5507E works normally with a very small input capacitor. However, this leads to a possible high-voltage spike. An efficient solution is to add a TVS diode at the input to absorb the possible input-voltage spike. Simultaneously, keep the inrush current small during hot-plugging. A TVS diode such as the SMA6J5.0A is recommended.

### Setting the Storage Voltage

Set the storage voltage by choosing the external feedback resistors R3 and R4 (see Figure 6).

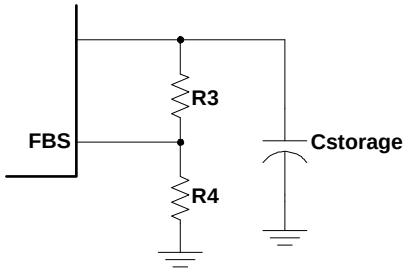



**Figure 6: Storage Feedback Circuit**

The storage voltage can be determined with Equation (1):

$$V_{STORAGE} = (1 + \frac{R3}{R4}) \times V_{FBS} \quad (1)$$

Where $V_{FBS}$ is 0.79V, typically.

R3 and R4 are not critical for normal operation. Select R3 and R4 to be higher than 10kΩ to account for the bleed current. For example, if R4 is 14kΩ, then R3 can be calculated with Equation (2):

$$R3 = \frac{14k\Omega \times (V_{STORAGE} - V_{FBS})}{V_{FBS}} \quad (2)$$

For a 12V storage voltage, R3 is 200kΩ.

Table 1 lists the recommended resistors for different storage voltages.

**Table 1: Resistor Pairs for $V_{STORAGE}$**

| $V_{STORAGE}$ (V) | R3 (kΩ) | R4 (kΩ) |
|---|---|---|
| 8 | 127 | 14 |
| 12 | 200 | 14 |
| 20 | 340 | 14 |

### Selecting the Release Voltage and $V_{BUS}$ Capacitors

Select the release voltage by choosing the external feedback resistors R1 and R2 (see Figure 7).

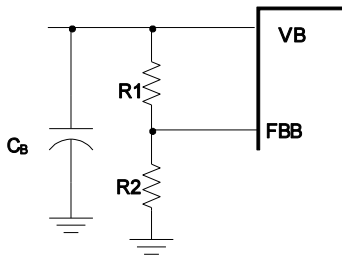



**Figure 7: Release Feedback Circuit**

The release voltage ($V_{RELEASE}$) can be calculated with Equation (3):

$$V_{RELEASE} = (1 + \frac{R1}{R2}) \times V_{FBB} \quad (3)$$

$V_{FBB}$ is 0.79V, typically. However, R1 and R2 not only determine the release voltage, but also affect loop stability. Choose R2 a with 2k to 10k resistor (4.02k is typically recommended) for the low-side divider resistor for stable performance with $C_B$ = 22µF. Table 2 lists the recommended resistor values for different release voltages.

**Table 2: Resistor Pairs for $V_{RELEASE}$**

| $V_{RELEASE}$ (V) | R1 (kΩ) | R2 (kΩ) |
|---|---|---|
| 4.2 | 17.4 | 4.02 |
| 2.9 | 10.7 | 4.02 |

### Selecting the Storage Capacitor

The storage capacitor stores energy during normal operation and releases it to VB when VIN loses input power. Use a general-purpose electrolytic capacitor or low-profile POS capacitor for most applications. One 4.7µF ceramic capacitor in parallel with the storage capacitor is recommended if the electrolytic capacitor ESR is high.

Select a storage capacitor with a voltage rating that exceeds the targeted storage voltage. Consider the capacitance reduction with the DC voltage offset when choosing the capacitor. Different capacitors have a different capacitance de-rating performance. Choose a capacitor with enough of a voltage rating to guarantee sufficient capacitance.

The required capacitance depends on the time of the dying gasp for a typical application. Assume the release current is $I_{RELEASE}$ when the VB voltage is regulated at $V_{RELEASE}$ for the DC/DC converter, the storage is $V_{STORAGE}$, and the required dying gasp time is $\tau_{DASP}$. The required storage capacitance can then be calculated with Equation (4):

$$C_S = \frac{2 \times V_{RELEASE} \times I_{RELEASE} \times \tau_{DASP}}{V_{STORAGE}^2 - V_{RELEASE}^2} \quad (4)$$

Consider the power loss during release. The buck converter efficiency is about 85% in most applications. Select storage capacitance at $1.18xC_S$ to ensure enough releasing time. If $I_{RELEASE}$ = 1A, $\tau_{DASP}$ = 20ms, $V_{STORAGE}$ = 12V, and $V_{RELEASE}$ = 4.2V, then the required storage capacitance is 1570µF.

For typical applications using a 5V input supply, set the storage voltage above 10V to fully utilize the high-voltage energy and minimize the storage capacitance requirements. Generally, 16V POS capacitors or 25V electrolytic capacitors are recommended.

### Selecting the External Diode

An external diode parallel with the high-side power MOSFET (HS-FET) is optional for normal charge-mode operation. This diode improves the boost efficiency slightly. The diode voltage rating should be higher than the storage voltage, and the current rating should be higher than the boost charge current.

### Setting the Input Hot-Swap Current Limit

Connect a resistor from ILIM to GND to set the current-limit value. For example, a 1.2kΩ resistor sets the current limit to about 4.1A. Table 3 lists the recommended resistors for different current limit values.

**Table 3: $I_{LIM}$ vs. $R_{LIM}$**

| $I_{LIM}$ (A) | $R_{LIM}$ (kΩ) |
|---|---|
| 4.6 | 1.07 |
| 4.1 | 1.2 |
| 3.6 | 1.4 |
| 1.6 | 3.2 |

### Selecting the Inductor

The inductor is necessary to supply constant current to the load. Since boost mode and buck mode share the same inductor, and generally the buck mode current is higher, an inductor that at least supports the buck mode releasing current is recommended.

Select the inductor based on the buck-release mode. If the storage voltage is $V_S$, then the release voltage is $V_R$, and the buck running is fixed at a 1.2MHz frequency. The inductance value can be calculated with Equation (5):

$$L = \frac{V_R}{\Delta I_L \times F_{SW}} \times (1 - \frac{V_R}{V_S}) \quad (5)$$

Where $\Delta I_L$ is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum inductor peak current.

### Setting the Bus Voltage Rise Time

Connect a capacitor to DVDT to set the bus voltage start-up slew rate and soft-start time. Leave DVDT floating for the default soft-start time (around 0.8ms from 0V to 5V). Table 4 lists the recommended capacitors for different soft-start times at a 5V input condition.

**Table 4: Soft-Start vs. Capacitor Value**

| $\tau_R$ (ms) | $C_{dv/dt}$ (nF) |
|---|---|
| 5.3 | 10 |
| 53 | 100 |

## PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. A 4-layer layout is recommended to achieve better thermal performance and simplify layout. For best results, refer to Figure 8 and Figure 9 and follow the guidelines below.

1) Use short, wide, and direct traces in the high-current paths (VIN, VB, VBO, SW, STRG, and PGND).
2) Place the decoupling capacitor as close to VB and PGND as possible.
3) Place the decoupling capacitor as close to STRG and PGND as possible.
4) Keep the switching node SW short and away from the feedback network.
5) Place the external feedback resistors as close to FB as possible.
6) Keep the BST voltage path (BST, C4, and SW) as short as possible.

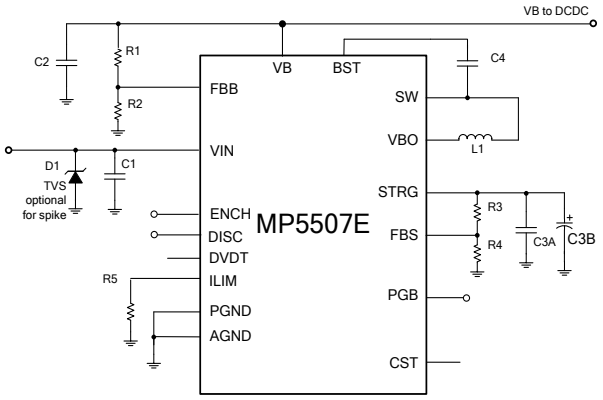
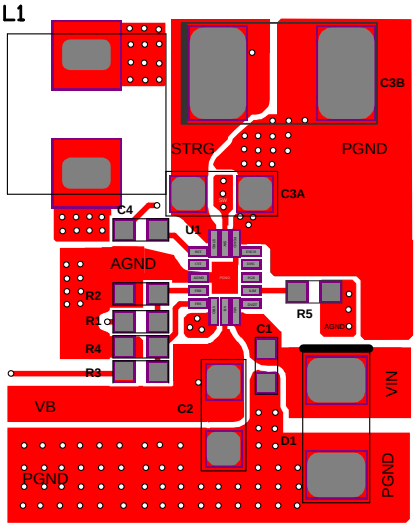
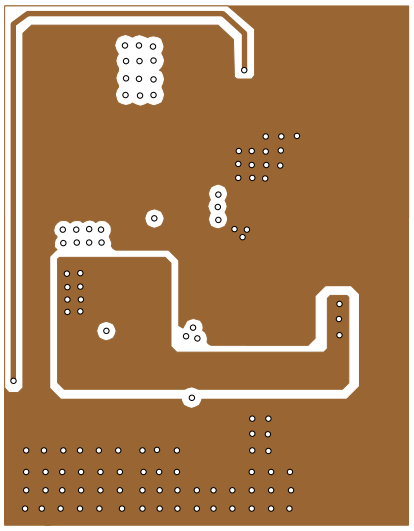


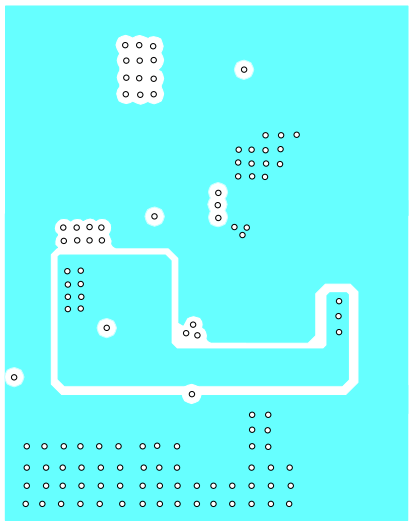

**Figure 8: Schematic for Layout**



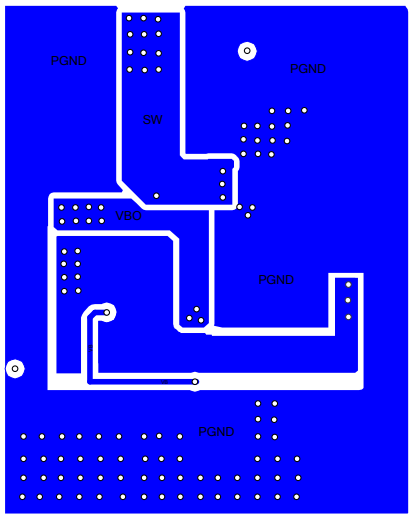

**Top Layer**



**Inner 1 Layer**



**Inner 2 Layer**




**Bottom Layer**

**Figure 9: Recommended Layout**

### Design Example

Table 5 is a design example following the application guidelines for the specifications below.

**Table 5: Design Example**

| Parameter | Symbol | Value | Units |
|---|---|---|---|
| Input voltage | $V_{IN}$ | 3.3 | V |
| Storage voltage | $V_{STRG}$ | 12 | V |
| Bus backup voltage | $V_{RLS}$ | 2.9 | V |
| Bus backup max load | $I_{RELEASE}$ | 3 | A |

The detailed application schematic is shown in Figure 10. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section. For more device applications, please refer to the related evaluation board datasheet.

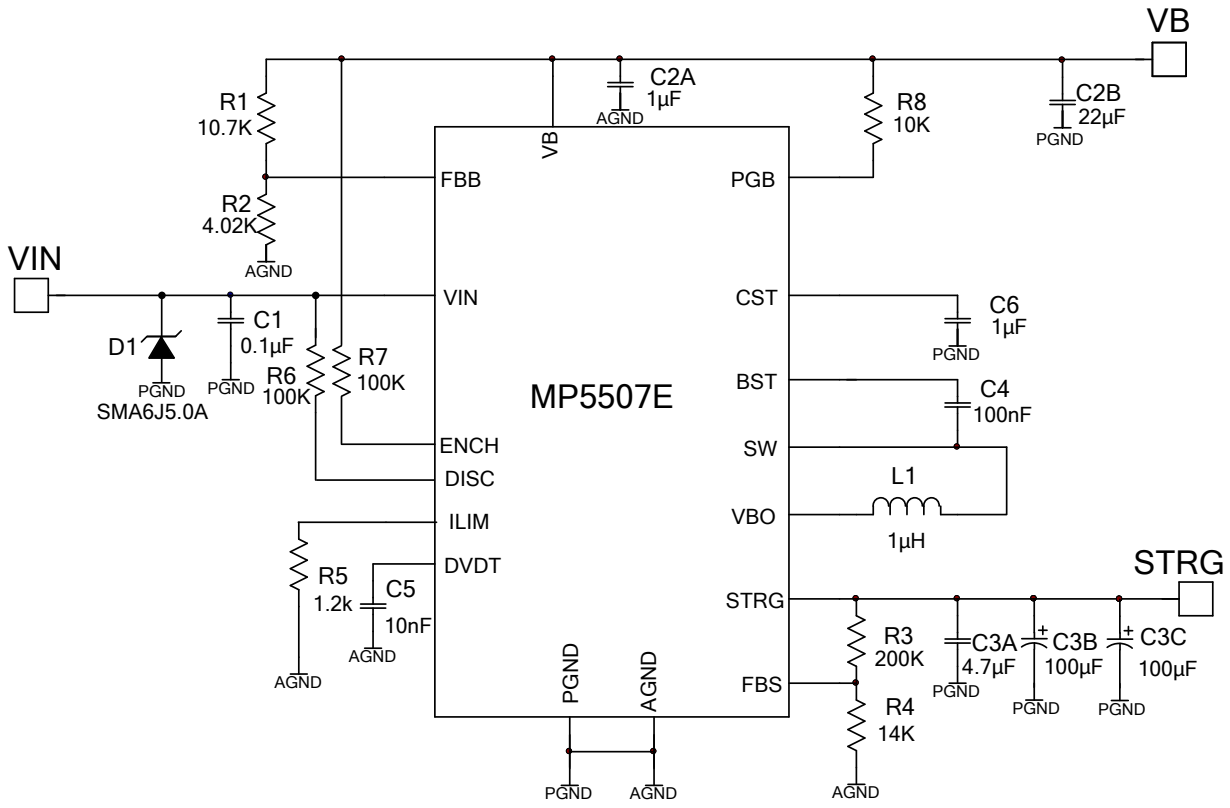
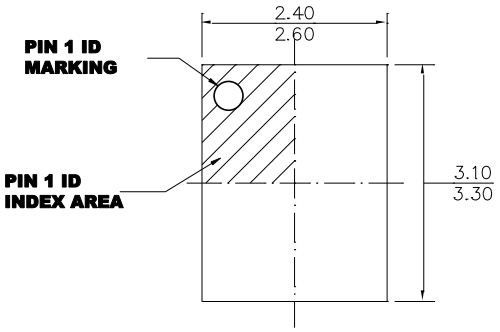


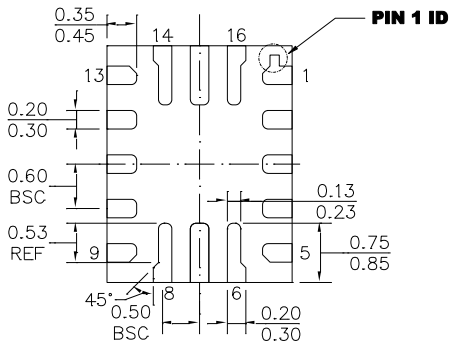

**Figure 10: Detailed Application Schematic**

# PACKAGE INFORMATION

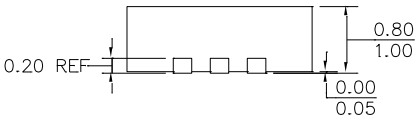
## QFN-16 (2.5mmx3.2mm)



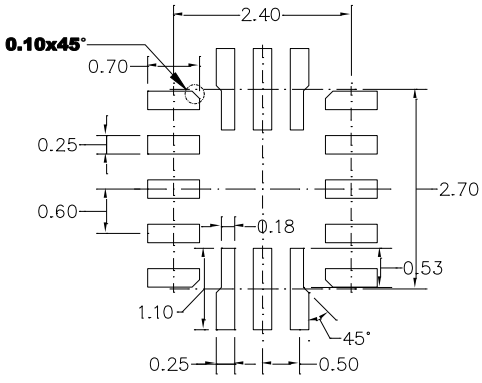

**TOP VIEW**




**BOTTOM VIEW**




**SIDE VIEW**




**RECOMMENDED LAND PATTERN**

**NOTE:**

**1) ALL DIMENSIONS ARE IN MILLIMETERS.**
**2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.**
**3) JEDEC REFERENCE IS MO-220.**
**4) DRAWING IS NOT TO SCALE.**