MP5505E

7V, 4A, High-Efficiency, Energy Storage and Management Unit

DESCRIPTION

The MP5505E is a lossless energy storage and management unit targeted toward solid-state and hard-disk drive applications. The highly integrated input current limit and energy storage-and-release management make the system solution very compact.

The internal input current limit block with dV/dt control prevents inrush current during system start-up. The bus voltage start-up slew rate is programmable, and a power-on reset function is included for hot-swapping. MPS's patented energy storage-and-release management control circuit minimizes the storage capacitor requirement. It pumps the input voltage to a higher storage voltage and releases the energy over a hold-up time to the system in the case of an input outage. The storage voltage and the release voltage are both programmable for different system applications.

The MP5505E requires a minimal number of readily available, standard, external components and is available in a QFN-20 (3mmx4mm) package.

FEATURES

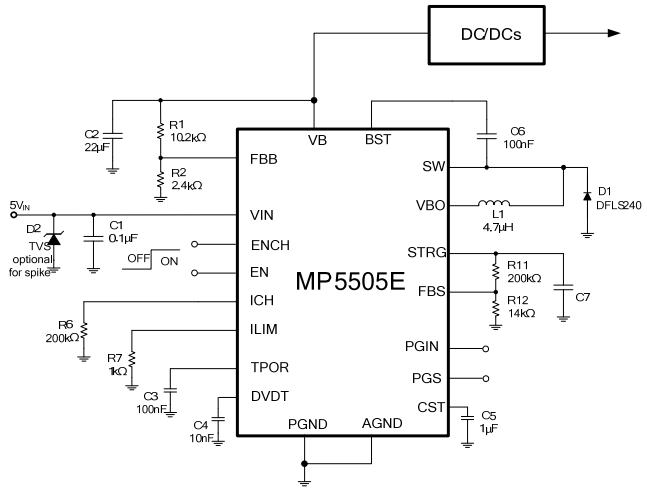
- Wide 2.7V to 7V Operating Input Range
- Input Current Limiter with Integrated 60mΩ MOSFET
- Up to 4.5A Input Current Limit
- Reverse-Current Protection
- 6V Bus Clamping Voltage
- Power-On Reset
- Adjustable dV/dt Slew Rate for Bus Voltage Start-Up
- Internal 30mΩ Disconnect Switch
- Internal 70mΩ and 60mΩ Power Switches for Energy Storage and Release Management Circuits
- Thermal Protection
- EN and Power Good Indicators
- Available in a QFN-20 (3mmx4mm) Package

APPLICATIONS

- Solid-State Drives (SSD)
- Hard-Disk Drives
- Power Back-Up/Battery Hold-Up Supplies

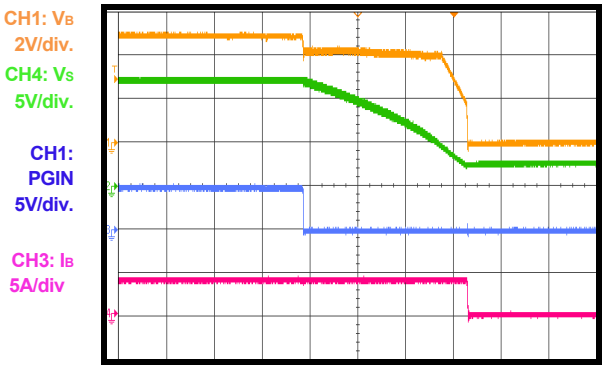
All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. "MPS", the MPS logo, and "Simple, Easy Solutions" are trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

TYPICAL APPLICATION



Release

I_B = 4A, C_{STRG} = 1000µF



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking
MP5505EGL	QFN-20 (3mmx4mm)	*See Below*

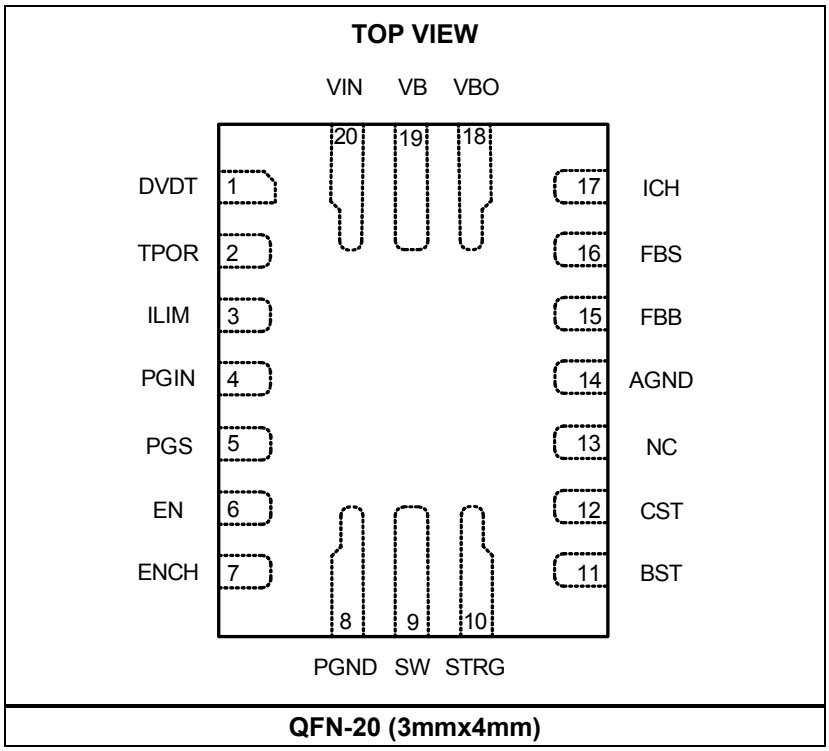
* For Tape & Reel, add suffix –Z (e.g.: MP5505EGL–Z).

TOP MARKING

MPYW
5505
ELLL

MP: MPS prefix
Y: Year code
W: Week code
5505E: First five digits of the part number
LLL: Lot number

PACKAGE REFERENCE



QFN-20 (3mmx4mm)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

PIN FUNCTIONS

QFN-20 (3mm×4mm) Pin #	Name	Description
1	DVDT	**Slew-rate control pin for VB voltage during start-up.** Connect a capacitor from DVDT to GND to program a different VB charge-up slew rate. Leave DVDT open for the default soft-start time (around 0.9ms from 0V to VIN).
2	TPOR	**Power-on reset delay time for VB start-up.** When VIN and EN are ready (after the programmable delay time), VB starts to charge up. Connect a capacitor between TPOR and GND to select a different delay time. Leave TPOR open for the default power-on reset delay time (0.4ms).
3	ILIM	**Input current limit setting.** Connect a resistor between ILIM and GND to adjust the current limit of the input current limiter. ILIM *cannot* be left open.
4	PGIN	**VB power good indicator.** PG_{IN} is an open-drain output. PG_{IN} goes high if the FBB voltage exceeds 1.03 x V_{FBB} (typically 0.825V). PG_{IN} goes low if the FBB voltage drops below 1.0 x V_{FBB} (0.801V).
5	PGS	**Storage voltage power good indicator.** PGS is an open-drain output. PGS goes high if the FBS voltage exceeds 0.95 x V_{FBS} (0.755V). PGS goes low if the FBS voltage drops below 0.9 x V_{FBS} (0.715V).
6	EN	**On/off control for the MP5505E.** When EN is pulled low, all functions of the MP5505E are disabled (for both the input current limiter and the charge/release circuitry). Ensure that the EN voltage is high during the release.
7	ENCH	**On/off control for the charge/release circuitry.** When ENCH is pulled down, the release circuitry is disabled. Note that ENCH must be kept high to achieve energy release.
8	PGND	**Power ground.**
9	SW	**Switch output for the charge/release circuitry.** Connect a small inductor between SW and VBO.
10	STRG	**Storage voltage.** Connect appropriate storage capacitors for the energy storage and release operation.
11	BST	**Bootstrap for the charge/release circuitry.** The internal bidirectional switcher requires a bootstrap capacitor (100nF) from BST to SW to supply the high-side switch driver voltage during release.
12	CST	**High-side switch driving voltage storage.** The MP5505E supports energy when the storage voltage is close to the VB regulated voltage.
13	NC	**No connection.**
14	AGND	**IC signal ground.**
15	FBB	**Bus voltage feedback sense.** FBB sets the bus-release voltage.
16	FBS	**Storage voltage feedback sense.** FBS sets the storage voltage.
17	ICH	**Boost mode current limit adjustment.** ICH *cannot* be pulled to VCC or an external voltage source. Connect a 68 - 200kΩ resistor from ICH to GND.
18	VBO	**Internal Boost.** VBO is the input voltage after passing through the input isolation MOSFET.
19	VB	**Internal bus voltage.** Place a 22 - 47μF ceramic capacitor as close to VB as possible.
20	VIN	**Input supply voltage.** The MP5505E operates from an unregulated 2.7 - 7V input. Place a 0.1μF (or larger) ceramic capacitor as close to VIN as possible. A TVS diode at the input is necessary if the VIN spike is high. Refer to the Selecting the Input Capacitor and TVS section on page 13 for additional details.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 8.0V
V_{STRG} ..... -0.3V to 35V
V_{SW} ..... -0.3V to V_{STRG} + 0.3V
V_{BST} ..... -0.3V to V_{STRG} + 6.5V
V_{CST} ..... -0.3V to 40V
All other pins ..... -0.3V to 6.5V
Continuous power dissipation (T_A = +25°C) (2) 2.6W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Operating temperature ..... -40°C to +85°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 2.7V to 7V
Bus voltage (V_B) ..... 2.7V to 6V
Storage voltage (V_{STRG}) ..... V_{IN} to 30V
Operating junction temp. (T_J) .... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

	θ_{JA}	θ_{JC}	
QFN-20 (3mmx4mm)	48	10	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, T_J = -40°C to +125°C, typical value is tested at T_J = +25°C. The limit over temperature is guaranteed by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input supply voltage range	V_{IN}		2.7		7	V
Supply current (shutdown)	I_S	V_{EN} = 0V, T_J = 25°C			2	μA
Supply current (quiescent)	I_Q	$V_{EN/ENCH}$ = 2V, $V_{FBB/FBS}$ = 1V			2	mA
Thermal shutdown (5)	T_{SD}			150		°C
Thermal shutdown hysteresis (5)	T_{HYS}			30		°C
VIN under-voltage lockout threshold rising	$INUV_R$			2.4	2.7	V
VIN under-voltage lockout threshold hysteresis	$INUV_{HYS}$			0.38		V
EN/ENCH UVLO threshold rising	EN_R				1.2	V
EN/ENCH UVLO threshold falling	EN_F		0.4			V
Current-limit MOSFET on resistance	R_{DSON}	T_J = 25°C		60	65	mΩ
Input current limit	ILIM	R_{ILIM} = 1.4kΩ	3.1	3.6	4.1	A
Off-state leakage current	I_{LEAK}	V_{IN} = 6V, V_B = 0V or V_B = 6V, V_{IN} = 0V, T_J = 25°C			2	μA
Clamping voltage	V_{CLAMP}	V_{IN} = 7V	5.5	6	6.5	V
Rise time (dV/dt)	τ_R	DVDT pin floating	0.5	0.9	1.5	ms
		$C_{dv/dt}$ = 10nF		10		
		$C_{dv/dt}$ = 100nF		100		
Internal reset delay time	τ_D	TPOR pin floating		0.4		ms
		C_{TPOR} = 100nF		100		
		C_{TPOR} = 500nF		500		
Pre-charge current	I_{CH_PRE}			130		mA
Charge peak current @ boost mode	I_{CH}	R_{ICH} = 100kΩ, V_{IN} = 5V, L = 4.7μH	300	540	800	mA
Boost disconnect switch R_{on}	R_{dison}	Vs =10V, T_J = 25°C		30	35	mΩ
Energy management HS R_{on}	R_{Hon}			70		mΩ
energy management LS R_{on}	R_{Lon}			60		mΩ
Feedback voltage	V_{FBB}		0.789	0.801	0.813	V
	V_{FBS}		0.783	0.795	0.807	
Feedback current	I_{FBB}	V_{FBB} = 0.801V			50	nA
	I_{FBS}	V_{FBS} = 0.795V			50	nA

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_J = -40°C to +125°C, typical value is tested at T_J = +25°C. The limit over temperature is guaranteed by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
PGS high threshold	PG_{H_S}			0.95		V_{FBS}
PGS low threshold	PG_{L_S}			0.9		V_{FBS}
PGS delay	PG_{D_S}			20		µs
PGS sink-current capability	V_{PG_S}	Sink 4mA			0.4	V
PGS leakage current	I_{PGS_L}	V_{PGS} = 3.3V			120	nA
PGIN high threshold	PG_{H_IN}			1.03		V_{FBB}
PGIN low threshold	PG_{L_IN}			1		V_{FBB}
PGIN delay	PG_{D_IN}			0.5		µs
PGIN sink-current capability	V_{PG_IN}	Sink 4mA			0.4	V
PGIN leakage current	I_{PGIN_L}	V_{PGIN} = 3.3V			120	nA
Buck-mode dumping current limit	I_{DUMP}		4.4	6	7.5	A
Release-buck switching frequency	f_{s_RLS}			500		kHz
VB under-voltage lockout threshold rising (6)	$INUVB_R$		1.8	2.2	2.5	V
VB under-voltage lockout threshold hysteresis (6)	$INUVB_{HYS}$		0.1	0.25	0.4	V

NOTES:

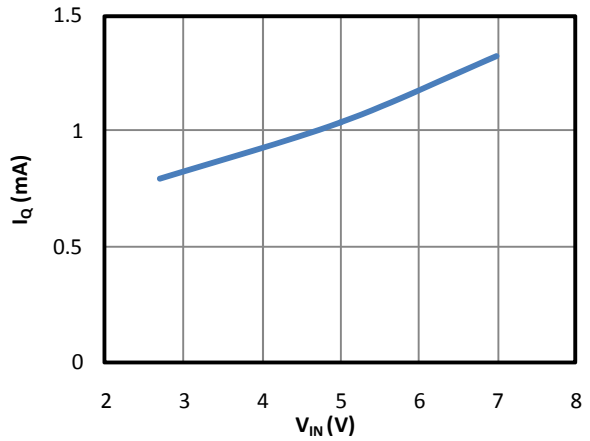
5) Guaranteed by characterization, not tested in production.
6) VB UVLO is applied to energy storage-and-release circuitry.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

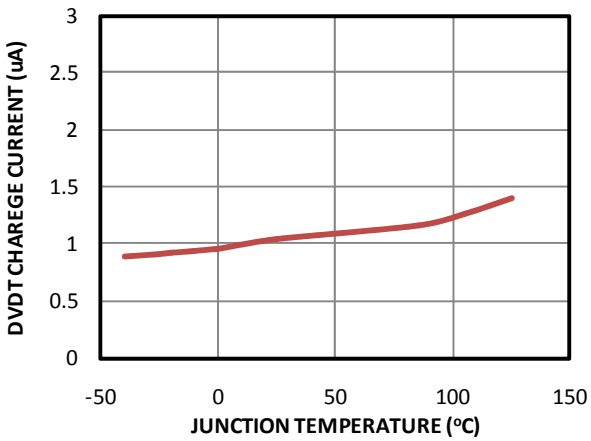
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, $V_{STORAGE}$ = 12V, $V_{RELEASE}$ = 4.2V, L = 4.7µH, T_A = 25°C, unless otherwise noted.

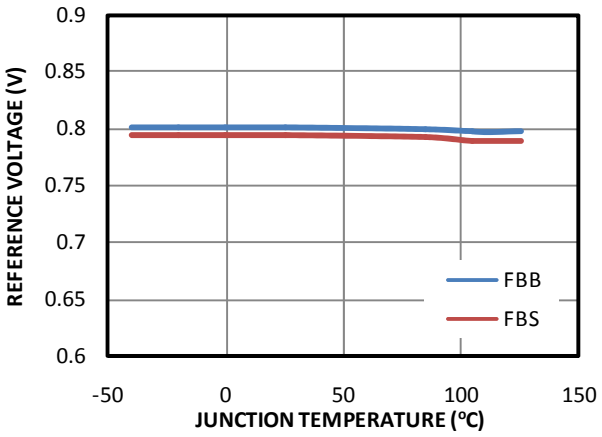
Quiescent Current vs. Input Voltage



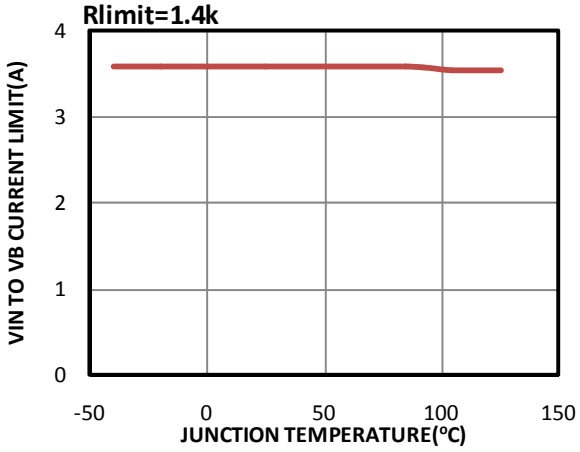
DVDT Charge Current vs. Temperature



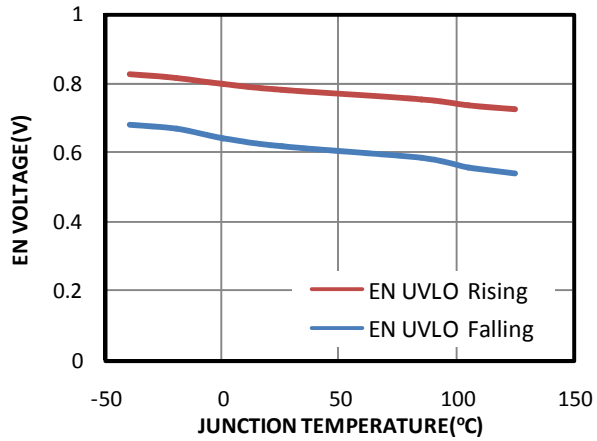
Reference Voltage vs. Temperature



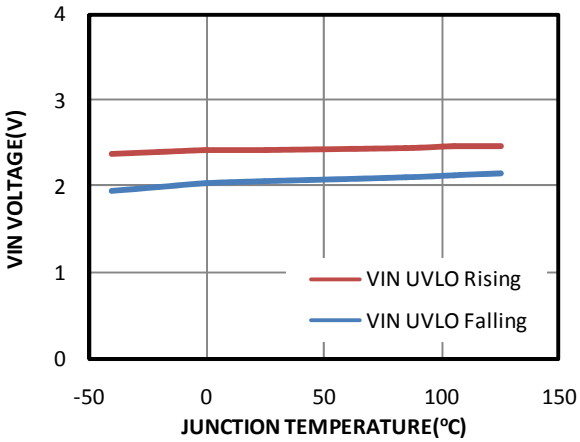
V_{IN} to VB Current Limit vs.Temperature Rlimit=1.4k



EN UVLO vs. Temperature



V_{IN} UVLO vs. Temperature

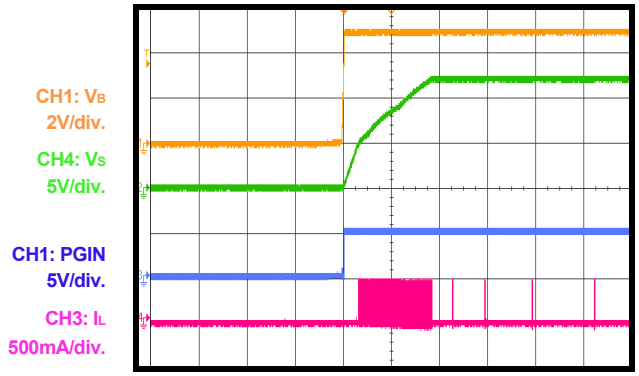


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

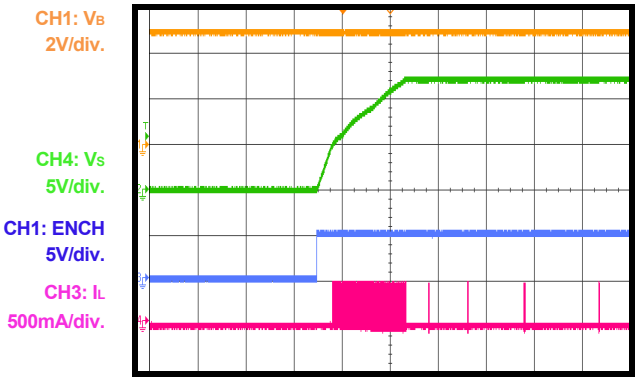
Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 5V, $V_{STORAGE}$ = 12V, $V_{RELEASE}$ = 4.2V, L = 4.7µH, T_A = 25°C, unless otherwise noted.

V_{IN} On



200ms/div.

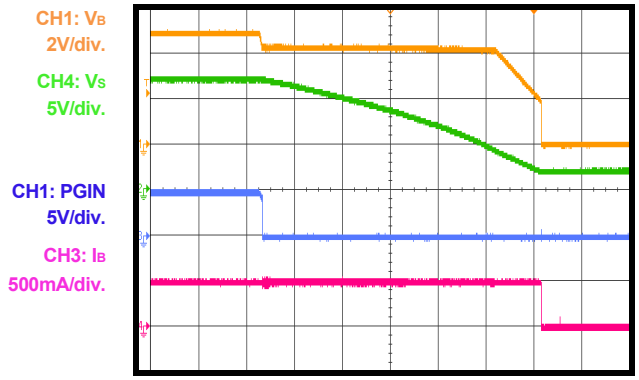
ENCH On



200ms/div.

Release

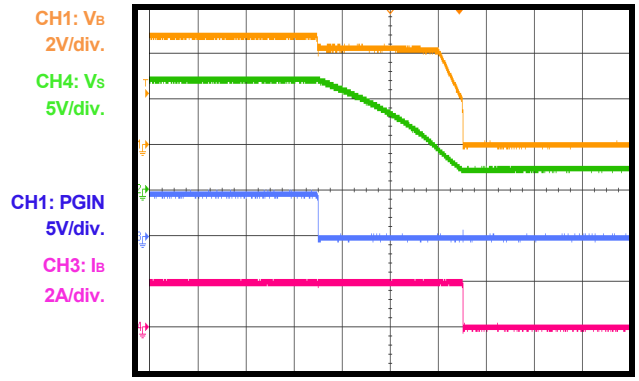
I_B = 0.5A, C_{STRG} = 2x1000µF



10ms/div.

Release

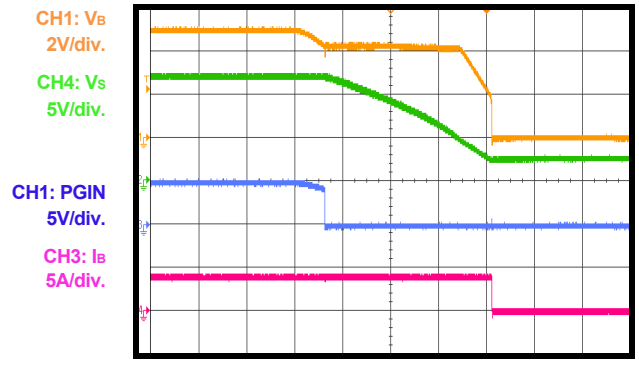
I_B = 2A, C_{STRG} = 2x1000µF



5ms/div.

Release

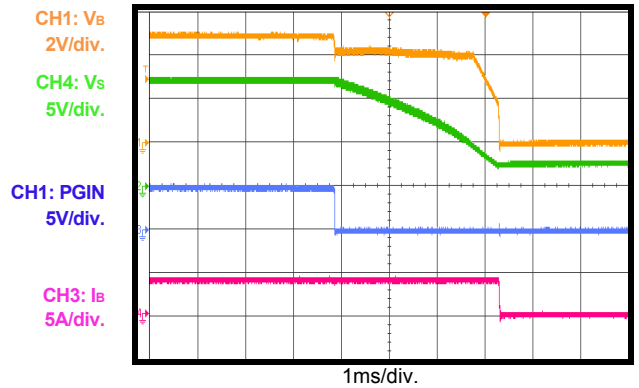
I_B = 4A, C_{STRG} = 2x1000µF



2ms/div.

Release

I_B = 4A, C_{STRG} = 1000µF



1ms/div.

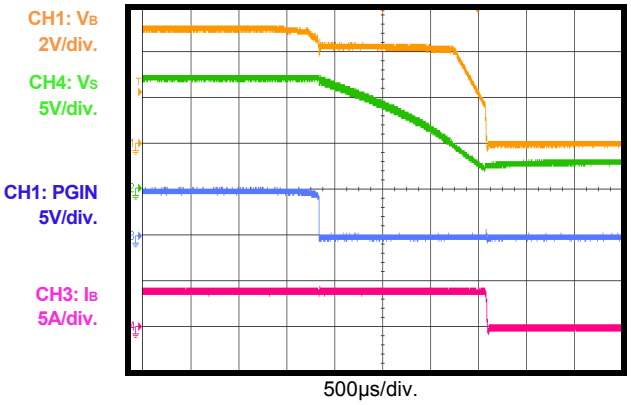
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 5V, $V_{STORAGE}$ = 12V, $V_{RELEASE}$ = 4.2V, L = 4.7µH, T_A = 25°C, unless otherwise noted.

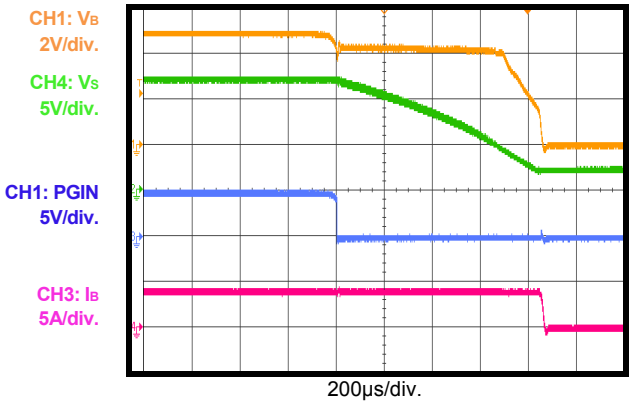
Release

I_B = 4A, C_{STRG} = 470µF



Release

I_B = 4A, C_{STRG} = 220µF



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

BLOCK DIAGRAM

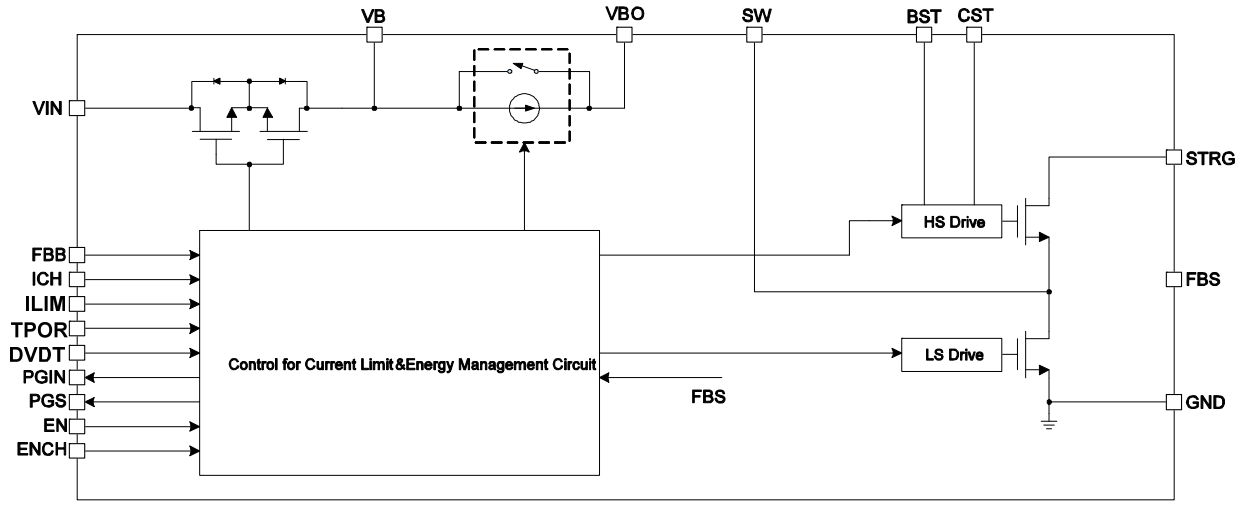


Figure 1: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

OPERATION

The MP5505E is an energy storage and management unit in a QFN-20 (3mmx4mm) package. The MP5505E provides a very compact and efficient energy management solution for typical solid-state drive or hard-disk drive applications. MPS's patented lossless energy storage-and-release management circuits use a bidirectional buck/boost converter to achieve optimal energy transfer and provide the most cost-effective energy storage solution.

The integrated boost converter raises the energy storage voltage level. The storage feedback resistor divider sets the storage voltage. If the input shuts down suddenly, the internal buck converter transfers the energy from the storage capacitor to the bus and holds the bus voltage when the system consumes the energy from the storage capacitor. The buck converter can work in 100% duty cycle operation to deplete the stored energy completely.

Start-Up

When VIN starts up, the VB bus voltage is charged from 0 almost to VIN. The VB rising slew rate is controlled by the DVDT capacitance. This function prevents input inrush current and provides protection to the entire system.

EHCH is used to enable the storage charge and release circuitry. If ENCH is already high before VB finishes the DVDT process, the storage charge circuitry works automatically when VIN is higher than the UVLO (typically 2.4V).

The storage charge circuitry operates in two modes: pre-charge mode (where the STRG voltage is charged to the VB voltage using a current source) and boost mode (where the STRG voltage is charged to set the voltage). Pre-charge mode charges the STRG voltage up to the VB voltage using a nearly constant current source (around 130mA). When the STRG voltage is close to VB, and the VB voltage is higher than a certain threshold (where the corresponding FBB is higher than 0.825V), boost mode is initiated.

Boost mode charges the STRG voltage to the target voltage. Figure 2 shows the charging build-up process when ENCH is high before VB starts up.

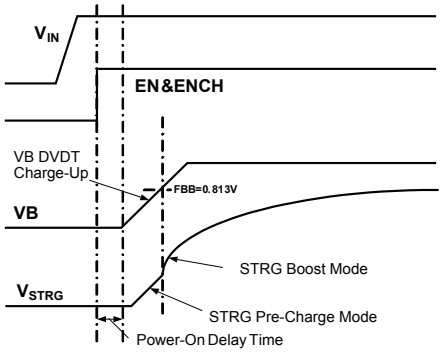


Figure 2: Charging Process

It is strongly recommended to enable ENCH after VB has settled (see Figure 3). Because release mode is triggered when the FBB voltage is lower than 0.79V, if ENCH is enabled before VB has settled, the VB and FBB voltage may be pulled below 0.79V when boost-charge starts working. This makes the MP5505E enter release mode accidently since there is a 23mV hysteresis between boost mode and release mode. To avoid this, enable ENCH after VB settles. Figure 3 shows the charging build-up process when ENCH is enabled after VB settles.

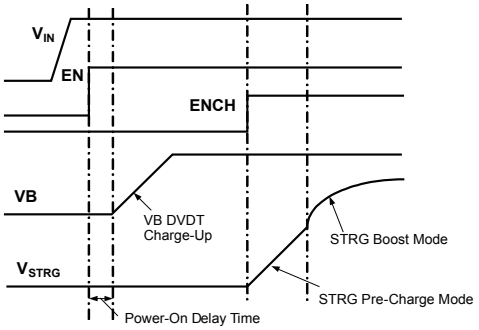


Figure 3: Charging Process when EN and ENCH are Separated

Storage Voltage

After the start-up period, the internal boost converter regulates the storage voltage automatically to a set value. The MP5505E uses burst mode to minimize the converter's power loss. When the storage voltage drops below the set voltage, burst mode initiates and charges the storage capacitor. During the burst period, the current limit and the low-side

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

MOSFET (LS-FET) control the switch. When the LS-FET turns on, the inductor current increases until it reaches its current limit. The boost current limit can be programmed by a 68 - 200kΩ ICH resistor. After reaching the current limit, the LS-FET turns off for the set minimum off time. At the end of this minimum off time, if the feedback voltage remains below the 0.795V internal reference, the LS-FET turns on again. Otherwise, the MP5505E waits until the voltage drops below the threshold before turning on the LS-FET.

Release

The MP5505E monitors the input and bus voltages continuously. Once the bus voltage drops below the selected release voltage (such as when losing input power), the internal boost converter stops charging and works in buck-release mode. In buck mode, the part transfers energy from the high-voltage storage capacitor to the low-voltage bus capacitor. Determine the release voltage by selecting resistor values for the bus resistor divider.

The released buck applies a fixed-frequency constant-on-time (COT) control and enables a fast transition between the charge and release modes. The buck converter works at 100% duty cycle until the storage capacitor voltage approaches the bus voltage. Then the storage and bus voltages drop until they reach the DC/DC converter's UVLO (see Figure 4).

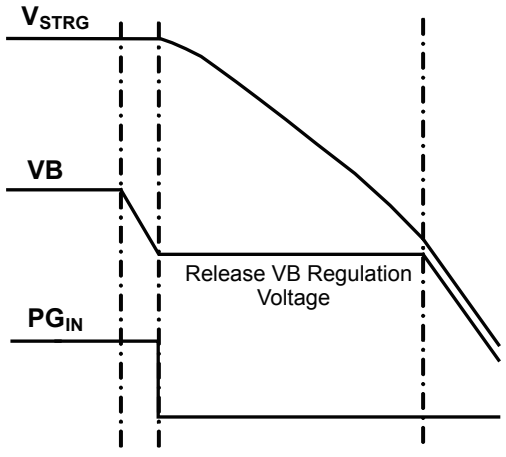


Figure 4: Release Times

During the buck release mode, if the load is too high and the buck switching peak current limit is triggered, the MP5505E prolongs the HS-FET off period. This way, the inductor current can ramp down in each cycle and prevent a switching current runaway.

Input Current Limit

The input current limiter controls the input inrush current of the internal hot-swap MOSFET carefully to prevent inrush current from the input to the bus. A capacitor connected to dV/dt sets the soft-start time. Despite the soft-start process, ILIM can limit the steady-state current. Connect a resistor between ILIM and GND to set the current limit.

Reverse-Current Protection

The hot-swapping circuit uses reverse-current protection to prevent the storage energy from transferring back to the input when the energy is released from the storage capacitors to the bus. The hot-swap MOSFET turns on when the input voltage exceeds the VIN UVLO threshold during start-up (or when the input voltage is about 0.2V higher than the VB voltage). The hot-swap MOSFET turns off when the input voltage falls below the bus voltage during release (or the input falls below the PGIN threshold).

Start-Up Sequencing

Connect a capacitor across DVDT to program the soft-start time. The energy storage capacitors charge during the soft start. Very short dV/dt times can trigger the current-limit threshold. Select a DVDT capacitor based on the storage capacity.

Storage Power-Good Indicator (PGS)

When the voltage on the storage feedback (FBS) drops below 0.9 x V_{FBS}, the MP5505E pulls PGS low internally. When the FBS voltage is above 0.95 x V_{FBS}, PGS goes high.

Bus Power-Good Indicator (PGIN)

When the voltage on the bus feedback (FBB) falls below 1.0 x V_{FBB}, the MP5505E pulls PGIN low to indicate the release status. When the MP5505E works in boost mode, PGIN is pulled high to indicate the charging status.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

APPLICATION INFORMATION

Selecting the Input Capacitor and TVS

Capacitors at VIN are recommended to absorb possible voltage spikes during input power turn-on, input switch hard-off (during power-off), or other special conditions. The application determines the capacitor. For example, if the input power trace is too long (with a higher parasitic inductance) during the input switch hard-off period, more energy pumps into the input. This means more input capacitors are needed to ensure that the input voltage spike remains in a safe range. Use a 0.1μF (or larger) capacitor based on the spike condition.

Consider the inrush current requirements when selecting an input capacitor. Typically, more input capacitors result in a higher input inrush current during hot-plugging. A smaller input capacitor is needed for a smaller inrush current. The MP5505E works normally with a very small input capacitor. However, this leads to a possible high-voltage spike. An efficient solution is to add a TVS diode at the input to absorb the possible input voltage spike. At the same time, keep the inrush current small during hot-plugging. A typical TVS diode is recommended (e.g.: SMA6J5.0A).

Setting the Storage Voltage

Set the storage voltage by choosing the external feedback resistors R11 and R12 shown in Figure 5.

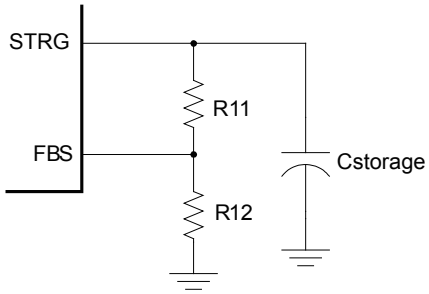


Figure 5. Storage Feedback Circuit

The storage voltage can be determined with Equation (1):

$$V_{STORAGE} = (1 + \frac{R11}{R12}) \times V_{FBS} \quad (1)$$

Where V_{FBS} is 0.795V, typically.
R11 and R12 are not critical for normal operation. R11 and R12 should be higher than 10kΩ to account for the bleed current. For example, if R12 is 14kΩ, R11 is then determined with Equation (2):

$$R11 = \frac{14k\Omega \times (V_{STORAGE} - V_{FBS})}{V_{FBS}} \quad (2)$$

For a 12V storage voltage, R11 is 196kΩ.

Table 1 lists the recommended resistor values for different storage voltages.

Table 1: Resistor Pairs for $V_{STORAGE}$

$V_{STORAGE}$(V)	R11 (kΩ)	R12 (kΩ)
8	127	14
12	196	14
20	340	14

Selecting Release Voltage and VBus Capacitors

Select the release voltage by choosing the external feedback resistors R1 and R2 as shown in Figure 6.

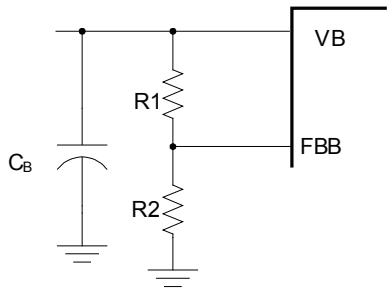


Figure 6: Release Feedback Circuit

Similarly, the release voltage can be calculated with Equation (3):

$$V_{RELEASE} = (1 + \frac{R1}{R2}) \times V_{FBB} \quad (3)$$

Where V_{FBB} is 0.801V, typically. R2 should be lower than 5kΩ (2.4kΩ is recommended). Table 2 lists the recommended resistor values for different release voltages.

Table 2: Resistor Pairs for $V_{RELEASE}$

$V_{RELEASE}$ (V)	R1 (kΩ)	R2 (kΩ)
4.2	10.2	2.4
2.9	10.5	4.02

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

Selecting the Storage Capacitor

The storage capacitor stores energy during normal operation and releases this energy to VB when VIN loses input power. Use a general-purpose electrolytic capacitor or low-profile POS capacitor for most applications. One 4.7µF ceramic capacitor is recommended if the electrolytic capacitor ESR is high.

Select a storage capacitor with a voltage rating that exceeds the targeted storage voltage. Consider the capacitance reduction with the DC voltage offset when choosing the capacitors. Different capacitors have different capacitance de-rating performances. Choose a capacitor with enough voltage rating to guarantee sufficient capacitance.

The required capacitance depends on the length of the dying gasp for a typical application. Assume the release current is $I_{RELEASE}$ (when the VB voltage is regulated at $V_{RELEASE}$ for the DC/DC converter), the storage is $V_{STORAGE}$, and the required dying gasp time is τ_{DASP}. The required storage capacitance can then be calculated with Equation (4):

$$C_S = \frac{2 \times V_{RELEASE} \times I_{RELEASE} \times \tau_{DASP}}{V_{STORAGE}^2 - V_{RELEASE}^2} \quad (4)$$

Considering the power loss during release, the buck converter can run up to 90% efficiency in most applications. Select the storage capacitance at 1.1xCs to ensure enough release time. If $I_{RELEASE}$ = 1A, τ_{DASP} = 20ms, $V_{STORAGE}$ = 12V, and $V_{RELEASE}$ = 4.2V, then the required storage capacitance is 1500µF.

For typical applications using a 5V input supply, set the storage voltage above 10V to fully utilize the high-voltage energy and minimize the storage capacitance requirements. Generally, use a 16V POS capacitor or 25V electrolytic capacitor.

Selecting the External Diode

For release mode, there must be one Schottky diode between SW and PGND. This diode helps conduct a low-side current during high-switching current conditions. Small-package diodes, such as DFLS240 or better, are recommended due to their low voltage drop and high power capabilities.

Setting the Input Hot-Swap Current Limit

Connect a resistor from ILIM to GND to set the current limit value. For example, a 1.4kΩ resistor sets the current limit to about 3.6A. Table 3 lists the recommended resistor values for different current limit values.

Table 3: I_{LIM} vs. R_{LIM}

I_{LIM} (A)	R_{LIM} (kΩ)
4.6	1.05
4.1	1.2
3.6	1.4
1.5	3.3

Selecting the Inductor

An inductor is necessary for supplying constant current to the load. Since boost mode and buck mode share the same inductor, and the buck mode current is higher generally, an inductor that at least supports the buck mode release current is recommended.

Select the inductor based on the buck-release mode. If the storage voltage is V_S, then the release voltage is V_R and the buck running is fixed at a 500kHz frequency. The inductance value can be calculated with Equation (5):

$$L = \frac{V_R}{\Delta I_L \times F_{SW}} \times (1 - \frac{V_R}{V_S}) \quad (5)$$

Where ΔI_L is the peak-to-peak inductor ripple current (which can be set in the range of 30 - 40% of the full release current).

The inductor should not saturate under the maximum inductor peak current.

Setting the Power-On Reset Delay Time

Connect a capacitor to TPOR to set the power-on reset delay time. Leave TPOR floating for the default delay time (around 0.4ms). Table 4 lists the recommended capacitors for different delay times. To eliminate the power-on reset delay, connect TPOR to VIN directly.

Table 4: Reset Delay vs. Capacitor Value

T_D (mS)	C_{TPOR} (nF)
100	100
500	500

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

Setting the Bus Voltage Rise Time

Connect a capacitor to DVDT to set the bus voltage start-up slew rate and soft-start time. Leave DVDT floating for the default soft-start time (around 0.9ms from 0 - 5V). Table 5 lists the recommended capacitor values for different soft-start times at a 5V input condition.

Table 5. Soft Start vs. Capacitor Value

T_R (mS)	$C_{dv/dt}$ (nF)
10	10
100	100

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. A 4-layer layout is recommended to achieve better thermal performance and simplify layout. For best results, refer to Figure 7 and follow the guidelines below.

1. Use short, wide, and direct traces in the high-current paths (VIN, VB, VBO, SW, STRG, and GND).
2. Place the Schottky diode (D1) between SW and PGND with the smallest loop possible.
3. Place the decoupling capacitor across VB and GND as close as possible.
4. Place the decoupling capacitor across STRG and GND as close as possible.
5. Keep the switching node (SW) short and away from the feedback network.
6. Place the external feedback resistors next to the FB pins.
7. Keep the BST voltage path (BST, C6, R10, and SW) as short as possible.

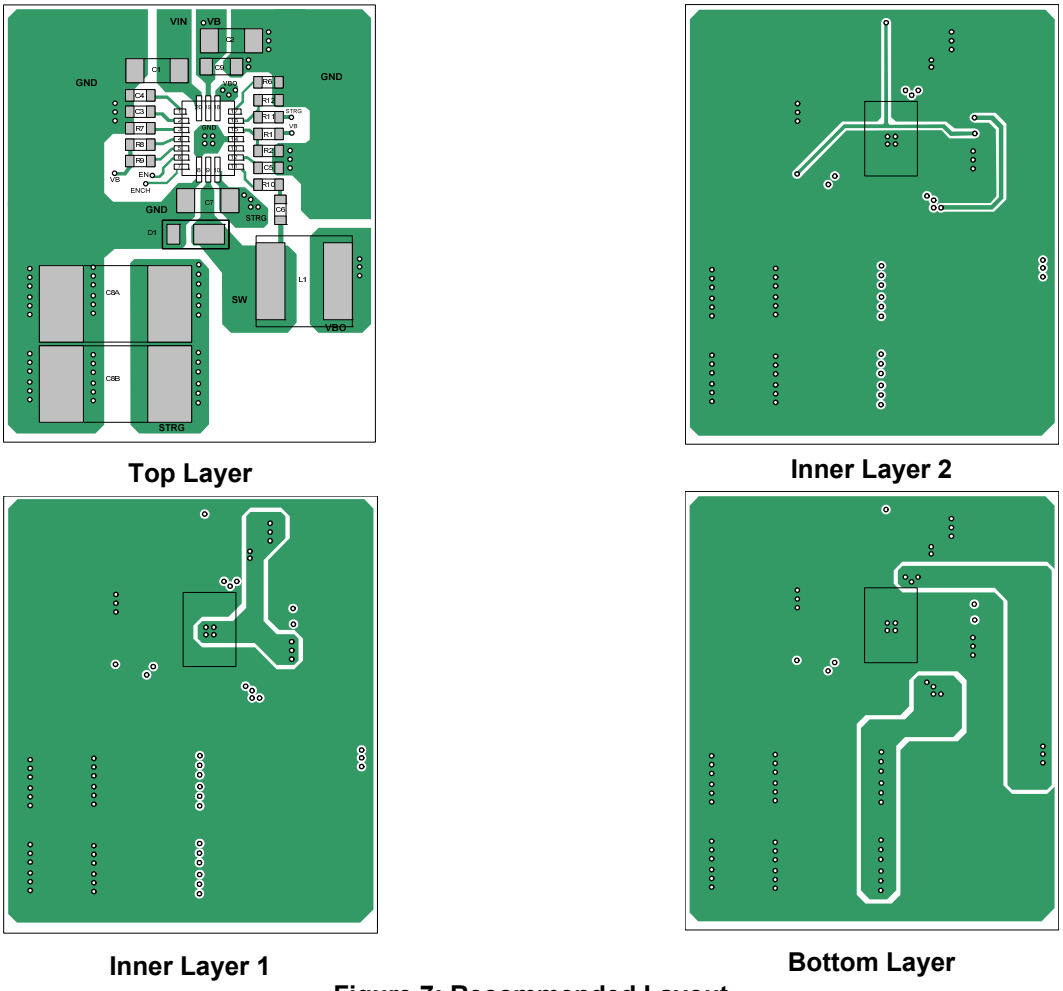


Figure 7: Recommended Layout

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

Design Example

Table 6 shows a design example following the application guidelines for the specifications below.

The detailed application schematic is shown in Figure 8. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section. For more device applications, please refer to the related evaluation board datasheets.

Table 6: Design Example

Parameter	Symbol	Value	Units
Input voltage	V_{IN}	5	V
Charge voltage	V_{STRG}	12	V
Regulated-bus voltage at Pfail	V_{RLS}	4.2	V
Buck mode max output current at Pfail	$I_{RELEASE}$	4	A

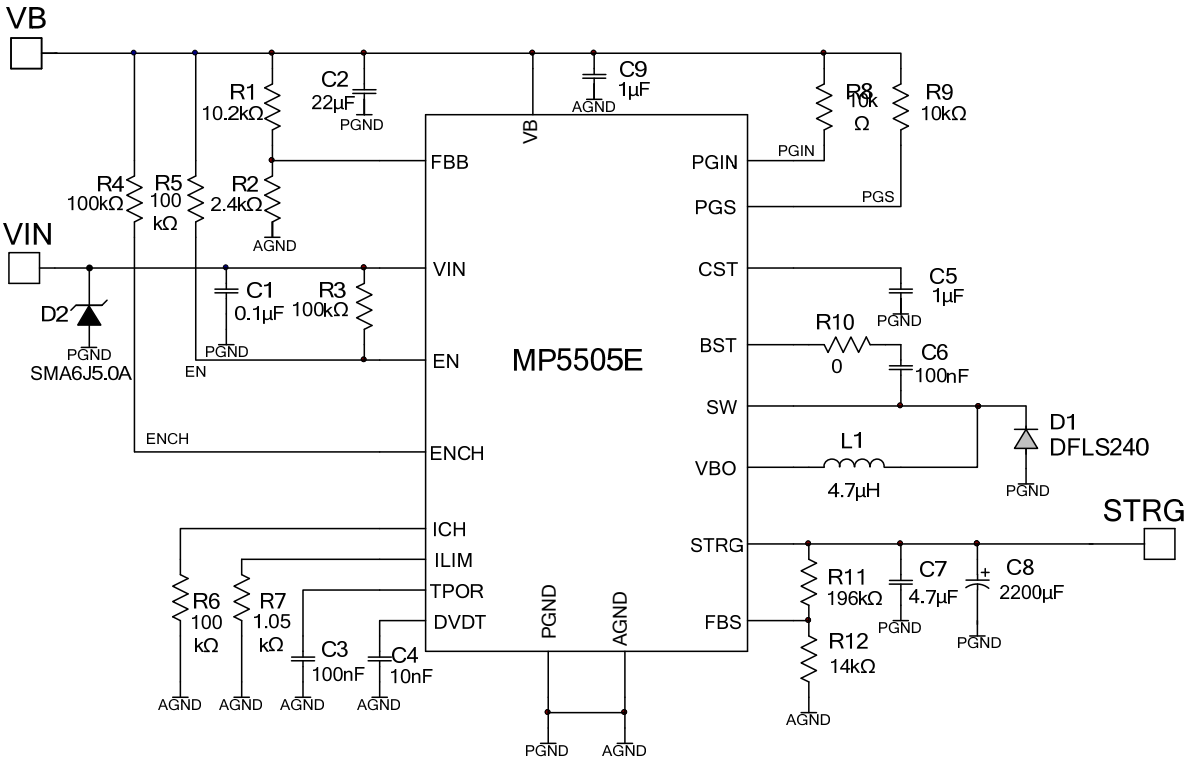
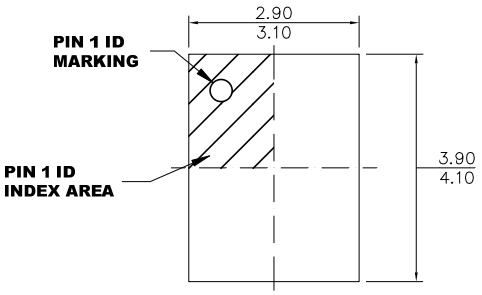


Figure 8: Detailed Application Schematic

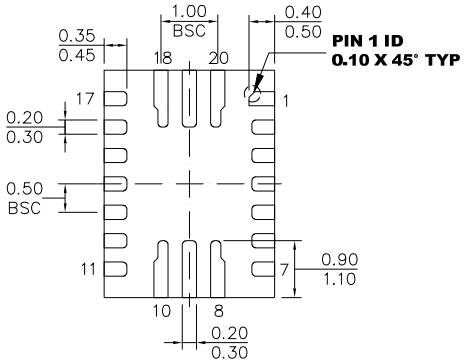
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

PACKAGE INFORMATION

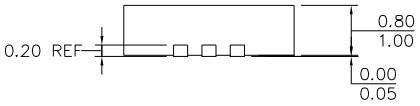
QFN-20 (3mmx4mm)



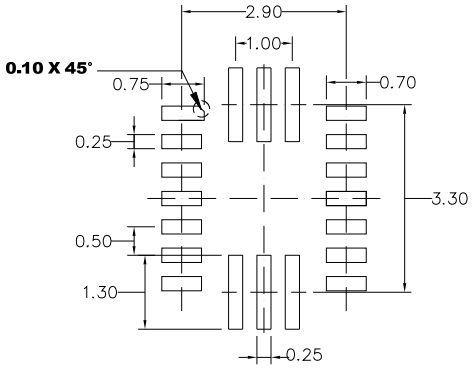
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

Revision History

Revision #	Revision Date	Description	Pages Updated
1.01	05/15/2020	The units of 'PGIN high threshold' and 'PGIN low threshold' in EC table on page 6 are changed from V_{FBS} to V_{FBB}.	P6

NOTICE: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third-party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.