MP5491

Quad-Channel, Laser Diode Current Source IC for Optical Modules

DESCRIPTION

The MP5491 integrates four high-accuracy current sources for laser diodes (LDs), which makes this device well-suited for the transmitter optical subassembly (TOSA) of quad, small form-factor pluggable (QSFP) optical modules.

The device integrates 6-channel GPO outputs. These outputs status can be configured via the I²C interface.

The MP5491 requires a minimal number of external components, and it is available in a space-saving WLCSP-36 (3mmx4.25mm) package.

FEATURES

- 4-Channel Accurate Current Source
- Configurable Current for 10-Bit Digital-to-Analog Converter (DAC)
- Up to 250mA Current per Channel
- Configurable Current Source Slew Rate
- Output Discharging for the Disabled IDx Pin(s)
- Current Source Output Short-Circuit Protection (SCP)
- 6-Channel Independent GPO Outputs
- I²C Control Interface
- I²C Hardware Reset (HRESET)
- Available in a WLCSP-36 (3mmx4.25mm) Package

APPLICATIONS

- Optical Modules

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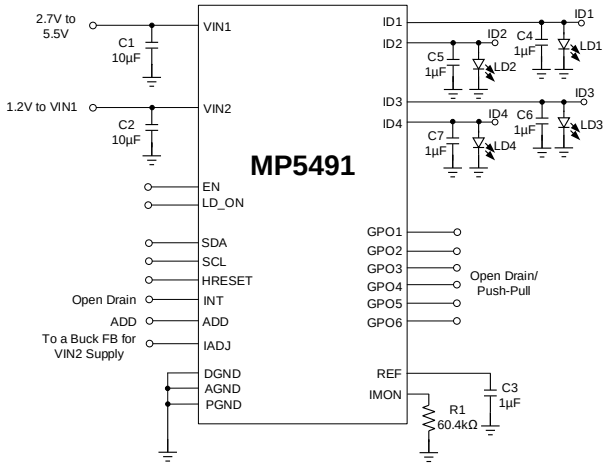
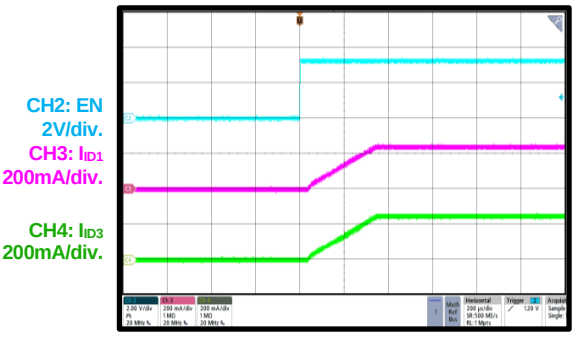
TYPICAL APPLICATION



EN On

ID1 = ID3 = 250mA, SR bit = 01



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP5491GC-0000	WLCSP-36 (3mmx4.25mm)	*See Below*	1
MP5491GC-xxxx**	WLCSP-36 (3mmx4.25mm)		

* For Tape & Reel, add suffix -Z (e.g. MP5491GC-xxxx-Z).

** “xxxx” is the configuration code identifier for the register setting stored in the MOTP. The default code is “0000” (MP5491GC-0000). Each “x” can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number, even if ordering the “0000” code.

TOP MARKING

MPYYWW
MP5491
LLLLLL
AABBID

MP: MPS prefix
YY: Year code
WW: Week code
MP5491: Part number
LLLLLL: Lot number
AABBID: Wafer ID

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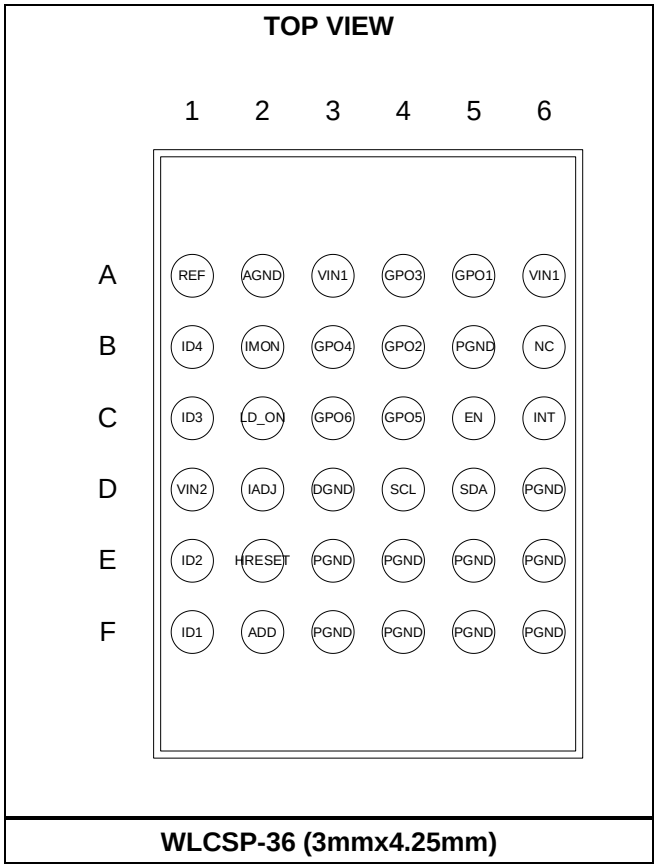
PACKAGE REFERENCE



WLCSP-36 (3mmx4.25mm)

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PIN FUNCTIONS

Pin #	Name	Description
A1	REF	**2.5V reference**. Bypass the REF pin with a 1μF ceramic capacitor connected to AGND.
A2	AGND	**Analog ground.**
A3, A6	VIN1	**Power supply input for analog and digital circuitry.** Bypass the VIN1 pin with a 10μF ceramic capacitor connected to AGND.
A4	GPO3	**GPO output port 3.** The output signal can be adjusted via the I²C.
A5	GPO1	**GPO output port 1.** The output signal can be adjusted via the I²C.
B1	ID4	**Channel 4 current source.** The ID4 pin's output current is controlled by an internal register.
B2	IMON	**Current reference setting pin.** Connect the IMON pin to a high-accuracy resistor with a low temperature coefficient resistor (e.g. 60.4kΩ) to AGND.
B3	GPO4	**GPO output port 4.** The output signal can be adjusted via the I²C.
B4	GPO2	**GPO output port 2.** The output signal can be adjusted via the I²C.
B5, D6, E3, E4, E5, E6, F3, F4, F5, F6	PGND	**Power ground.**
B6	NC	**No internal connection.**
C1	ID3	**Channel 3 current source.** The ID3 pin's output current is controlled by an internal register.
C2	LD_ON	**Channel 1–4 current source enable control.**
C3	GPO6	**GPO output port 6.** The output signal can be adjusted via the I²C.
C4	GPO5	**GPO output port 5.** The output signal can be adjusted via the I²C.
C5	EN	**Enable pin.** The EN pin controls all of the MP5491's analog circuits. The I²C interface and registers are not controlled by the EN pin.
C6	INT	**Interrupt pin.** The INT pin is an open-drain output.
D1	VIN2	**Power supply for current source ID1~ID4.** Bypass the VIN2 pin with a 10μF ceramic capacitor connected to PGND.
D2	IADJ	**Adjustable interface**. Connect the IADJ pin to a buck's FB pin so that it can control the buck's output via the I²C setting. Float this pin if it is not used.
D3	DGND	**Digital ground.**
D4	SCL	**I²C clock signal input.**
D5	SDA	**I²C data pin.**
E1	ID2	**Channel 2 current source.** The ID2 pin's output current is controlled by an internal register.
E2	HRESET	**I²C interface hardware reset pin.** A high logic refreshes the I²C interface but keeps the I²C register values.
F1	ID1	**Channel 1 current source.** The ID1 pin's output current is controlled by an internal register.
F2	ADD	**Address setting for the I²C.** Connect one resistor from the ADD pin to AGND; different resistors set different I²C addresses.

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ABSOLUTE MAXIMUM RATINGS (1)

V_{VIN1}, V_{VIN2}..... .-0.3V to +6.5V
All other pins.....-0.3V to +6.25V
Continuous power dissipation (T_A = 25°C) (2) (4)
.....5W
Junction temperature (T_J)..... 150°C
Lead temperature.....260°C
Storage temperature.....-65°C to +150°C

ESD Ratings

Human body model (HBM) ..... .±2000V
Charged-device model (CDM).....±1000V

Recommended Operating Conditions (3)

Supply voltage (V_{IN1}).....2.7V to 5.5V
Supply voltage (V_{IN2}).....1.2V to V_{IN1}
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

WLCSP-36(3mmx4.25mm)
EV5491-C-00A (4).....25..... 6.... °C/W
JESD51-7 (5) .....27.8 .... 6.6 .. °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on the EV5491-C-00A, 4-layer, 1oz, 51mmx51mm PCB.
5) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

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ELECTRICAL CHARACTERISTICS

V_{IN1} = 3.3V, V_{IN2} = 1.8V, T_J = -40°C to 125°C [6], unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
VIN1 under-voltage lockout (UVLO) rising threshold	V_{IN1_R}		2.25	2.4	2.55	V
VIN1 UVLO hysteresis	V_{IN1_HYS}			200		mV
VIN2 UVLO rising threshold	V_{IN2_R}		0.8	0.9	1	V
VIN2 UVLO hysteresis	V_{IN2_HYS}			135		mV
Supply current	I_{IN1}	EN on, ID1~ID4 on, no load		4.5	5.5	mA
		EN off		2.3	3	mA
Logic Input (EN, HRESET, and LD_ON Pins)						
Input logic high voltage			0.8			V
Input logic low voltage					0.4	V
Internal pull-down resistor				1		MΩ
ID Pin Current Source						
Current range		R_{IMON} = 60.4kΩ	0		250	mA
VIN2 to ID pin dropout voltage		Load = 250mA			400	mV
Discharge resistor		Pull LD_ON low		10		Ω
LD_ON turn-on delay [7]	t_{LD_ON}	From LD_ON high to ID current start rising, SR bits = 01		30		µs
LD_ON turn-off delay [7]	t_{LD_OFF}	From LD_ON low to ID current start dropping		2		µs
ID current slew rate		SR bits = 01		0.75		mA/µs
ID current accuracy		IDx = 100mA	-1.5		+1.5	%
		IDx = 200mA	-2		+2	%
Short-circuit protection (SCP) hiccup time period [7]		IDx short to PGND		80		ms
Analog Signals						
IADJ source current capability				15.5		µA
IADJ sink current capability				-15.5		µA
Reference voltage			2.485	2.5	2.515	V
IMON voltage			1.195	1.2	1.205	V
Interrupt (INT)						
INT pin output low voltage		Sink 5mA			0.4	V
INT pin leakage current		INT logic high, pull up to 3.3V			1	µA
Thermal Warning and Shutdown						
Thermal shutdown temperature [7]	T_{SD}			160		°C
Thermal shutdown recovery hysteresis [7]	T_{SD-HYS}			30		°C
Thermal warning threshold [7]	T_{WARN}			120		°C
Thermal warning hysteresis [7]	$T_{WARN-HYS}$			20		°C

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN1} = 3.3V, V_{IN2} = 1.8V, T_J = -40°C to 125°C (6), unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
I^2C Interface						
SCL, SDA input high voltage			1.2			V
SCL, SDA input low voltage					0.4	V
SDA output low voltage		Sink 5mA			0.4	V

Notes:

6) Not tested in production; guaranteed by over-temperature correlation.
7) Guaranteed by engineer sample characterization. Not tested in production.

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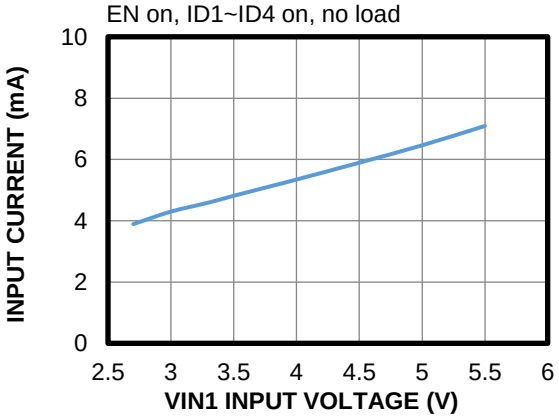
TYPICAL CHARACTERISTICS

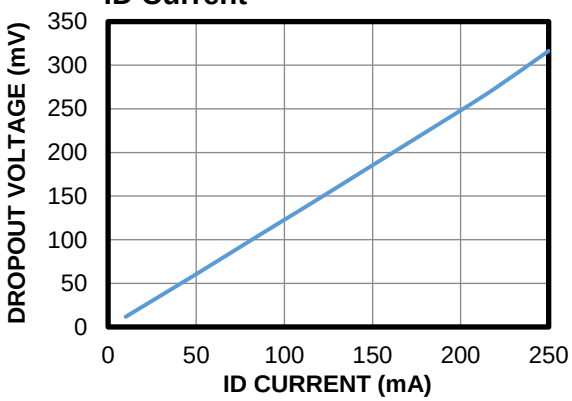
V_{IN1} = 3.3V, V_{IN2} = 1.8V, T_A = 25°C, unless otherwise noted.

Input Current vs. VIN1 Input Voltage

EN on, ID1~ID4 on, no load

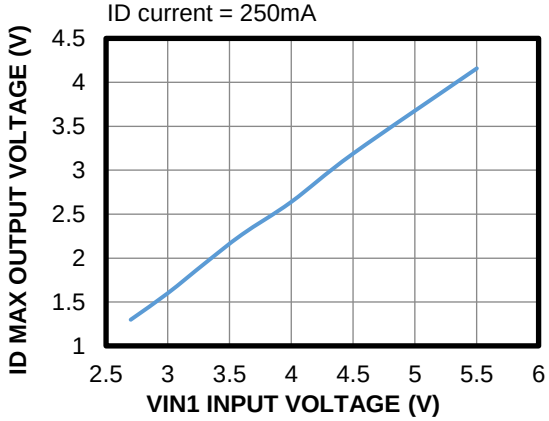


VIN2 to ID Dropout Voltage vs. ID Current



ID Max Output Voltage vs. VIN1 Input Voltage

ID current = 250mA



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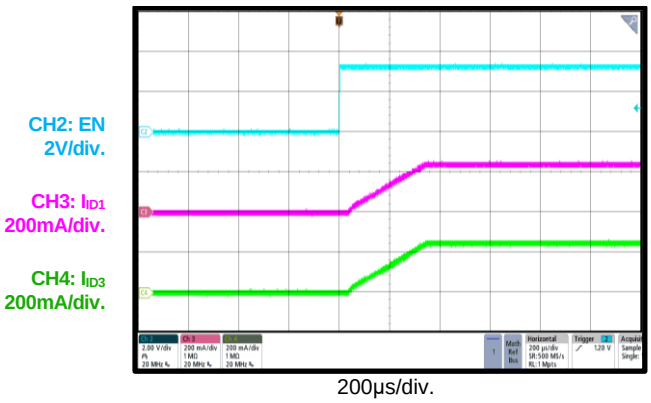
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN1} = 3.3V, V_{IN2} = 1.8V, T_A = 25°C, unless otherwise noted.

EN On

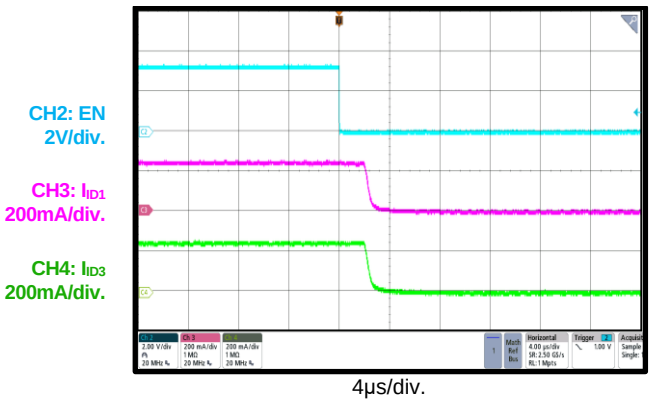
ID1 = ID3 = 250mA, SR bit = 01



200µs/div.

EN Off

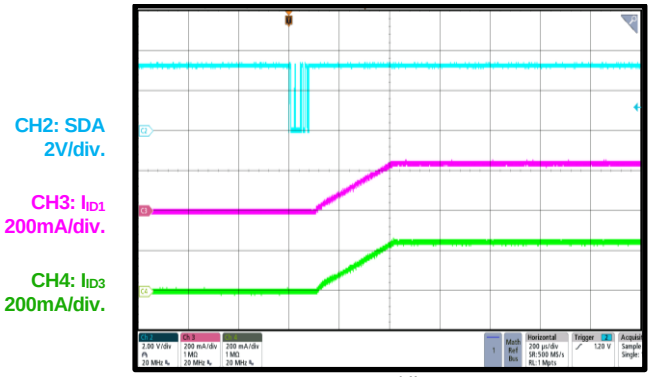
ID1 = ID3 = 250mA, SR bit = 01



4µs/div.

ID_EN Bit On

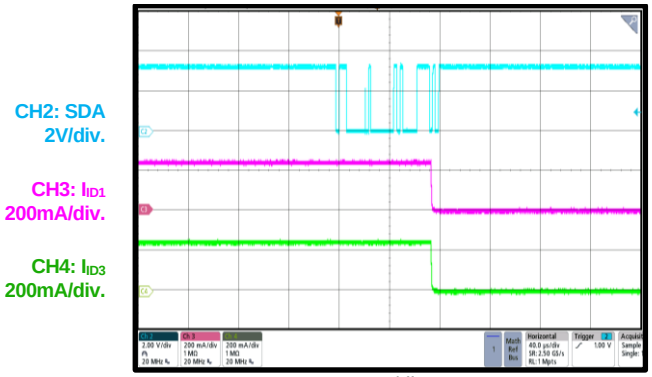
ID1 = ID3 = 250mA, SR bit = 01



200µs/div.

ID_EN Bit Off

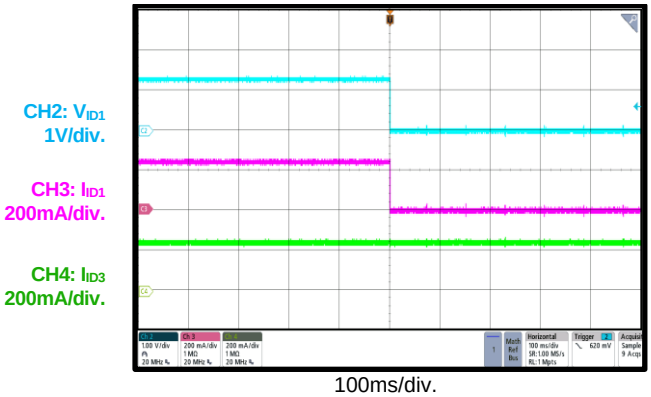
ID1 = ID3 = 250mA, SR bit = 01



40µs/div.

SCP Entry

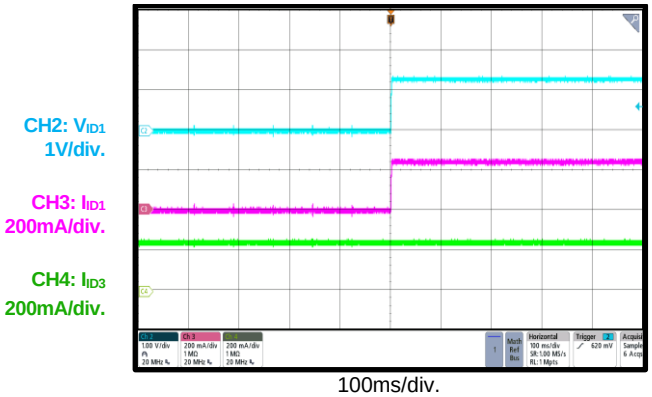
ID1 = ID3 = 250mA, auto-recovery mode



100ms/div.

SCP Recovery

ID1 = ID3 = 250mA, auto-recovery mode



100ms/div.

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FUNCTIONAL BLOCK DIAGRAM

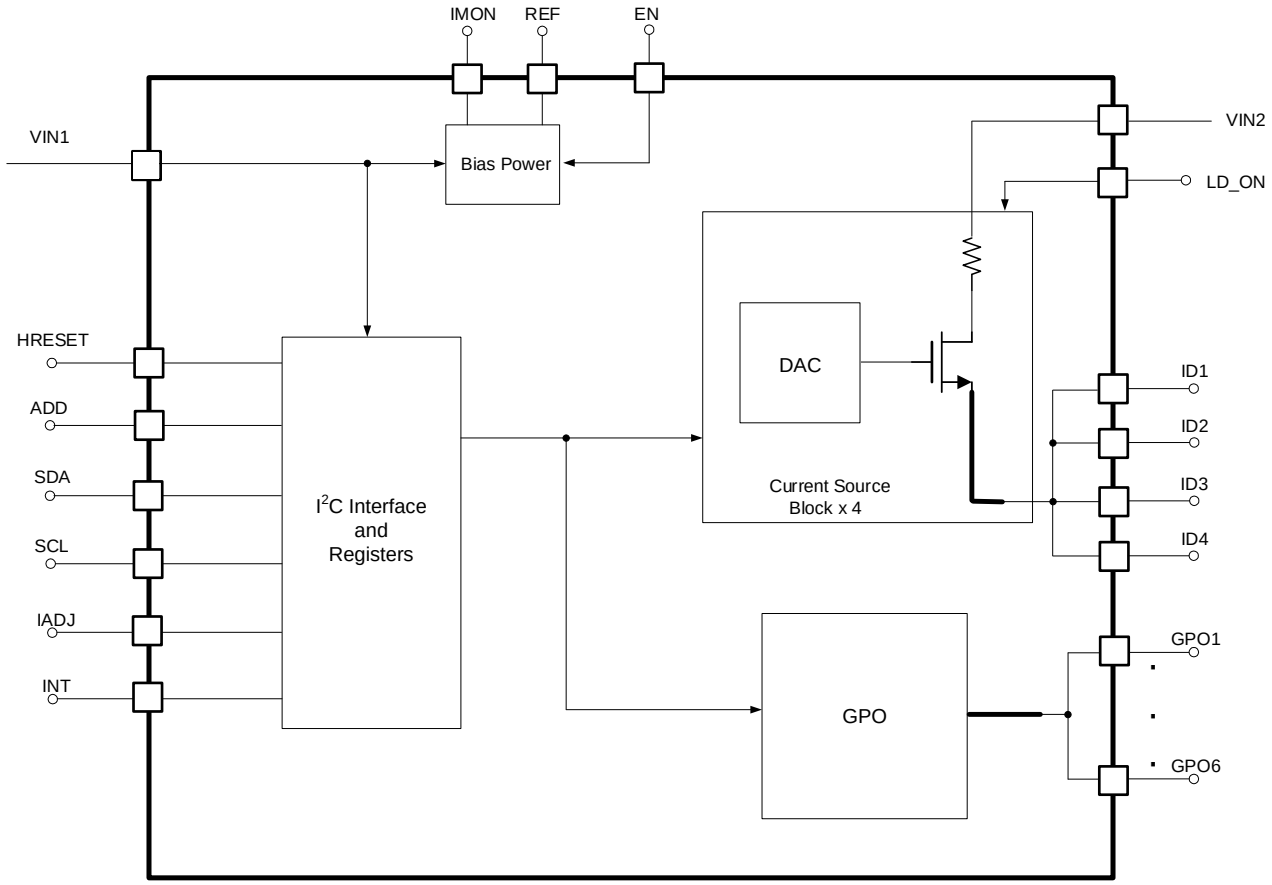

Figure 1: Functional Block Diagram

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OPERATION

The MP5491 integrates four high-accuracy current sources for laser diodes (LDs), which is suitable for transmitter optical subassembly (TOSA) of quad, small form-factor pluggable (QSFP) optical modules. The MP5491 also provide 6-channel GPO outputs.

All output rails can be adjusted via the I2C bus or preset by the multi-page one-time programmable (MOTP) memory. The I²C interface provides adjustable default output current scaling. Refer to registers 07h~0Eh starting on page 23 for more details.

Power Supply and Enable Control

The MP5491 requires two external power sources. Its start-up is determined by the external power source statuses on the VIN1, VIN2, and EN pins.

VIN1 supplies all internal biases and control circuits, while VIN2 provides the power for the IDx outputs and GPOx pull-up power. The VIN2 voltage (V_{IN2}) should not exceed the VIN1 voltage (V_{IN1}) in application.

The enable control includes the EN pin and EN bit. IDx and GPOx start working when both the EN pin and EN bit are in high logic, but the I²C interface is not controlled by EN pin and EN bit.

The ID block has an independent LD_ON pin controlling when ID is on/off. The IDx outputs are active only when LD_ON pin is at a high logic (see Figure 2). LD_ON can shut off ID within 2µs.

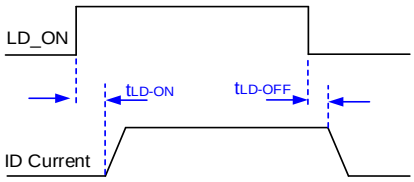

Figure 2: LD_ON Delay Time

High-Accuracy Current Source

The MP5491 integrates a 4-channel, high-accuracy current sources from ID1 to ID4. All channels are powered by the VIN2 source.

The ID power offers an accurate current source, as configured via the IDx registers (07h~0Eh) based on 0.25mA/LSB. The MP5491 can support up to 250mA of current sourcing.

The IDx pin's output voltage is limited by voltage level of VIN1 and VIN2. See the Typical Characteristics section on page 8 for more information.

Laser Short-Circuit Protection (SCP)

The MP5491 integrates laser short-circuit protection (SCP) circuitry. Once the system senses the ID1~ID4 pin's output voltage is below 0.3V, the chip turns off the port for protection. After the protection is triggered, the MP5491 can recover after a set time or enter latch-off mode based on the ID_SCP_MODE setting. This protection is disabled during the internal soft start.

If the IDx pin opens without a laser diode connection, the output voltage rises up close to V_{IN2}. Ensure that all external components can operate at a safe state.

IADJ Function

The MP5491 offers an IADJ pin to assist an external buck converter providing an output voltage supply to the VIN2 pin by connecting the IADJ pin to an external switching regulator's FB pin (see Figure 3). The MP5491 can sink or source a configurable current (0.122µA/LSB) to adjust the buck's output voltage based on the IADJ register's setting. This function can provide a suitable V_{IN2} to improve efficiency.

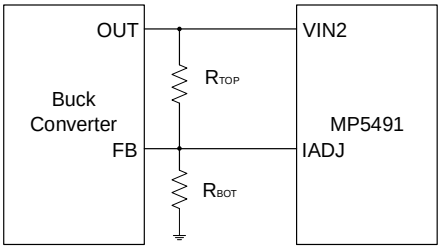

Figure 3: IADJ Application

Interrupt (INT)

The MP5491 offers an INT pin to send an interrupt signal. The INT pin pulls low if any bit in the INT (32h) register is triggered and the INT source is not masked.

If the INT bit is cleared, the INT pin rises high again and waits for the next interrupt event. If a second interrupt event occurs while the INT pin is low, the INT pin's state does not change to high until all interrupt sources are cleared.

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Thermal Warning and Shutdown

Thermal warning and shutdown prevent the part from operating at exceedingly high temperatures. When the silicon die temperature exceeds 120°C, the MP5491 sets the OT_WARN bit to 1. If the die temperature exceeds 160°C, the MP5491 sets the OT bit to 1, and the system enters a shutdown state. The MP5491 restarts when the temperature drops to 130°C.

Slave Address

To support multiple MP5491 devices through one I^2C bus, use the ADD pin to configure the I^2C address for each MP5491. Connect a resistor from the ADD pin to ground to set the slave address. Table 1 shows the ADD pin configuration with different resistor values.

Table 1: ADD Pin Configuration

R_{ADD}	I^2C Slave Address	
43kΩ/short to GND	0x60	1100 000
75kΩ	0x62	1100 010
105kΩ	0x64	1100 100
130kΩ/float	0x66	1100 110

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I²C INTERFACE

I²C Serial Interface Description

The I²C is a 2-wire, bidirectional serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are externally pulled to a bus voltage when they are idle. Connecting to the line, a master device generates the SCL signal and device address and arranges the communication sequence. The MP5491's interface is an I²C slave that can support fast-mode (400kHz) communication.

The I²C interface adds flexibility to the power supply solution. The IDx currents and GPO output states can be instantaneously controlled via the I²C interface.

When the master sends the address as an 8-bit value, the 7-bit address should be followed by 0 or 1 to indicate write or read operation, respectively.

Start and Stop Commands

The start and stop commands are signaled by the master device which signifies the beginning and the end of the I²C transfer. The start (S) command is defined as the SDA signal transitioning from high to low while the SCL is high. The stop (P) command is defined as the SDA signal transitioning from low to high while the SCL is high. Figure 4 shows the start and stop commands.

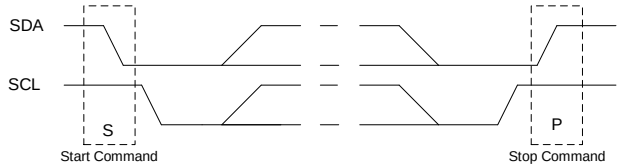

Figure 4: Start and Stop Command

The master then generates the SCL clocks, then it transmits the device address and the read/write (R/W) direction bit on the SDA line.

Transfer Data

Data is transferred in 8-bit or 16-bit bytes by the SDA line. Each byte of data must be followed by an acknowledge (ACK) bit.

I²C Update Sequence

The MP5491 requires a start command, a valid I²C address, a register address byte, and a data byte for a single data update. After receiving each byte, the MP5491 acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MP5491. The MP5491 performs an update on the falling edge of the least significant bit (LSB) byte.

Figure 5 shows an I²C example writing to a single register. Figure 6 shows an I²C example writing to multiple registers. Figure 7 on page 14 shows an I²C example reading a register.

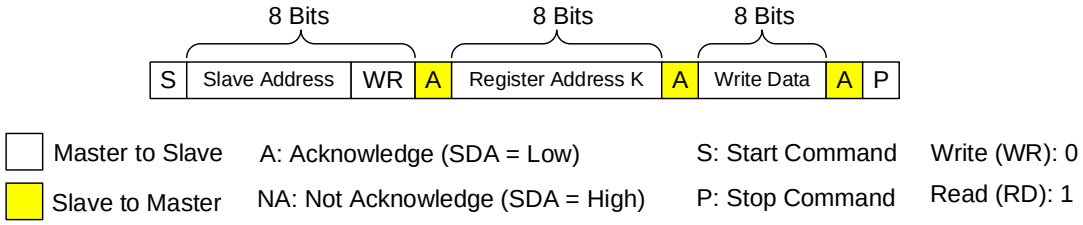

Figure 5: I²C Write Example (Write Single Register)

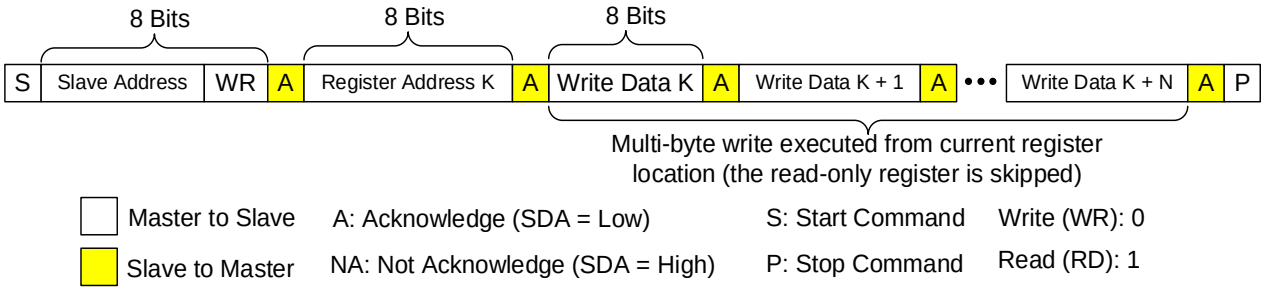

Figure 6: I²C Write Example (Write Multi Register)

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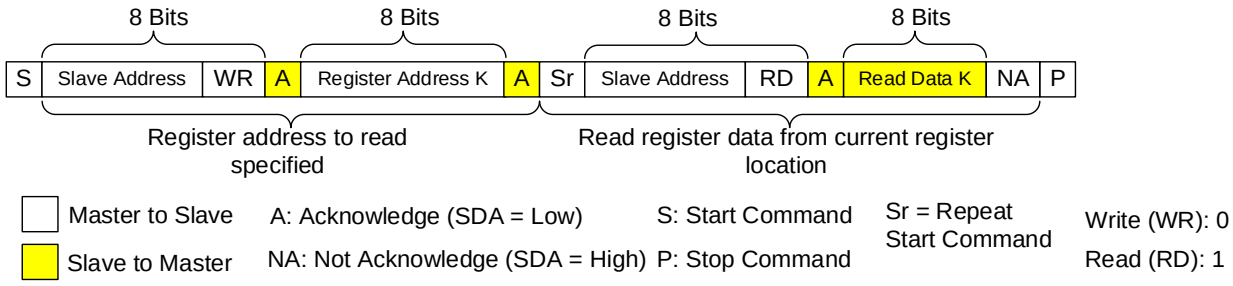

Figure 7: I²C Read Example (Read Single Register)

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REGISTER DESCRIPTION

MOTP eFuse Configuration Table

ADD	Name	D7	D6	D5	D4	D3	D2	D1	D0
0x00	CTL0	SYSEN	RESERVED		ID_DELAY_BASE_TIME		RESERVED		
0x01	CTL1	ID_EN	ID_DELAY_SLOT			ID1_EN	ID2_EN	ID3_EN	ID4_EN
0x03	CTL2	GPO_EN	GPO1_EN	GPO2_EN	GPO3_EN	GPO4_EN	GPO5_EN	GPO6_EN	RESERVED
0x07	ID	MSB_8_BIT_OF_ID_CURRENT							
0x08		RESERVED			SLEW_RATE		RESERVED	LSB_2_BIT_OF_ID_CURRENT	
0x0D	GPO_ CONFIG	GPO1	GPO2	GPO3	GPO4	GPO5	GPO6	RESERVED	
0x0E	GPO_ PULL-UP	PL1	PL2	PL3	PL4	PL5	PL6	RESERVED	
0x11	PROTECT	ID SCP MODE	RESERVED						

MOTP EFUSE TABLE DESCRIPTION

CTL0 (00h)

Format: Unsigned binary

The CTL0 command enables SYS and sets the ID delay base time.

Bits	Access	Bit Name	Default	Description
D[7]	R	SYSEN	0	Enables the system by default. If the VIN1 and EN pin's voltages exceed their ULVO thresholds and the SYSEN bit is set to 1, the MP5491 starts to work. 0: Disabled 1: Enabled
D[6:5]	R	RESERVED	00	Reserved.
D[4:3]	R	ID_DELAY_BASE_ TIME	00	Sets the ID current source start-up time. Calculate the start-up delay based on ID_DELAY_SLOT multiplied by ID_DELAY_BASE_TIME. D[4:3] / Slot Base Time (ms): 00 / 0.25; 01 / 0.5; 10 / 1; 11 / 2
D[2:0]	R	RESERVED	000	Reserved.

Figure 8 shows the time delays set by ID_DELAY_BASE_TIME.

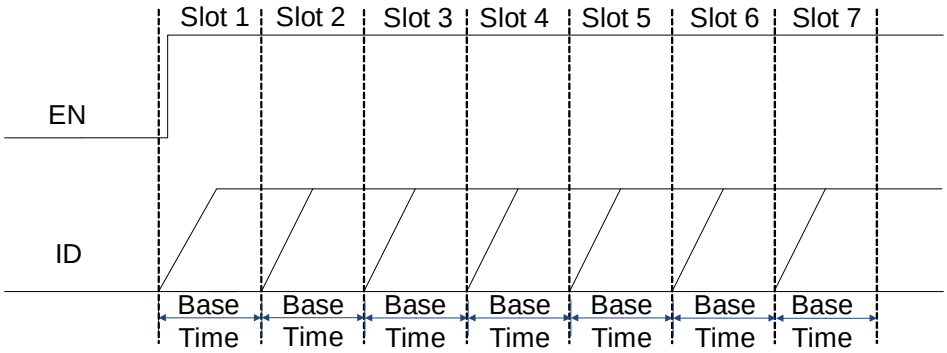

Figure 8: Time Delays

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CTL1 (01h)

Format: Unsigned binary

The CTL1 command enables the ID block and sets the start-up delay slot.

Bits	Access	Bit Name	Default	Description
D[7]	R	ID_EN	0	Enables the ID block. This bit is masked if ID_DELAY_SLOT is not set to 000. 0: Disabled 1: Enabled
D[6:4]	R	ID_DELAY_SLOT	000	Sets the default ID turn-on delay default value after the EN bit is set. Calculate the start-up delay based on ID_DELAY_SLOT multiplied by ID_DELAY_BASE_TIME.
D[3]	R	ID1_EN	1	Enables the ID1 output. 0: Disabled 1: Enabled
D[2]	R	ID2_EN	1	Enables the ID2 output. 0: Disabled 1: Enabled
D[1]	R	ID3_EN	1	Enables the ID3 output. 0: Disabled 1: Enabled
D[0]	R	ID4_EN	1	Enables the ID4 output. 0: Disabled 1: Enabled

D[6:4]	Slot	D[6:4]	Slot
000	Enable digital EN	100	Slot 4
001	Slot 1	101	Slot 5
010	Slot 2	110	Slot 6
011	Slot 3	111	Slot 7

Figure 9 shows the turn-on delays set by ID_DELAY_SLOT.

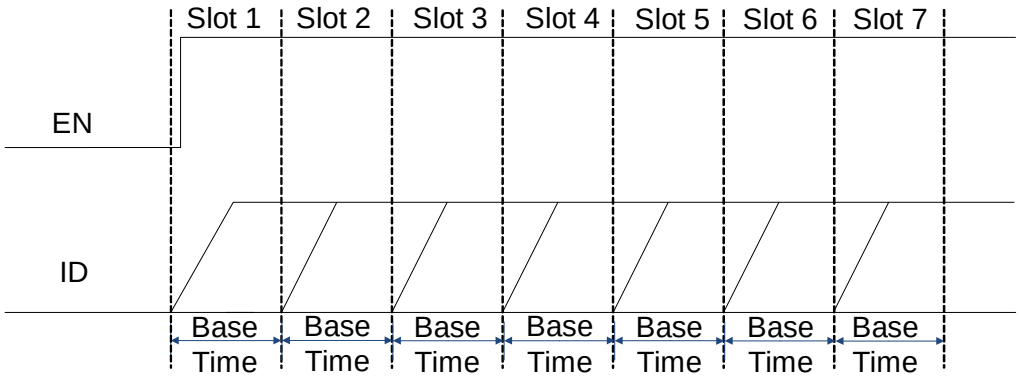

Figure 9: Time Delays

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CTL2 (03h)

Format: Unsigned binary

The CTL2 command enables the GPO block and GPO1~GPO6.

Bits	Access	Bit Name	Default	Description
D[7]	R	GPO_EN	0	Enables the GPO block. Each GPOx port can be enabled only after this bit is enabled. 0: Disabled 1: Enabled
D[6]	R	GPO1_EN	1	Enables the GPO1 output. 0: Disabled 1: Enabled
D[5]	R	GPO2_EN	1	Enables the GPO2 output. 0: Disabled 1: Enabled
D[4]	R	GPO3_EN	1	Enables the GPO3 output. 0: Disabled 1: Enabled
D[3]	R	GPO4_EN	1	Enables the GPO4 output. 0: Disabled 1: Enabled
D[2]	R	GPO5_EN	1	Enables the GPO5 output. 0: Disabled 1: Enabled
D[1]	R	GPO6_EN	1	Enables the GPO6 output. 0: Disabled 1: Enabled
D[0]	R	RESERVED	0	Reserved.

ID (07h)

Format: Unsigned binary

The ID (07h) command configures the 8 most significant bits (MSB) to set the current for all 4 channels.

Bits	Access	Bit Name	Default	Description
D[7:0]	R	MSB_8_BIT_OF_ID_CURRENT	0000 0000	Sets the 8 MSB for the IDx output current. The current ranges between 0mA and 250mA by connecting a 60.4kΩ resistor from the IMON pin to AGND. These MOTP bits configure the current value for all 4 channels.

ID (08h)

Format: Unsigned binary

The ID (08h) command configures the 2 least significant bits (LSB) to set the current slew rate for all 4 channels.

Bits	Access	Bit Name	Default	Description
D[7:5]	R	RESERVED	000	Reserved.

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D[4:3]	R	SLEW_RATE	01	Sets the IDx output's current rising slew rate. These MOTP bits configure the current slew rate for all 4 channels. 00: 1.5mA/μs 01: 0.75mA/μs 10: 0.375mA/μs 11: 0.1875mA/μs
D[1:0]	R	LSB_2_BIT_OF_ID_CURRENT	00	Sets the 2 LSB for the IDx output current. The current ranges between 0mA and 250mA by connecting a 60.4kΩ resistor from the IMON pin to AGND. These MOTP bits configure the current value for all 4 channels.

GPO_CONFIG (0Dh)

Format: Unsigned binary

The GPO_CONFIG command sets the output status for the GPO1~GPO6 pins.

Bits	Access	Bit Name	Default	Description
D[7]	R	GPO1	0	Sets the GPO1 pin's output status. 0: Output low 1: Output high
D[6]	R	GPO2	0	Sets the GPO2 pin's output status. 0: Output low 1: Output high
D[5]	R	GPO3	0	Sets the GPO3 pin's output status. 0: Output low 1: Output high
D[4]	R	GPO4	0	Sets the GPO4 pin's output status. 0: Output low 1: Output high
D[3]	R	GPO5	0	Sets the GPO5 pin's output status. 0: Output low 1: Output high
D[2]	R	GPO6	0	Sets the GPO6 pin's output status. 0: Output low 1: Output high
D[1:0]	R	RESERVED	00	Reserved.

GPO_PULL-UP (0Eh)

Format: Unsigned binary

The GPO_PULL-UP commands sets the output structure of the GPO1~GPO6 pins.

Bits	Access	Bit Name	Default	Description
D[7]	R	PL1	0	Sets the GPO1 pin's output structure. 0: Open-drain output. 1: Push-pull output. Internally pull up to VIN2 when it outputs high
D[6]	R	PL2	0	Sets the GPO2 pin's output structure. 0: Open-drain output. 1: Push-pull output. Internally pull up to VIN2 when it outputs high

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D[5]	R	PL3	0	Sets the GPO3 pin's output structure. 0: Open-drain output. 1: Push-pull output. Internally pull up to VIN2 when it outputs high
D[4]	R	PL4	0	Sets the GPO4 pin's output structure. 0: Open-drain output. 1: Push-pull output. Internally pull up to VIN2 when it outputs high
D[3]	R	PL5	0	Sets the GPO5 pin's output structure. 0: Open-drain output. 1: Push-pull output. Internally pull up to VIN2 when it outputs high
D[2]	R	PL6	0	Sets the GPO6 pin's output structure. 0: Open-drain output. 1: Push-pull output. Internally pull up to VIN2 when it outputs high
D[1:0]	R	RESERVED	00	Reserved.

PROTECT (11h)

Format: Unsigned binary

The PROTECT command sets the ID1~ID4 pin's output protection mode.

Bits	Access	Bit Name	Default	Description
D[7]	R	ID_SCP_MODE	0	Sets the ID output protection mode. If latch-off mode is enabled, the output can be re-enabled again by V_{IN1} under-voltage lockout (UVLO), V_{IN2} UVLO, LD_ON pin UVLO, EN pin UVLO, or the digital EN bits (including ID_EN bit and the respective IDx_EN bit). 0: Automatically recover after a protection is triggered 1: Latch-off after a protection is triggered
D[6:0]	R	RESERVED	000 0000	Reserved.

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I²C REGISTER MAP

Add	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x00	CTL0	R/W	SYSEN	RESERVED (8)		ID_DELAY_BASE_TIME		RESERVED (8)			0000 0000
0x01	CTL1	R/W	ID_EN	ID_DELAY_SLOT			ID1_EN	ID2_EN	ID3_EN	ID4_EN	0000 1111
0x03	CTL2	R/W	GPO_EN	GPO1_EN	GPO2_EN	GPO3_EN	GPO4_EN	GPO5_EN	GPO6_EN	RESERVED (8)	0111 1110
0x07	ID1	R/W	MSB_8_BIT_OF_ID1_CURRENT								0000 0000
0x08			RESERVED (8)			SLEW_RATE		RESERVED (8)	LSB_2_BIT_OF_ID1_CURRENT		0000 1000
0x09	ID2	R/W	MSB_8_BIT_OF_ID2_CURRENT								0000 0000
0x0A		R/W	RESERVED (8)			SLEW_RATE		RESERVED (8)	LSB_2_BIT_OF_ID2_CURRENT		0000 1000
0x0B	ID3	R/W	MSB_8_BIT_OF_ID3_CURRENT								0000 0000
0x0C		R/W	RESERVED (8)			SLEW_RATE		RESERVED (8)	LSB_2_BIT_OF_ID3_CURRENT		0000 1000
0x0D	ID4	R/W	MSB_8_BIT_OF_ID4_CURRENT								0000 0000
0x0E		R/W	RESERVED (8)			SLEW_RATE		RESERVED (8)	LSB_2_BIT_OF_ID4_CURRENT		0000 1000
0x19	GPO_CONFIG	R/W	GPO1	GPO2	GPO3	GPO4	GPO5	GPO6	RESERVED (8)		0000 0000
0x1A	GPO_PULL-UP	R/W	PL1	PL2	PL3	PL4	PL5	PL6	RESERVED (8)		0000 0000
0x29	PROTECT	R/W	ID_SCP_MODE	RESERVED (8)							0000 0000
0x2D	CTL3	R/W	RESERVED (8)			ID_DISCHARGE	RESERVED (8)		INT_REFRESH	RESERVED (8)	1111 0000
0x2E	STATUS1	R	RESERVED (8)						ID1_FLG	ID2_FLG	0000 0000
0x2F	STATUS2	R	ID3_FLG	ID4_FLG	RESERVED (8)				GPO1_FLG	GPO2_FLG	0000 0000
0x30	STATUS3	R	GPO3_FLG	GPO4_FLG	GPO5_FLG	GPO6_FLG	LD_ON_FLG	RESERVED (8)	VIN2_UV	RESERVED (8)	0000 1010
0x31	STATUS4	R	GPO1_OUTPUT	GPO2_OUTPUT	GPO3_OUTPUT	GPO4_OUTPUT	GPO5_OUTPUT	GPO6_OUTPUT	RESERVED (8)		0000 0000
0x32	INT	R	RESERVED (8)			ID_SCP	RESERVED (8)		OT_WARN	OT	0000 0000
0x34	MASK	R/W	RESERVED (8)			ID_SCP_MSK	RESERVED (8)		OT_WARN_MSK	OT MSK	0000 0000
0x36	IADJ	R/W	IADJ_PROGRAM								0000 0000

Notes:

8) Do not change the reserved register; otherwise it may work abnormally.

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I²C REGISTER DESCRIPTION

CTL0 (00h)

Format: Unsigned binary

The CTL0 command enables SYS and sets the default ID delay base time.

Bits	Access	Bit Name	Default	Description
D[7]	R	SYSEN	0	Enables the system by default. If the VIN1 and EN pin's voltages exceed their ULVO thresholds and the SYSEN bit is set to 1, the MP5491 starts to work. 0: Disabled 1: Enabled
D[6:5]	R	RESERVED	00	Reserved.
D[4:3]	R	ID_DELAY_BASE_ TIME	00	Sets the default ID current source start-up time. Calculate the start-up delay based on ID_DELAY_SLOT multiplied by ID_DELAY_BASE_TIME. D[4:3] / Slot Base Time (ms): 00 / 0.25; 01 / 0.5; 10 / 1; 11 / 2
D[2:0]	R	RESERVED	000	Reserved.

Figure 10 shows the time delays set by ID_DELAY_BASE_TIME.

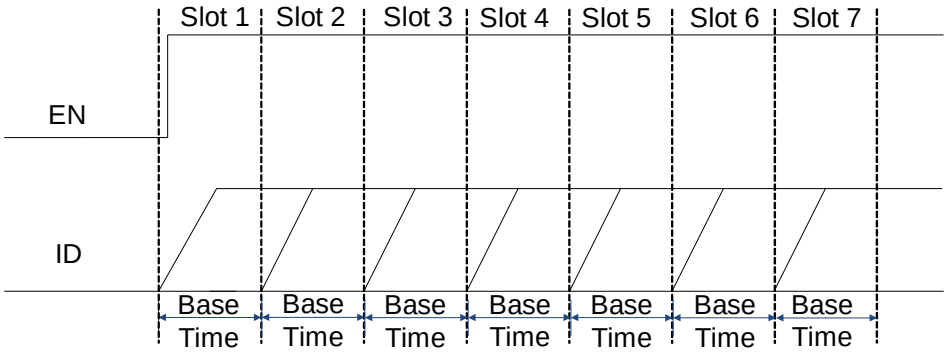

Figure 10: Time Delays

CTL1 (01h)

Format: Unsigned binary

The CTL1 command enables the ID block and sets the default start-up delay slot.

Bits	Access	Bit Name	Default	Description
D[7]	R	ID_EN	0	Enables the ID block. This bit is masked if ID_DELAY_SLOT is not set to 000. 0: Disabled 1: Enabled

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D[6:4]	R	ID_DELAY_SLOT	000	Sets the default ID turn-on delay default value after the EN bit is set. Calculate the start-up delay based on ID_DELAY_SLOT multiplied by ID_DELAY_BASE_TIME.

D[6:4]	Slot	D[6:4]	Slot
000	Enable digital EN	100	Slot 4
001	Slot 1	101	Slot 5
010	Slot 2	110	Slot 6
011	Slot 3	111	Slot 7

D[3]	R	ID1_EN	1	Enables ID1. 0: Disabled 1: Enabled
D[2]	R	ID2_EN	1	Enables ID2. 0: Disabled 1: Enabled
D[1]	R	ID3_EN	1	Enables ID3. 0: Disabled 1: Enabled
D[0]	R	ID4_EN	1	Enables ID4. 0: Disabled 1: Enabled

Figure 11 shows the turn-on delays set by ID_DELAY_SLOT.

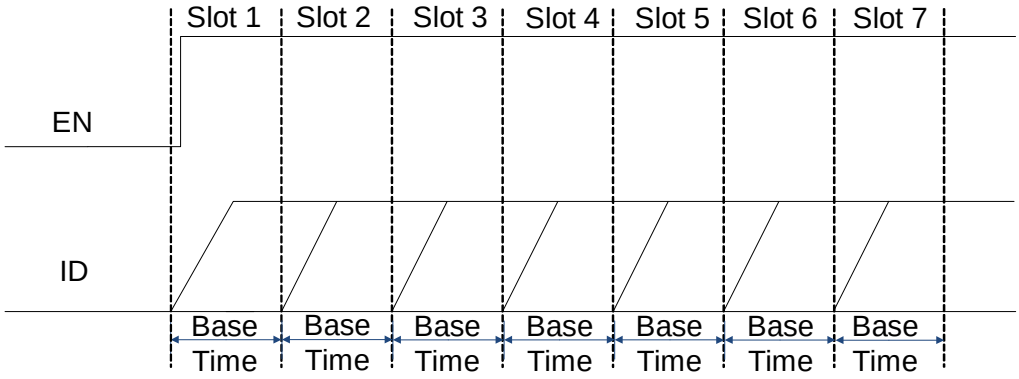

Figure 11: Time Delays

CTL2 (03h)

Format: Unsigned binary

The CTL2 command enables the GPO1~GPO6 pins.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	GPO_EN	0	Enables every GPOx. When this bit is high, the GPOx pins can operate. 0: Disabled 1: Enabled
D[6]	R/W	GPO1_EN	1	Enables GPO1. 0: Disabled 1: Enabled

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D[5]	R/W	GPO2_EN	1	Enables GPO2. 0: Disabled 1: Enabled
D[4]	R/W	GPO3_EN	1	Enables GPO3. 0: Disabled 1: Enabled
D[3]	R/W	GPO4_EN	1	Enables GPO4. 0: Disabled 1: Enabled
D[2]	R/W	GPO5_EN	1	Enables GPO5. 0: Disabled 1: Enabled
D[1]	R/W	GPO6_EN	1	Enables GPO6. 0: Disabled 1: Enabled
D[0]	R/W	RESERVED	0	Reserved.

ID1 (07h/08h)

Format: Unsigned binary

The ID1 command sets the ID1 pin's current and slew rate.

ID1 (07h)

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	MSB_8_BIT_OF_ID1_CURRENT	0000 0000	Set the ID1 current from 0mA to 250mA via register ID1 (07h, bits D[7:0] and 08h, bits D[1:0]). Each step is 0.25mA.The current is 0.25mA x Decimal (the register value). Setting these bits to 0 may shutdown this IC or result in an offset current.

ID1 (08h)

Bits	Access	Bit Name	Default	Description
D[7:5]	R/W	RESERVED	000	Reserved.
D[4:3]	R/W	SLEW_RATE	01	Sets the ID1 pin's slew rate. 00: 1.5mA/μs 01: 0.75mA/μs 10: 0.375mA/μs 11: 0.1875mA/μs
D[2]	R/W	RESERVED	0	Reserved.
D[1:0]	R/W	LSB_2_BIT_OF_ID1_CURRENT	00	Set the ID1 current from 0mA to 250mA via register ID1 (07h, bits D[7:0] and 08h, bits D[1:0]). Each step is 0.25mA.The current is 0.25mA x Decimal (the register value). Setting these bits to 0 may shutdown this IC or result in an offset current.

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ID2 (09h/0Ah)

Format: Unsigned binary

The ID2 command sets the ID2 pin's current and slew rate.

ID2 (09h)

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	MSB_8_BIT_OF_ID2_CURRENT	0000 0000	Set the ID2 current from 0mA to 250mA via register ID2 (09h, bits D[7:0] and 0Ah, bits D[1:0]). Each step is 0.25mA.The current is 0.25mA x Decimal (the register value). Setting these bits to 0 may shutdown this IC or result in an offset current.

ID2 (0Ah)

Bits	Access	Bit Name	Default	Description
D[7:5]	R/W	RESERVED	000	Reserved.
D[4:3]	R/W	SLEW_RATE	01	Sets the ID2 pin's slew rate. 00: 1.5mA/μs 01: 0.75mA/μs 10: 0.375mA/μs 11: 0.1875mA/μs
D[2]	R/W	RESERVED	0	Reserved.
D[1:0]	R/W	LSB_2_BIT_OF_ID2_CURRENT	00	Set the ID2 current from 0mA to 250mA via register ID2 (09h, bits D[7:0] and 0Ah, bits D[1:0]). Each step is 0.25mA.The current is 0.25mA x Decimal (the register value). Setting these bits to 0 may shutdown this IC or result in an offset current.

ID3 (0Bh/0Ch)

Format: Unsigned binary

The ID3 command sets the ID3 pin's current and slew rate.

ID3 (0Bh)

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	MSB_8_BIT_OF_ID3_CURRENT	0000 0000	Set the ID3 current from 0mA to 250mA via register ID3 (0Bh, bits D[7:0] and 0Ch, bits D[1:0]). Each step is 0.25mA.The current is 0.25mA x Decimal (the register value). Setting these bits to 0 may shutdown this IC or result in an offset current.

ID3 (0Ch)

Bits	Access	Bit Name	Default	Description
D[7:5]	R/W	RESERVED	000	Reserved.
D[4:3]	R/W	SLEW_RATE	01	Sets the ID3 pin's slew rate. 00: 1.5mA/μs 01: 0.75mA/μs 10: 0.375mA/μs 11: 0.1875mA/μs
D[2]	R/W	RESERVED	0	Reserved.

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D[1:0]	R/W	LSB_2_BIT_OF_ID3_CURRENT	00	Set the ID3 current from 0mA to 250mA via register ID3 (0Bh, bits D[7:0] and 0Ch, bits D[1:0]). Each step is 0.25mA.The current is 0.25mA x Decimal (the register value). Setting these bits to 0 may shutdown this IC or result in an offset current.

ID4 (0Dh/0Eh)

Format: Unsigned binary

The ID4 command sets the ID4 pin's current and slew rate.

ID4 (0Dh)

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	MSB_8_BIT_OF_ID4_CURRENT	0000 0000	Set the ID4 current from 0mA to 250mA via register ID4 (0Dh, bits D[7:0] and 0Eh, bits D[1:0]). Each step is 0.25mA.The current is 0.25mA x Decimal (the register value). Setting these bits to 0 may shutdown this IC or result in an offset current.

ID4 (0Eh)

Bits	Access	Bit Name	Default	Description
D[7:5]	R/W	RESERVED	000	Reserved.
D[4:3]	R/W	SLEW_RATE	01	Sets the ID4 pin's slew rate. 00: 1.5mA/μs 01: 0.75mA/μs 10: 0.375mA/μs 11: 0.1875mA/μs
D[2]	R/W	RESERVED	0	Reserved.
D[1:0]	R/W	LSB_2_BIT_OF_ID4_CURRENT	00	Set the ID4 current from 0mA to 250mA via register ID4 (0Dh, bits D[7:0] and 0Eh, bits D[1:0]). Each step is 0.25mA.The current is 0.25mA x Decimal (the register value). Setting these bits to 0 may shutdown this IC or result in an offset current.

GPO_CONFIG (19h)

Format: Unsigned binary

The GPO_CONFIG command sets the output status for the GPO1~GPO6 pins.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	GPO1	0	Sets the GPO1 pin's output status. 0: Output low 1: Output high
D[6]	R/W	GPO2	0	Sets the GPO2 pin's output status. 0: Output low 1: Output high
D[5]	R/W	GPO3	0	Sets the GPO3 pin's output status. 0: Output low 1: Output high
D[4]	R/W	GPO4	0	Sets the GPO4 pin's output status. 0: Output low 1: Output high

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D[3]	R/W	GPO5	0	Sets the GPO5 pin's output status. 0: Output low 1: Output high
D[2]	R/W	GPO6	0	Sets the GPO6 pin's output status. 0: Output low 1: Output high
D[1:0]	R/W	RESERVED	00	Reserved.

GPO_PULL-UP (1Ah)

Format: Unsigned binary

The GPO_PULL-UP command sets the output structure of the GPO1~GPO6 pins.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	PL1	0	Sets the GPO1 pin's output structure. 0: Open-drain output. 1: Push-pull output. Internally pull up to VIN2 when it outputs high
D[6]	R/W	PL2	0	Sets the GPO2 pin's output structure. 0: Open-drain output. 1: Push-pull output. Internally pull up to VIN2 when it outputs high
D[5]	R/W	PL3	0	Sets the GPO3 pin's output structure. 0: Open-drain output. 1: Push-pull output. Internally pull up to VIN2 when it outputs high
D[4]	R/W	PL4	0	Sets the GPO4 pin's output structure. 0: Open-drain output. 1: Push-pull output. Internally pull up to VIN2 when it outputs high
D[3]	R/W	PL5	0	Sets the GPO5 pin's output structure. 0: Open-drain output. 1: Push-pull output. Internally pull up to VIN2 when it outputs high
D[2]	R/W	PL6	0	Sets the GPO6 pin's output structure. 0: Open-drain output. 1: Push-pull output. Internally pull up to VIN2 when it outputs high
D[1:0]	R/W	RESERVED	00	Reserved.

PROTECT (29h)

Format: Unsigned binary

The PROTECT command sets the ID short-circuit protection (SCP) mode.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	ID_SCP_MODE	0	Sets the ID protection mode after triggering the laser short-circuit condition. If latch-off mode is enabled, VIN1, VIN2, EN, LD_ON or the digital EN (including the ID_EN bit and respective IDx_EN bits) are re-enabled can start up again. 0: Automatically recover 1: Latch-off

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D[6:0]	R/W	RESERVED	000 0000	Reserved.

CTL3 (2Dh)

Format: Unsigned binary

The CTL3 command enables the ID1~ID4 pin's discharge feature and refreshes INT.

Bits	Access	Bit Name	Default	Description
D[7:5]	R/W	RESERVED	111	Reserved.
D[4]	R/W	ID_DISCHARGE	1	Enables the ID discharge feature. 0: Do not discharge 1: Discharge when ID is disabled
D[3]	R/W	RESERVED	0	Reserved.
D[2]	R/W	INT_REFRESH	0	Warn refresh all I^2C code to default value. 0: Do not refresh 1: Force a refresh then automatically recover to 0
D[1:0]	R/W	RESERVED	00	Reserved.

STATUS1 (2Eh)

Format: Unsigned binary

The STATUS1 command monitors the operation statuses of ID1 and ID2.

Bits	Access	Bit Name	Default	Description
D[7:2]	R	RESERVED	0000 00	Reserved.
D[1]	R	ID1_FLG	0	Indicates the ID1 pin's operation status. 0: Disabled 1: Enabled
D[0]	R	ID2_FLG	0	Indicates the ID2 pin's operation status. 0: Disabled 1: Enabled

STATUS2 (2Fh)

Format: Unsigned binary

The STATUS2 command monitors operation statuses of ID3, ID4, GPO1. and GPO2.

Bits	Access	Bit Name	Default	Description
D[7]	R	ID3_FLG	0	Indicates the ID3 pin's operation status. 0: Disabled 1: Enabled
D[6]	R	ID4_FLG	0	Indicates the ID4 pin's operation status. 0: Disabled 1: Enabled
D[5:2]	R	RESERVED	0000	Reserved.
D[1]	R	GPO1_FLG	0	Indicates the GPO1 port's operation status. 0: Disabled 1: Enabled

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D[0]	R	GPO2_FLG	0	Indicates the GPO2 port's operation status. 0: Disabled 1: Enabled

STATUS3 (30h)

Format: Unsigned binary

The STATUS3 command monitors operation statuses of GPO3~GPO6, LD_ON, and VIN2_UV.

Bits	Access	Bit Name	Default	Description
D[7]	R	GPO3_FLG	0	Indicates the GPO3 port's operation status. 0: Disabled 1: Enabled
D[6]	R	GPO4_FLG	0	Indicates the GPO4 port's operation status. 0: Disabled 1: Enabled
D[5]	R	GPO5_FLG	0	Indicates the GPO5 port's operation status. 0: Disabled 1: Enabled
D[4]	R	GPO6_FLG	0	Indicates the GPO6 port's operation status. 0: Disabled 1: Enabled
D[3]	R	LD_ON FLG	1	Indicates the LD_ON operation status. 0: Disabled 1: Enabled
D[2]	R	RESERVED	0	Reserved.
D[1]	R	VIN2_UV	1	Indicates the V_{IN2} under-voltage lockout (UVLO) status. 0: Not good 1: Good
D[0]	R	RESERVED	0	Reserved.

STATUS4 (31h)

Format: Unsigned binary

The STATUS4 command monitors the output statuses of GPO1~GPO6.

Bits	Access	Bit Name	Default	Description
D[7]	R	GPO1_OUTPUT	0	Indicates the GPO1 pin's output status. 0: Low 1: High
D[6]	R	GPO2_OUTPUT	0	Indicates the GPO2 pin's output status. 0: Low 1: High
D[5]	R	GPO3_OUTPUT	0	Indicates the GPO3 pin's output status. 0: Low 1: High
D[4]	R	GPO4_OUTPUT	0	Indicates the GPO4 pin's output status. 0: Low 1: High

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D[3]	R	GPO5_OUTPUT	0	Indicates the GPO5 pin's output status. 0: Low 1: High
D[2]	R	GPO6_OUTPUT	0	Indicates the GPO6 pin's output status. 0: Low 1: High
D[1:0]	R	RESERVED	00	Reserved.

INT (32h)

Format: Unsigned binary

The INT command monitors the statuses of ID_SCP, OT_WARN, and OT.

Bits	Access	Bit Name	Default	Description
D[7:5]	R	RESERVED	000	Reserved.
D[4]	R	ID_SCP	0	Indicates the ID short-circuit protection (SCP) status and controls the INT pin. 0: Good 1: Not good
D[3:2]	R	RESERVED	00	Reserved.
D[1]	R	OT_WARN	0	Indicates the over-temperature (OT) warning status and controls the INT pin. 0: Good 1: Not good
D[0]	R	OT	0	Indicates the OT status and controls the INT pin. 0: Good 1: Not good

MASK (34h)

Format: Unsigned binary

The MASK command masks the INT pin's behavior.

Bits	Access	Bit Name	Default	Description
D[7:5]	R/W	RESERVED	000	Reserved.
D[4]	R/W	ID_SCP_MSK	0	When this bit is set to 0, the ID_SCP bit is not masked and controls the INT pin. 0: Not masked 1: Masked
D[3:2]	R/W	RESERVED	00	Reserved.
D[1]	R/W	OT_WARN_MSK	0	When this bit is set to 0, the OT_WARN bit is not masked and controls the INT pin. 0: Not masked 1: Masked
D[0]	R/W	OT_MSK	0	When this bit is set to 0, the OT bit is not masked and controls the INT pin. 0: Not masked 1: Masked

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IADJ (36h)

Format: Unsigned binary

The IADJ command sets the IADJ pin's sink/source current.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	IADJ_PROGRAM	0	0: Use a source current from the MP5491 to the buck converter's FB resistor divider to regulate the buck's output voltage lower 1: Use a sink current from the buck converter's FB resistor divider to the ground through the MP5491's IADJ pin. This can regulate the buck's output voltage to be higher than the FB resistor divider's set voltage
D[6:0]	R/W		000 0000	These bits set the IADJ's current. Each step is 0.122μA. When selecting a source: The IADJ current is 0.122μA x Decimal (register value) The buck converter's output can be calculated with the following equation: $\left(1+\frac{R_{TOP}}{R_{BOT}}\right) x\ V_{FB}-R_{TOP}\ x\ IADJ$ Where R_{TOP} and R_{BOT} is buck converter feedback resistor, V_{FB} is buck reference voltage. When selecting a sink: The IADJ current is 15.5μA - 0.122μA x Decimal (register value). The buck converter's output can be calculated with the following equation: $\left(1+\frac{R_{TOP}}{R_{BOT}}\right) x\ V_{FB}+R_{TOP}\ x\ IADJ$

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APPLICATION INFORMATION

Selecting the Output Capacitor

The output capacitors (C4~C7) help to reduces noise. It is recommended to use 1μF ceramic capacitors for the best performance.

Selecting the Input Capacitor

For stable operation, decoupling capacitors (C1 and C2) are required between VIN1/VIN2 and connected to the GND pins. It is recommended to add 10μF ceramic capacitors on the VIN1/VIN2 pins.

IMON Setting

The MP5491 can set 0.25mA/LSB for the IDx output, and it supports up to 250mA of current sourcing with a 60.4kΩ resistor connected from IMON to AGND.

Design Example

Table 2 lists a design example following the application guidelines for the specifications below.

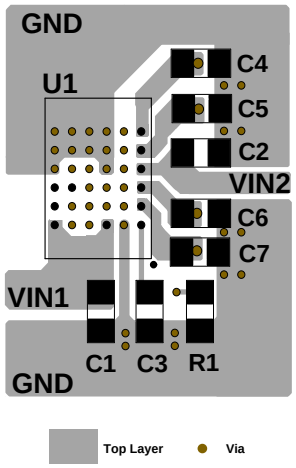
Table 2: Design Example

V_{IN1}	3.3V
V_{IN2}	1.8V
ID1~ID4	100mA

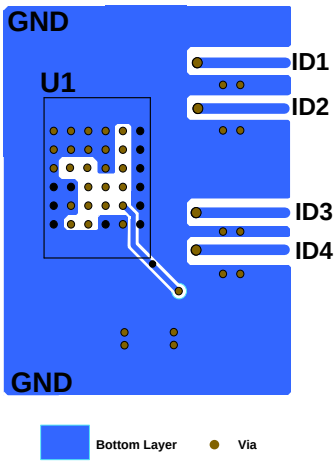
PCB Layout Guidelines

PCB layout is critical for ripple rejection and thermal performance. For the best results, refer to follow the guidelines and refer to Figure 12:

1. Place the capacitor (C1 and C3) as close as possible to the VIN1/REF and AGND pins.
2. Place the capacitor (C2, and C4~C7) as close as possible to the VIN2/ID1~ID4 and PGND pins.
3. All the input and output capacitors' grounds should be connected to the PGND pins with short and wide traces.



Top Layer



Bottom Layer

Figure 12: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUIT

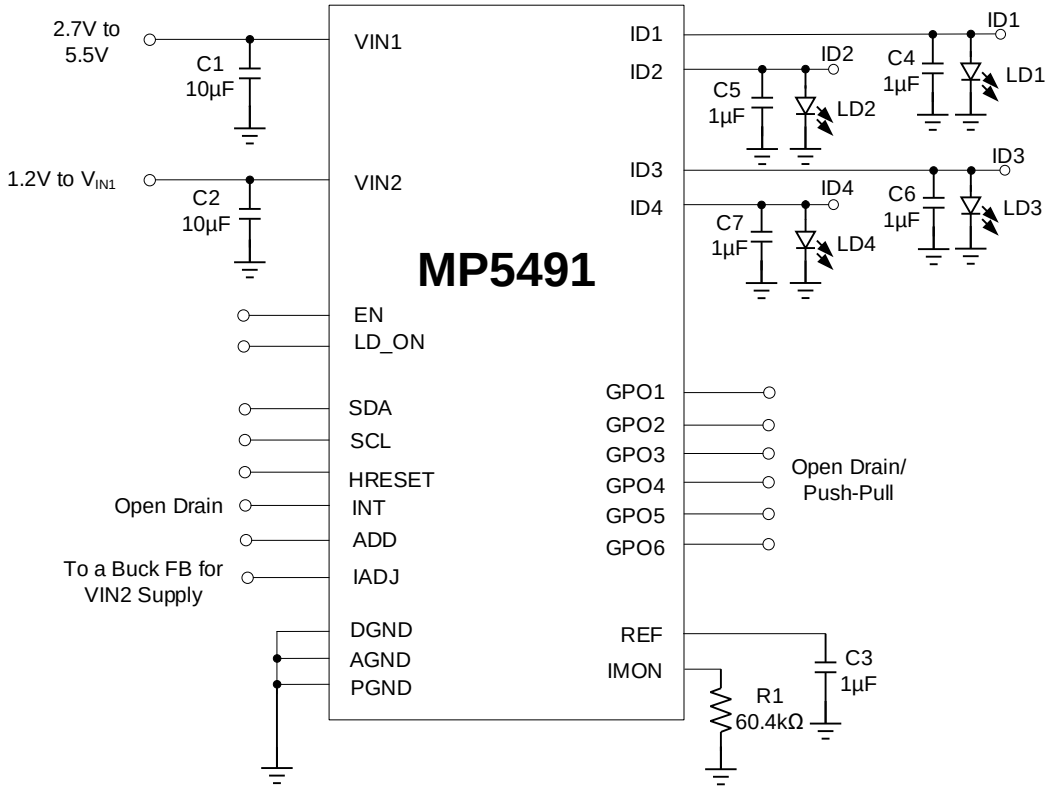

Figure 13: Typical Application Circuit

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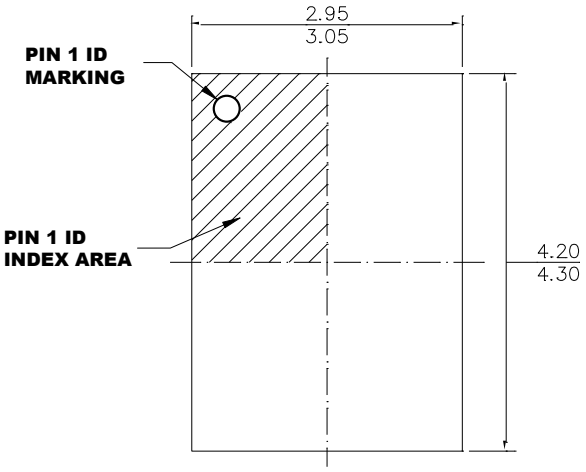
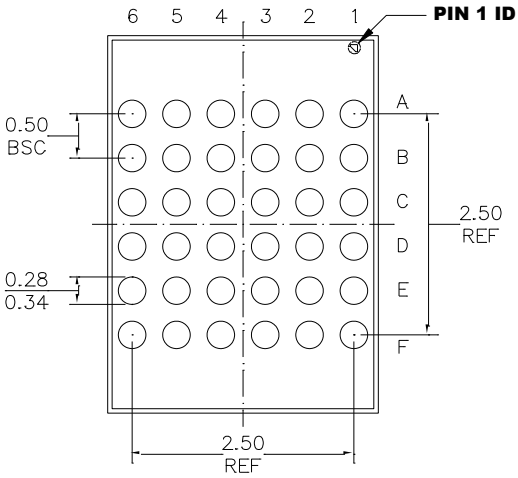
PACKAGE INFORMATION

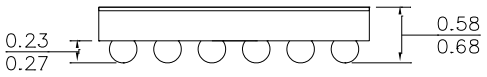
WLCSP-36 (3mmx4.25mm)



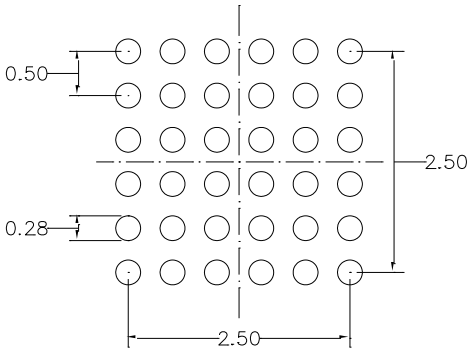
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) BALL COPLANARITY SHALL BE 0.05 MILLIMETER MAX.
3) JEDEC REFERENCE IS MO-211.
4) DRAWING IS NOT TO SCALE.

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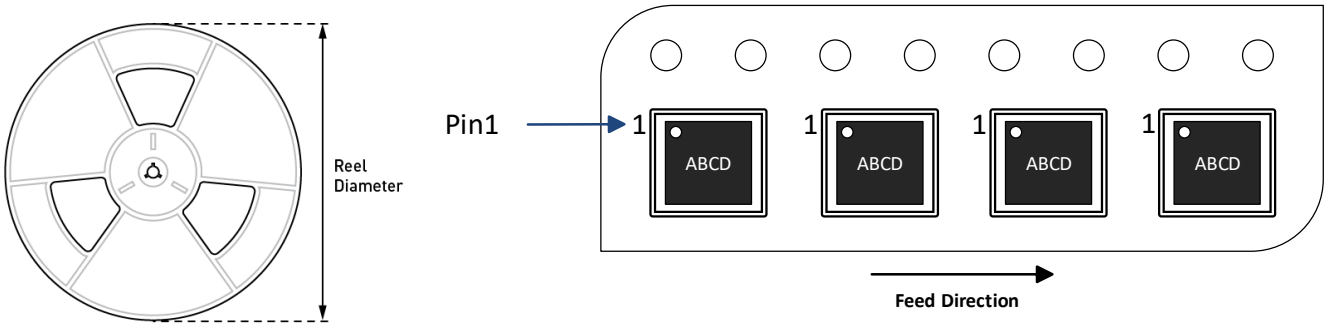
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP5491GC-xxxx-Z	WLCSP-36 (3mmx4.25mm)	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/29/2024	Initial Release	-

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