MP5099E

Dual-Channel Current-Limit Switch with Current Monitor and SATAIG Control

DESCRIPTION

The MP5099E is a protection device that protects circuitry on the output from transients on the input. It also prevents undesired shorts at the input and transients from the output. The MP5099E is a small on resistance ($R_{DS(ON)}$), low quiescent current (I_Q), dual-channel current-limit switch.

At start-up, the inrush current is limited by the slew rate at the output. The slew rate is controlled by a capacitor at the SS pin (C_{SS}). The maximum load at the output is current-limited. The current limit magnitude is fixed internally.

The output voltage (V_{OUT}) is limited by the over-voltage protection (OVP) function. The output current (I_{OUT}) of each rail can be monitored by a resistor connected to the IMON pins.

The device is available in a space-saving TQFN-10 (2mmx3mm) package.

FEATURES

- Integrated 5V/12V Input Dual E-Fuse
- 24V/100ms Maximum Surge Input Voltage (V_{IN1}) Tolerance for 12V Bus (Channel 1)
- 16V/100ms Maximum Surge V_{IN2} Tolerance for 5V Bus (Channel 2)
- Integrated Dual-Channel Current-Limit Switch
- 40mΩ/40mΩ Low On Resistance ($R_{DS(ON)}$) for Channel 1/2 Current-Limit Switch
- 316μA/355μA Typical Low Quiescent Current (I_Q) for Channel 1/2
- Configurable Soft-Start Time (t_{SS})
- Fixed 4A/2.95A Trip/Hold Current Limit for Channel 1
- Fixed 3A/2.2A Trip/Hold Current Limit for Channel 2
- Reverse Current Protection for Channel 2
- 5.7V Typical Over-Voltage Protection (OVP) Threshold for Channel 2
- 15V Typical OVP Threshold for Channel 1
- Over-Current Protection (OCP) with Hiccup Mode
- Thermal Shutdown with Hiccup Mode
- Available in a TQFN-10 (2mmx3mm) Package

APPLICATIONS

- Hard Disk Drives (HDDs)
- Solid-State Drives (SSDs)
- Hot-Swap Applications

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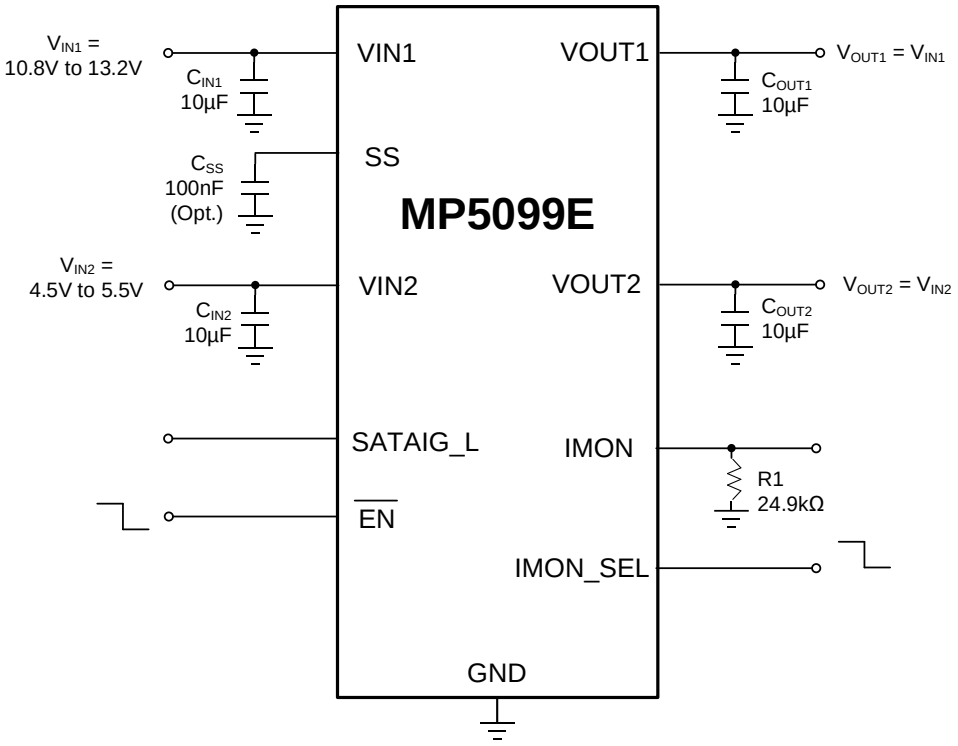
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP5099EGDT	TQFN-10 (2mmx3mm)	*See Below*	1

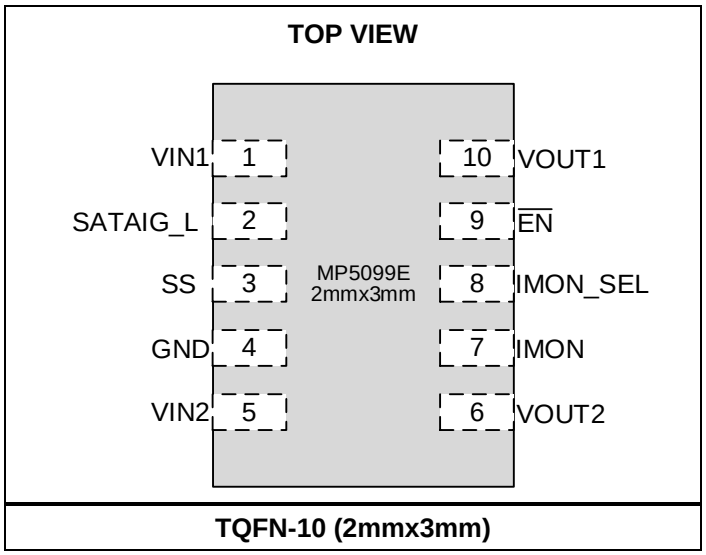
* For Tape & Reel, add suffix -Z (e.g. MP5099EGDT-Z).

TOP MARKING

$\overline{\text{BXD}}$
YWW
LLLL

BXD: Product code of MP5099EGDT
Y: Year code
WW: Week code
LLLL: Lot number

PACKAGE REFERENCE



TQFN-10 (2mmx3mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	VIN1	**Channel 1 supply voltage.** The typical input voltage of channel 1 (V_{IN1}) is 12V. A ceramic capacitor is required to decouple the input rail. Connect VIN1 using a wide PCB trace.
2	SATAIG_L	**EN logic control pin.** The EN input is ignored when SATAIG_L is low; the EN input is effective when SATAIG_L is high or floating. Once SATAIG_L is high, it is latched. This latch is cleared if either V_{IN1} or V_{IN2} under-voltage lockout (UVLO) occurs.
3	SS	**Channel 1 soft start pin.** Connect a capacitor from SS to ground to set the soft-start time (t_{SS}).
4	GND	**System ground.**
5	VIN2	**Channel 2 supply voltage.** The typical input voltage of channel 2 (V_{IN2}) is 5V. A ceramic capacitor is required to decouple the input rail. Connect VIN2 using a wide PCB trace.
6	VOUT2	**Channel 2 output terminal.**
7	IMON	**Current monitor pin.** Connect a resistor from IMON1 to ground to set the current monitor gain.
8	IMON_SEL	**Current monitor channel selection pin.** If IMON_SEL is driven high, IMON detects the channel 1 output current (I_{OUT1}). If IMON_SEL is floated or driven low, IMON detects the channel 2 output current (I_{OUT2}).
9	$\overline{EN}$	**Enable pin for both channel 1 and channel 2.** $\overline{EN}$ is a digital input that turns the regulator on or off. Float $\overline{EN}$ or drive $\overline{EN}$ low to turn on the regulator; drive it high to turn off the regulator.
10	VOUT1	**Channel 1 output terminal.**

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN1}, V_{OUT1} .....-0.3V to +22V
Input positive transient (CH1: 100ms)..... 24V
V_{IN2}, V_{OUT2} .....-0.3V to +15V
Input positive transient (CH2: 100ms)..... 16V
EN .....-0.3V to +6.5V
All other pins .....-0.3V to +5V
Junction temperature (T_J) ..... -40°C to +150°C
Lead temperature .....260°C
Continuous power dissipation (T_A = 25°C) (2) (4)
TQFN 3.1W

Recommended Operating Conditions (3)

CH1 continuous voltage.....10.2V to 14.5V
CH2 continuous voltage.....4.6V to 5.5V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

TQFN-10 (2mmx3mm)
EV5099E-D-00A (4) ..... 40 ..... 4.... °C/W
JESD51-7 (5) ..... 70 ..... 5.... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on the EV5099E-D-00A, a 2-layer PCB, 54mmx46mm.
5) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

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ELECTRICAL CHARACTERISTICS

V_{IN1} = 12V, V_{IN2} = 5V, C_{OUT1} = C_{OUT2} = 10µF, T_J = -40°C to + 125°C (6), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Quiescent current	I_{Q_CH1}	$V_{\overline{EN}}$ = low		316		µA
	I_{Q_CH2}	$V_{\overline{EN}}$ = low		355		µA
Shutdown current	I_{SD_CH1}	$V_{\overline{EN}}$ = high		33		µA
	I_{SD_CH2}	$V_{\overline{EN}}$ = high		69		µA
Power FET						
On resistance	$R_{DS(ON)_CH1}$	T_J = 25°C		40		mΩ
		T_J = 125°C			65	mΩ
	$R_{DS(ON)_CH2}$	T_J = 25°C		40		mΩ
		T_J = 125°C			65	mΩ
Under-Voltage Protection (UVP) and Over-Voltage Protection (OVP)						
Under-voltage lockout (UVLO) rising threshold	V_{UVLO_CH1}		7.7	8.5	9.3	V
	V_{UVLO_CH2}		3.8	4.0	4.2	V
UVLO hysteresis	$V_{UVLOHYS_CH1}$			800		mV
	$V_{UVLOHYS_CH2}$			0.3		V
Output OV clamp voltage	V_{OVLO_CH1}		13.8	15	16	V
	V_{OVLO_CH2}		5.5	5.7	6.2	V
Output OV response time (7)	$t_{OUT_OV_CH1}$	C_{OUT} = 10µF, add 30Ω load resistor, V_{IN1} = 12V to 18V/10µs		2		µs
	$t_{OUT_OV_CH2}$	C_{OUT} = 10µF, add 10Ω load resistor, V_{IN2} = 5V to 7V/10µs		2		µs
Current Limit						
Current limit at normal operation	$I_{LIMIT_NO_CH1_TRIP}$		-10%	4	+10%	A
	$I_{LIMIT_NO_CH2_TRIP}$		-10%	3	+10%	A
	$I_{LIMIT_SC_CH1_HOLD}$			2.95		A
	$I_{LIMIT_SC_CH2_HOLD}$			2.2		A
Current limit response time (7)	t_{CL_CH1}			15		µs
	t_{CL_CH2}			15		µs
Secondary current limit (7)	I_{LIMITH_CH1}			8		A
	I_{LIMITH_CH2}			8		A
Hiccup mode on time	t_{HICP_ON}			2		ms
Hiccup mode off time	$t_{HICP\ OFF}$			200		ms
Reverse current threshold	$I_{LIMIT_RC_CH2}$	T_J = 25°C, V_{OUT2} = 4.5V to 5.5V	0.9		1.7	A
Reverse current response time (7) (8)	$t_{REV_RESPONSE}$	V_{OUT2} = 5V, V_{IN2} dV/dt = -50mV/µs			12	µs

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN1} = 12V, V_{IN2} = 5V, C_{OUT1} = C_{OUT2} = 10µF, T_J = -40°C to + 125°C (6), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Current Monitor						
Current monitor sense gain	G_{IMON_CH1}		24.5	27	29.5	µA/A
	G_{IMON_CH2}		26	28.5	31	µA/A
Current monitor sense offset	I_{OFFSET_CH1}	I_{OUT1} = 0A		2.5		µA
	I_{OFFSET_CH2}	I_{OUT2} = 0A		1.7		µA
Current monitor voltage range (7)	V_{IMON}		0		2.65	V
Enable (EN) Control						
$\overline{EN}$ rising threshold	$V_{\overline{EN}_RISING}$		1.2	1.3	1.4	V
$\overline{EN}$ falling threshold	$V_{\overline{EN}_FALLING}$		1	1.1	1.2	V
$\overline{EN}$ pull-down resistance	$R_{\overline{EN}_PD}$			0.3		MΩ
SATAIG_L Control						
SATAIG_L rising threshold	$V_{SATAIG_L_R}$		1.1	1.2	1.3	V
SATAIG_L falling threshold	$V_{SATAIG_L_F}$		0.8	0.9	1	V
Soft Start (SS)						
SS current	I_{SS_CH1}		3.6	4.8	7	µA
SS time	t_{SS}	SS pin floating, V_{OUT1} 10% to 90%		12		ms
Over-Temperature Protection (OTP)						
Thermal shutdown (7)	T_{SD}			150		°C
Thermal shutdown hysteresis (7)	T_{SDHYS_CH1}			25		°C
	T_{SDHYS_CH2}			25		°C

Notes:

6) Not tested in production. Guaranteed by over-temperature correlation.
7) Guaranteed by design or engineering sample characterization.
8) The response time is defined as the time interval from triggering the reverse current threshold to when the reverse MOSFET completely turns off.

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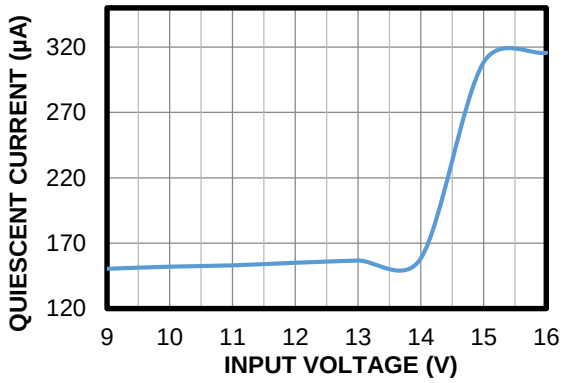
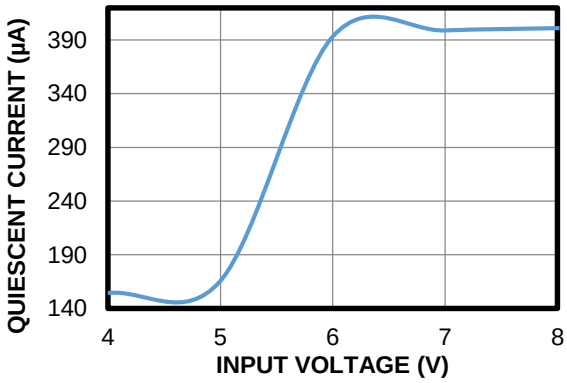
TYPICAL CHARACTERISTICS

V_{IN1} = 12V, V_{IN2} = 5V, T_A = 25°C, unless otherwise noted.

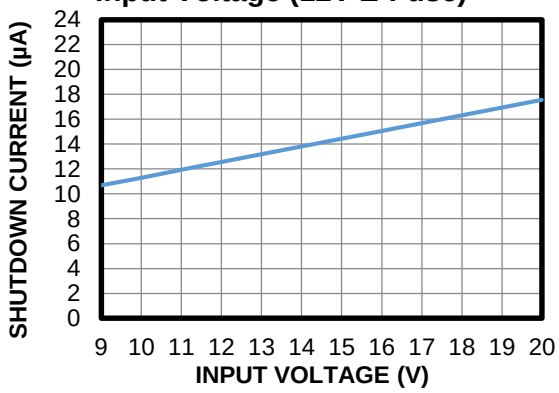
Quiescent Current vs. Input Voltage (12V E-Fuse)



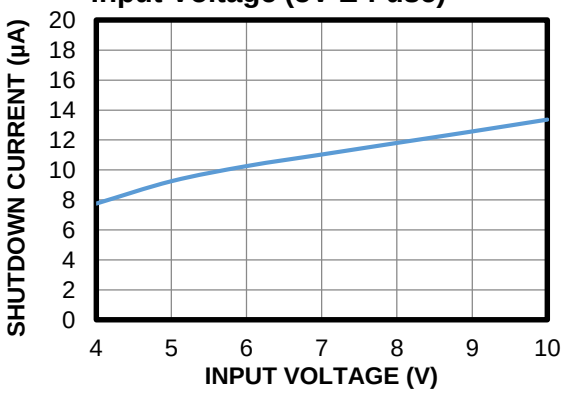
Quiescent Current vs. Input Voltage (5V E-Fuse)



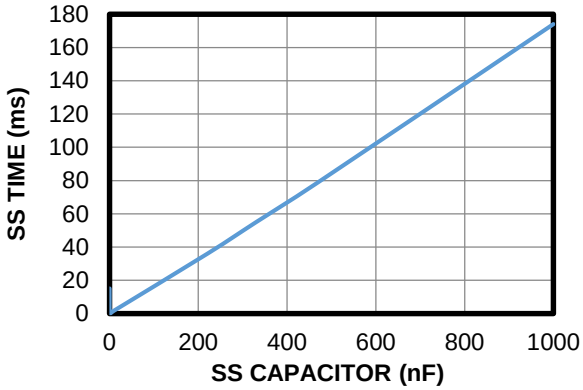
Shutdown Current vs. Input Voltage (12V E-Fuse)



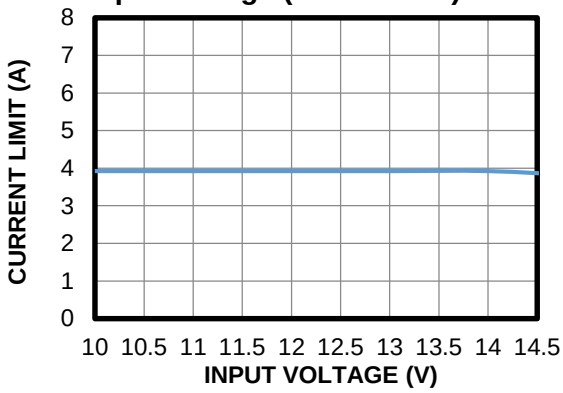
Shutdown Current vs. Input Voltage (5V E-Fuse)



SS Time vs. SS Capacitor (12V E-Fuse)



Current Limit vs. Input Voltage (12V E-Fuse)



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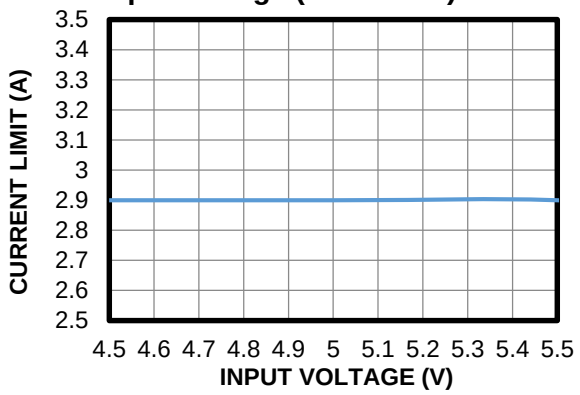
TYPICAL CHARACTERISTICS *(continued)*

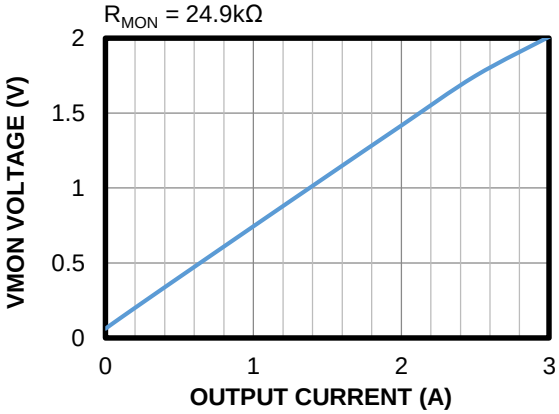
V_{IN1} = 12V, V_{IN2} = 5V, T_A = 25°C, unless otherwise noted.

Current Limit vs. Input Voltage (5V E-Fuse)



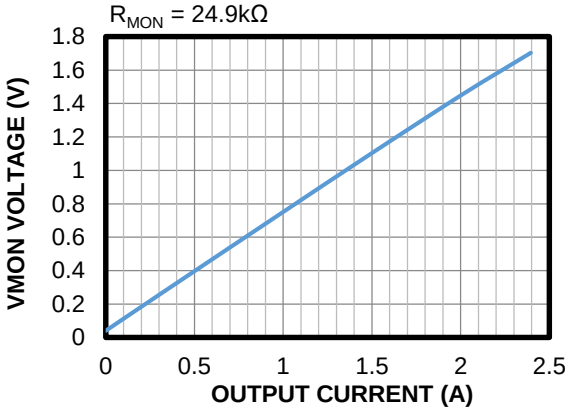
VMON Voltage vs. Output Current (12V E-Fuse)

R_{MON} = 24.9kΩ



VMON Voltage vs. Output Current (5V E-Fuse)

R_{MON} = 24.9kΩ



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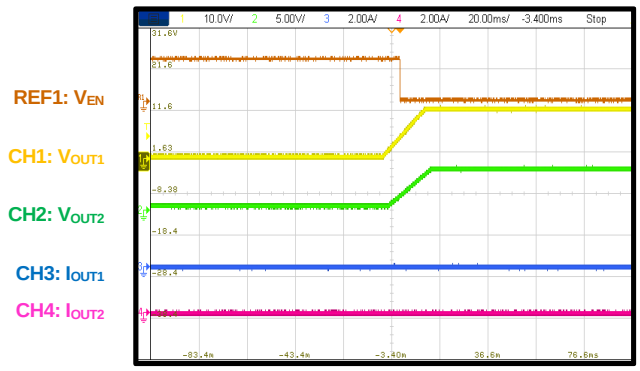
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN1} = 12V, V_{IN2} = 5V, T_A = 25°C, unless otherwise noted.

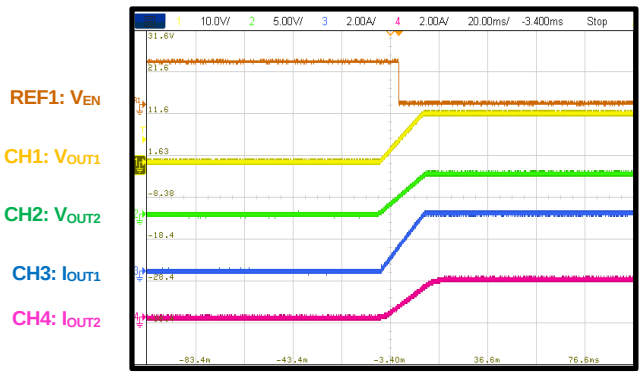
CH1/CH2 EN On Logic

I_{OUT1} = I_{OUT2} = 0A



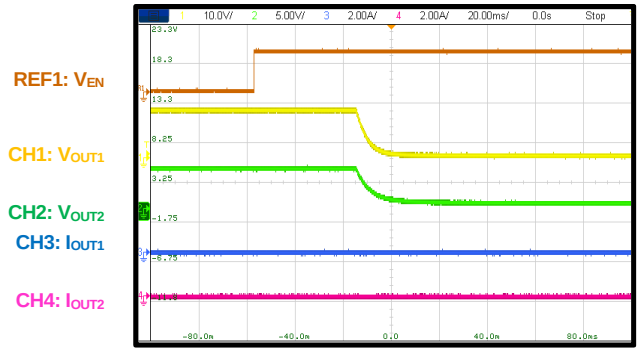
CH1/CH2 EN On Logic

I_{OUT1} =3A, I_{OUT2} = 2A



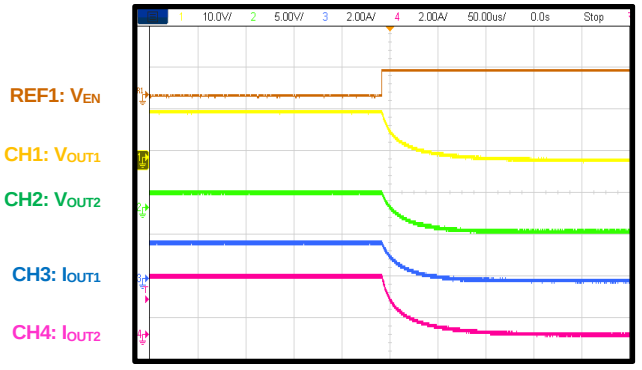
CH1/CH2 EN Off Logic

I_{OUT1} = I_{OUT2} = 0A



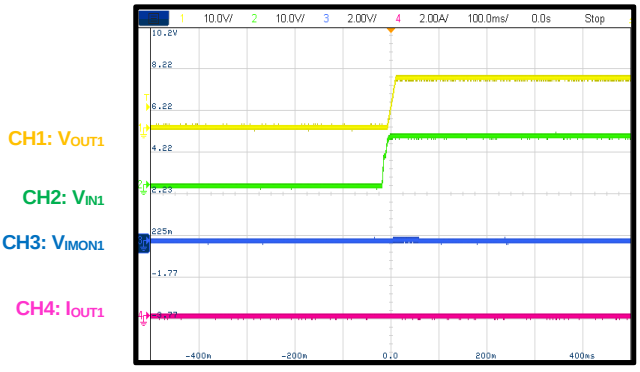
CH1/CH2 EN Off Logic

I_{OUT1} =3A, I_{OUT2} = 2A



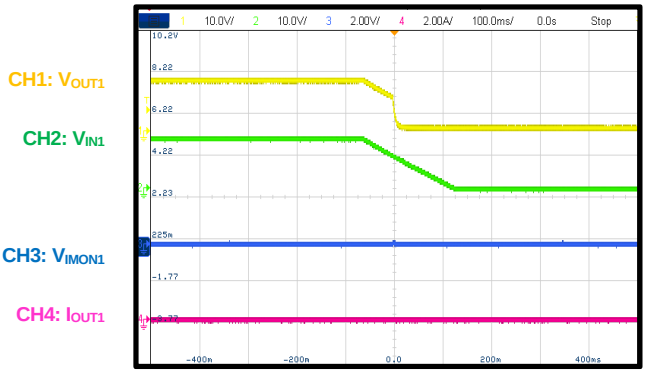
VIN1 Start-Up without Load (12V E-Fuse)

V_{IN2} = 5V, I_{OUT1} = 0A



VIN1 Shutdown without Load (12V E-Fuse)

V_{IN2} = 5V, I_{OUT1} = 0A



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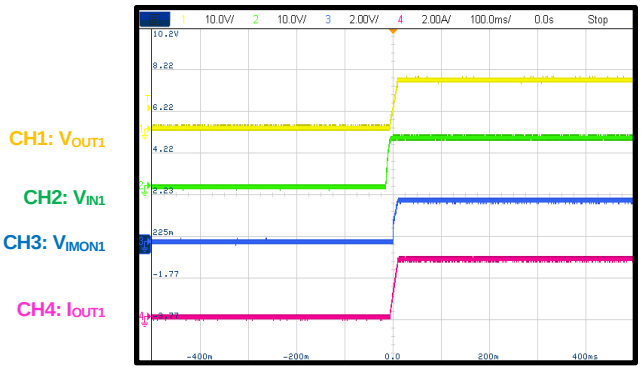
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN1} = 12V, V_{IN2} = 5V, T_A = 25°C, unless otherwise noted.

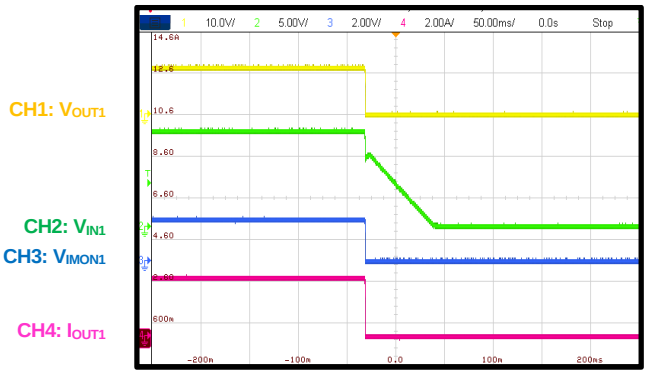
VIN1 Start-Up with 3A Load (12V E-Fuse)

I_{OUT1} = 3A, V_{IN2} = 5V



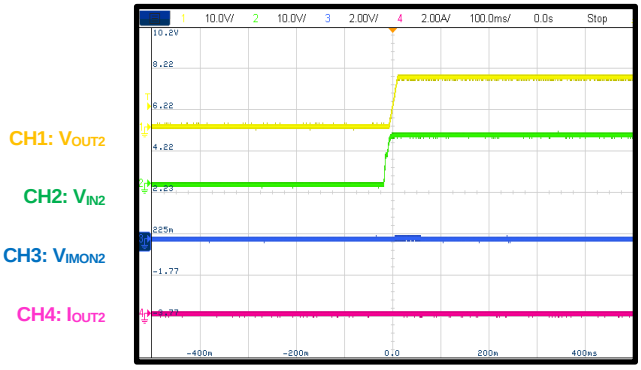
VIN1 Shutdown with 3A Load (12V E-Fuse)

I_{OUT1} = 3A, V_{IN2} = 5V



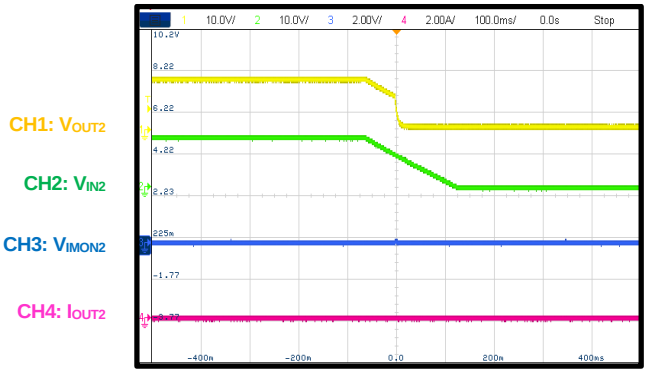
VIN2 Start-Up without Load (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 0A



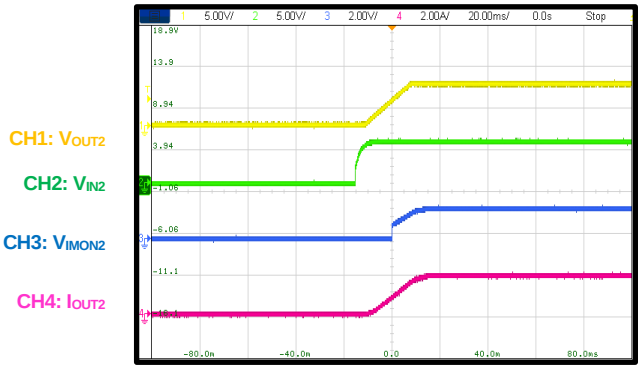
VIN2 Shutdown without Load (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 0A



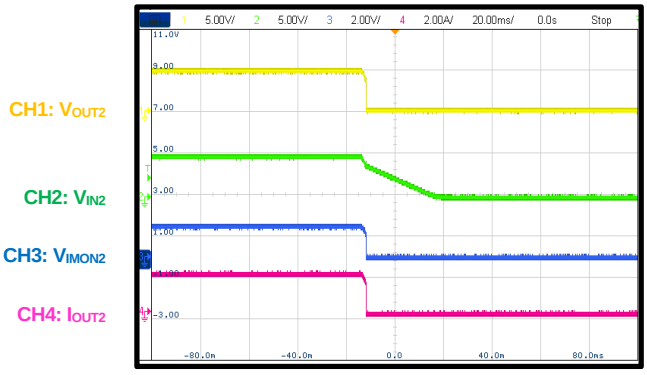
VIN2 Start-Up with 2A Load (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 2A



VIN2 Shutdown with 2A Load (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 2A



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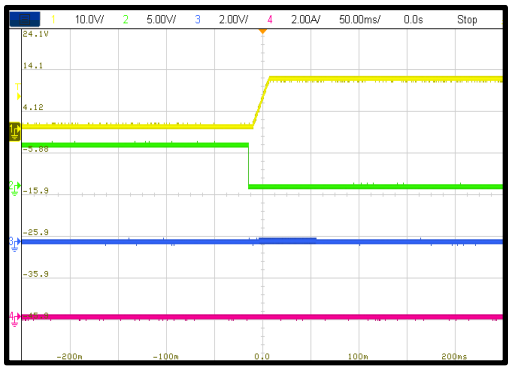
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN1} = 12V, V_{IN2} = 5V, T_A = 25°C, unless otherwise noted.

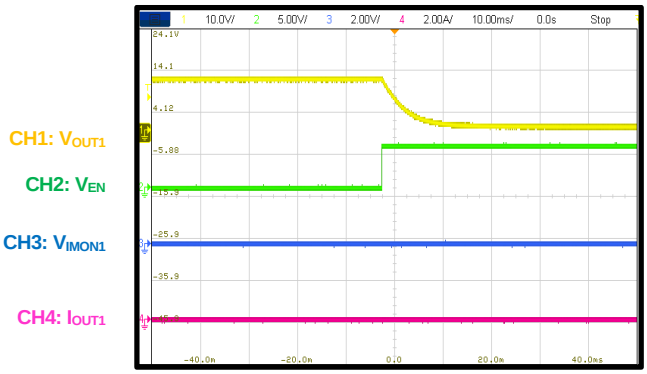
EN Start-Up without Load (12V E-Fuse)

V_{IN2} = 5V, I_{OUT1} = 0A



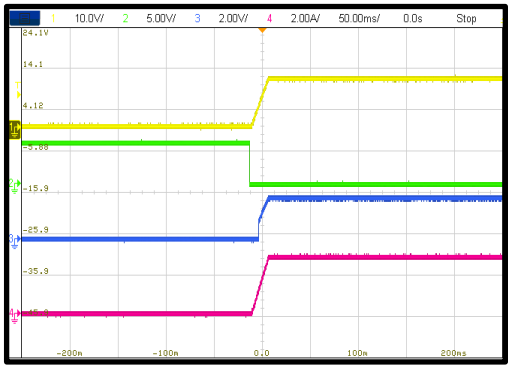
EN Shutdown without Load (12V E-Fuse)

V_{IN2} = 5V, I_{OUT1} = 0A



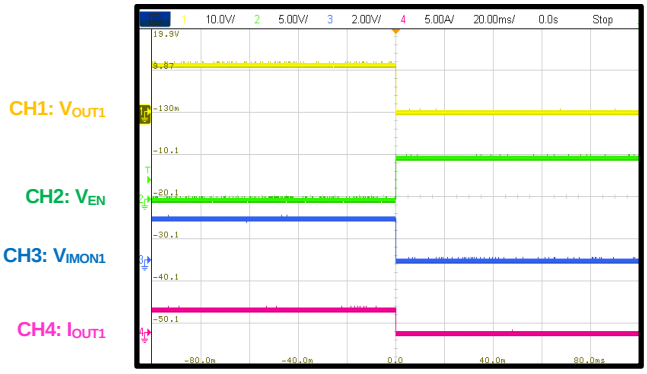
EN Start-Up with 3A Load (12V E-Fuse)

V_{IN2} = 5V, I_{OUT1} = 3A



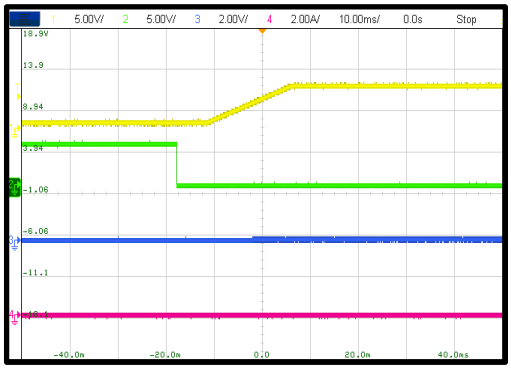
EN Shutdown with 3A Load (12V E-Fuse)

V_{IN2} = 5V, I_{OUT1} = 3A



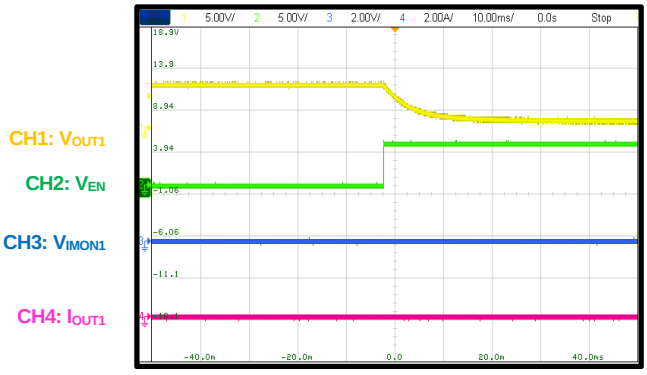
EN Start-Up without Load (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 0A



EN Shutdown without Load (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 0A



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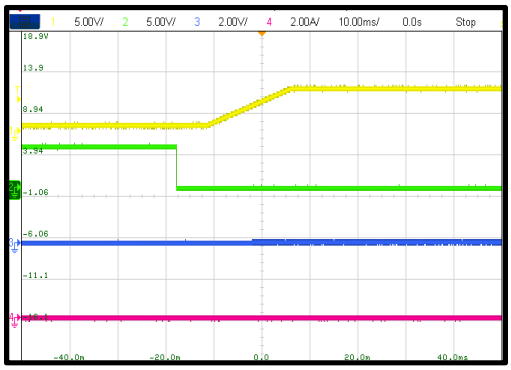
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN1} = 12V, V_{IN2} = 5V, T_A = 25°C, unless otherwise noted.

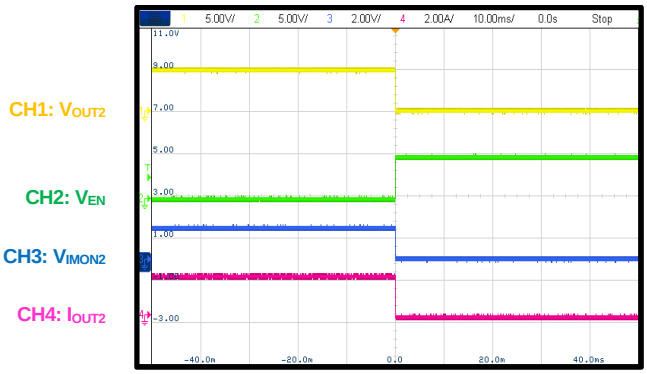
EN Start-Up with 2A Load (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 2A

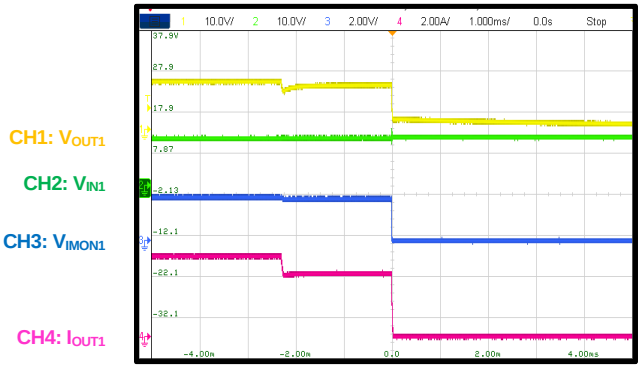


EN Shutdown with 2A Load (5V E-Fuse)

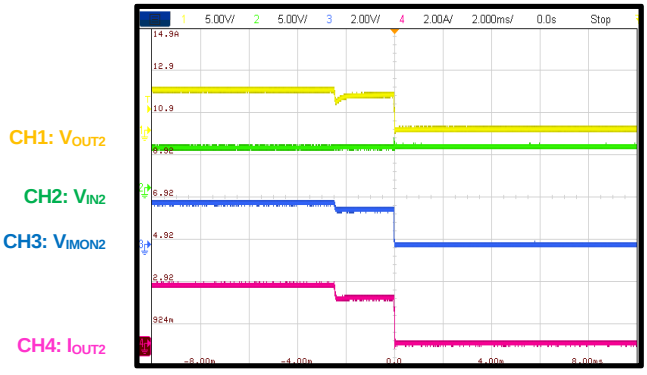
V_{IN1} = 12V, I_{OUT2} = 2A



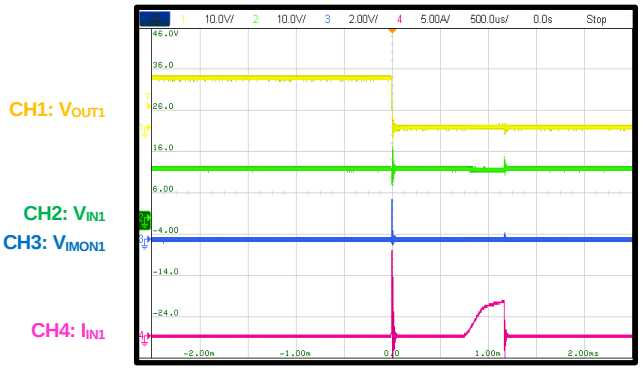
Current Limit (12V E-Fuse)



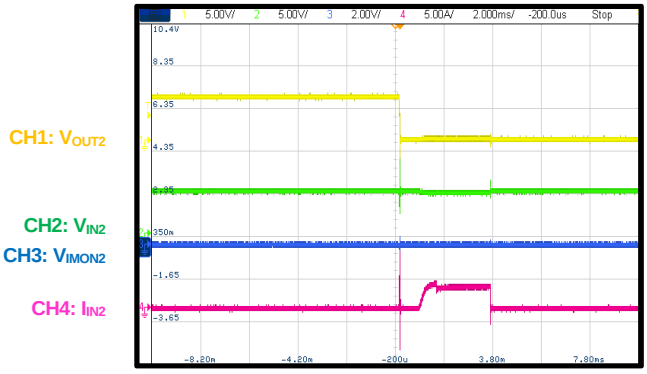
Current Limit (5V E-Fuse)



Short-Circuit Entry (12V E-Fuse)



Short-Circuit Entry (5V E-Fuse)



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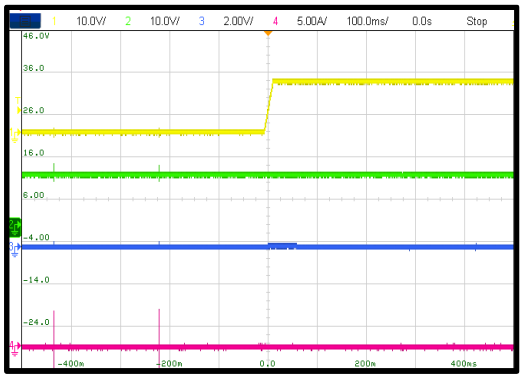
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN1} = 12V, V_{IN2} = 5V, T_A = 25°C, unless otherwise noted.

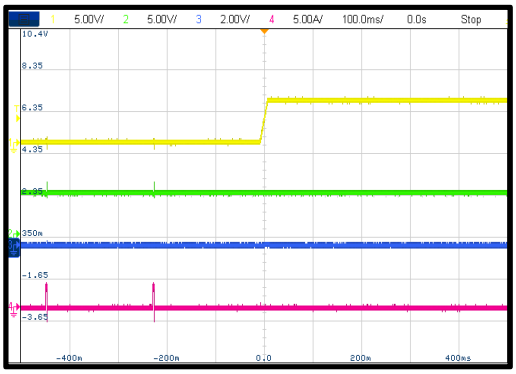
Short-Circuit Recovery (12V E-Fuse)

CH1: V_{OUT1}
CH2: V_{IN1}
CH3: V_{IMON1}
CH4: I_{IN1}



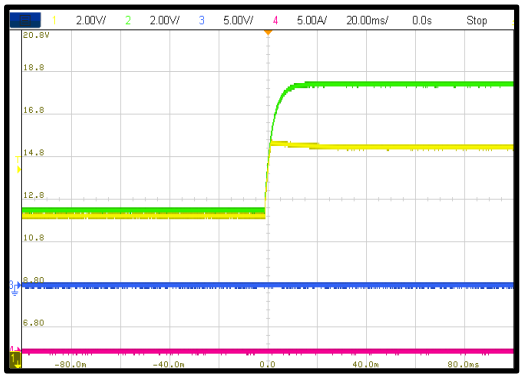
Short-Circuit Recovery (5V E-Fuse)

CH1: V_{OUT2}
CH2: V_{IN2}
CH3: V_{IMON2}
CH4: I_{IN2}



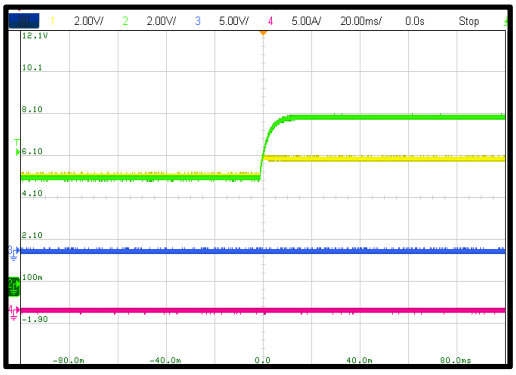
Output Over-Voltage Protection (12V E-Fuse)

CH2: V_{IN1}
CH3: V_{IMON1}
CH4: I_{OUT1}
CH1: V_{OUT1}



Output Over-Voltage Protection (5V E-Fuse)

CH1: V_{OUT2}
CH3: V_{IMON2}
CH2: V_{IN2}
CH4: I_{OUT2}



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FUNCTIONAL BLOCK DIAGRAM

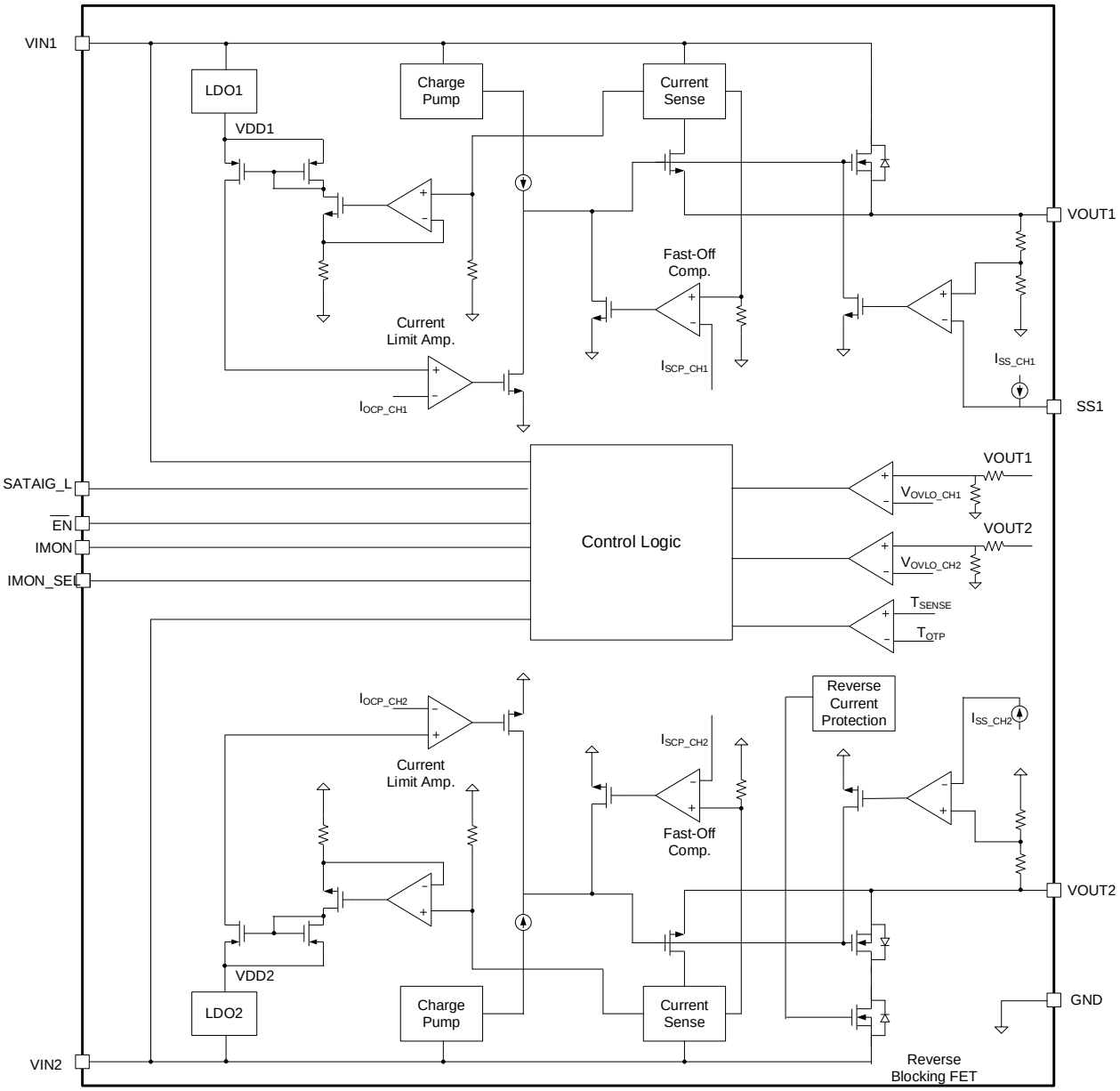

Figure 1: Functional Block Diagram

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OPERATION

The MP5099E is a dual-channel current-limit switch that limits the inrush current to the load when a circuit card inserts into a live backplane power source. This limits the backplane's voltage drop as well as the dV/dt of the voltage to the load. It offers an integrated solution to monitor the input voltage ($V_{IN1/2}$), output voltage ($V_{OUT1/2}$), output current ($I_{OUT1/2}$), and die temperature, eliminating the requirement of an external current-sense power resistor, power MOSFET, and thermal sense device.

The MP5099E employs a reverse current block function for the 5V channel (channel 2). If channel 2's reverse current reaches the reverse protection current threshold, then only channel 2 turns off.

Under-Voltage Lockout (UVLO)

The MP5099E's channel 1 can be used in the 12V input supply system, and channel 2 can be used in the 5V input supply system. High energy transients occur during normal operation or during hot swaps. These transients depend on the parasitic inductance and resistance of the wire, as well as a capacitor at the VCC node. If a power clamp (e.g. TVS or TransZorb) diode is not used, then the e-fuse must be able to withstand the transient voltage. The MP5099E integrates a high-voltage MOSFET and also uses a high-voltage circuit for the VCC node to guarantee safe operation.

If each channel's input supply falls below the under-voltage lockout (UVLO) threshold, then both channels' outputs shut down. Once both supplies exceed their UVLO thresholds, the output of the two channels are enabled.

Soft Start (SS)

Connect a capacitor to the SS pin to set channel 1's soft-start time (t_{SS}). A constant current source charges the SS capacitor (C_{SS}), which results in a linear ramping voltage on the SS pin. Channel 1's output voltage (V_{OUT1}) rises at a similar slew rate to the SS voltage (V_{SS}).

t_{SS} is a function of C_{SS}. The soft-start time from 0% to 100% V_{OUT} ($t_{DV/DT}$) can be calculated with Equation (1):

$$t_{DV/DT}(ms) = \frac{1V \times C_{SS}(nF)}{I_{SS}} \quad (1)$$

Where I_{SS} is the soft-start current, and 1V is the internal reference voltage (V_{REF}). Once the SS pin is charged up to 1V, soft start finishes.

When floating the SS pin, the default t_{SS} is typically 12ms.

Fast Output Over-Voltage Protection (OVP)

To protect downstream loading when a surge voltage occurs at the input, the MP5099E provides output over-voltage protection (OVP). An accurate and fast comparator monitors the output's over-voltage (OV) condition. If $V_{OUT1/2}$ exceeds the threshold, the internal MOSFETs' gate is quickly pulled down and regulated to a set value to clamp $V_{OUT1/2}$ at the OVP threshold. The fast loop response speed (2µs typically) minimizes the OV overshoot.

Current Limit

When the MP5099E is active, if each load reaches the trip current threshold (the current triggers over-current protection) or a short is present, then both channels' outputs shut down and the part switches to constant-current (hold current) mode. If the over-current (OC) condition remains for longer than 2ms, the MP5099E enters hiccup protection mode. The IC automatically restarts after a 200ms off time and repeats this operation until the OC condition is removed.

Channel 1's trip current is set to 4A internally, and its hold current is 2.95A. Channel 2's trip current is set to 3A internally, and its hold current is 2.2A.

Channel 2 has reverse current protection. If the channel 2's reverse current reaches the reverse current protection threshold, only channel 2 turns off. It recovers after $V_{IN2} > V_{OUT2} + 200mV$ (V_{OUT2} is between 4.5V and 5.5V).

Current Monitor

The MP5099E provides current monitoring for channel 1 and channel 2. The MP5099E has an IMON_SEL pin that selects the output current monitor channel. Drive IMON_SEL high to monitor channel 1's output current (IOUT1); float or drive this pin low to monitor channel 2's output current (I_{OUT2}).

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The IMON pin generates a current proportional to channel 1 and channel 2's load current. Connect a resistor (R_{IMON}) to IMON to generate the current monitor voltage ($V_{IMON1/2}$). The effective $V_{IMON1/2}$ range (between 0V and 2.65V) guarantees sensing linearity. $V_{IMON1/2}$ depends on the R_{IMON} value, and $V_{IMON1/2}$ is clamped when $I_{OUT1/2}$ exceeds a set value, respectively.

Table 1 shows the recommended IMON resistances for common IMON clamp voltages. When R_{IMON} = 24.9kΩ, the V_{IMON1} clamping voltage is 2.15V, and the V_{IMON2} clamping voltage is typically 1.88V.

Table 1: IMON Resistor Selection for Common IMON Clamp Voltages

V_{CLAMP1} (V)	V_{CLAMP2} (V)	R_{IMON} (kΩ)
2.1	1.8	24.9 (1%)

V_{IMON} can be calculated with Equation (2):

$$V_{IMONX}(mV) = G_{IMON_CHX}(\mu A/A) \times I_{OUT}(A) \times R_{IMON}(k\Omega) + I_{OFFSET_CHX}(\mu A) \times R_{IMON}(k\Omega) \quad (2)$$

Where G_{IMON_CHx} is the current monitor sense gain, R_{IMON} is the current monitor sense resistor, and I_{OFFSET_CHx} is the current monitor sense offset. x = 1 or 2, depending on the channel.

Short-Circuit Protection (SCP)

If the load current increases rapidly due to a short-circuit event, the current may exceed the current limit threshold before the control loop is able to respond. If the current reaches a secondary current limit level of 8A, a fast turn-off circuit activates to turn off the power FET (see Figure 1 on page 14). The fast turn-off circuit helps limit the peak current through the switch, which prevents V_{IN} from dropping drastically.

The total short circuit response time is shorter than 1µs. After the FET switches off, the part restarts. During the restart process, if the short still exists, the MP5099E regulates the gate voltage to hold the current at a normal current limit level. The IC enters hiccup mode with a 200ms off time.

Enable ($\overline{EN}$) Control

$\overline{EN}$ is a digital control pin that turns the current limit switch on and off. Pull $\overline{EN}$ low or float $\overline{EN}$ to turn on the FETs; pull $\overline{EN}$ high to turn off the FETs. An internal 800kΩ resistor is connected from $\overline{EN}$ to GND.

SATAIG_L Control

SATAIG_L is a digital control pin that activates the EN signal. When SATAIG_L is low, the EN input is ignored; when SATAIG_L is high or floating, the EN input is active.

SATAIG_L latches after it goes high. The SATAIG_L can only be cleared from its latched state after V_{IN1} or V_{IN2} UVLO is triggered.

Thermal Shutdown

The MP5099E monitors the die temperature internally to prevent the IC from operating at exceedingly high temperatures. If the die temperature exceeds the thermal shutdown threshold (typically 150°C), then both channels shut down. Once the temperature drops below about 125°C, both channels resume normal operation.

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APPLICATION INFORMATION

Setting the Soft-Start Time (t_{SS})

The soft-start time from 0% to 100% V_{OUT} ($t_{DV/DT}$) can be calculated with Equation (3):

$$t_{DV/DT}(ms) = \frac{1V \times C_{SS}(nF)}{I_{SS}} \quad (3)$$

Where I_{SS} is the soft-start current, and 1V is the internal reference voltage (V_{REF}).

Design Example

Table 2 shows a design example following the application guidelines for certain specifications.

Table 2: Design Example

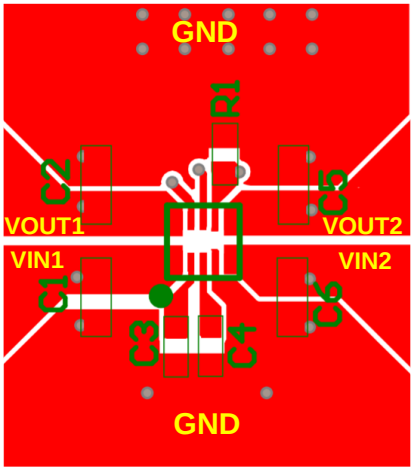
V_{IN1}	12V
V_{OUT1}	12V
V_{IN2}	5V
V_{OUT2}	5V

Figure 3 on page 18 shows the detailed application circuit. For the typical performance and waveforms, see the Typical Characteristics Section starting on page 7. For more device applications, refer to the related evaluation board datasheet.

PCB Layout Guidelines

The PCB layout is vital for improved performance. For the best results, refer to Figure 2 and follow the guidelines below:

1. Place the high-current paths (VINx and VOUTx) close to the device using short, direct, and wide traces.
2. Place the input capacitors close to the VIN and GND pins.
3. To improve thermal performance, connect the VINx and VOUTx pads to the large VINx and VOUTx planes, respectively.
4. Place the SS capacitor close to the SS pin.



Top Layer

Figure 2: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUIT

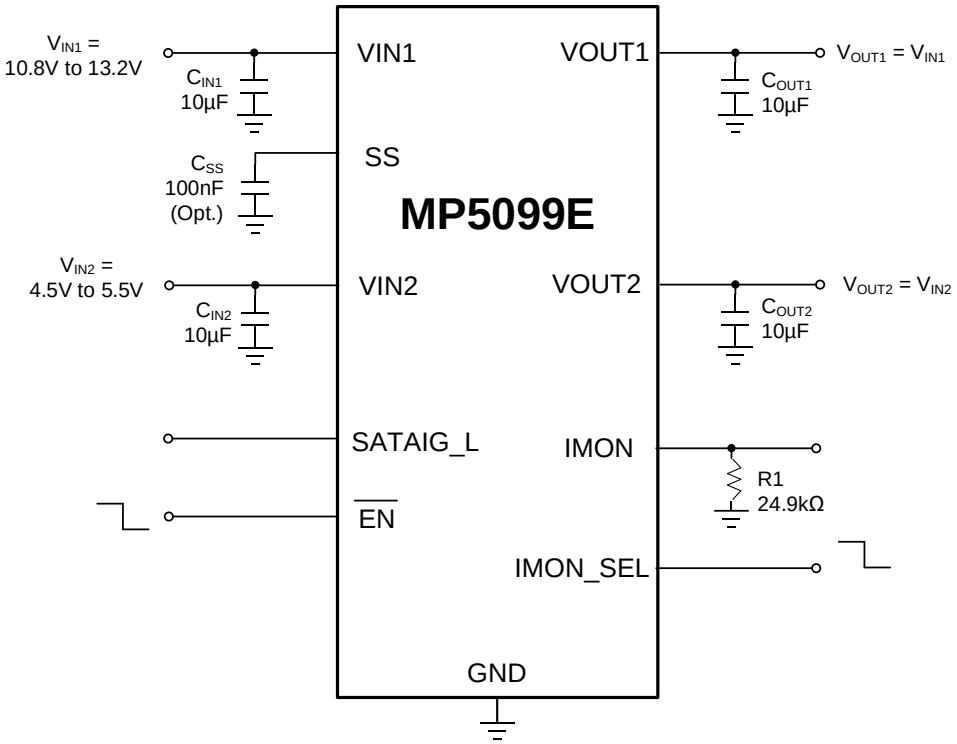

Figure 3: Typical Application Circuit

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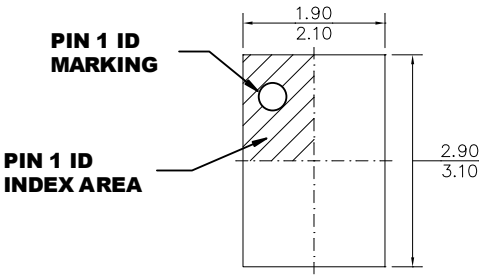
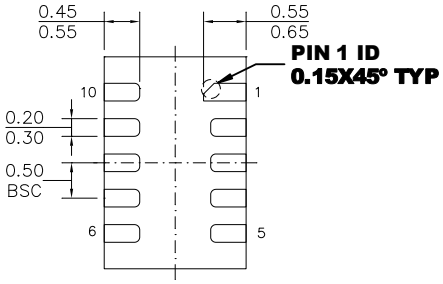
PACKAGE INFORMATION

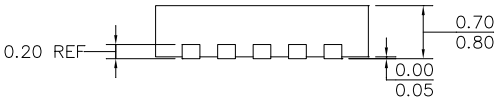
TQFN-10 (2mmx3mm)



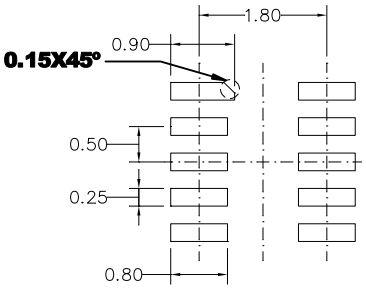
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

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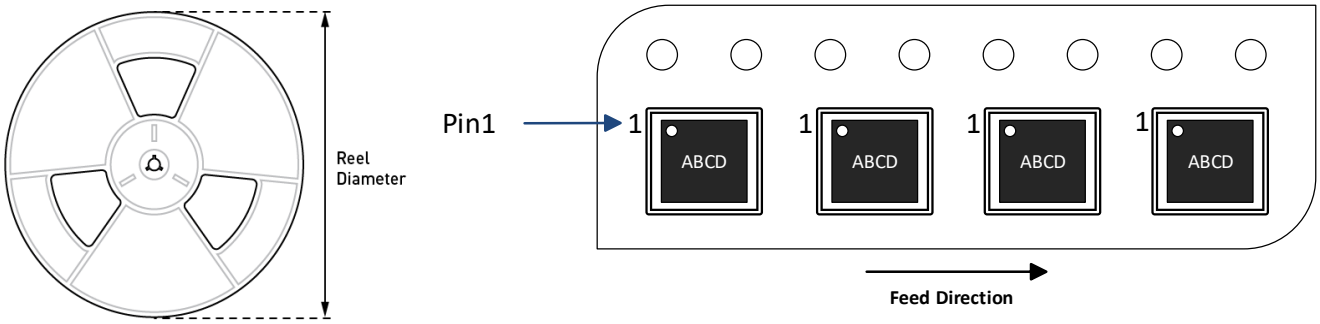
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP5099EGDT-Z	TQFN-10 (2mmx3mm)	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	12/16/2024	Initial Release	-

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