MP5092

Dual 5.5V, 7.5A Programmable Current Low R_{DSON} Load Switch with Output Discharge Function

The Future of Analog IC Technology

DESCRIPTION

The MP5092 integrated a dual load switches to provide load protection covering 0.5V to 5.5V voltage range. Any one channel can work alone. Each channel can provide 7.5A load capability. With the small R_{DSON} in tiny package, MP5092 provides very high efficient and space saving solution in notebook and tablet or other portable devices applications.

With the soft start function, the MP5092 can avoid inrush current during circuit start up. MP5092 also provides different functions, like programmable soft start time, output discharge functions, OCP and thermal shutdown features.

The max load at the output (source) is current limited. This is accomplished by utilizing a sense FET topology. The magnitude of the current limit is controlled by an external resistor from ILIM pin to ground.

Tiny 18 pins QFN 2mmx3mm of MP5092 is available in space saving package.

FEATURES

- Integrated 10mΩ Low RDSON FETs
- Adjustable Start Up Slew Rate
- Wide VIN Range from 0.5V to 5.5V
- <1uA Shutdown Current
- Programmable 7.5A Current Limit Range
- Output Discharge Function
- Enable Pin
- <200ns Short-Circuitry Response Protection
- Thermal Protection
- Small QFN-18 (2mmx3mm) Package for Space Saving

APPLICATIONS

- Notebook and Tablet Computers
- Portable Devices
- Solid State Drivers
- Handheld Devices

All MPS parts are lead-free and adhere to the RoHS directive. For MPS green status, please visit MPS website under Products, Quality Assurance page.

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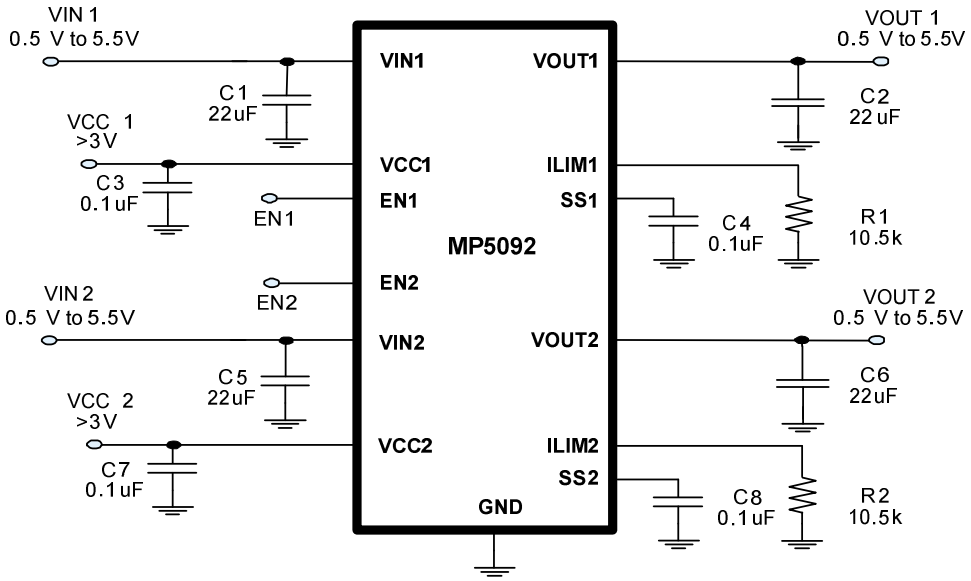
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP5092GD	QFN-18 (2mmx3mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP5092GD–Z);

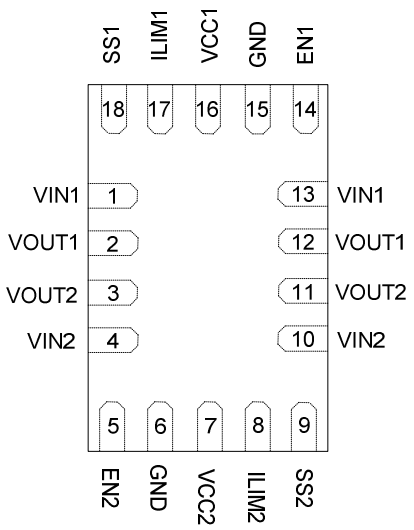
TOP MARKING

AKFY
LLL

AKF: product code of MP5092GD;
Y: year code;
LLL: lot number;

PACKAGE REFERENCE

TOP VIEW



QFN-18 (2mmx3mm)

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ABSOLUTE MAXIMUM RATINGS (1)

$V_{IN1/2}$ ..... –0.3V to +6.5V
$V_{CC1/2}$ ..... –0.3V to +6.5V
$V_{OUT1/2}$ ..... –0.3V to +6.5V
All Other Pins.....–0.3V to Vcc+0.3 V
Junction Temperature.....150°C
Lead Temperature .....260°C
Continuous Power Dissipation (2)
QFN18 (2mmx3mm) 1.8W

Recommended Operating Conditions (3)

Supply Voltage $V_{IN1/2}$..... 0.5V to 5.5V
Supply Voltage $V_{CC1/2}$..... 3V to 5.5V
Output Voltage $V_{OUT1/2}$..... 0.5V to 5.5V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4)	θ_{JA}	θ_{JC}	
QFN-18 (2mmx3mm) ……..….	70	15	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 3.6V, V_{CC} = 3.6V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input and Supply Voltage Range						
Input Voltage	V_{IN}		0.5		5.5	V
Supply Voltage	V_{CC}		3		5.5	V
Supply Current (Single Channel)						
Off State Leakage Current	I_{OFF}	V_{IN}=5V, EN=0			1	μA
V_{CC} Standby Current	I_{STBY}	V_{CC}=5V, EN=0		0.1	1	μA
		V_{CC}=5V, Enable, No load		220	330	
Power FET						
ON Resistance	R_{DSON}	V_{CC}=5.0V		10		mΩ
		V_{CC}=3.3V		12		
Thermal Shutdown and Recovery						
Shutdown Temperature(5)	T_{STD}			155		°C
Hysteresis(5)	T_{HYS}			30		°C
Under/Over Voltage Protection (Single Channel)						
V_{CC} Under Voltage Lockout Threshold	V_{CC_UVLO}	UVLO Rising Threshold		2.6	2.8	V
UVLO Hysteresis	$V_{UVLOHYS}$			200		mV
Soft Start						
SS pull-up current	I_{SS}	Fixed slew rate		9		μA
Enable						
EN Rising Threshold	V_{ENH}		1.3	1.5	1.7	V
EN Hysteresis	V_{ENHYS}			400		mV
ILIM						
Current limit(5)	I_{OUT}	R_{LIM}=10.5kΩ, rise Io, record its peak value		7.5		A
Current Limit Accuracy(6)		R_{LIM}=50kΩ	1.54	1.64	1.74	A
Discharge Resistance (Single Channel)						
Resistance	R_{DIS}			200		Ω

Notes:

5) Guarantee by characterization -Not production tested.

6) If sense current is smaller than 1.5A, the accuracy will be affected by some internal offset.

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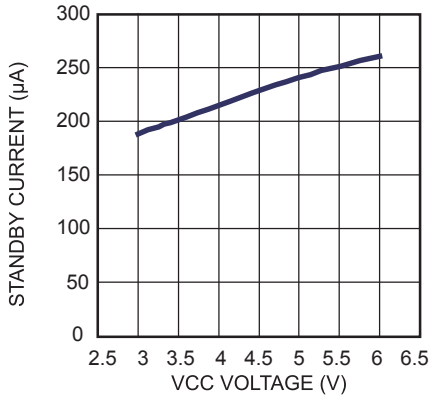
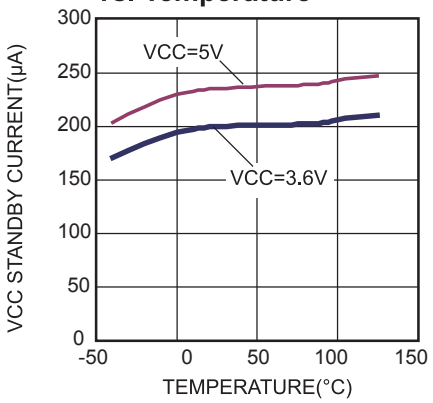
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.6V, V_{CC} = 3.6V, R_{LIM}=10.5k, T_A = 25°C, unless otherwise noted.

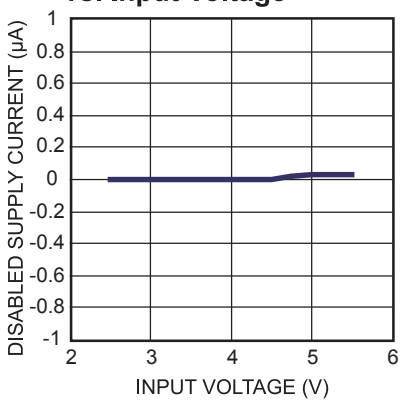
Vcc Standby Current vs. Vcc



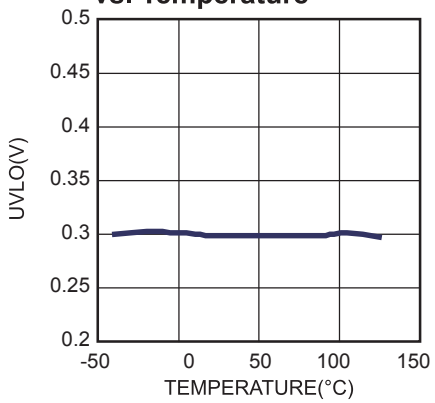
Vcc Standby Current vs. Temperature



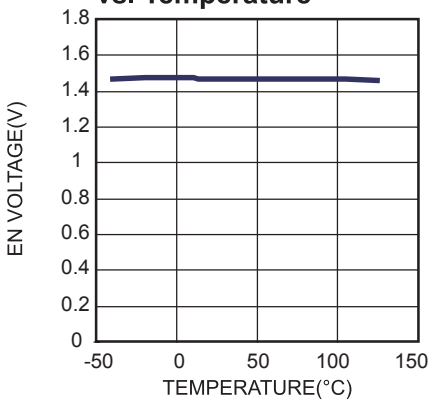
Disabled Supply Current vs. Input Voltage



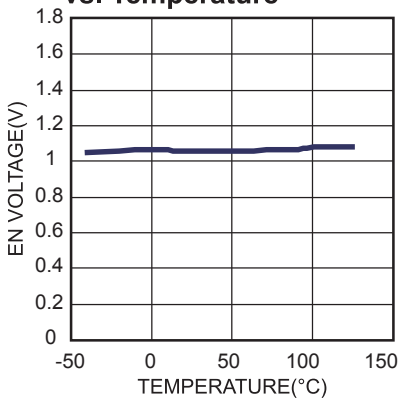
VIN UVLO Rising Threshold vs. Temperature



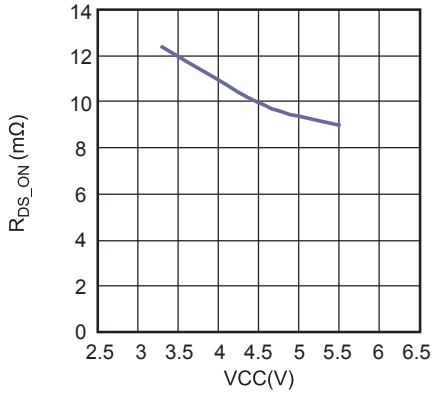
EN Rising Threshold vs. Temperature



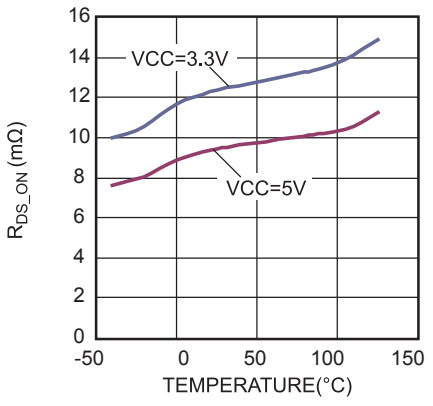
EN Falling Threshold vs. Temperature



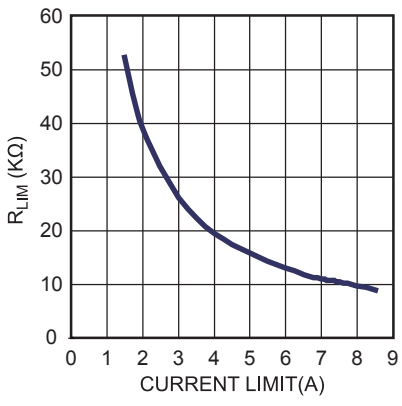
R_{DS_ON} vs.Vcc



R_{DS_ON} vs. Temperature



Current Limit vs R_{LIM}



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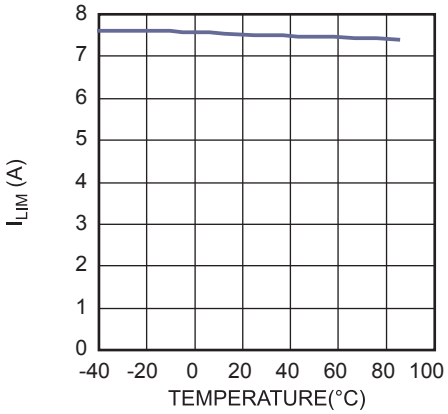
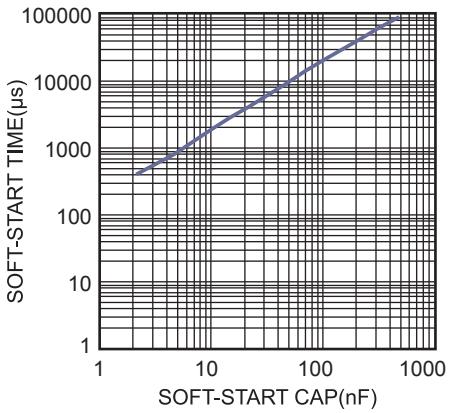
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, V_{CC} = 3.6V, R_{LIM}=10.5k, T_A = 25°C, unless otherwise noted.

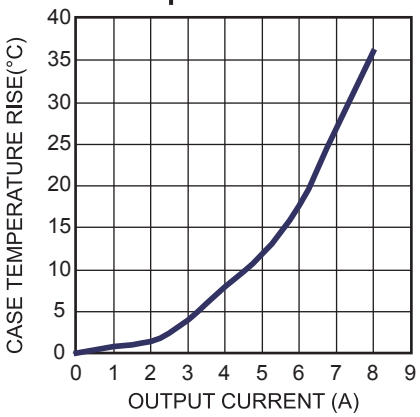
I_{LIM} vs. Temperature



Soft-Start vs.Cap



Case Temperature Rise vs. Output Current



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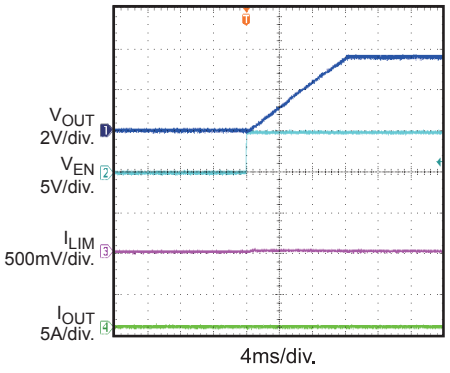
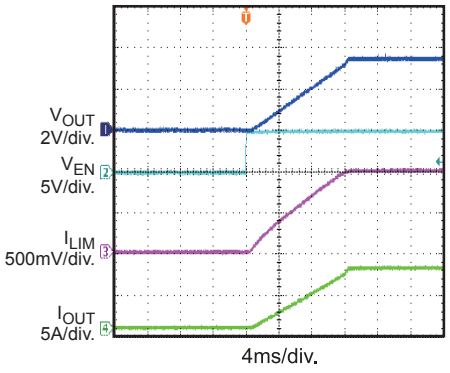
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, V_{CC} = 3.6V, R_{LIM}=10.5k, T_A = 25°C, unless otherwise noted.

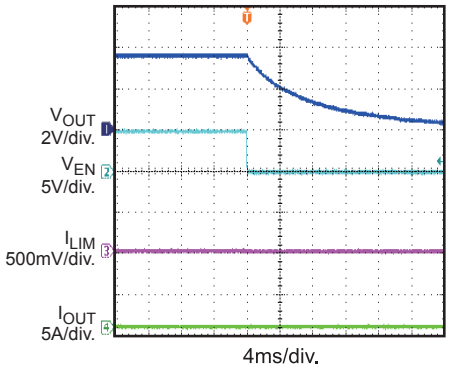
Enable Startup
V_{IN} =3.6V, V_{CC}=3.6V, No Load



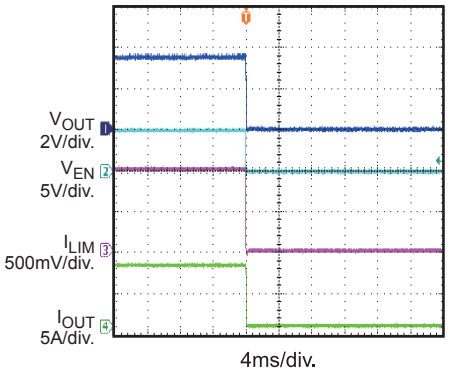
Enable Startup
V_{IN} =3.6V, V_{CC}=3.6V, 7A Load



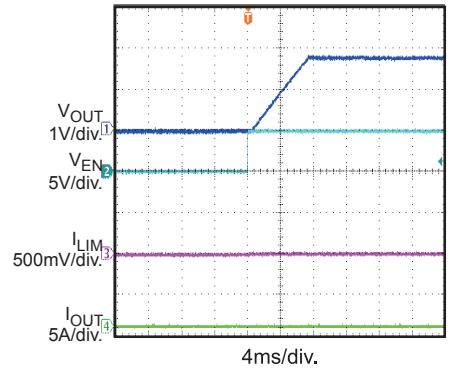
Enable Shutdown
V_{IN} =3.6V, V_{CC}=3.6V, No Load



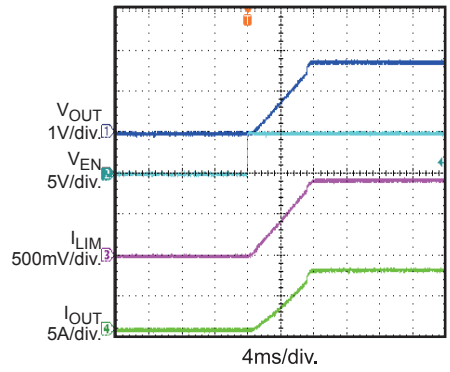
Enable Shutdown
V_{IN} =3.6V, V_{CC}=3.6V, 7A Load



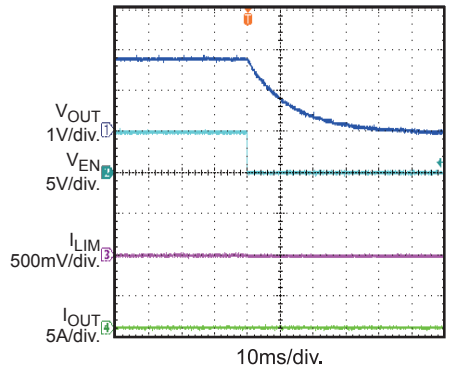
Enable Startup
V_{IN}=1.8V, V_{CC}=3.6V, No Load



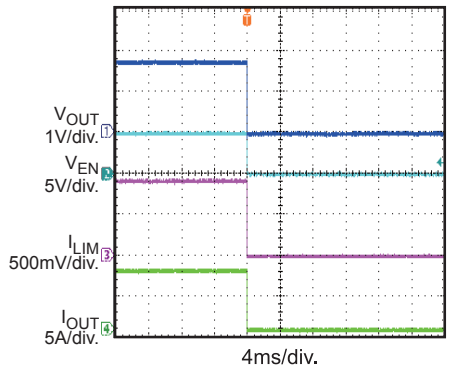
Enable Startup
V_{IN}=1.8V, V_{CC}=3.6V, 7A Load



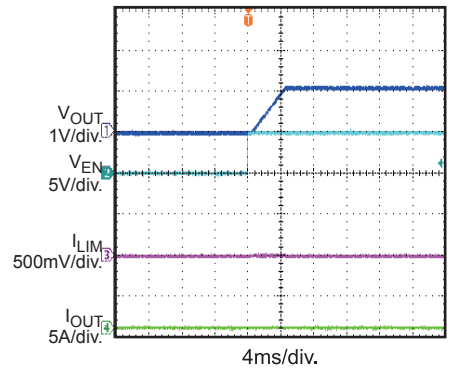
Enable Shutdown
V_{IN}=1.8V, V_{CC}=3.6V,No Load



Enable Shutdown
V_{IN}=1.8V, V_{CC}=3.6V, 7A Load



Enable Startup
V_{IN}=1.1V, V_{CC}=3.6V, No Load



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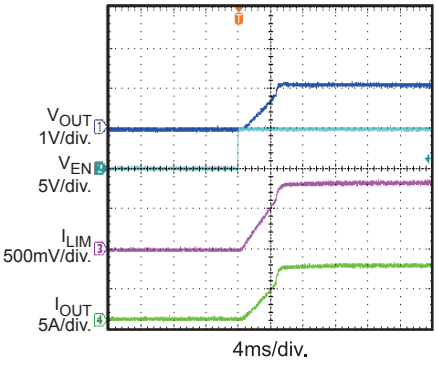
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, V_{CC} = 3.6V, R_{LIM}=10.5k, T_A = 25°C, unless otherwise noted.

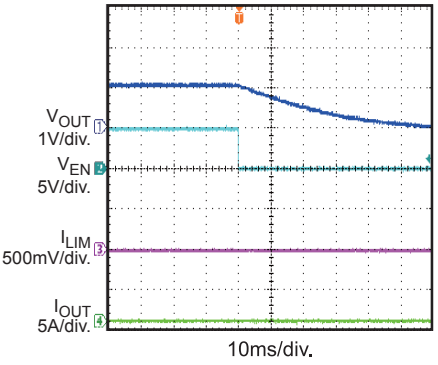
Enable Startup

V_{IN}=1.1V, V_{CC}=3.6V, 7A Load



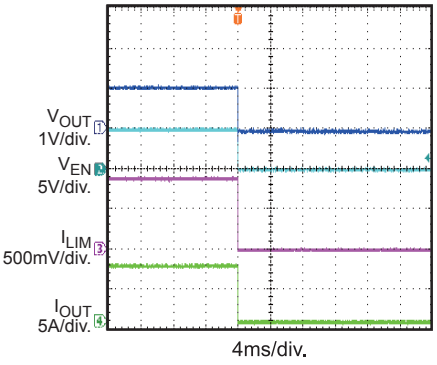
Enable Shutdown

V_{IN}=1.1V, V_{CC}=3.6V, No Load



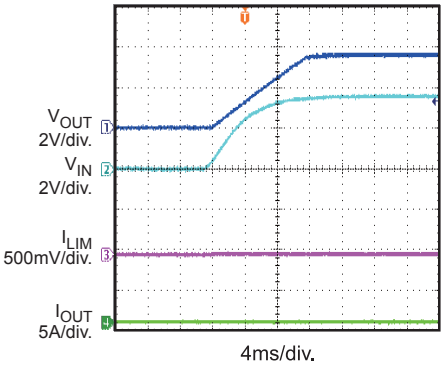
Enable Shutdown

V_{IN}=1.1V, V_{CC}=3.6V, 7A Load



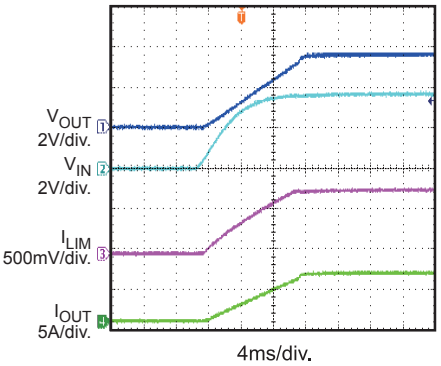
Power Up

V_{IN} =3.6V, V_{CC}=3.6V, No Load



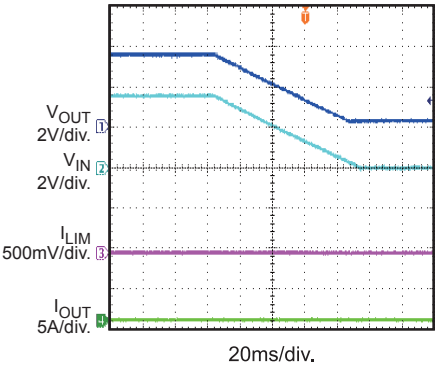
Power Up

V_{IN} =3.6V, V_{CC}=3.6V, 7A Load



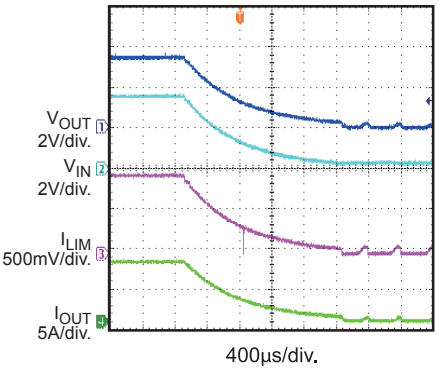
Power Down

V_{IN} =3.6V, V_{CC}=3.6V, No Load



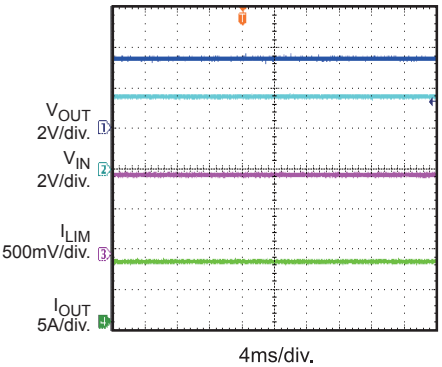
Power Down

V_{IN} =3.6V, V_{CC}=3.6V, 7A Load



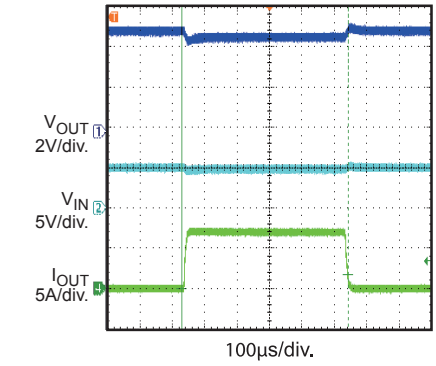
Steady State

V_{IN} =3.6V, V_{CC}=3.6V, 7A Load



Load Transient Response

V_{IN} =5V, V_{CC}=3.3V, I_{OUT}=0A to 7A



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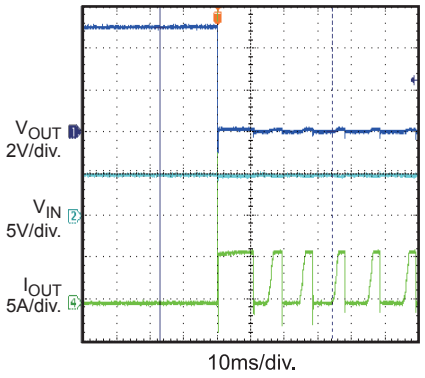
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, V_{CC} = 3.6V, R_{LIM}=10.5k, T_A = 25°C, unless otherwise noted.

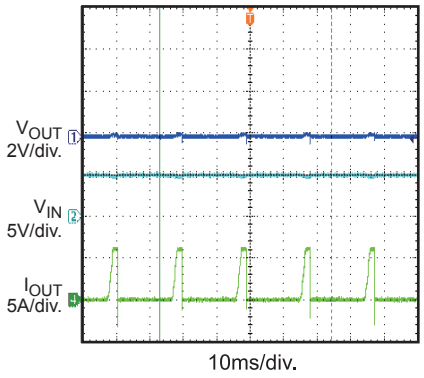
SCP Entery

V_{IN} =5V, V_{CC}=3.3V, R_{LIM}=10.5k



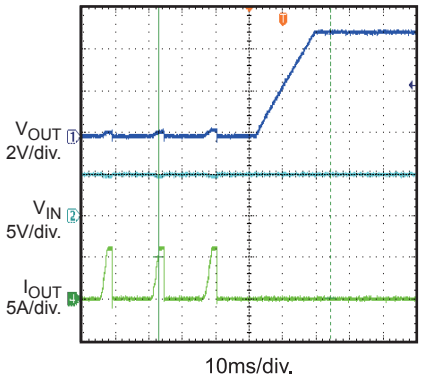
SCP Steady State

V_{IN} =5V, V_{CC}=3.3V, R_{LIM}=10.5k



SCP Recovery

V_{IN} =5V, V_{CC}=3.3V, R_{LIM}=10.5k



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PIN FUNCTIONS

(2x3)QFN18 Pin #	Name	Description
1, 13	VIN1	Input Power Supply of Switch 1.
2, 12	VOUT1	Output to the Load of Switch 1.
3, 11	VOUT2	Output to the Load of Switch 2.
4, 10	VIN2	Input Power Supply of Switch 2.
5	EN2	Enable Input of Switch 2. Pulling this pin below the specified threshold shuts the chip down.
6, 15	GND	Ground.
7	VCC2	Switch 2's Supply Voltage to the Control Circuitry.
8	ILIM2	Output Current Limit Configure of Switch 2. Place a resistor to ground to set the overload current limit level.
9	SS2	Soft start control pin of load Switch 2. Connecting a capacitor from this pin to ground to set the soft start time.
14	EN1	Enable Input of Switch 1. Pulling this pin below the specified threshold shuts the chip down.
16	VCC1	Switch 1's Supply Voltage to the Control Circuitry.
17	ILIM1	Output Current Limit Configure of Switch 1. Place a resistor to ground to set the overload current limit level.
18	SS1	Soft Start Control Pin of Load Switch 1. Connecting a capacitor from this pin to ground to set the soft start time.

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BLOCK DIAGRAM

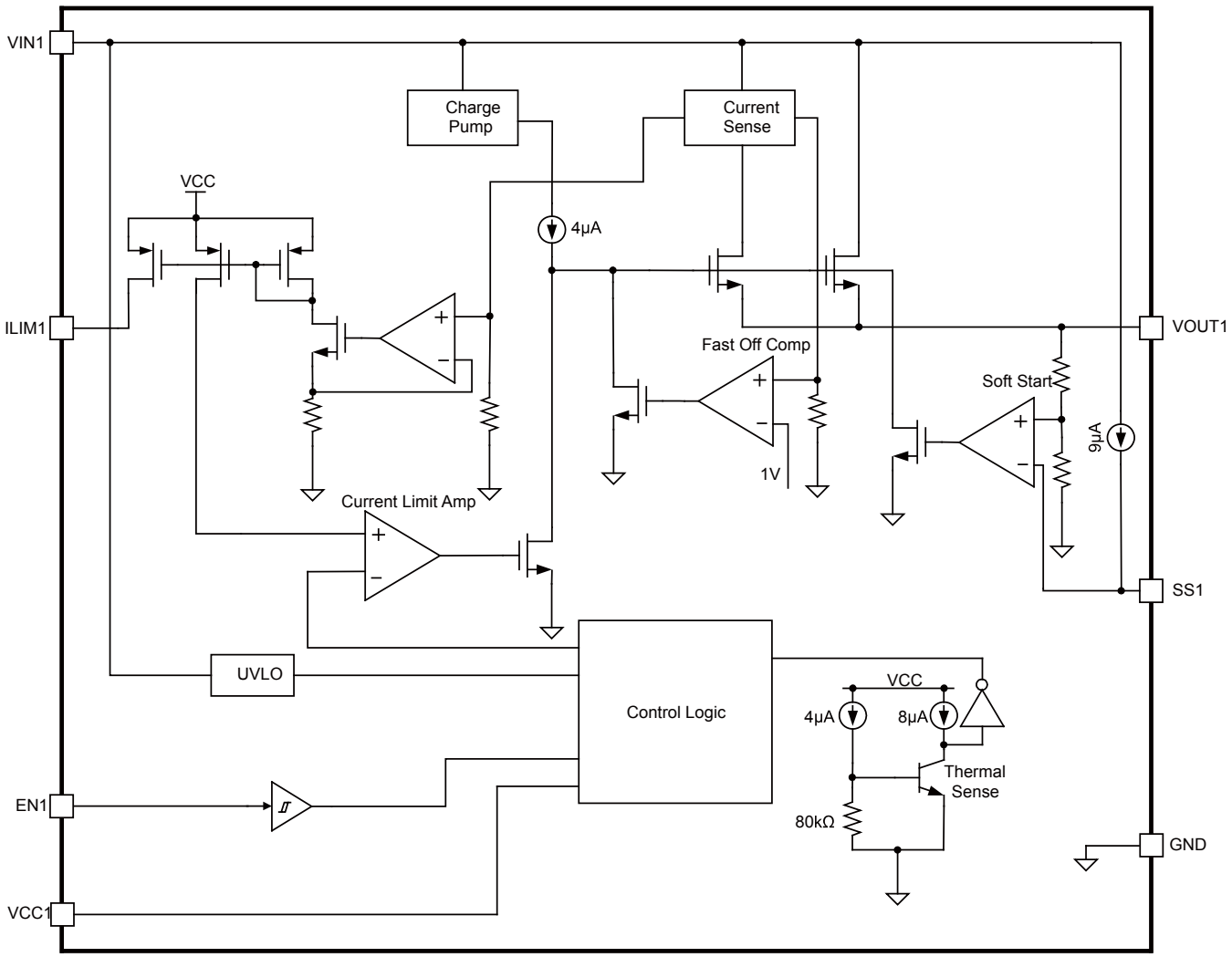

Figure 1: Functional Block Diagram

(Only Channel 1 Included, Channel 2 is the same)

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OPERATION

The MP5092 is designed to limit the in-rush current to the load when a circuit card is inserted into a live backplane power source; thereby limiting the backplane's voltage drop and the slew rate of the voltage to the load. MP5092 integrated two independent load switches. Any one channel can work alone. Each channel can provide 7.5A load capability. It provides an integrated solution to monitor output current to eliminate the need for an external current power MOSFET, and current sense device.

Enable

When input voltage is greater than the under-voltage lockout threshold (UVLO), typically 0.5V, MP5092 can be enabled by pulling EN pin to higher than 1.5V. Pulling down to ground will disable MP5092.
The recommend start up sequence is power up V_{IN} first. After V_{IN} is ready, pull EN voltage to high.

Current Limit

The MP5092 provides a constant current limit that can be programmed by an external resistor. Once the device reaches its current limit threshold, the internal circuit regulates the gate voltage to hold the current in the power FET constant. The typical response time is about 20μs and the output current may have a small overshoot during this time period.

The pre-set current limit value can be calculated by below equation:

$$I_{LIM}(A) = \frac{82000}{R_{LIM}(\Omega)} \qquad (1)$$

R_{LIM} is R1 and R2 which are placed between ILIM1/2 pin to ground in Figure 4.

If the current limit block starts to regulate the output current, the power loss on power MOSFET will cause the IC temperature rise. If the junction temperature rose to high enough, it will trigger thermal shutdown. After thermal shutdown happened, it will disable the output until the over temperature fault remove. The over temperature threshold is 155°C and hysteresis is 30°C.**Bias Vcc Supply**

Vcc is the bias supply for internal analog circuit. It is better to have a decouple capacitor to filter the noise. If the main power voltage V_{IN} is higher than 3V, the Vcc can be directly connected to V_{IN}.

Short-Circuit Protection

If the load current increases rapidly due to a short circuit, the current may exceed the current limit threshold by a lot before the control loop can respond. If the current reaches an internal secondary current limit level (about 13A), a fast turn-off circuit activates to turn off the power FET. This limits the peak current through the switch to limit the input voltage drop. The total short circuit response time is about 200ns. If fast off works, it will keep off the power FET for 80us. After that time period, it will re-turn on power FET..

Output Discharge

MP5092 has output discharge function. This function can discharge the Vo by internal pull down resistance when IC disabled and the load is very light.

Soft-Start

A capacitor connected to the SS pin determines the soft-start time. There is an internal 9uA constant current source charge SS cap and ramps up the voltage on the SS pin. The output voltage rises at 3 times the slew rate to the SS voltage.

The soft-start time can be calculated by below equation:

$$T_{SS}(ms) = \frac{1}{3} \times \frac{V_{OUT}(V) \cdot C_{SS}(nF)}{I_{SS}(uA)} \qquad (2)$$

T_{SS} is the soft-start time, I_{SS} is internal 9uA constant current, C_{SS} is external soft-start cap.

The suggestion minimum SS cap should be bigger than 4.7nF. If the SS pin is floated or SS cap is too small, the Vo rising time will be just limited by power MOS charge time.

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APPLICATION INFORMATION

ILIM Resistor Selection

The current limit value can be set by ILIM resistor. The current limit can be gotten by equation (1).

The current limit threshold is suggested to 10% ~ 20% higher than maximum load current. For example, if the system's full load is 7A, set the current limit to 7.7A.

ILIM Capacitor Selection

The internal advanced auto-zero comparator bring a high accuracy of current limit. The auto-zero will also cause some little jitter on ILIM pin. To get a more stable ILIM, a small ceramic capacitor can be mounted between ILIM and ground. Suggested place a ILIM capacitor less than 1nF.

Soft Start Capacitor Selection

There is an internal 9uA constant current source charge SS cap and ramps up the voltage on the SS pin. The output voltage rises follow 3 times the slew rate of SS voltage.

If the inrush on output current reached the current limit during start up (like with large output cap or very large load), MP5092 will limit the output current and the same time, SS time will be increased (Figure 2).

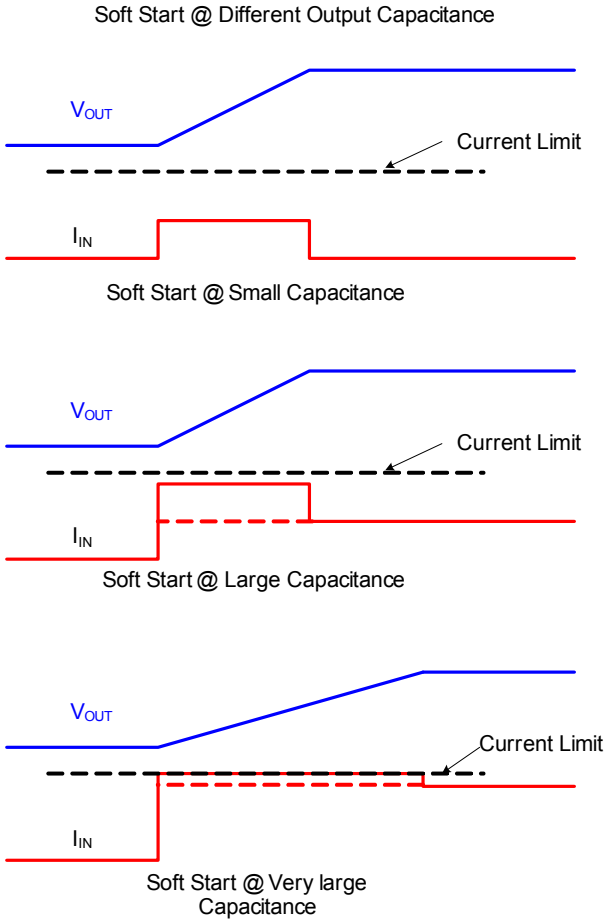

Figure 2: Soft Start Periods at different output capacitance

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Design Example

Some design examples are provided below. See Table 1 and Figure 3.

Table 1

V_{IN} (V)	Current limit (A)	R_{LIM} (kΩ)	SS cap (nF)	SS time (ms)
5	3	26.1	22	4
5	5	15.8	47	9
5	7.5	10.5	100	20

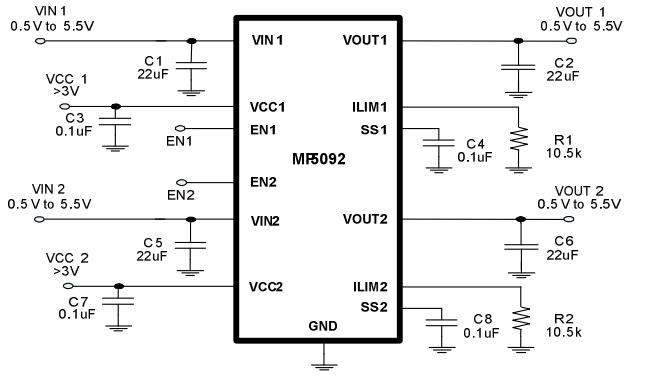

Figure 3: Typical Application Schematic

Layout Guide

PCB layout is very important to achieve stable operation. Please follow these guidelines and take below figure for reference (take schematic in Figure 3 as an example). Place ILIM resistor (R1 and R2 in Figure 3) close to ILIM1/2 pin, input cap close to V_{CC} pin. Put enough vias around IC to achieve better thermal performance.

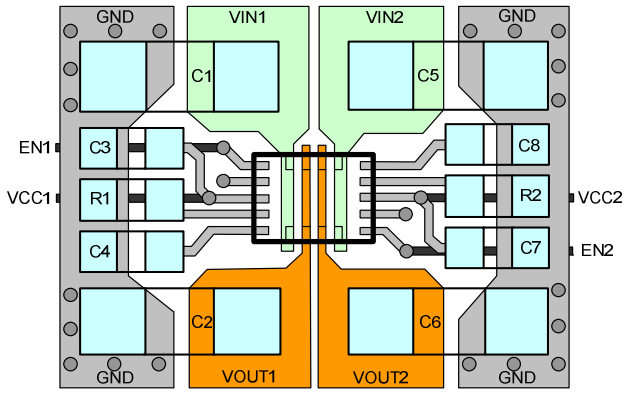

Figure 4: Recommended Layout

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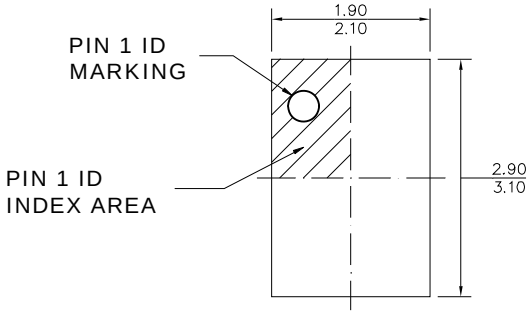
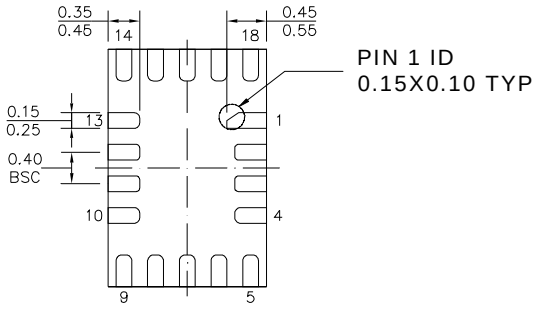
PACKAGE INFORMATION

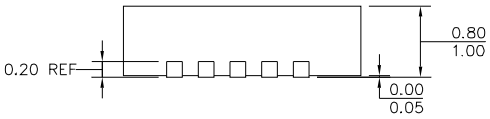
QFN18 (2mmx3mm)



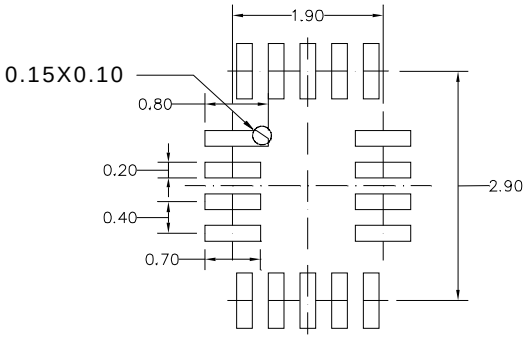
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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