# MP5056

## 28V, 7mΩ $R_{DS(ON)}$, Hot-Swap Protection Device with Current Monitoring

## DESCRIPTION

The MP5056 is a hot-swap protection device designed to protect circuitry on its output from transients on its input. It also protects its input from undesired shorts and transients coming from its output.

During start-up, the slew rate at the output limits the inrush current. An external capacitor connected to the SS pin controls the slew rate. The maximum output load is current-limited using a sense FET topology. A low-power resistor between the ISET pin and ground controls the magnitude of the current limit ($I_{LIMIT}$). An internal charge pump drives the gate of the power device, which allows for a power MOSFET with a very low on resistance (7mΩ). The MP5056 includes an IMON option that produces a voltage proportional to the current flowing through the power device, which is set via a resistor connected between the IMON pin and ground.

Full protection features include current-limit protection, thermal shutdown, and damaged MOSFET detection. Both current-limit protection and thermal shutdown offer configurable auto-retry or latch-off mode. The device also features under-voltage lockout protection (UVLO).

The MP5056 is available in a QFN-22 (3mmx5mm) package.

## FEATURES

- 7mΩ Integrated Power MOSFET
- 5A to 15A Adjustable Current Limit ($I_{LIMIT}$)
- Output Current ($I_{OUT}$) Measurement
- ±10% Current Monitoring Accuracy
- Fast Response for Short Protection (200ns)
- PG Detection and FLTB Indication
- PG Asserts Low at $V_{IN}$ = 0V
- Damaged MOSFET Detection
- External Soft Start (SS)
- Under-Voltage Lockout (UVLO) Protection
- Thermal Shutdown
- Available in a QFN-22 (3mmx5mm) Package

## APPLICATIONS

- Hot Swap
- Home Appliances
- PC Cards
- Storage Devices

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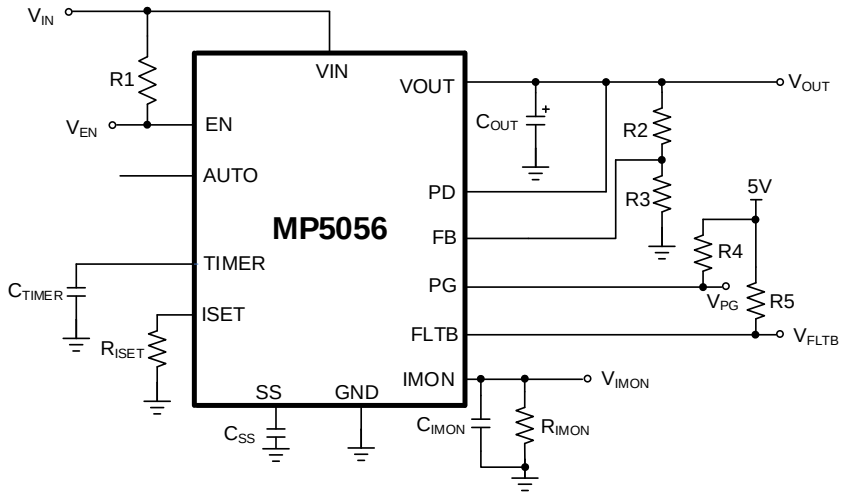
## TYPICAL APPLICATION





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## ORDERING INFORMATION

| Part Number* | Package | Top Marking | MSL Rating** |
|---|---|---|---|
| MP5056GQV | QFN-22 (3mmx5mm) | *See Below* | 1 |

* For Tape & Reel, add suffix -Z (e.g. MP5056GQV-Z).

** Moisture Sensitivity Level Rating.

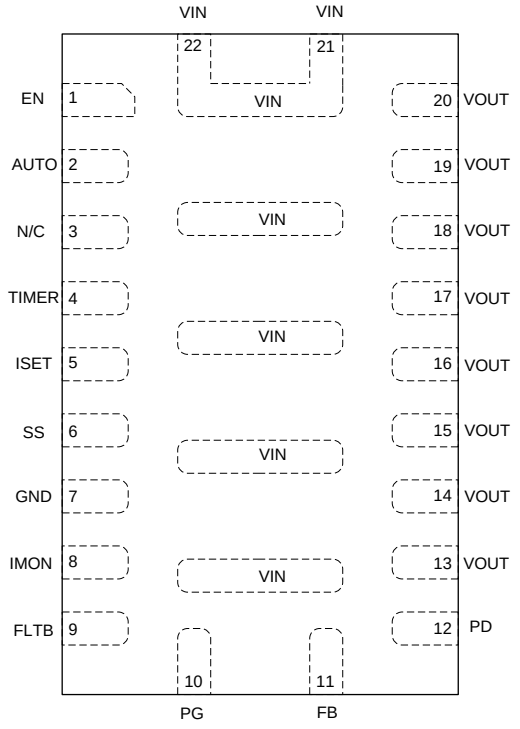
## TOP MARKING

MPYW
5056
LLL

MP: MPS prefix
Y: Year code
W: Week code
5056: First four digits of the part number
LLL: Lot number

## PACKAGE REFERENCE

**TOP VIEW**




**QFN-22 (3mmx5mm)**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## PIN FUNCTIONS

| Pin # | Name | Description |
|---|---|---|
| 1 | EN | **Enable.** Pull the EN pin above 1.8V to turn the device on; pull EN below 1.6V to turn it off. |
| 2 | AUTO | **Auto-reset enable.** Float AUTO pin or pull AUTO above 2.5V to enable auto-reset mode once a fault is removed. If AUTO is pulled to ground, then the MP5056 latches off if a fault occurs. |
| 3 | NC | **Not connected.** Float this pin. |
| 4 | TIMER | **Timer setting.** An external capacitor sets the hot-plug insertion delay time, fault timeout period, and restart time. |
| 5 | ISET | **Current limit setting.** Connect a resistor between the ISET pin and ground to set the current limit ($I_{LIMIT}$) value. |
| 6 | SS | **Soft start.** An external capacitor connected to the SS pin sets the soft-start time ($t_{SS}$). The internal circuit controls the output voltage ($V_{OUT}$) slew rate during start-up. Float SS to set $t_{SS}$ at its minimum time (1ms). |
| 7 | GND | **Ground.** |
| 8 | IMON | **Output current monitoring.** The IMON pin provides a voltage proportional to the current flowing through the power device. Connect a resistor between the IMON pin and ground to set the gain. Do not float IMON. |
| 9 | FLTB | **Fault bar.** The FLTB pin is an open-drain output that is pulled to ground if an over-current (OC) fault or thermal shutdown occurs. Pull FLTB up to an external power supply via a 100kΩ resistor. |
| 10 | PG | **Power good.** The PG pin is an open-drain output. Pull PG up to an external power supply via a resistor. PG is pulled high to indicate that the power is good. PG is pulled low to indicate that the output has dropped below its set threshold. PG starts working once the pull-up supply is enabled, even if the VIN and EN pins are disabled. |
| 11 | FB | **Feedback.** An external resistor divider connected to the output sets the $V_{OUT}$ value at which PG is enabled. The rising threshold is 0.6V, with a 60mV hysteresis. |
| 12 | PD | **Output discharge.** Connect the PD and VOUT pins to provide a 500Ω load to discharge the output if the input voltage ($V_{IN}$) drops below the $V_{IN}$ UVLO threshold, or if the EN voltage ($V_{EN}$) is between 0.6V and its rising threshold. Float PD to disable this function. |
| 13, 14, 15, 16, 17, 18, 19, 20 | VOUT | **Output.** $V_{OUT}$ is controlled by the IC. |
| 21, 22 (exposed pads) | VIN | **Input power supply.** |


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## ABSOLUTE MAXIMUM RATINGS (1)

Input voltage ($V_{IN}$) ..... -0.3V to +36V
$V_{OUT}$, $V_{PD}$..... -0.3V to +30V
All other pins..... -0.3V to +6.5V
Continuous power dissipation ($T_A$ = 25°C) (2)…..
…..…….2.7W
Power dissipation ($T_A$ = 25°C, 10ms single pulse)
.....215W
Maximum current ($T_A$ = 25°C)…… 25A
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature..... -65°C to +150°C

### *ESD Ratings*

Human body model (HBM) .....±2kV
Charged device model (CDM) .....±750V

### *Recommended Operating Conditions*

Operating $V_{IN}$ range ..... 6V to 28V
Operating junction temp ($T_J$) .... -40°C to +125°C

### *Thermal Resistance* $\theta_{JA}$ $\theta_{JC}$

| | | |
|---|---|---|
| QFN-22 (3mmx5mm) | | |
| JESD51-7 (3) | 46 | 10 °C/W |
| EV5056-QV-00A (4) | 30 | 2 °C/W |

**Notes:**

1) Absolute maximum ratings are rated under room temperature, unless otherwise noted. Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature $T_J$ (MAX), the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$ (MAX) = ($T_J$ (MAX) - $T_A$) / $\theta_{JA}$. Exceeding the maximum allowable power dissipation can lead to excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Measured on JESD51-7, 4-layer PCB.
4) Measured on the EV5056-QV-00A (8.5cmx8.5cm), 2-layer PCB.


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## ELECTRICAL CHARACTERISTICS

**$V_{IN}$ = 12V, $R_{ISET}$ = 10kΩ, $C_{OUT}$ = 220µF, $T_J$ = -40°C to +125°C (5), typical values are tested at $T_J$ = 25°C, unless otherwise noted.**

| Parameters | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Supply Current** | | | | | | |
| Quiescent current | $I_Q$ | $V_{EN}$ is high, no load | | 1 | 2 | mA |
| | | Latch-off mode | | 0.7 | 1.2 | mA |
| | | $V_{EN}$ = 0V, $V_{IN}$ = 12V | | 1 | 10 | µA |
| **Power MOSFET** | | | | | | |
| On resistance | $R_{DS(ON)}$ | | | 7 | 12 | mΩ |
| Off-state leakage current | $I_{OFF}$ | $V_{IN}$ = 28V, $V_{EN}$ = 0V, $V_{OUT}$ = 0V, $T_J$ = 25°C | | | 1 | µA |
| **Thermal Shutdown** | | | | | | |
| Thermal shutdown threshold (6) | | | | 167 | | °C |
| Thermal shutdown hysteresis (6) | | Auto-retry mode only | | 28 | | °C |
| **Under-Voltage Lockout (UVLO) Protection** | | | | | | |
| UVLO rising threshold | $V_{UVLO_RISING}$ | | | 4.15 | 5.5 | V |
| UVLO falling threshold | $V_{UVLO_FALLING}$ | | 2.7 | 3.8 | 5 | V |
| UVLO hysteresis | $V_{UVLO_HYS}$ | | | 250 | | mV |
| **AUTO Pin** | | | | | | |
| Low-level input voltage | $V_{AUTO_LOW}$ | Latch-off mode | | | 1 | V |
| High-level input voltage | $V_{AUTO_HIGH}$ | Auto-retry mode | 2.5 | | | V |
| **Soft Start (SS)** | | | | | | |
| SS pin pull-up current | $I_{SS}$ | $I_{SS}$ changes with the input | 3 | 6 | 9 | µA |
| **Current Limit ($I_{LIMIT}$)** | | | | | | |
| $I_{LIMIT}$ during normal operation | $I_{LIMIT_NOR}$ | $R_{ISET}$ = 10kΩ | 10.5 | 12.5 | 14.5 | A |
| Current monitor accuracy | | $I_{OUT}$ = 6A | -10 | | +10 | % |
| $I_{LIMIT}$ response time (6) | | $I_{LIMIT}$ = 3A, add a 3Ω load | | 20 | | µs |
| Secondary $I_{LIMIT}$ (6) | $I_{LIMIT_H}$ | Any value of $R_{ISET}$ | | 25 | | A |
| Short-circuit protection (SCP) response time (6) | | | | 200 | | ns |
| **TIMER** | | | | | | |
| TIMER high threshold | $V_{TIMER_HIGH}$ | | 1 | 1.23 | 1.4 | V |
| TIMER low threshold | $V_{TIMER_LOW}$ | Over-current (OC) restart cycle | 0.09 | 0.20 | 0.35 | V |
| Fault restart duty cycle | | | 0.1 | 0.25 | 0.5 | % |
| Insertion delay time charge current | $I_{INSERT}$ | | 15 | 40 | 60 | µA |
| Fault detection charge current | $I_{FLT_DET}$ | | 80 | 200 | 300 | µA |
| Fault restart sink current | $I_{FLT_SINK}$ | | 0.15 | 0.5 | 0.8 | µA |
| Discharge on resistance | | $I_{OUT}$ < $I_{LIMIT}$ | 15 | 35 | 80 | Ω |


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## ELECTRICAL CHARACTERISTICS *(continued)*

**$V_{IN}$ = 12V, $R_{ISET}$ = 10kΩ, $C_{OUT}$ = 220µF, $T_J$ = -40°C to +125°C [5], typical values are tested at $T_J$ = 25°C, unless otherwise noted.**

| Parameters | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Enable (EN)** | | | | | | |
| EN rising threshold | $V_{EN_RISING}$ | | 1.4 | 1.8 | 2.2 | V |
| EN falling threshold | $V_{EN_FALLING}$ | | 1.2 | 1.6 | 2 | V |
| EN hysteresis | $V_{EN_HYS}$ | | | 200 | | mV |
| **Feedback (FB)** | | | | | | |
| FB rising threshold | $V_{FB_RISING}$ | | 0.51 | 0.6 | 0.69 | V |
| FB falling threshold | $V_{FB_FALLING}$ | | 0.45 | 0.54 | 0.63 | V |
| FB hysteresis | $V_{FB_HYS}$ | | | 60 | | mV |
| **Fault Bar (FLTB) and Power Good (PG)** | | | | | | |
| Low-level output voltage | $V_{OUT_LOW}$ | 1mA sink current | | 0.1 | 0.3 | V |
| Off-state leakage current | $I_{FLTB_LKG}$ | $V_{FLTB}$ = 5V | | | 1 | µA |
| Fault bar propagation delay | | Pull $V_{ISET}$ up from 0V to 1V | 5 | 20 | 40 | µs |
| PG low-level output voltage with a 100kΩ resistor | $V_{OUT_LOW_100}$ | $V_{IN}$ = 0V, pull $V_{PG}$ up to 3.3V via a 100kΩ resistor | | 500 | 800 | mV |
| PG low-level output voltage 10kΩ resistor | $V_{OUT_LOW_10}$ | $V_{IN}$ = 0V, pull $V_{PG}$ up to 3.3V via a 10kΩ resistor | | 600 | 800 | mV |

**Notes:**

5) Guaranteed by over-temperature correlation. Not tested in production.
6) Derived from bench characterization. Not tested in production.


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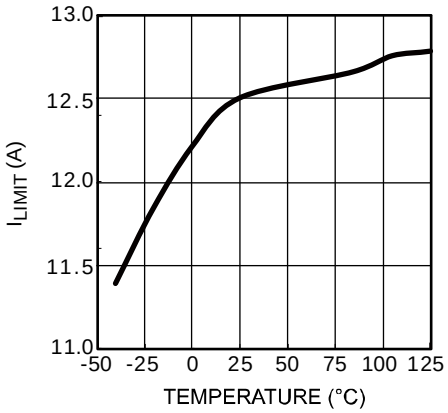
## TYPICAL CHARACTERISTICS

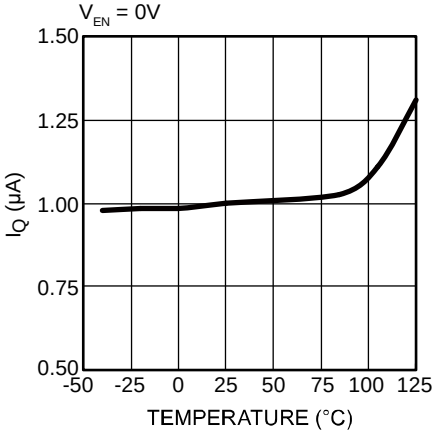
**$V_{IN}$ = 12V, $C_{OUT}$ = 220µF, $C_{TIMER}$ = 220nF, $R_{ISET}$ = 10kΩ, unless otherwise noted.**

### Current Limit vs. Temperature



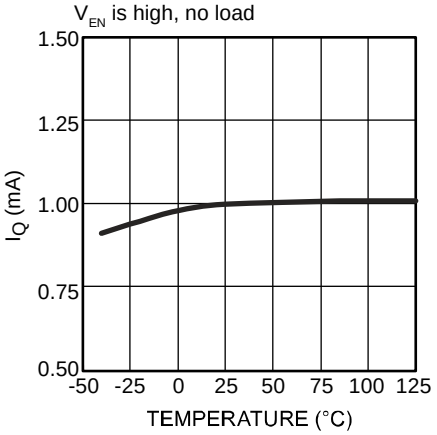

### Quiescent Current vs. Temperature

$V_{EN}$ = 0V

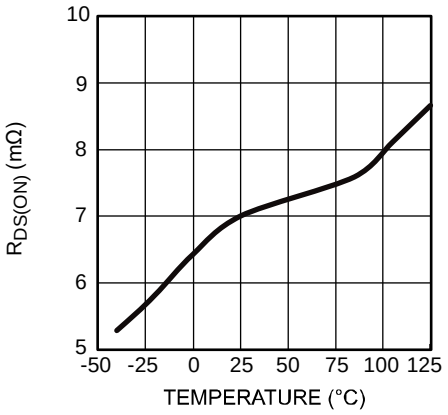



### Quiescent Current vs. Temperature

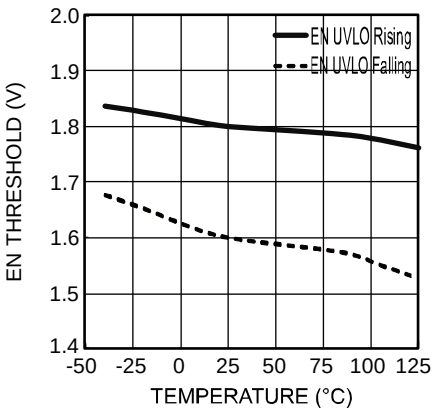
$V_{EN}$ is high, no load



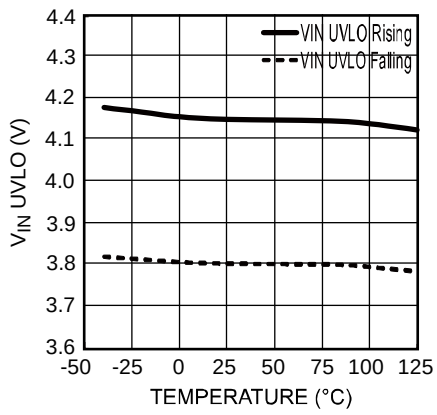

### $R_{DS(ON)}$ vs.Temperature




### EN UVLO Threshold vs. Temperature




### $V_{IN}$ UVLO Threshold vs. Temperature





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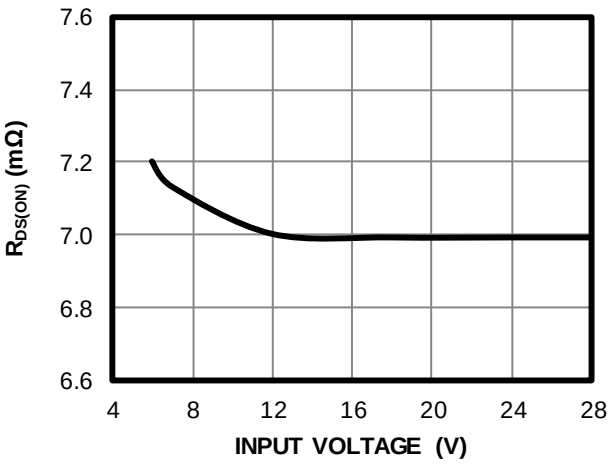
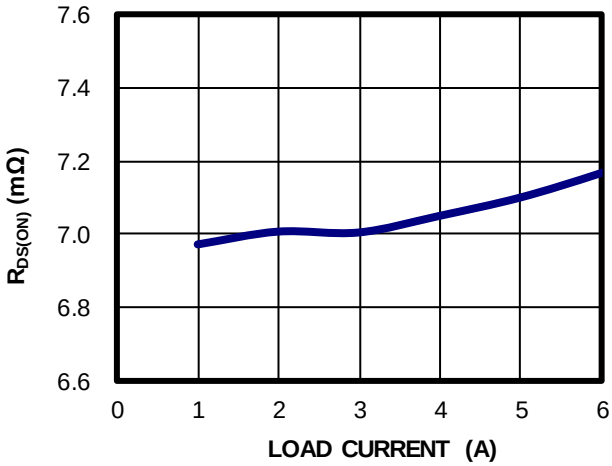
## TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{IN}$ = 12V, $C_{OUT}$ = 220µF, $C_{TIMER}$ = 220nF, $C_{SS}$ = 10nF, $R_{ISET}$ = 10kΩ, $T_A$ = 25°C, unless otherwise noted.**

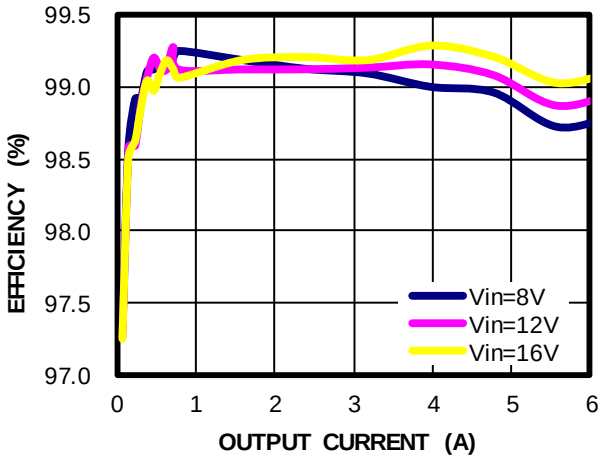
**$R_{DS(ON)}$ vs. Input Voltage**



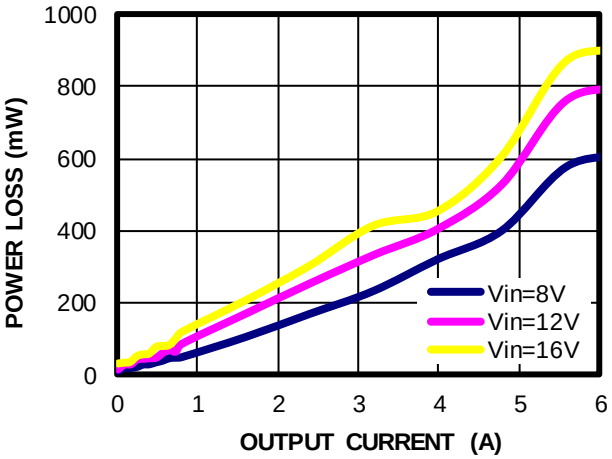

**$R_{DS(ON)}$ vs. Load Current**




**Efficiency vs. Output Current**




**Power Loss vs. Output Current**





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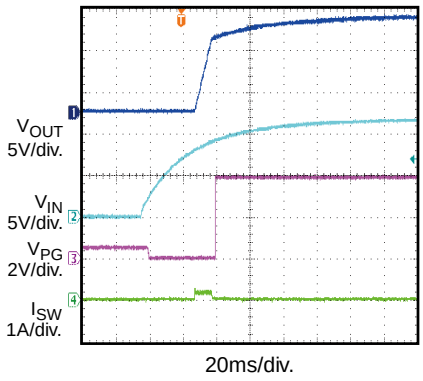
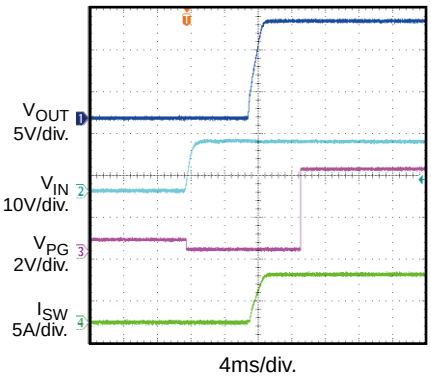
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 12V, $C_{OUT}$ = 220µF, $C_{TIMER}$ = 220nF, $C_{SS}$ = 10nF, $R_{ISET}$ = 10kΩ, $T_A$ = 25°C, unless otherwise noted.**

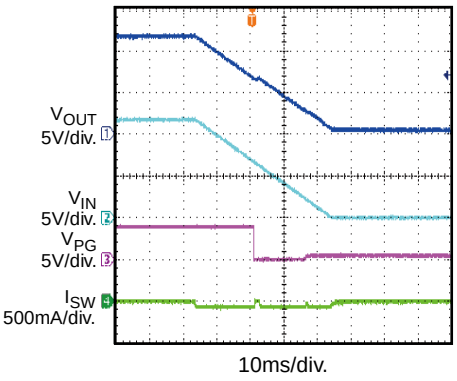
### Start-Up through VIN
$I_{OUT}$ = 0A



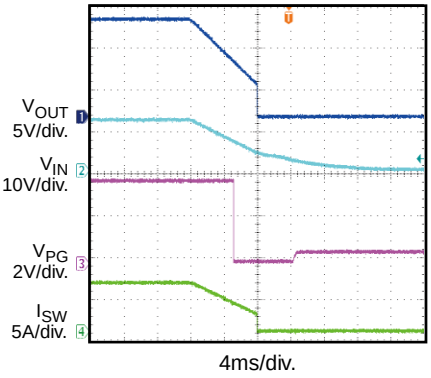

### Start-Up through VIN
$I_{OUT}$ = 6A



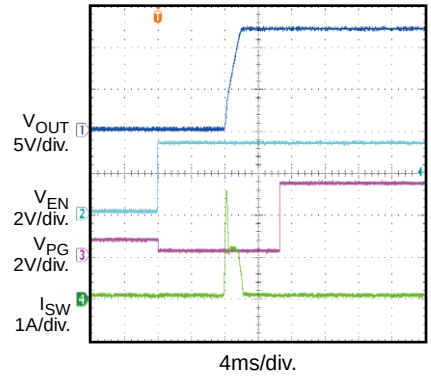

### Shutdown through VIN
$I_{OUT}$ = 0A



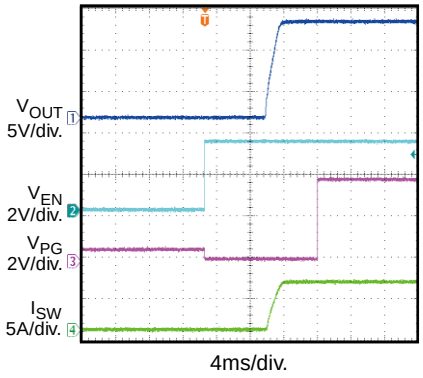

### Shutdown through VIN
$I_{OUT}$ = 6A



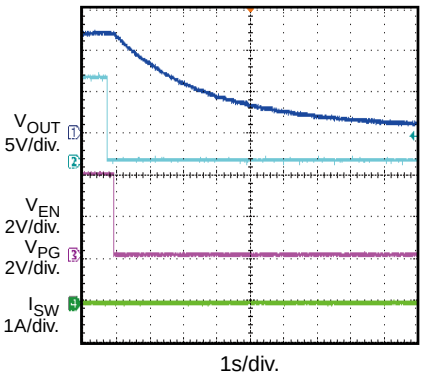

### Start-Up through EN
$I_{OUT}$ = 0A



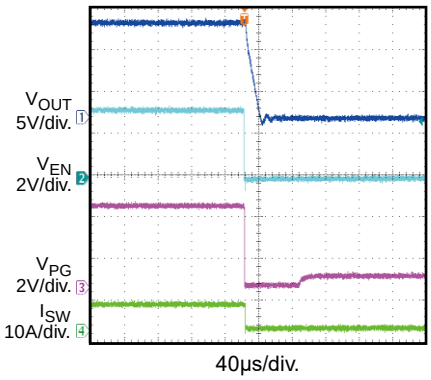

### Start-Up through EN
$I_{OUT}$ = 6A



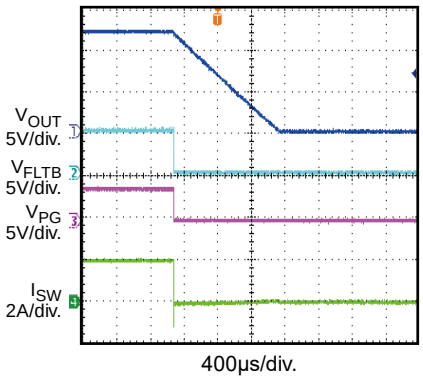

### Shutdown through EN
$I_{OUT}$ = 0A




### Shutdown through EN
$I_{OUT}$ = 6A




### Thermal Shutdown
$I_{OUT}$ = 2A, latch-off mode





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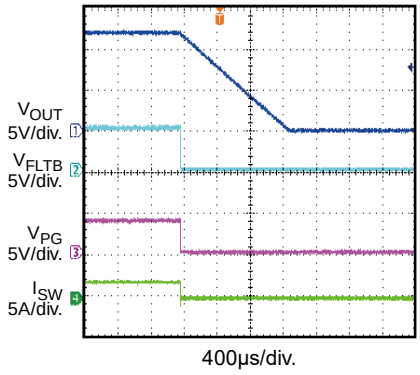
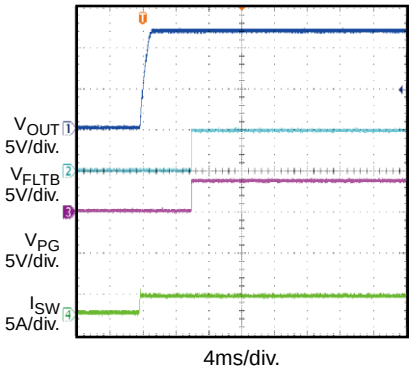
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 12V, $C_{OUT}$ = 220µF, $C_{TIMER}$ = 220nF, $C_{SS}$ = 10nF, $R_{ISET}$ = 10kΩ, $T_A$ = 25°C, unless otherwise noted.**

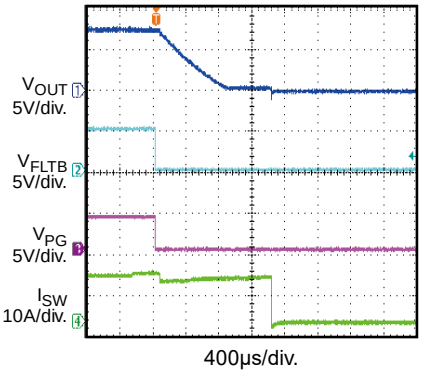
### Thermal Shutdown
$I_{OUT}$ = 2A, auto-retry mode



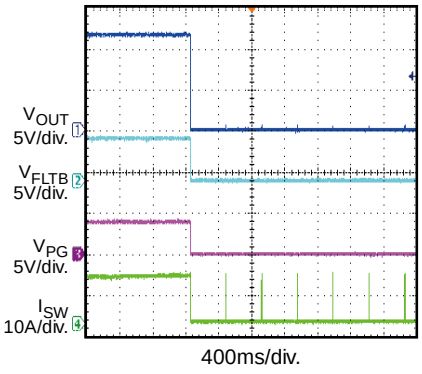

### Thermal Recovery
$I_{OUT}$ = 2A, auto-retry mode



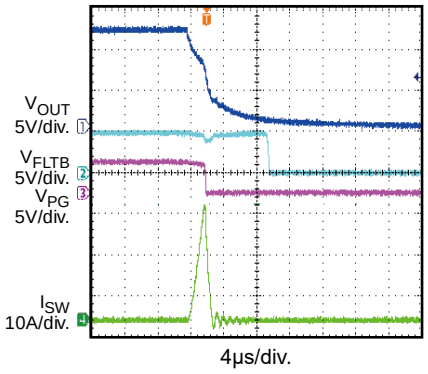

### OCP Entry
$V_{IN}$ = 12V, latch-off mode



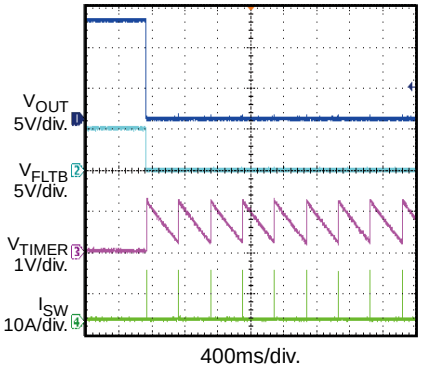

### OCP Entry
$V_{IN}$ = 12V, auto-retry mode



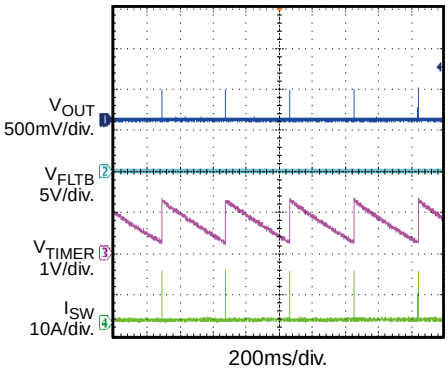

### SCP Entry
$V_{IN}$ = 12V, latch-off mode



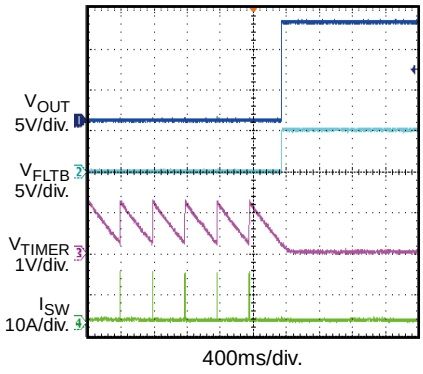

### SCP Entry
$V_{IN}$ = 12V, auto-retry mode




### SCP Steady State
$V_{IN}$ = 12V, auto-retry mode




### SCP Recovery
$V_{IN}$ = 12V, auto-retry mode





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# FUNCTIONAL BLOCK DIAGRAM

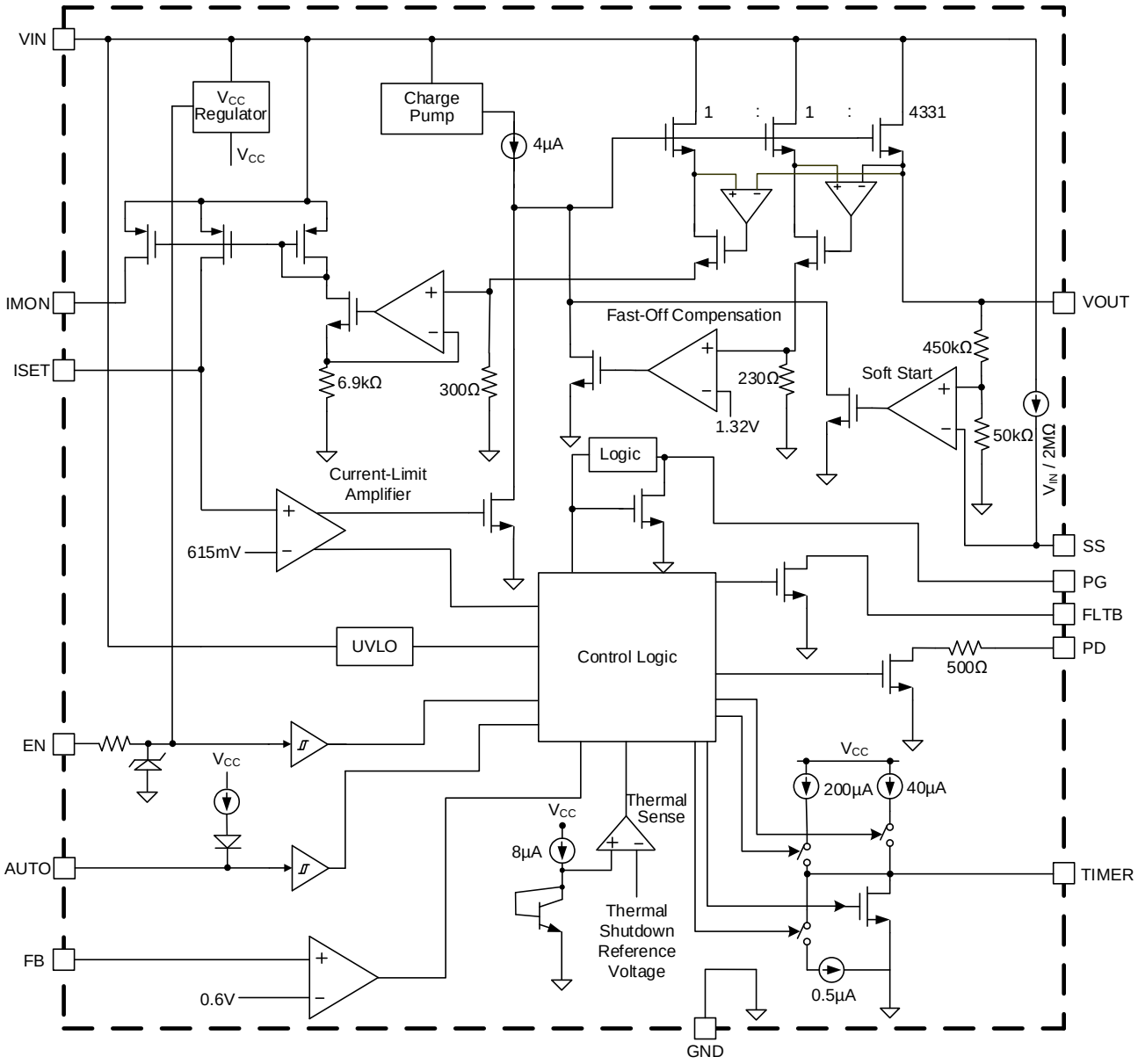


**Figure 1: Functional Block Diagram**


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## OPERATION

The MP5056 protects circuitry on its output from transients on its input. It also protects its input from undesired shorts and transients coming from its output. The device provides an integrated solution to monitor the input voltage ($V_{IN}$), output voltage ($V_{OUT}$), output current ($I_{OUT}$), and die temperature. This means that an external current-sense resistor, power MOSFET, and thermal sense device are not required for this solution.

### Current Limit ($I_{LIMIT}$)

The MP5056 provides a constant current limit ($I_{LIMIT}$) that can be configured via an external resistor. If the device reaches its $I_{LIMIT}$ threshold, then the internal circuit regulates the gate voltage to keep the MOSFET current constant. To limit the current, the gate-to-source voltage ($V_{GS}$) should drop from 5V to about 1V. The typical response time is about 20µs. $I_{OUT}$ may have a small overshoot during this period.

If $I_{LIMIT}$ is triggered, then the fault timer starts. If $I_{OUT}$ drops below the $I_{LIMIT}$ threshold before the end of the fault timeout period, then the MP5056 resumes normal operation. If the over-current (OC) condition remains after the fault timeout period, then the MOSFET turns off. The subsequent behavior relates to the AUTO pin configuration. If the temperature reaches the thermal shutdown threshold during the fault timeout period, then the MOSFET turns off.

Float the AUTO pin to have the the part operate in auto-retry mode during over-current protection (OCP). If the device detects an OC condition, and AUTO is pulled to ground, then the part enters latch-off mode.

If the device reaches either $I_{LIMIT}$ or its thermal shutdown threshold, then the FLTB pin is pulled low with a propagation delay (20µs) to indicate a fault. The desired $I_{LIMIT}$ during normal operation is set by the external current-limit resistor.

### Thermal Shutdown

Thermal shutdown prevent the device from thermal runaway. If the silicon die temperature exceeds the thermal shutdown threshold (167°C), then the power MOSFET shuts down. Once the temperature drops below 139°C, the device starts up again.

### Short-Circuit Protection (SCP)

If the load current ($I_{LOAD}$) increases rapidly due to a short circuit, the current may significantly exceed the $I_{LIMIT}$ threshold before the control loop can respond. If the current reaches the 25A secondary $I_{LIMIT}$ level, then a fast turn-off circuit turns off the MOSFET via a 100mA pull-down gate discharge current (see Figure 2 on page 13). This limits the peak current through the MOSFET, which limits the $V_{IN}$ drop. The total short-circuit response time is about 200ns. The FLTB pin is pulled low once $I_{LIMIT}$ reaches a 25A. FLTB remains low until the circuit resumes normal operation.

### Fault Timer and Restart

If the current reaches its OCP threshold, then a fault timer current source (200µA) charges the external TIMER capacitor ($C_{TIMER}$). If the $I_{LIMIT}$ state is removed before the TIMER pin voltage ($V_{TIMER}$) reaches 1.23V, then the MP5056 resumes normal operation. A low-value resistor discharges $C_{TIMER}$ once $V_{TIMER}$ reaches 1.23V. If the $I_{LIMIT}$ state continues once $V_{TIMER}$ reaches 1.23V, then the MOSFET turns off. The subsequent restart procedure depends on the selected retry configuration.

If the AUTO pin is pulled low or pulled to ground, then the MP5056 latches off. Cycle the power on VIN or EN to remove the fault latch and resume normal operation.

Float the AUTO pin or pull AUTO above 2.5V to have the device operate in auto-retry mode (see Figure 3 on page 13). At the end of the fault timeout period, the MOSFET turns off and a low-current sink (0.5µA) discharges the external $C_{TIMER}$.

If $V_{TIMER}$ reaches its low threshold (0.2V), then the part restarts. If the fault condition remains, then the fault timeout period and restart timer are repeated.


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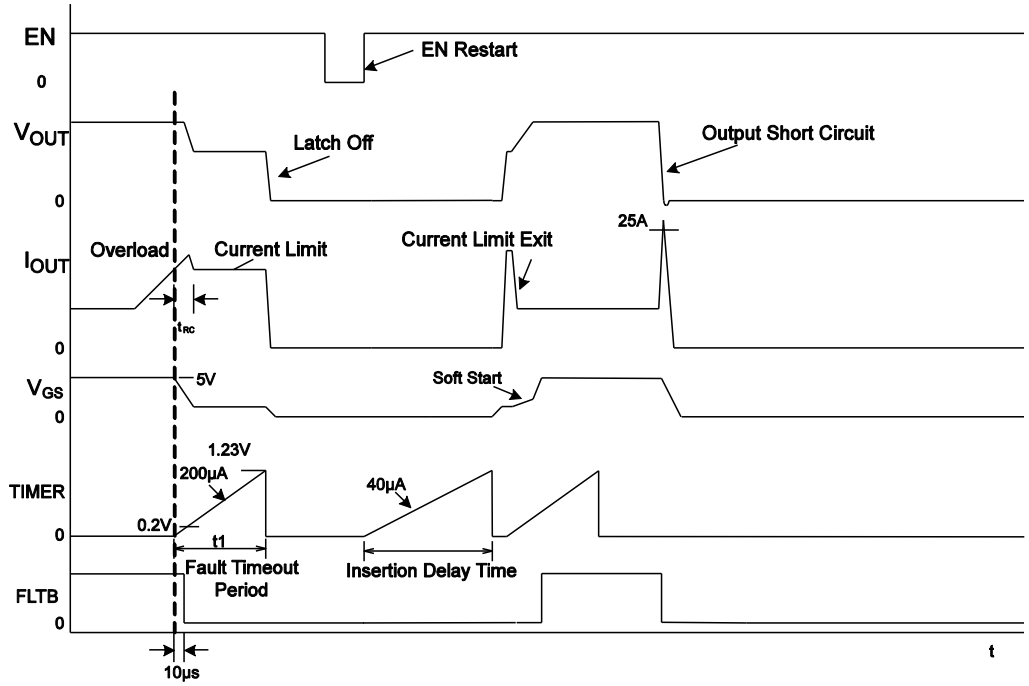


**Figure 2: OCP with Latch-Off Mode (AUTO is Pulled Low)**

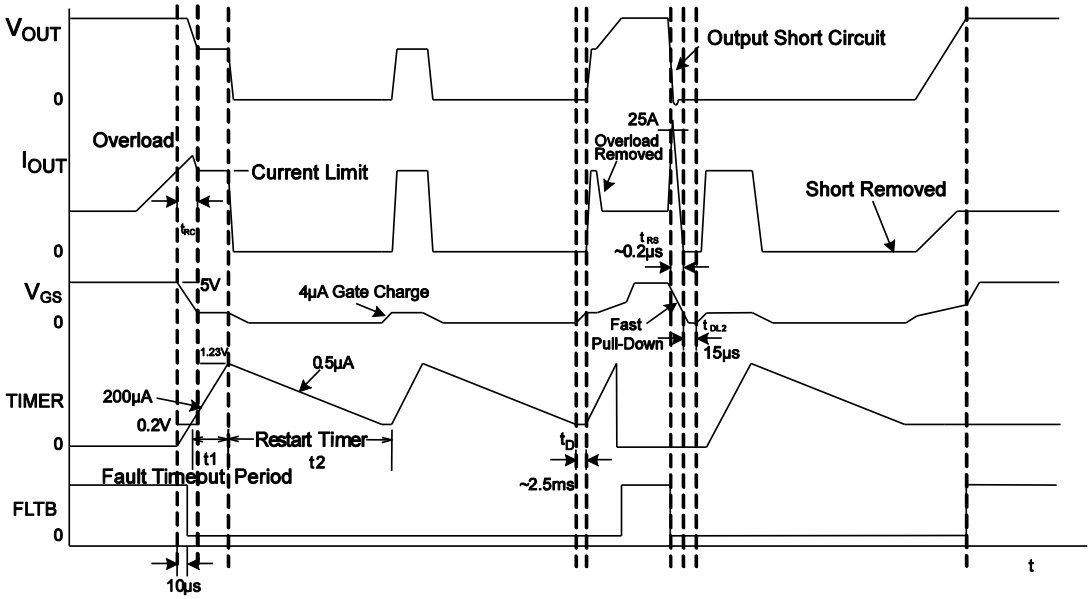


**Figure 3: OCP with Auto-Retry Mode (AUTO is Pulled High)**


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### Power Good (PG)

The power good (PG) pin indicates whether $V_{OUT}$ is within the normal range, relative to $V_{IN}$. PG is the open drain of a MOSFET. Pull the PG pin up to an external power supply via a 100kΩ resistor. During start-up, PG's output is pulled low. This directs the system to remain off, which minimizes the output load to reduce the inrush current and power dissipation during start-up.

The PG signal is pulled high once the device meets the following conditions:

- $V_{FB}$ exceeds 0.6V
- $V_{GS}$ exceeds 3V
- $V_{OUT}$ exceeds ($V_{IN}$ - 1V)

Then the system can draw full power.

If the feedback (FB) voltage ($V_{FB}$) drops below 0.54V, $V_{GS}$ drops below 3V, or $V_{OUT}$ drops below ($V_{IN}$ - 1V), then PG is pulled low.

PG is also pulled low if either the EN voltage ($V_{EN}$) drops below its falling threshold or $V_{IN}$ UVLO is triggered.

Without an input, PG remains at logic low in the presence of a pull-up supply.

### Fault Bar (FLTB)

The fault bar (FLTB) pin is an open-drain output that indicates whether a fault has occurred. Pull FLTB up to an external power supply via a 100kΩ resistor.

If the device reaches its $I_{LIMIT}$, or the die temperature exceeds the thermal shutdown threshold, then the MOSFET is shorted before start-up. The fault output is pulled low with a propagation delay (20µs) to indicate a fault has occurred. If a short occurs and the current reaches its secondary $I_{LIMIT}$ (25A), then FLTB is pulled low with an 8µs delay.

FLTB is pulled high once the part resumes normal operation, which means $V_{OUT}$ has exceeded the PG rising threshold, and the MOSFET is fully on ($V_{GS}$ > 3V).

### External Pull-Up Voltage for PG and FLTB

PG and FLTB require an external power supply. The open-drain output of PG can work with an external pull-up voltage, even while $V_{IN}$ is 0V and EN is disabled. Use a 100kΩ pull-up resistor for PG and FLTB.

### Start-Up Sequence

For hot-swap applications, the MP5056's input can experience a voltage spike or transient during the hot swap. This spike is caused by parasitic inductance on the input trace and input capacitor. An insertion delay time set by $C_{TIMER}$ stabilizes $V_{IN}$. $V_{IN}$ rises immediately, and a 30Ω resistor pulls the internal $V_{GS}$ low (see Figure 4).

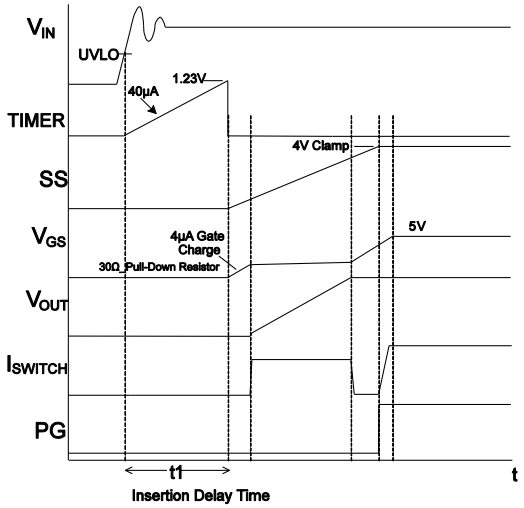


**Figure 4: Start-Up Sequence**

The TIMER pin is charged via a constant-current source (40µA) once $V_{IN}$ exceeds its UVLO threshold. If $V_{TIMER}$ reaches 1.23V, then a 4µA current source pulls up $V_{GS}$, and $V_{TIMER}$ drops. Once the gate voltage reaches its threshold ($V_{GSTH}$), $V_{OUT}$ rises. The soft-start capacitor ($C_{SS}$) determines the soft-start time ($t_{SS}$).

### Soft Start (SS)

$C_{SS}$ determines $t_{SS}$. Once the insertion delay time ends, a constant-current source that is proportional to $V_{IN}$ ramps up the SS voltage ($V_{SS}$). $V_{OUT}$ rises at a similar slew rate to $V_{SS}$.

$C_{SS}$ can be calculated with Equation (1):

$$C_{SS} = \frac{10 \times t_{SS}}{R_{SS}} \quad (1)$$

Where $R_{SS}$ is the soft-start resistor (2MΩ).

For example, a 100nF capacitor sets $t_{SS}$ at 20ms.

If the load capacitance is extremely large, the current required to maintain the preset $t_{SS}$ may exceed $I_{LIMIT}$. At this point, the load capacitor and $I_{LIMIT}$ determine the $V_{OUT}$ rise time.


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Float the SS pin to generate the minimum $t_{SS}$. A 4μA current source pulls up the gate of the MOSFET. The gate charge current controls the $V_{OUT}$ rise time. The minimum $t_{SS}$ is about 1ms.

### Enable (EN)

If $V_{EN}$ exceeds its rising threshold, then the part starts up. If $V_{EN}$ drops below its falling threshold, then the part shuts down.

If $V_{EN}$ drops below 0.6V, then the part goes into the lowest shutdown current mode. If $V_{EN}$ exceeds 0.6V, but is below the EN rising threshold, then the part remains in shutdown mode with a slightly larger current.

If EN enables the part, the insertion delay timer starts. Once the insertion delay time ends, the internal 4μA current source charges the MOSFET's gate. It takes about 1.5ms to charge $V_{GS}$ to its threshold value. Then $V_{OUT}$ rises according to the soft-start slew rate.

### Damaged MOSFET Detection

The MP5056 can detect a shorted pass MOSFET during start-up by treating output voltages that exceed ($V_{IN}$ - 1V) as a short on the MOSFET. The FLTB pin is pulled low to indicate a fault has occurred, and the MOSFET remains off. Once $V_{OUT}$ drops below ($V_{IN}$ - 1V), the device starts up and resumes normal operation.

### Internal VCC Sub-Regulator

The MP5056 has an internal 5V linear sub-regulator that powers the low-voltage circuitry. This regulator takes $V_{IN}$, and operates across the entire $V_{IN}$ range. If $V_{IN}$ exceeds 5V, then the regulator output is in full regulation. Lower input voltages result in lower output voltages. The regulator is enabled once $V_{IN}$ exceeds its UVLO threshold and $V_{EN}$ is high. In EN shutdown mode, the internal VCC regulator is disabled to reduce power dissipation.

### Output Discharge (PD Pin)

If the PD pin is connected to the output, then the part is in pull-down mode. If $V_{IN}$ drops below its UVLO threshold, or if $V_{EN}$ is between 0.6V and its rising threshold, then an integrated 500Ω pull-down resistor connected to the output discharges $V_{OUT}$. Connect a resistor between the PD and VOUT pins for a slower output drop. Float PD to disable this pull-down mode.

### Auto-Reset (AUTO Pin)

Float the AUTO pin to have the part operate in auto-retry mode. If the part exceeds its thermal limit or current limit timeout in auto-retry mode, then the part shuts down. It starts up again once the temperature drops 28°C or the restart timer is complete.

If the AUTO pin is pulled to ground, then the part operates in latch-off mode. In latch-off mode, the output latches off if a thermal fault or $I_{LIMIT}$ fault occurs. Toggle EN or cycle the power on VIN to remove the fault latch and restart the part.

### Under-Voltage Lockout (UVLO) Protection

If $V_{IN}$ drops below its UVLO threshold, then the output is disabled and the PG pin is pulled low. If $V_{IN}$ exceeds its UVLO threshold, then the output can be enabled via EN.

### Output Current Monitoring

The IMON pin provides a voltage that is proportional to $I_{OUT}$ (the current flowing through the power device). Tie a resistor to ground to set the output gain. Place a 100nF capacitor between the IMON and GND pins to smooth the indicator voltage.


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# APPLICATION INFORMATION

### Setting the Current Limit ($I_{LIMIT}$)

The MP5056's $I_{LIMIT}$ should exceed the maximum load current ($I_{LOAD_MAX}$). This allows for tolerance in the current-sense value. $I_{LIMIT}$ can be estimated with Equation (2):

$$I_{LIMIT} = \frac{0.6(V)}{R_{ISET}} \times 20 \times 10^4 (A) \quad (2)$$

Table 1 shows the resistor values for different $I_{LIMIT}$ settings.

**Table 1: Resistor Values for Different Current Limit Settings**

| $R_{ISET}$ (kΩ) | $I_{LIMIT}$ (A) |
|---|---|
| 7.5 | 15.9 |
| 10 | 12 |
| 20 | 6.08 |

Figure 5 shows the relationship between the ISET resistance ($R_{ISET}$) and $I_{LIMIT}$.

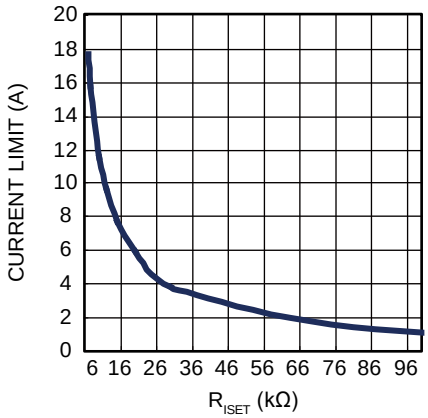


**Figure 5: $I_{LIMIT}$ vs. $R_{ISET}$**

### Current Monitoring

The MP5056 provides MOSFET current monitoring. Connect a resistor ($R_{IMON}$) to ground to set the output gain. The IMON current ($I_{IMON}$) can be calculated with Equation (3):

$$I_{IMON} = \frac{I_{MOSFET}}{10^5} \quad (3)$$

Where $I_{MOSFET}$ is the power MOSFET's current.

The IMON pin provides a voltage that is proportional $I_{OUT}$. Connect a 10kΩ resistor between the IMON and GND pins to obtain this voltage (100mV/A). Connect a 100nF capacitor between the IMON and GND pins to smooth the indicator voltage.

### Design Example

Figure 7 on page 18 shows the detailed application schematic. For more details, see the Typical Performance Characteristics section on page 8.

For more detailed device applications, refer to the related evaluation board datasheet.


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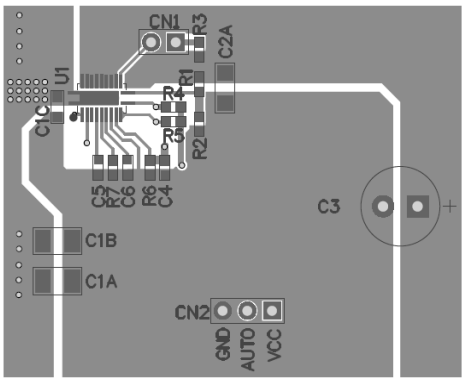
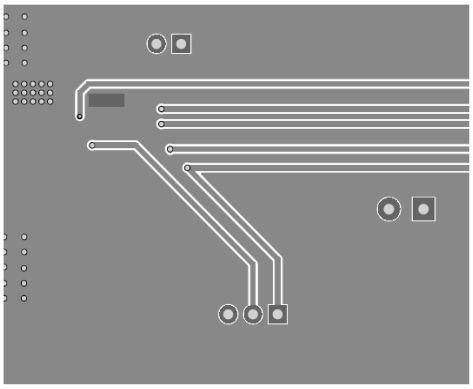
## PCB Layout Guidelines [7]

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 6 and follow the guidelines below:

1. Place the high-current paths (GND, VIN, and OUT) as close to the device as possible using short, direct, and wide traces.
2. Place a small bypass capacitor near the VIN pin to minimize transients on the input supply line.
3. Place the external feedback resistors near the FB pin.
4. Avoid placing vias on the FB trace.
5. Connect the VIN and GND pads to a large copper plane to improve thermal performance.
6. Place the input and output capacitors as close to the device as possible to reduce parasitic inductance.
7. Place multiple vias on the thermal pad, and provide a large copper area near the VIN pin to improve thermal performance. Ensure that all of the input pins are connected to obtain equal current distribution in all legs.
8. Place multiple vias on the thermal pad, and provide a large copper area near the OUT pin to improve thermal performance. Ensure that all of the output pins are connected to obtain equal current distribution in all legs.




**Top Silk and Top Layer**



**Bottom Layer and Bottom Silk**

**Figure 6: Recommended PCB Layout**

**Note:**

7) The recommended PCB layout is based on Figure 7 on page 18.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# TYPICAL APPLICATION CIRCUIT

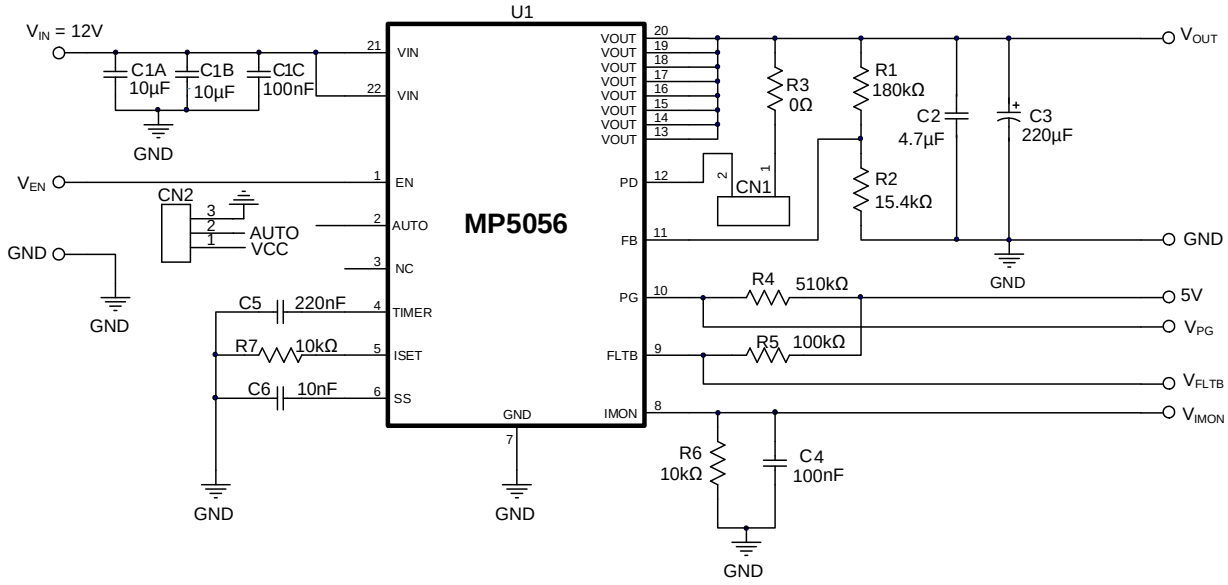


**Figure 7: Typical Application Circuit**


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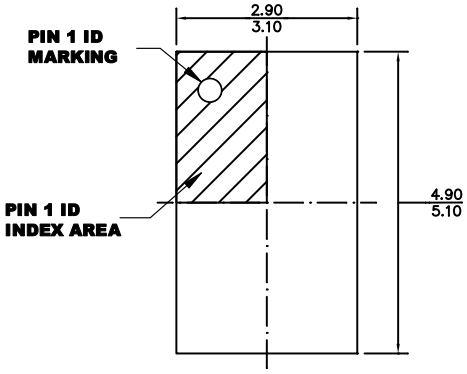
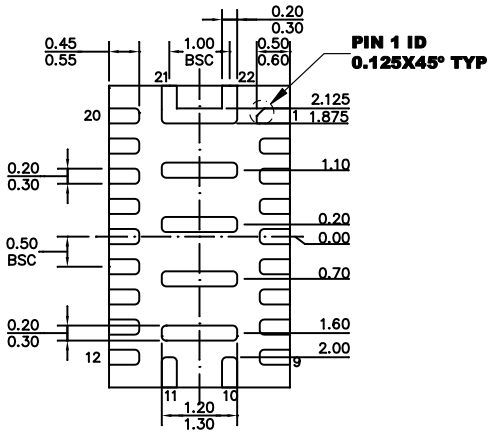
# PACKAGE INFORMATION

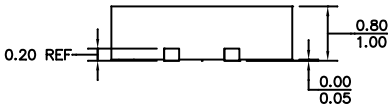
## QFN-22 (3mmx5mm)



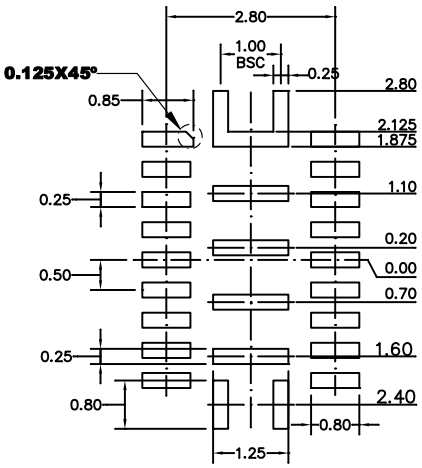

**TOP VIEW**




**BOTTOM VIEW**




**SIDE VIEW**




**RECOMMENDED LAND PATTERN**

**NOTE:**

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.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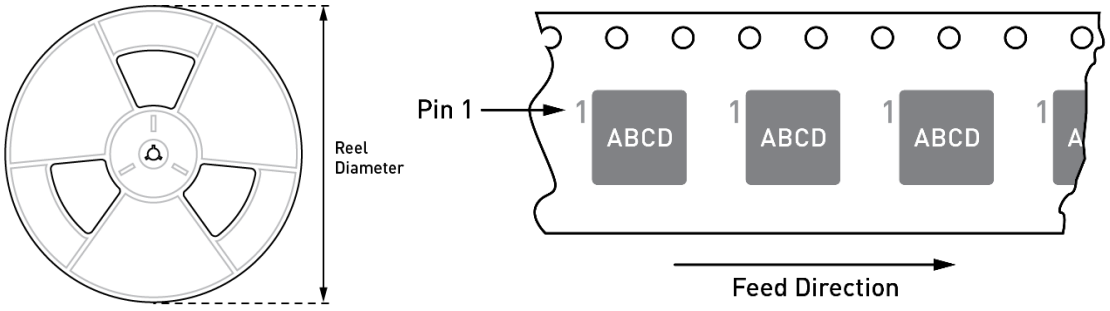
## CARRIER INFORMATION




| Part Number | Package Description | Quantity/ Reel | Quantity/ Tube | Quantity/ Tray | Reel Diameter | Carrier Tape Width | Carrier Tape Pitch |
|---|---|---|---|---|---|---|---|
| MP5056GQV-Z | QFN-22 (3mmx5mm) | 5000 | N/A | N/A | 13in | 12mm | 8mm |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## REVISION HISTORY

| Revision # | Revision Date | Description | Pages Updated |
|---|---|---|---|
| 1.0 | 10/3/2022 | Initial Release | - |

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