MP5030C

USB Charging Port Controller with Current Limit Switch, Supporting CDP, DCP, and QC3.0 Modes

DESCRIPTION

The MP5030C integrates a USB current-limit switch and charging port identification circuit. The MP5030C achieves 3A of continuous output current over a wide input supply range.

The output of the USB switch is current-limit programmable. The MP5030C supports dedicated charging port (DCP) and charging downstream port (CDP) schemes for battery charging specification (BC1.2), divider mode, 1.2V/1.2V mode, and quick-charge specification (QC 2.0/3.0) without the need for external user interaction.

The MP5030C provides linear line drop compensation for 5V outputs.

Full protection features include hiccup current limiting, input over-voltage protection (OVP), and thermal shutdown.

The MP5030C requires a minimal number of readily available, standard, external components to complete the USB switch and charging mode auto-detection solution. The MP5030C is available in a QFN-10 (1.5mmx2mm) package.

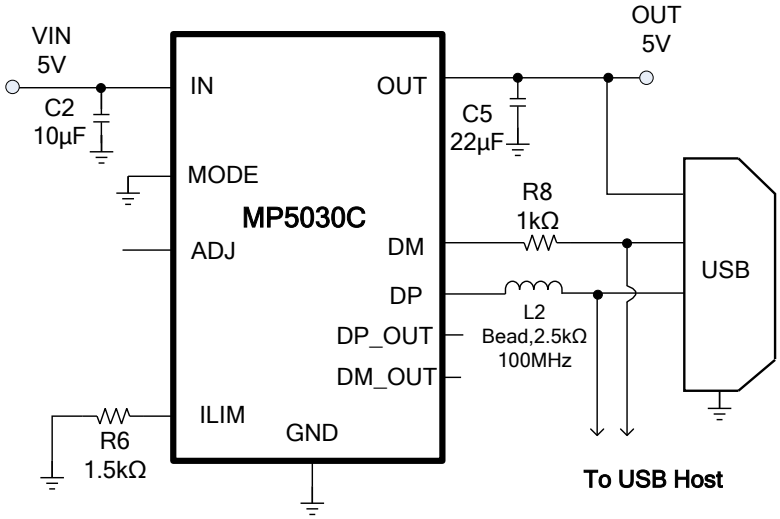
FEATURES

- Up to 14V Operating Input Voltage Range
- Support DCP Schemes for BC 1.2 without QC Mode, Divider Mode, and 1.2V/1.2V Mode
- Supports QC 3.0 Mode
- Support CDP Mode for USB 2.0 Data
- Line Drop Compensation for 5V Output
- Programmable High-Accuracy Current Limit
- 32mΩ Low $R_{DS(ON)}$ Power MOSFET
- Input Over-Voltage Shutdown Protection
- Compatible with Buck, Boost, AC/DC Converters
- Available in a QFN-10 (1.5mmx2mm) Package

APPLICATIONS

- USB Charging Downstream Port (CDP)
- USB Dedicated Charging Ports (DCP)

TYPICAL APPLICATION



CDP Mode Set-Up for USB2.0 Application

ORDERING INFORMATION

Part Number*	Package	Top Marking
MP5030CGQH	QFN-10 (1.5mmx2mm)	*See Below*

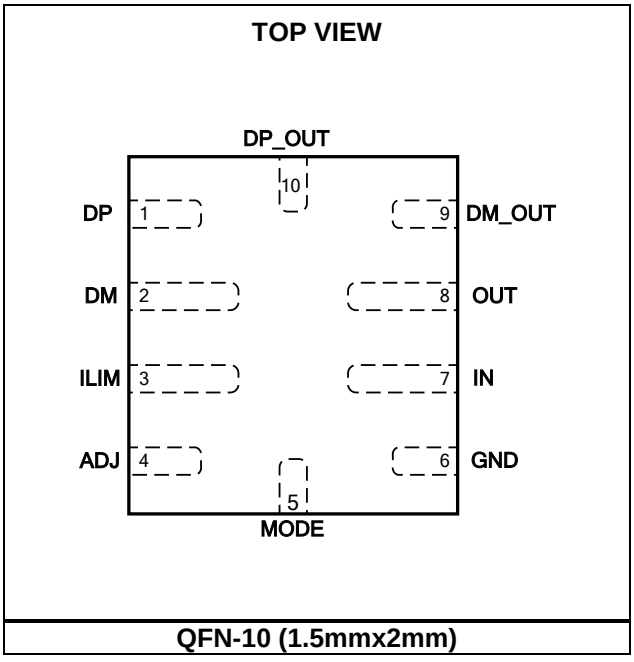
* For Tape & Reel, add suffix –Z (e.g. MP5030CGQH–Z)

TOP MARKING

GB
LL

GB: Product code of MP5030CGQH
LL: Lot number

PACKAGE REFERENCE



QFN-10 (1.5mmx2mm)

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) ..... -0.3V to +16V
Output voltage (V_{IN}) ..... -0.3V to +16V
All other pins..... -0.3V to +6V
Junction temperature.....150°C
Lead temperature .....260°C
Continuous power dissipation (T_A = +25°C) (2)
.....2.23W

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....Up to 14V (4)
Output voltage (V_{OUT}).....follow with V_{IN}
Output current (I_{OUT}).....up to 3A
Operating junction temp. (T_J). .. -40°C to +125°C

Thermal Resistance	***θ_{JA}***	***θ_{JC}***	
QFN-10 (1.5mmx2mm)			
EV5030C-QH-00C	56	18	... °C/W
JESD51-7 (5)	130	25	... °C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage. Measured on EV5030C-QH-00A, 2-layer PCB, 4.4cmx2.9cm, 2Oz copper.
3) The device is not guaranteed to function outside of its operating conditions.
4) For lower V_{IN} applications, refer to the Operation section on page 12.
5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, T_J = -40°C to 125°C (6), Typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
V_{IN} under-voltage lockout rising threshold	V_{IN_UVLO1}	ADJ starts to work	2.7	3.0	3.3	V
UVLO hysteresis	$V_{UVLOHYS1}$			880		mV
Second V_{IN} under-voltage lockout rising threshold	V_{IN_UVLO2}	Power MOSFET turn-on	3.7	3.9	4.1	V
Second UVLO hysteresis	$V_{UVLOHYS2}$			500		mV
Start-up delay	T_{Delay}	From UVLO rising to V_{OUT} = 100mV	4	5	6	ms
Supply current	I_Q	V_{IN} = 5V, no load		250	320	µA
USB Power MOSFET						
On resistance	R_{DSON}	V_{IN} = 5V		32	50	mΩ
Input discharge resistance	R_{DIS}	Turn-on during V_{IN} OVP or H to L voltage change period		72		Ω
Soft-start time	T_{SS}	V_{IN} = 5V, no load, 10% to 90%		290		µs
Current Limit Set						
USB current limit	I_{LIMIT}	R_{ILIM} = 1.5kΩ, V_{OUT} drops 10%	3.13	3.35	3.57	A
Output Voltage Control						
Default V_{IN}	V_{IN_Def1}	I_{OUT} = 0A, T_J = +25°C	-1%	5	+1%	V
	V_{IN_Def2}	T_J = -40°C to +125°C	-2%	5	+2%	
9V_{IN} voltage	V_{IN_9}	T_J = +25°C	-2%	9	+2%	V
12V_{IN} voltage	V_{IN_12}	T_J = +25°C	-2%	12	+2%	V
V_{ADJ} sink current capability	I_{sink}	V_{FB} = 800mV	500			µA
Line drop compensation	$V_{IN\_5\_C}$	I_{OUT} = 2.4A, only 5V_{IN} active		220	350	mV
Protection						
V_{IN} OVP threshold	V_{OV_TH}	V_{IN} rising edge, V_{IN} = 5V	110	115	120	%
		V_{IN} rising edge, V_{IN} = 9V	110	115	120	
		V_{IN} rising edge, V_{IN} = 12V	110	115	120	
V_{IN} OVP recovery	$V_{OV\_Recovery}$	Reset mode to 5V default	5.25	5.4	5.55	V
OVP deglitch time (7)	T_{OVP_DE}			10		µs
OCP on time of hiccup	T_{HIC_ON}			2		ms
OCP off time of hiccup	T_{HIC_OFF}			2		s
Shutdown temperature (7)	T_{STD}			160		°C
Hysteresis (7)	T_{HYS}			35		°C
MODE Selection						
MODE voltage	V_{MODE}	MODE = high, DCP mode with QC function	2.1			V
		MODE = float, DCP mode without QC function	0.9		1.9	
		MODE = low, CDP mode			0.5	

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_J = -40°C to 125°C (6), Typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
BC 1.2 DCP Mode						
DP/DM short resistance	R_{DP/DM_Short}	V_{DP} = 0.8V, I_{DM} = 1mA, T_J = +25°C			50	Ω
1.2V/1.2V Mode						
DP/DM output voltage	$V_{DP/DM\_1.2V}$		1.1	1.2	1.3	V
DP/DM output impedance	$R_{DP/DM\_1.2V}$			300		kΩ
Divider Mode						
DP/DM output voltage	$V_{DP/DM}$	V_{IN} = V_{OUT} = 5V	2.5	2.7	2.85	V
DP/DM output impendence	$R_{DP/DM}$		18	22	28	kΩ
Quick Charge 3.0 Mode						
Data detect voltage	V_{DAT_REF}		0.25	0.3	0.4	V
Output voltage select ref	V_{SEL_REF}		1.8	2	2.2	V
DP output impendence	R_{DP_QC}		250	350	450	kΩ
DM output impendence	R_{DM_QC}		15	20	25	kΩ
DM low glitch time	T_{Glitch_DM}			10		ms
DP high glitch time	T_{Glitch_DP}		1000		1500	ms
Output voltage change glitch time	$T_{Glitch\_V\_Change}$		20	40	60	ms
V_{BUS} voltage step	V_{step}		150	200	250	mV
CDP Mode						
DM CDP output voltage	V_{DM_SRC}	VDP = 0.6V	0.5	0.6	0.7	V
DP rising lower window threshold for V_{DM_SRC} activation	V_{DAT_RE}		0.25	0.3	0.4	V
DP rising lower window threshold hysteresis for V_{DM_SRC} activation	$V_{DAT\_RE\_HYS}$			50		mV
DP rising upper window threshold for V_{DM_SRC} de-activation	V_{LGC_SRC}			1.9	2	V
DP rising upper window threshold hysteresis for V_{DM_SRC} de-activation	$V_{LGC\_SRC\_HYS}$			200		mV
V_{DM_SRC} on/off deglitch time	$V_{DM\_SRC\_Deglitch}$		3.8	4.8	5.8	ms
RDP_Down, RDM_Down	R_{DP/DM_Down}		14.25	19.5	24.8	kΩ
DP/DM switch on resistance	$R_{ON\_DP/DM}$			2.5		Ω
DP to DP_OUT SW on cap (7)	C_{DP}	Same for DM switch		5.3		pF
3dB bandwidth of analog data SW (7)	F_{BW}		500			MHz

NOTES:

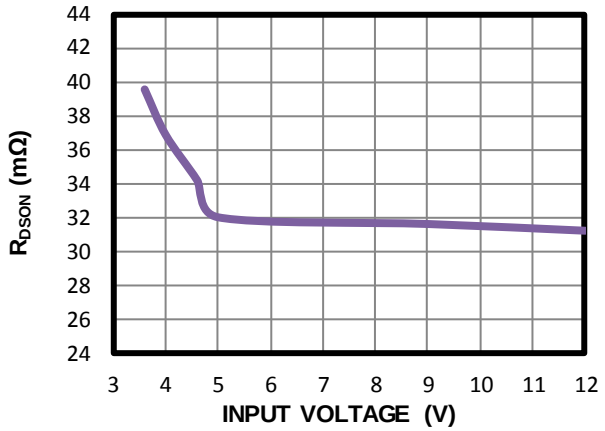
6) Guaranteed by over-temperature correlation, not tested in production.

7) Guaranteed by engineering sample characterization.

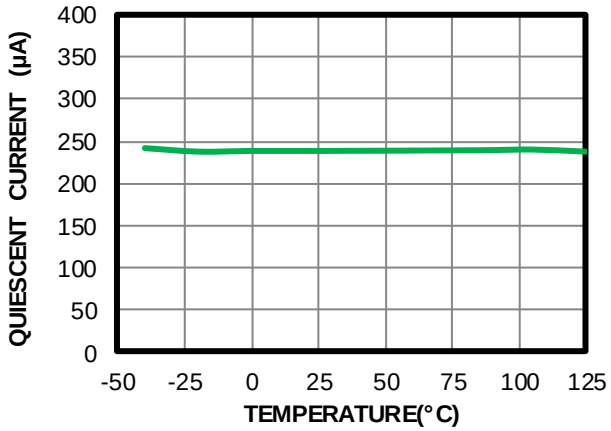
TYPICAL CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 5V, R_{ILIM} = 1.5kΩ, T_A = 25°C, unless otherwise noted.

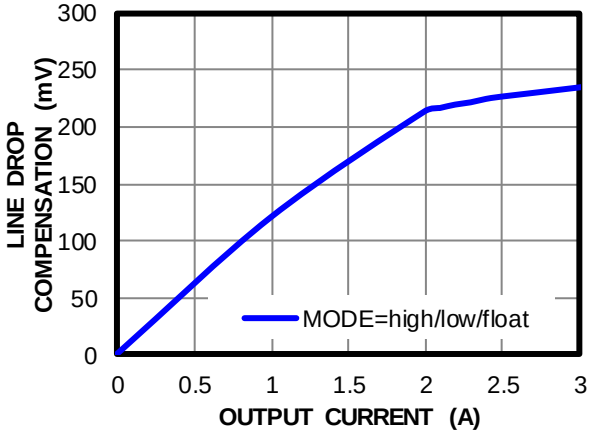
$R_{DS(ON)}$ vs. Input Voltage



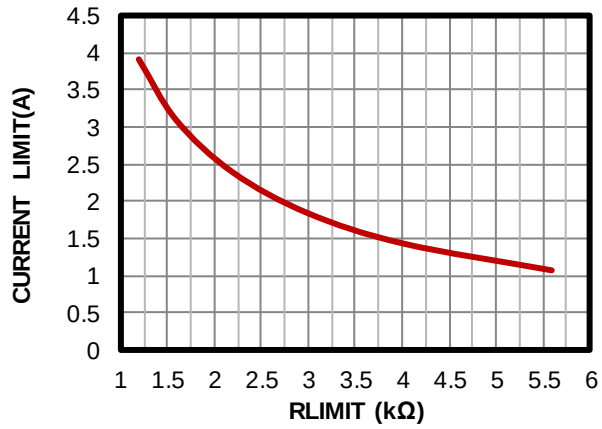
Quiescent Current vs. Temperature



Line Drop Compensation



Current Limit vs. R_{LIMIT}

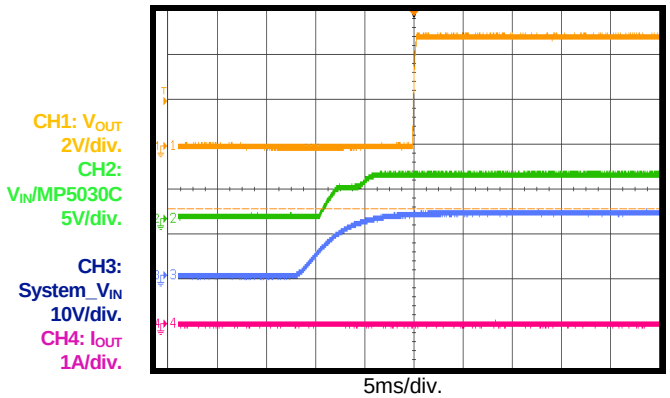


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 5V, R_{ILIM} = 1.5kΩ, T_A = 25°C, unless otherwise noted. Connect the MP5030C input to the MP2499A output. System_VIN is the MP2499A input voltage.

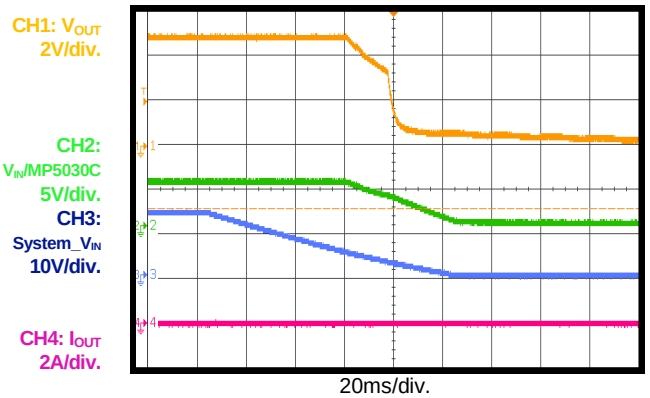
Start-Up through Input Voltage

I_{OUT} = 0A



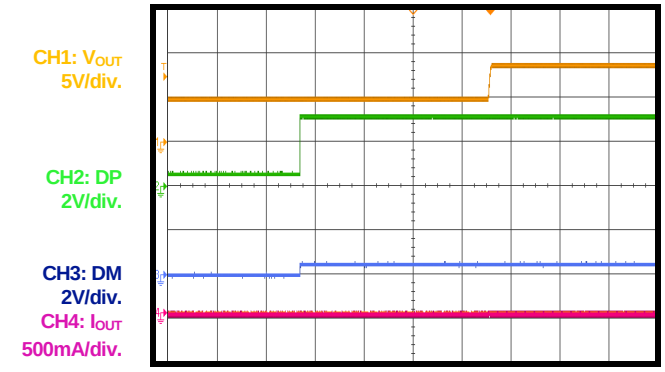
Shutdown through Input Voltage

I_{OUT} = 0A



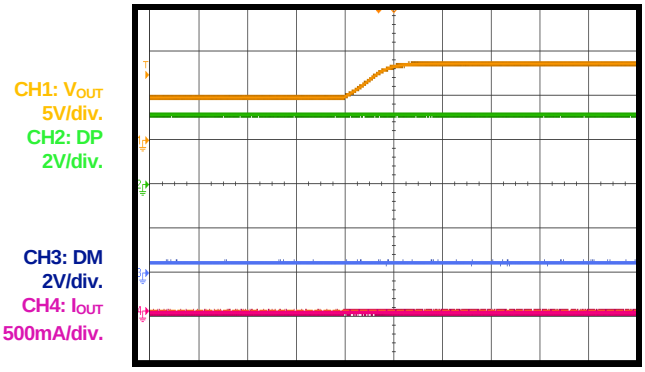
Mode Transition from 5V to 9V

I_{OUT} = 0A, from QC 2.0_5V to 9V



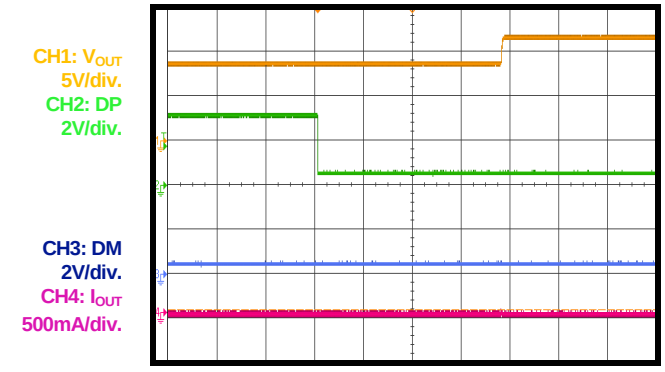
Mode Transition from 5V to 9V

Zoom in 5V to 9V slew rate



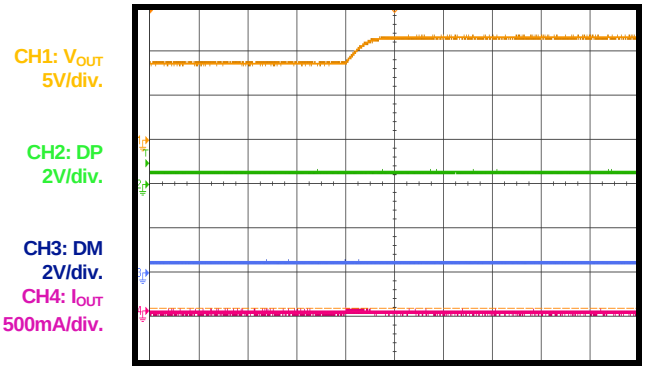
Mode Transition from 9V to 12V

I_{OUT} = 0A, from QC 2.0_9V to 12V



Mode Transition from 9V to 12V

Zoom in 9V to 12V slew rate

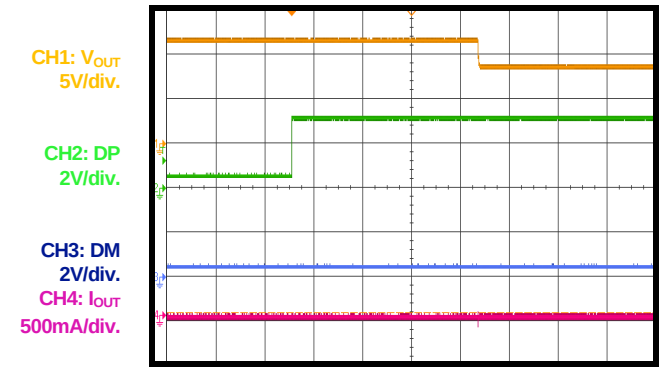


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 5V, R_{ILIM} = 1.5kΩ, T_A = 25°C, unless otherwise noted. Connect the MP5030C input to the MP2499A output. System_VIN is the MP2499A input voltage.

Mode Transition from 12V to 9V

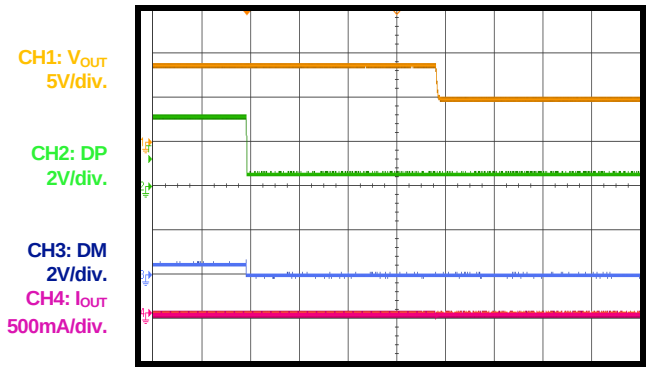
I_{OUT} = 0A, from QC 2.0_12V to 9V



10ms/div.

Mode Transition from 9V to 5V

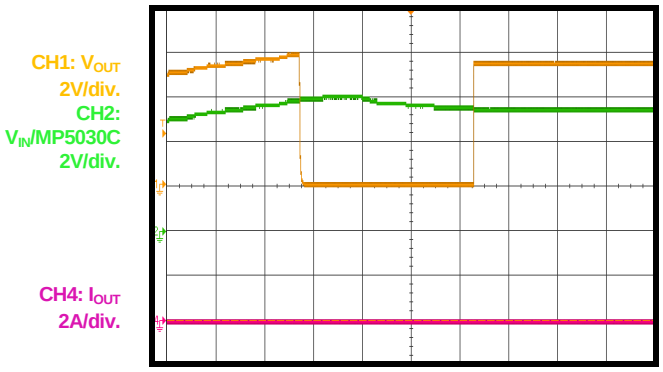
I_{OUT} = 0A, from QC 2.0_9V to 5V



10ms/div.

Input Over-Voltage Protection

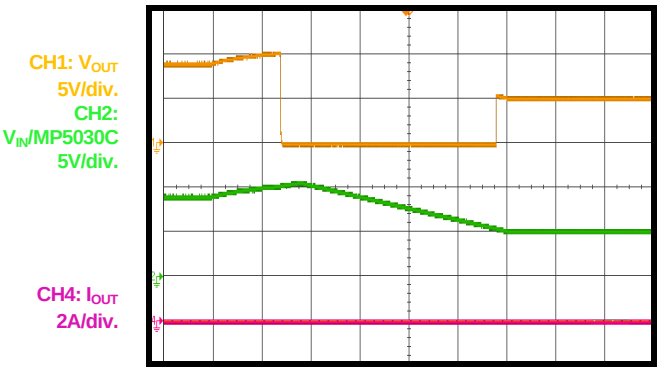
QC 5V Mode, I_{OUT} = 0A



1s/div.

Input Over-Voltage Protection

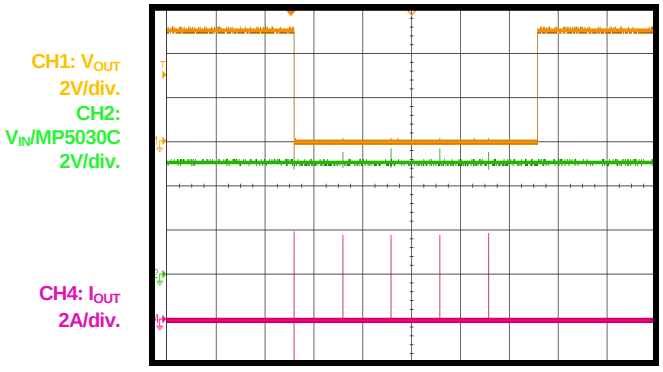
QC 9V Mode, I_{OUT} = 0A



2s/div.

Short-Circuit Protection Entry and Recovery

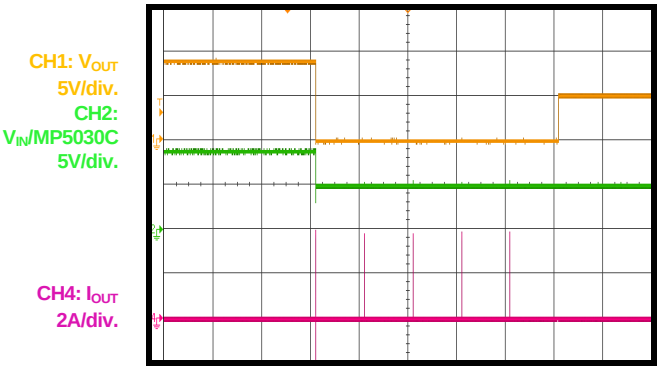
V_{IN} = 5V, I_{OUT} = 0A



2s/div.

Short-Circuit Protection Entry and Recovery

V_{IN} = 9V, I_{OUT} = 0A

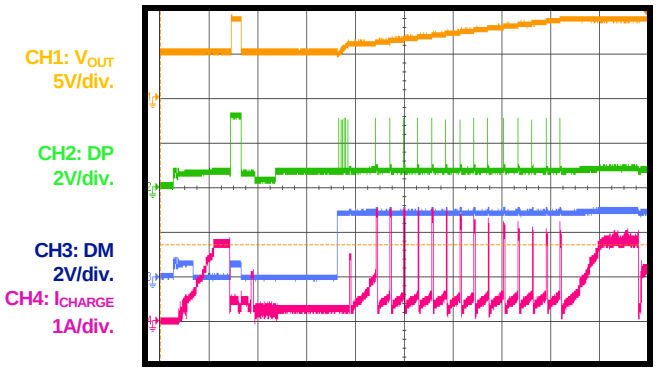


2s/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 5V, R_{ILIM} = 1.5kΩ, T_A = 25°C, unless otherwise noted. Connect the MP5030C input to the MP2499A output. System_VIN is the MP2499A input voltage.

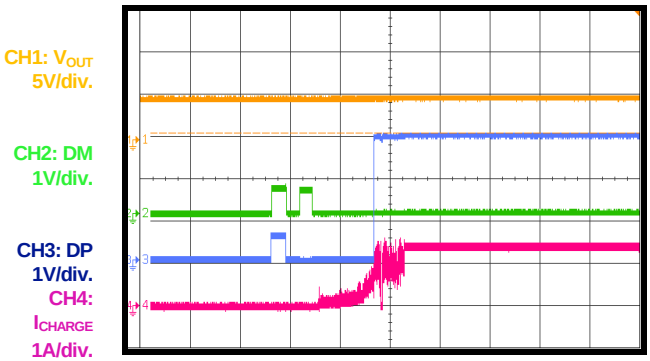
QC 3.0 Device Charging Test



2s/div.

CDP Mode Detection

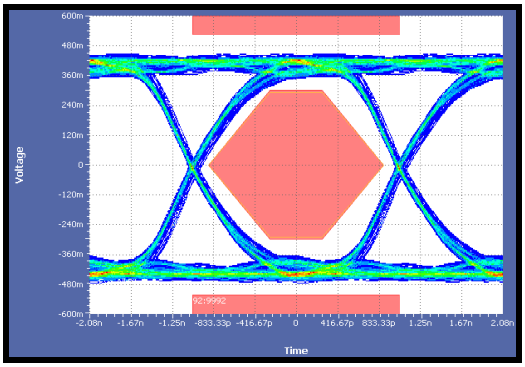
Mobile phone plug-in



200ms/div.

Eye Pattern Test

Recommended CDP mode set-up



PIN FUNCTIONS

Package Pin #	Name	Description
1	DP	**D+ data line to USB connector.** DP is the input/output used for handshaking with portable devices.
2	DM	**D- data line to USB connector.** DM is the input/output used for handshaking with portable devices.
3	ILIM	**Set the current limit level.** Place a resistor between ILIM and GND to achieve a high-accuracy current limit.
4	ADJ	**Output voltage adjustment.** ADJ sinks a current from the upstream DC/DC converter's FB pin to ground to regulate the DC/DC converter's output voltage. ADJ also supports line drop compensation.
5	MODE	**USB mode control.** Float MODE to operate the USB in DCP mode without the QC function. Pull MODE high to operate the USB in DCP mode with the QC function. Pull MODE low to operate the USB in CDP mode. MODE has a 1MΩ pull-up resistor to an internal +1.2V source.
6	GND	**Ground.**
7	IN	**Supply voltage.**
8	OUT	**Output of the USB current limit switch.**
9	DM_OUT	**D- data line to the USB host controller.**
10	DP_OUT	**D+ data line to the USB host controller.**

BLOCK DIAGRAM

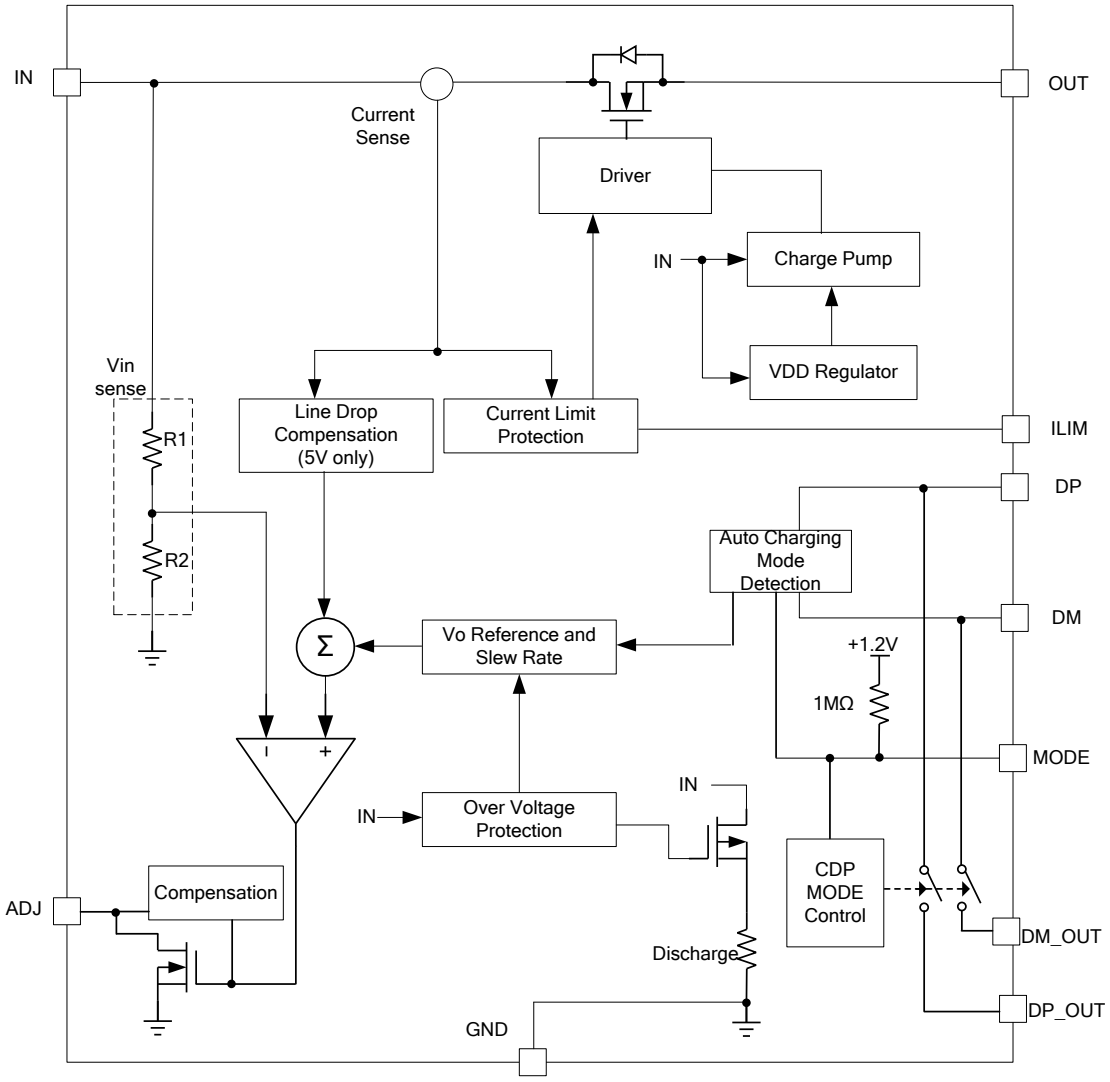


Figure 1: Functional Block Diagram

OPERATION

The MP5030C integrates a USB current-limit switch and charging port identification circuit. The MP5030C achieves 3A of continuous output current over a wide input supply range.

The output of the USB switch is current-limited with an adjustable current-limit threshold. The MP5030C supports the quick-charge specification (QC 3.0) and is backwards-compatible with QC 2.0. The MP5030C also supports DCP/CDP schemes for battery charging specification (BC1.2), divider mode, and 1.2V/1.2V mode without the need for external user interaction.

The MP5030C provides line drop compensation for a 5V output. Fault condition protection includes hiccup current limiting, input over-voltage protection (OVP), and thermal shutdown.

Operation Supply Voltage

The MP5030C has a two-stage input voltage threshold. The first threshold is around 3V, and the second threshold is the under-voltage lockout (UVLO) of the power MOSFET. When V_{IN} is higher than the first threshold, the MP5030C's ADJ block starts working and sinks a current to adjust the upstream regulator's output to an accurate 5V. Afterward, the MP5030C enters a fully working state.

Under-Voltage Lockout (UVLO)

UVLO protects the chip from operating at an insufficient supply voltage. The MP5030C's second UVLO comparator monitors the input voltage. Once the input voltage is higher than the second UVLO threshold, the power MOSFET starts to turn on with a controlled slew rate after a fixed delay.

Internal Soft Start (SS)

The internal soft-start prevents the output voltage from inrush current and overshooting during start-up.

MODE Selection

The MP5030C supports DCP and CDP modes through MODE control. Pull MODE high to operate the USB in DCP mode with the QC function. Float MODE to operate the USB in DCP mode without the QC function. Pull MODE low to operate the USB in CDP mode.

In DCP mode, the MP5030C can provide power for USB devices with protocol auto-detection. It supports the following charging schemes:

- USB battery charging specification BC1.2/Chinese Telecommunications Industry
- Standard YD/T 1591-2009
- Divider mode
- 1.2V/1.2V mode
- Quick-charge mode 2.0
- Quick-charge mode 3.0 (3.6 - 12V)

For better data transmission performance in CDP mode, use the MP5030C in USB CDP mode for handshaking. Bypass DP to DP_OUT. DM to DM_OUT switches internally (see Figure 2).

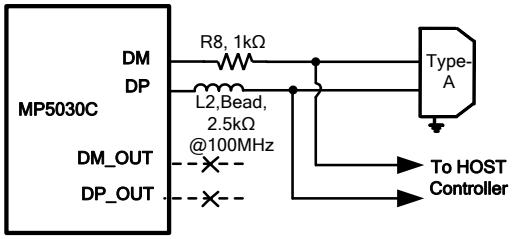


Figure 2: CDP Mode Set-Up

In CDP mode, the bus voltage (V_{BUS}) is always around 5V with current limit and line drop compensation (see Table 1).

Table 1: MODE Selection

MODE Status	Supported Charge Mode
Logic high	DCP mode, divider mode, QC2.0, QC3.0 mode, 1.2V/1.2V mode
Float	DCP mode without QC function, divider mode, 1.2V/1.2V mode
Logic low	CDP mode, $5V_{OUT}$ with line drop compensation

Connect DP and DM with a 150Ω resistor for DCP without QC mode.

Line Drop Compensation

The MP5030C can compensate for an output voltage drop, such as high impedance caused by a long trace, to maintain a fairly constant 5V load-side voltage. Line drop compensation is achieved through ADJ. The MP5030C increases the input voltage by 220mV at a 2.4A output current (see Figure 3).

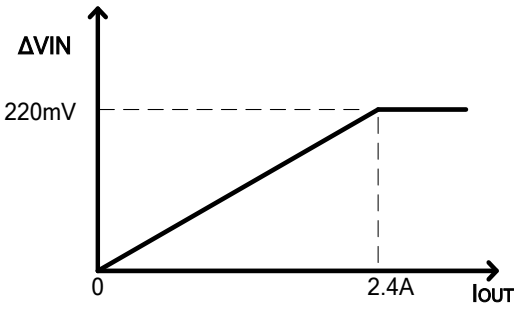


Figure 3: Line Drop Compensation

V_{ADJ} sinks a controlled current slowly. The line drop compensation amplitude increases linearly as the load current increases.

In no-load condition, if the input voltage is lower than 5V (typical), ADJ sinks a current to regulate the upstream regulator's output voltage to 5V. If the input voltage is higher than 5V (typical), the MP5030C no longer regulates the input voltage.

Input Over-Voltage and Discharge

To protect the downstream device from an over-voltage condition, the MP5030C provides an input over-voltage protection (OVP) shutdown function. Since the MP5030C supports the QC 3.0 protocol, it has a dynamic OVP threshold.

An accurate and fast comparator monitors the over-voltage condition of the input. If the input voltage rises above the threshold, the gate of the internal MOSFET is pulled low quickly, and the power MOSFET is shut down. Simultaneously, the input-to-ground discharge path is active. When the input voltage falls below 5.4V (typical), the MP5030C exits OVP mode.

The OVP shutdown function is blanked during the high-to-low voltage mode change period.

The input-to-ground discharge resistance is always active during the high-to-low voltage mode change period. The discharge path is turn-off when FB is lower than 108% times the reference voltage (V_{REF}) with 20ms of additional delay (see Figure 4).

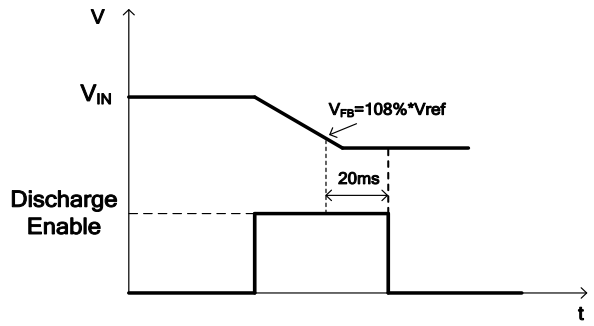


Figure 4: Input Discharge during High Voltage to Low Voltage Transition

QC mode is reset during the OVP rising edge.

Over-Current Protection (OCP)

The MP5030C provides a constant current limit. The current limit threshold is adjustable by an external resistor.

Once the device reaches its current limit threshold, the internal circuit regulates the gate voltage to hold the current in the power MOSFET constant.

The external resistor (R_{Limit}) can set the current limit threshold. If an over-current (OC) condition occurs but V_{OUT} is higher than 3.5V, the MP5030C works at a constant current (CC) limit mode without hiccup mode. If the OC is triggered and V_{OUT} is lower than 3.5V for 2ms, the MP5030C enters hiccup mode. In hiccup mode, the MP5030C turns off the power MOSFET (see Figure 5).

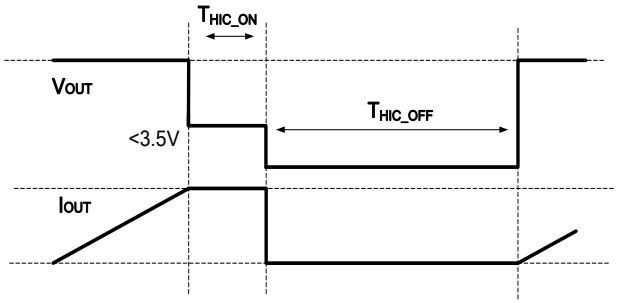


Figure 5: Over-Current Protection

Short-Circuit Protection (SCP)

If the load current increases rapidly due to a short circuit, the current may exceed the current-limit threshold greatly before the control loop can respond. If the current reaches an internal secondary current-limit level (about 6A), a fast turn-off circuit activates to turn off the power MOSFET. This limits the peak current through the switch to limit the input voltage drop. The typical fast-off response time value is 700ns. If the fast off-works, the power MOSFET remains off for 80μs. Afterward, the power MOSFET turns on again. If the part is still in a short-circuit condition, the MP5030C treats this as an over-current condition and enters hiccup mode or thermal shutdown. After the short-circuit condition is removed, the MP5030C recovers automatically.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 160°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 135°C), the chip is enabled again.

APPLICATION INFORMATION

Selecting the Input Capacitor

Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. A 22µF ceramic capacitor is recommended for most applications. The input capacitor must also consider pre-stage converter stability. The input capacitor of the MP5030C is the output capacitor of the converter. Ensure that the converter is stable with an additional output capacitor.

Selecting the Output Capacitor

Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. A 22µF ceramic capacitor is recommended for most applications.

Selecting the ILIM Resistor

The current limit value can be set by the ILIM resistor. See the current limit vs. ILIM resistor graph on page 6. Connecting the ILIM resistor to GND can set a maximum current limit of 4.3A. The current limit threshold should be 20% higher than the maximum load current. For example, if the system's full load is 3A, set the current limit to 3.6A.

Selecting the V_{ADJ} Resistor

ADJ has an internal, controlled, current sink. Line drop compensation is achieved through ADJ. The ADJ sink current capability is 500µA. It is recommended that the pre-side converter use a kΩ-level feedback resistor. The current through the high-side feedback resistor should be less than 500µA. Select R1 with Equation (1):

$$R1(k\Omega) > \frac{V_{OUT}(V) - V_{FB}(V)}{0.5} \quad (1)$$

There is another V_{ADJ} configuration to limit the maximum output voltage. Insert a resistor (R7) between FB and V_{ADJ}. With R7, the maximum output voltage can be limited by Equation (2):

$$V_{OUT\_Max}(V) = \frac{R_1 + R_2 // R_7}{R_2 // R_7} \times V_{FB}(V) \quad (2)$$

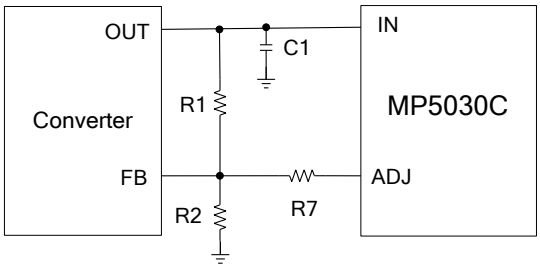


Figure 6: V_{ADJ} Set Maximum V_{OUT}

Other Considerations

The upstream DC/DC converter must have a current-limit threshold higher than the MP5030C's current limit.

PCB Layout Guidelines [8]

Efficient PCB layout is critical for stable operation and thermal dissipation. For best results, refer to Figure 7 and follow the guidelines below.

1. Use short, direct, and wide traces to connect the IC's IN/OUT pins.
2. Add vias under the IC.
3. Route the OUT trace on both PCB layers.
4. Place a ceramic input decoupling capacitor as close to IN and GND as possible to improve EMI performance.
5. Keep the V_{ADJ} trace to the pre-side converter FB pin as short as possible to prevent noise injection.

NOTE:

8) The recommended layout is based on the Typical Application Circuit in Figure 8 through Figure 10.

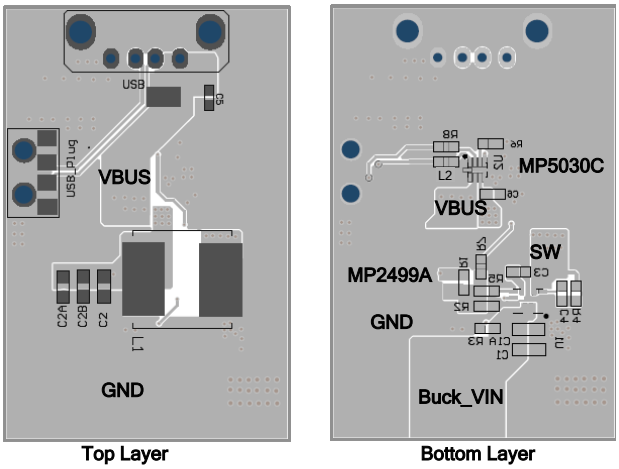


Figure 7: Recommended Layout

TYPICAL APPLICATION CIRCUITS

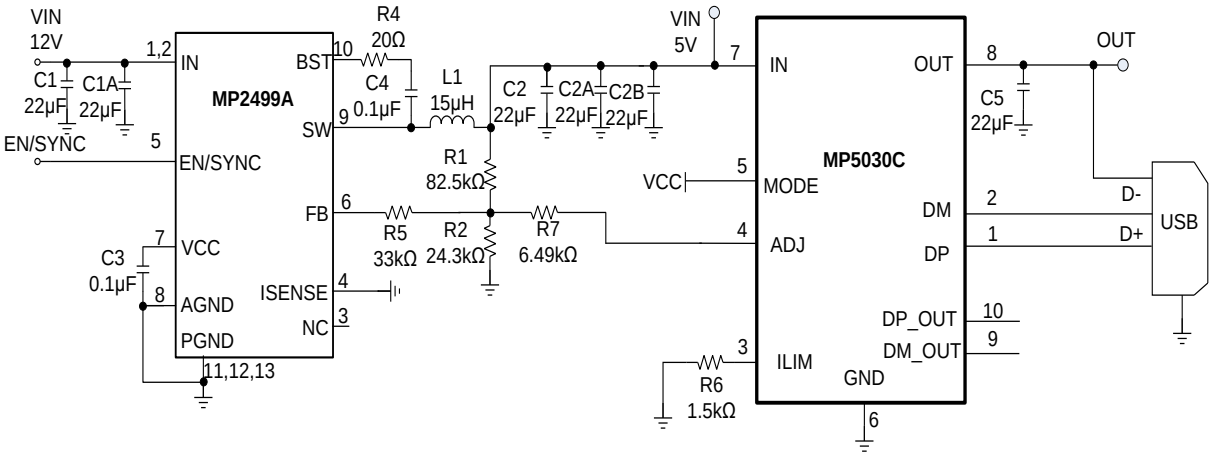


Figure 8: MP5030C + MP2499A for CLA Car Charger, DCP Mode w/ QC

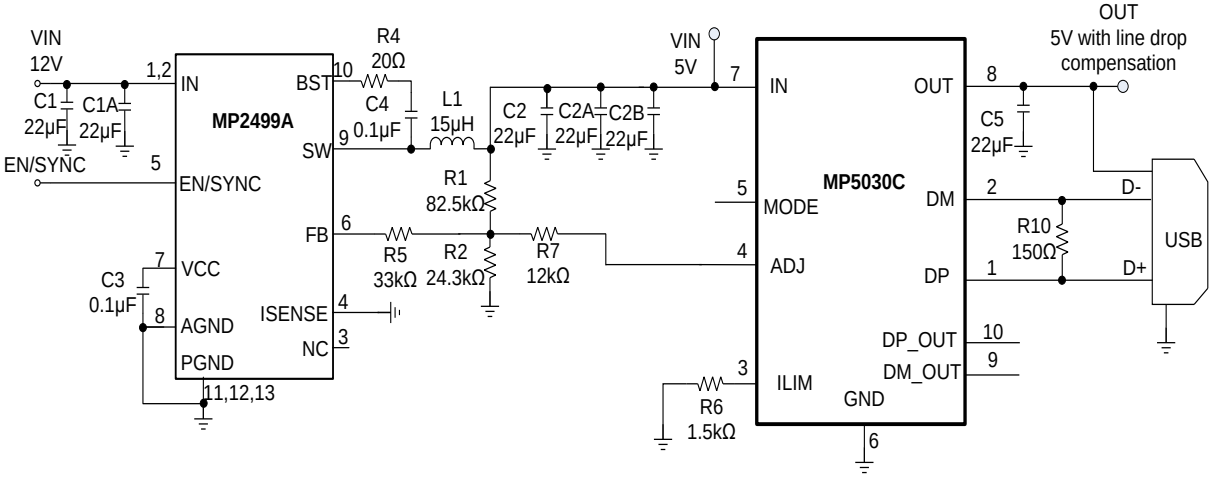


Figure 9: MP5030C + MP2499A for CLA Car Charger, DCP Mode w/o QC

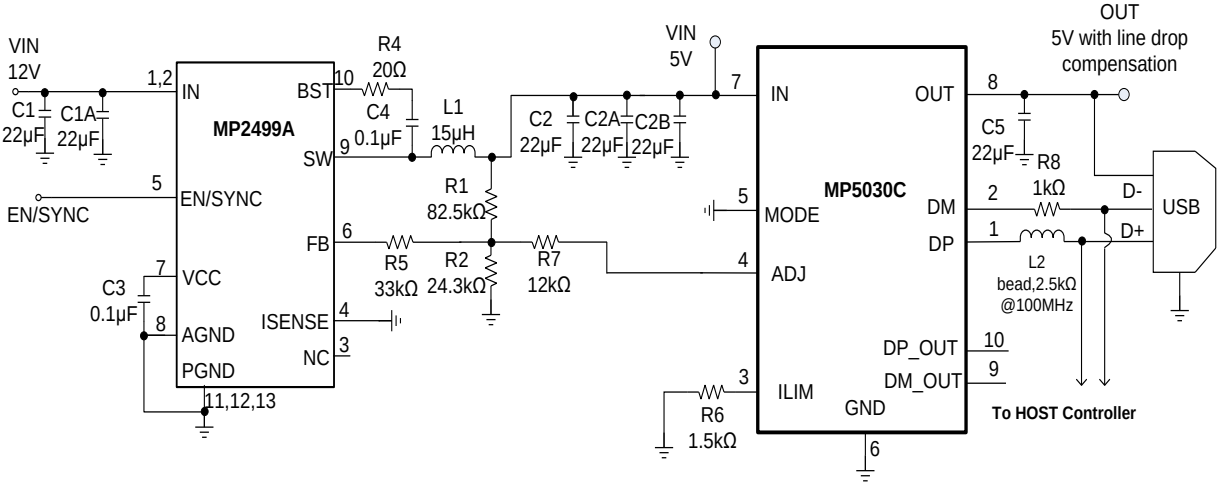
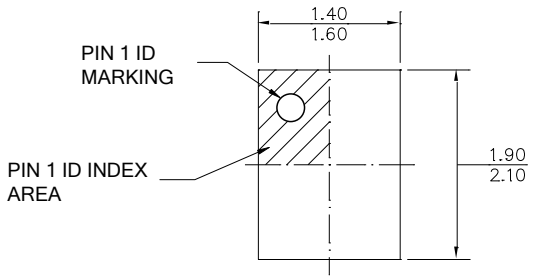


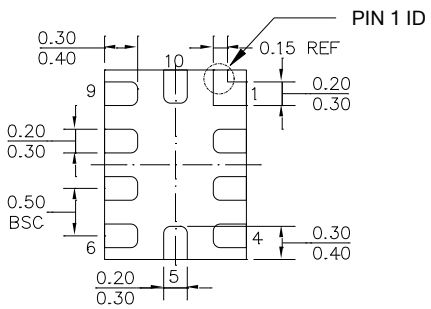
Figure 10: MP5030C + MP2499A for CDP Mode

PACKAGE INFORMATION

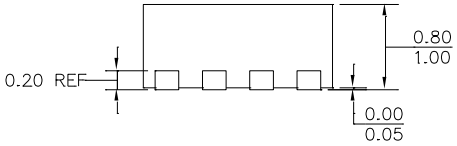
QFN-10 (1.5mmx2mm)



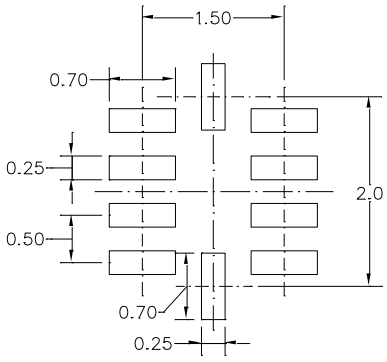
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.