MP5024

16V, 20A, 2.8mΩ $R_{DS(ON)}$, Hot-Swap Intelli-Fuse Solution

DESCRIPTION

The MP5024 is a hot-swap protection device designed to protect circuitry on its output from transients on its input. It also protects its input from undesired shorts and transients coming from its output. The device can achieve up to 20A of continuous output current (I_{OUT}) per device at room temperature.

The device limits the power supply voltage drop by limiting the inrush current to the load while a circuit card is inserted into a live backplane power source. It limits the internal MOSFET current (I_{FET}) by controlling the gate voltage (V_{GATE}) via a low-power resistor connected from ISET to ground and a soft-start ramp.

The MP5024 provides many features to simplify system design, such as an integrated current mirror to monitor I_{OUT} and integrated on-die temperature-sensing. This eliminates the need for an external current-sense power resistor, power MOSFET, and temperature-sense device.

The MP5024 provides rich fault protections, such as input voltage (V_{IN}) over-voltage protection (OVP), I_{OUT} over-current protection (OCP), short-circuit protection (SCP), and over-temperature protection (OTP). The MP5024 detects power MOSFET gate, source, and drain short conditions. The fault status can be indicated with the fault report output (FLT#/ALT#). The MP5024 also provides power good (PG) indication.

The PMBus interface provides V_{IN}, input current (I_{IN}), input energy (E_{IN}), output voltage (V_{OUT}), I_{OUT}, input power (P_{IN}), and output power (P_{OUT}) telemetry. The MP5024 monitors and reports fault statuses through the PMBus interface.

The MP5024 is available in a QFN-33 (3.5mmx4.5mm) package.

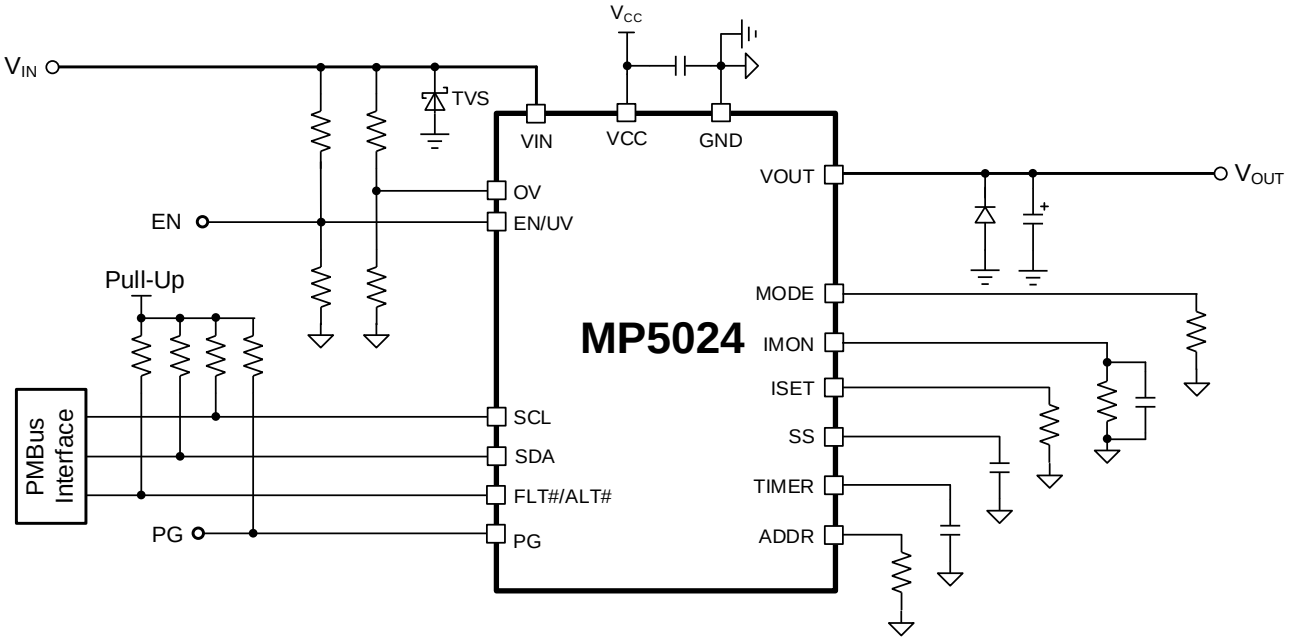
FEATURES

- 2.7V to 16V Operating Input Voltage (V_{IN}) Range
- Maximum 20A of Output Current (I_{OUT})
- PMBus Lite
- 2.8mΩ Integrated Power MOSFET
- ±1% IMON Reporting Accuracy
- 12-Bit ADC for I_{OUT} Reporting
- 10-Bit ADC for V_{IN}, V_{OUT}, and Temperature Monitoring
- Built-In MOSFET Driver
- 3.3V LDO Output
- Power Good (PG) Indication
- FLT#/ALT# Signal Output
- Integrated Current Sensing with Sense Output (IMON)
- Configurable Over-Current (OC) Limit and Short-Circuit (SC) Current Limit
- Configurable Input Under-Voltage Lockout (UVLO) Threshold via EN/UV Pin
- Configurable Input Over-Voltage Protection (OVP) Threshold
- Configurable Soft Start (SS)
- V_{IN} OVP, SCP, OCP, and OTP with Options for Latch-Off and Auto-Retry Mode
- Configurable Retry Delay Time
- Intelli-Fuse Junction Temperature Monitoring
- High-Precision E_{IN}, P_{IN}, P_{OUT}, and I_{OUT} Reporting
- PMBus Monitoring and Reporting for Fault Types
- Available in a QFN-33 (3.5mmx4.5mm) Package

APPLICATIONS

- Hot Swap
- PC Cards
- Disk Drives
- Servers
- Networking
- Laptops

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP5024GRM	QFN-33 (3.5mmx4.5mm)	*See Below*	1

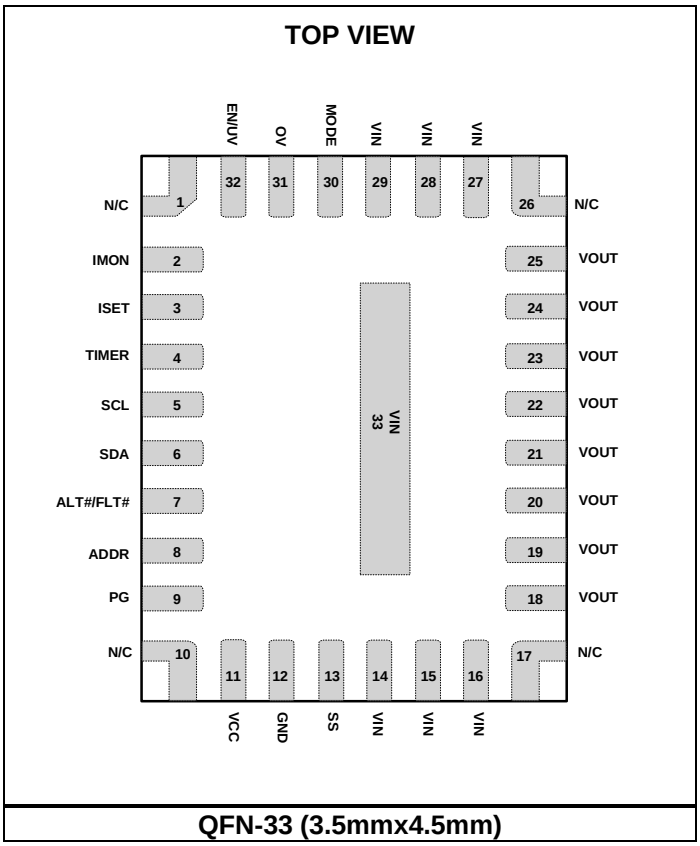
* For Tape & Reel, add suffix -Z (e.g. MP5024GRM-Z).

TOP MARKING

MPSYW
M5024
LLLLL

MPS: MPS prefix
Y: Year code
W: Week code
M5024: First four digits of the part number
LLLLL: Lot number

PACKAGE REFERENCE



QFN-33 (3.5mmx4.5mm)

PIN FUNCTIONS

Pin #	Name	Description
1, 10, 17, 26	N/C	**No connection.**
2	IMON	**Current monitor output.** The IMON pin provides a current proportional to the current flowing through the power device. To ensure that the PMBus can accurately report the output current (I_{OUT}), place a 2.49kΩ resistor (R_{IMON}) from IMON to ground. Place a capacitor exceeding 10nF in parallel with R_{IMON} during application.
3	ISET	**Current limit setting.** Place a resistor from the ISET pin to ground to set the over-current (OC) limit.
4	TIMER	**Timer setting.** An external capacitor sets the hot-plug insertion delay time and OC fault timeout period.
5	SCL	**PMBus clock input.**
6	SDA	**PMBus bidirectional data signal.**
7	FLT#	**Intelli-Fuse fault reporting output.** The FLT# pin is an open-drain output pin. FLT# asserts low and latches after a fault occurs. The faults that can trigger FLT# include an input over-voltage (OV) fault, output over-current (OC) fault, short-circuit (SC) fault, over-temperature (OT) fault, and MOSFET drain-to-source (DS)/gate-to-source (GS) short fault. This pin is either FLT# or ALT#, as selected by the MODE pin.
	ALT#	**PMBus alert open-drain output.** This pin is either FLT# or ALT#, as selected by the MODE pin.
8	ADDR	**PMBus address setting**. Connect a resistor from the ADDR pin to GND. ADDR works with the resistor on the MODE pin to determine the PMBus address.
9	PG	**Power good.** PG is an open-drain output. Pull PG up to an external power supply through a 10kΩ to 100kΩ resistor.
11	VCC	**Internal 3.3V LDO output.** Place a 1µF decoupling capacitor close to VCC and GND.
12	GND	**Ground.**
13	SS	**Soft-start time (t_{SS}) setting.** t_{SS} is set by an external capacitor connected to the SS pin. The internal circuitry controls the V_{OUT} slew rate during start-up.
14, 15, 16, 27, 28, 29, 33	VIN	**System input power supply.** The VIN pin is connected to the drain of the integrated power MOSFET.
18, 19, 20, 21, 22, 23, 24, 25	VOUT	**Output voltage.** The VOUT pin is connected to the source of the integrated power MOSFET. Place a Schottky diode between VOUT and GND to absorb the negative voltage spike.
30	MODE	**Mode selection.** Connect a resistor from the MODE pin to GND to select the protection mode (latch-off or auto-retry), as well as the output for pin 7 (ALT# or FLT#). MODE works with the ADDR pin to determine the PMBus address.
31	OV	**Input OV setting.** Connect the OV pin to the system's input voltage with a resistor divider to determine the input OV threshold.
32	EN/UV	**Enable control and input voltage under-voltage lockout (UVLO) setting.** The EN/UV pin is a control input that turns the device on/off. Drive EN/UV high to turn on the device; drive it low to turn off the device. Connect a resistor divider from VIN to GND, and tapped to EN/UV, to set the input voltage UVLO threshold. VCC is not controlled by EN/UV. Do not float EN/UV.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} (DC).....-0.3V to +20V
V_{IN} (1µs)..... 24V
V_{IN} (25ns)..... 29V
V_{OUT}.....-0.3V to +20V
All other pins.....-0.3V to +4.2V
Continuous power dissipation (T_A = 25°C) (2)
..... 3.05W
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +155°C

ESD Ratings (3)

Human body model (HBM) .....Class 1C
Charged-device model (CDM).....Class C2B

Recommended Operating Conditions (4)

V_{IN}..... 2.7V to 16V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (5) θ_{JA} θ_{JC}

QFN-33 (3.5mmx4.5mm)..... 40.9 ....34.5 . °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Followed ANSI/ESDA/JEDEC JS-001 for HBM and ANSI/ESDA/JEDEC JS-002 for CDM.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on a JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, R_{ISET} = 12kΩ, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Quiescent current	I_{Q_IN}	Intelli-Fuse on, no load		3.25	4	mA
		Fault latch off		3	3.5	mA
		Intelli-Fuse off with EN = 0, V_{IN} = 12V		2.7	3.5	mA
		Intelli-Fuse off with EN = 0, V_{IN} = 16V		2.7	3.5	mA
VCC Regulator and Under-Voltage Lockout (UVLO)						
VCC regulator output voltage	V_{CC}	I_{VCC} = 0mA	3.1	3.37	3.5	V
		I_{VCC} = 10mA		3.36		
		I_{VCC} = 20mA		3.35		
V_{CC} UVLO rising threshold	$V_{CC\_VTH\_R}$		2.36	2.46	2.56	V
V_{CC} UVLO falling threshold	$V_{CC\_VTH\_F}$		2.2	2.3	2.4	V
V_{CC} UVLO threshold hysteresis	V_{CC_HYS}			160		mV
Input Voltage (V_{IN}) Regulator and UVLO						
V_{IN} UVLO rising threshold	$V_{IN\_VTH\_R}$		2.46	2.56	2.66	V
V_{IN} UVLO falling threshold	$V_{IN\_VTH\_F}$		2.3	2.4	2.5	V
V_{IN} UVLO threshold hysteresis	V_{IN_HYS}			160		mV
EN/UV (Enable and V_{IN} UVLO)						
EN/UV input rising threshold	V_{EN_R}		1.15	1.21	1.27	V
EN/UV input falling threshold	V_{EN_F}		1.05	1.1	1.17	V
EN/UV hysteresis	V_{EN_HYS}			110		mV
EN/UV blanking time	t_{EN_BLANK}	EN recycling		1.3		ms
Over-Voltage (OV)						
Input rising threshold	V_{OV_R}		1.18	1.21	1.24	V
Input falling threshold	V_{OV_F}		1.075	1.135	1.195	V
Hysteresis	V_{OV_HYS}			75		mV
Power MOSFET						
On resistance	$R_{DS(ON)}$	T_J = 25°C, I_{OUT} = 2A, V_{IN} = 12V		2.8		mΩ
		T_J = 25°C, I_{OUT} = 2A, V_{IN} = 2.7V		2.8		
		T_J = 125°C, I_{OUT} = 2A, V_{IN} = 12V (6)		3.8		mΩ
		T_J = 125°C, I_{OUT} = 2A, V_{IN} = 2.7V (6)		3.8		mΩ
Off-state leakage current	I_{OFF}	V_{IN} = 16V, power FET off			1	μA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, R_{ISET} = 12kΩ, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Current Monitor Output (IMON)						
IMON sense gain	I_{IMON}/I_{FET}	I_{OUT} > 4A	19.8	20	20.2	μA/A
IMON sense offset		I_{OUT} > 4A	-0.5		+0.5	μA
Current Limit						
ISET voltage	V_{ISET}		-3%	0.6	+3%	V
Over-current (OC) internal current sensing gain		1/10 of IMON gain		2		μA/A
Current limit at normal operation	I_{OC_NOR}	R_{ISET} = 12kΩ	-6%	25	+6%	A
Short-circuit (SC) current limit	I_{SC}	I_{OC_NOR} ≤ 10A		20		A
		10A < I_{OC_NOR} < 25A		2 x I_{OC_NOR}		A
		I_{OC_NOR} ≥ 25A		50		A
Short-circuit protection (SCP) response time (6)	t_{SC}			200		ns
Start-up OC limit	I_{OC_SS}	I_{OC_NOR} < 10A		10		A
		10A < I_{OC_NOR} < 20A		I_{OC_NOR}		A
		I_{OC_NOR} > 20A		20		A
OC regulation time at soft start	t_{OC_REG}			1.5		ms
TIMER						
Upper threshold voltage	V_{TIMER_H}		1.11	1.21	1.31	V
Insertion delay charge current	I_{INSRT}		3.35	4	4.65	μA
Over-current protection (OCP) fault timeout charge current	I_{FLT_TIMER}		33.5	40	46.5	μA
Discharge $R_{DS(ON)}$	R_{TIMER}			10		Ω
Soft Start (SS)						
SS pull-up current	I_{SS}	V_{IN} = 12V	11.5	13.5	15.5	μA
Fault and Alert Output (FLT#/ALT#)						
Output low voltage	V_{OL_FLT}	Sink current 10mA			0.3	V
Off-state leakage current	I_{LK}	V_{FLT} = 3.3V			1	μA
Power Good (PG) Output						
PG rising threshold	$V_{PG\_VTH\_R}$	V_{IN} = 12V	85%	90%	95%	V_{IN}
		V_{IN} = 2.7V		V_{IN} - 0.5		V
PG falling threshold	$V_{PG\_VTH\_F}$	V_{IN} = 12V	70%	75%	80%	V_{IN}
		V_{IN} = 2.7V		V_{IN} - 0.7		V
Output low voltage	V_{OL_PG}	Sink current 10mA			0.3	V
Off-state leakage current	I_{LK}	V_{FLT} = 3.3V			1	μA
FET Short Detection						
FET drain-to-source short entry threshold	$V_{OUT\_DSTH\_ENT}$	V_{IN} = 12V	85%	90%	95%	V_{IN}
		V_{IN} = 2.7V		V_{IN} - 0.5		V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, R_{ISET} = 12kΩ, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
FET drain-to-source short recovery threshold	$V_{OUT\_DSTH\_EXT}$	V_{IN} = 12V	70%	75%	80%	V_{IN}
		V_{IN} = 2.7V		V_{IN} - 0.7		V
Gate-to-source short protection delay time (6)	t_{GS_ST}	V_{SS} > V_{CC} - 0.7	150	200	250	ms
ADDR						
ADDR current source	I_{ADDR}	T_J = 25°C	19.8	20	20.2	µA
		T_J = -40°C to +125°C	-5%	20	+5%	µA
MODE						
MODE current source	I_{MODE}	T_J = 25°C	19.8	20	20.2	µA
		T_J = -40°C to +125°C	-5%	20	+5%	µA
Thermal Shutdown						
Over-temperature threshold (6)	T_{J_OTP}			148		°C
Analog-to-Digital Converter (ADC) for IMON Sensing						
Voltage range (6)			0		1.28	V
ADC reference voltage (6)		T_J = 25°C	-0.5%	1.28	+0.5%	V
ADC resolution (6)				12		bits
DNL (6)		T_J = 25°C			1	LSB
Sample rate (6)	$f_{SR\_ADC\_IMON}$			10		kHz
ADC for V_{IN}, V_{OUT}, and Temperature Sensing						
Voltage range (6)			0		1.6	V
ADC reference voltage (6)		T_J = 25°C	-0.5%	1.6	+0.5%	V
ADC resolution (6)				10		bits
DNL (6)		T_J = 25°C			1	LSB
Sample rate (6)	f_{SR_ADC}			100		kHz
PMBus DC Characteristics						
Input high voltage	V_{IH}	SCL, SDA	2.1			V
Input low voltage	V_{IL}	SCL, SDA			0.8	V
Input leakage current		SCL, SDA	-10		+10	µA
Output low voltage (6)	V_{OL_PMBUS}	Sink 2mA, no PMBus communication			400	mV
Maximum voltage (6)	V_{MAX}	Transient voltage including ringing	-0.3	+3.3	+3.6	V
Pin capacitance (6)	C_{PIN}				10	pF
PMBus Timing Characteristics (1MHz) (6) (7)						
Operating frequency range	f_{PMB}		10		1000	kHz
Bus free time	t_{BUF}	Between stop and start command	0.5			µs
Holding time	t_{HD_STA}		0.26			µs
Repeated start command set-up time	t_{SU_STA}		0.26			µs
Stop command set-up time	t_{SU_STO}		0.26			µs
Data hold time	t_{HD_DAT}		0			ns

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, R_{ISET} = 12kΩ, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Data set-up time	t_{SU_DAT}		50			ns
Clock low timeout	$t_{TIMEOUT}$		25		35	ms
Clock low period	t_{LOW}		0.5			µs
Clock high period	t_{HIGH}		0.26		50	µs
Clock/data falling time	t_F				120	ns
Clock/data rising time	t_R				120	ns

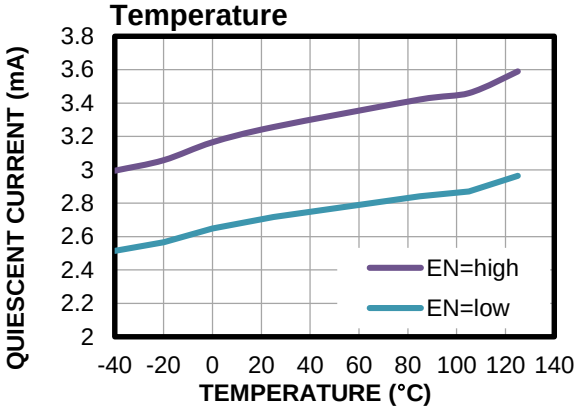
Notes:

6) Guaranteed by design.
7) The device supports 100kHz, 400kHz, and 1MHz bus speeds. The PMBus timing parameters in this table are for operation at 1MHz. If the PMBus operating frequency is 100kHz or 400kHz, refer to the SMBus specifications for timing parameters.

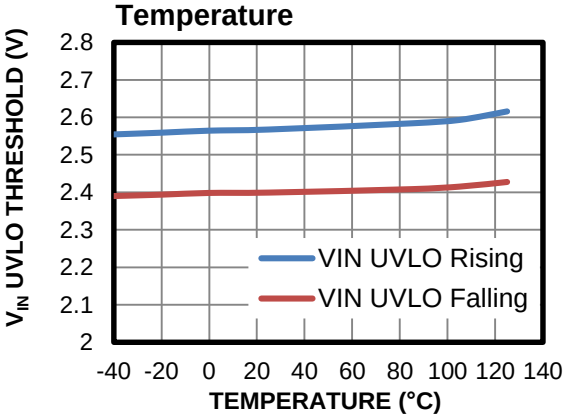
TYPICAL CHARACTERISTICS

V_{IN} = 12V, R_{IMON} = 2.49kΩ, R_{ISET} = 12kΩ, T_A = 25°C, unless otherwise noted.

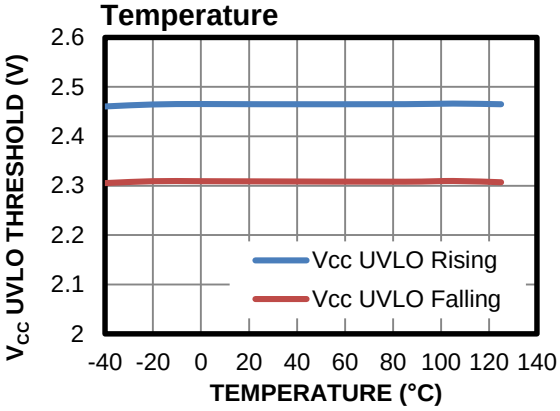
Quiescent Current vs. Temperature



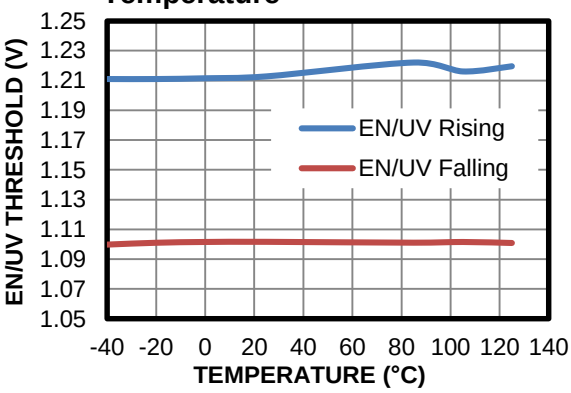
V_{IN} UVLO Threshold vs. Temperature



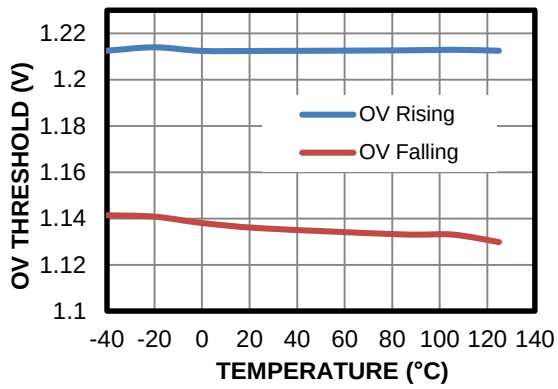
V_{CC} UVLO Threshold vs. Temperature



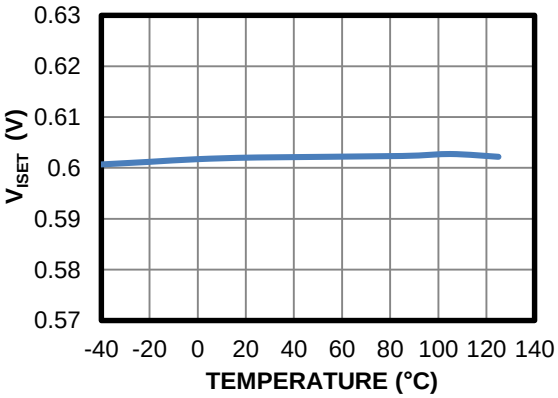
EN/UV Threshold vs. Temperature



OV Threshold vs. Temperature



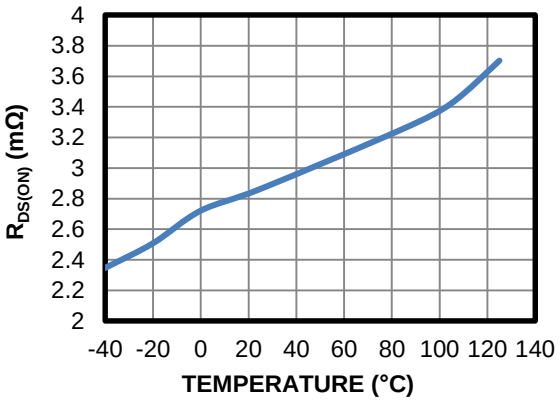
V_{ISET} vs. Temperature



TYPICAL CHARACTERISTICS *(continued)*

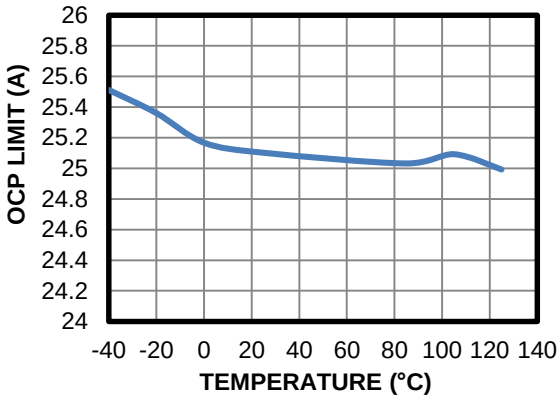
V_{IN} = 12V, R_{IMON} = 2.49kΩ, R_{ISET} = 12kΩ, T_A = 25°C, unless otherwise noted.

$R_{DS(ON)}$ vs. Temperature

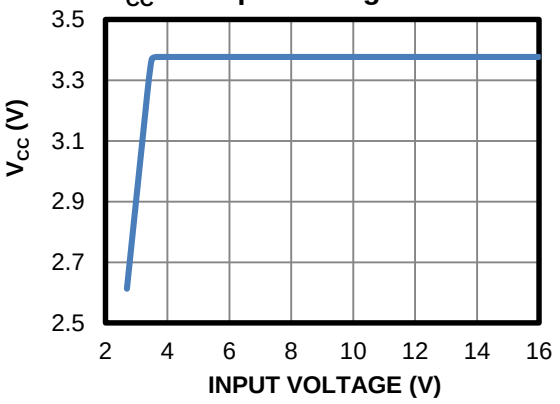


OCP Limit vs. Temperature

R_{ISET} = 12kΩ

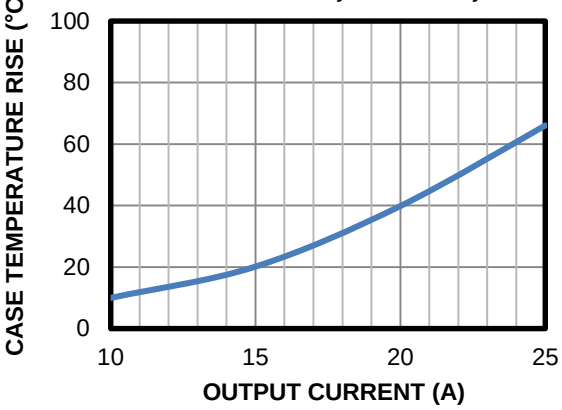


V_{CC} vs. Input Voltage



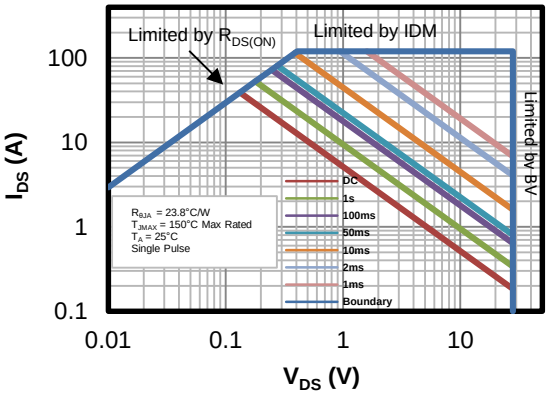
Case Temperature Rise

No air flow, measured on EV5024-V-00A, 6.35cm x 7.15cm, 4 layers, each layer 2oz



Sofe Operation Area (SOA)

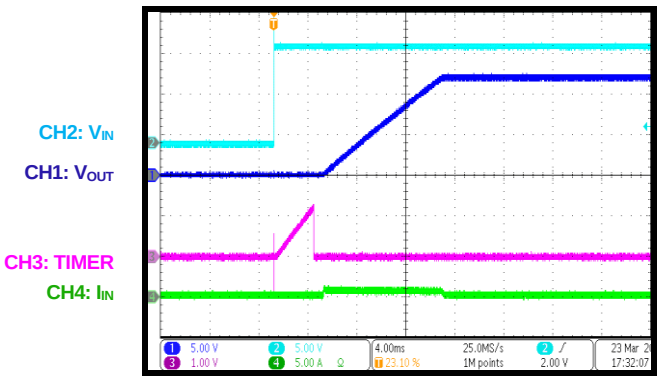
Tested on EV5024-V-00A, 6.35cm x 7.15cm, 4 layers, each layer 2oz



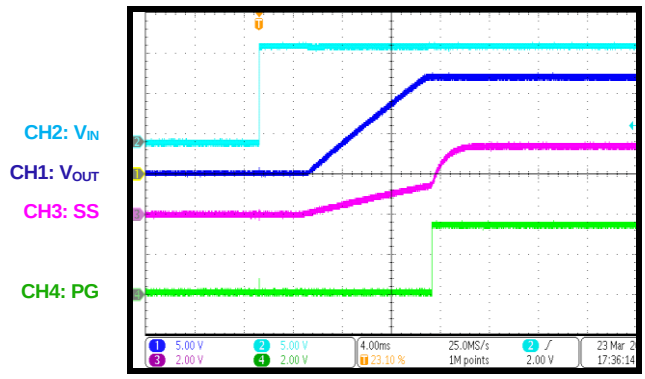
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, R_{IMON} = 2.49kΩ, R_{ISET} = 12kΩ, T_A = 25°C, unless otherwise noted.

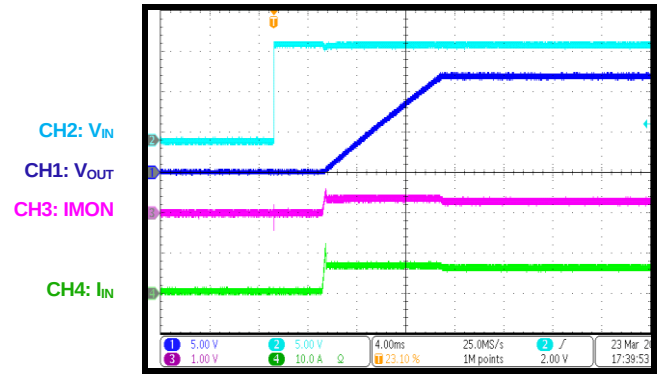
VIN Hot Plug
I_{OUT} = 0A



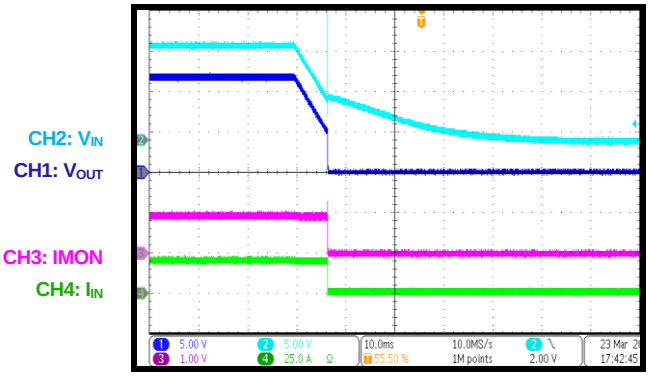
VIN Hot Plug
I_{OUT} = 0A



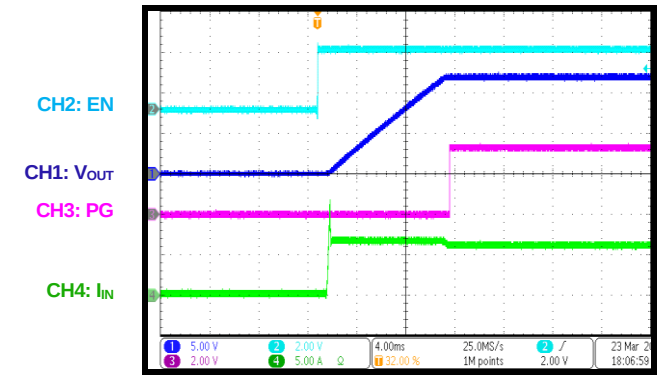
VIN Hot Plug
I_{OUT} = 6A



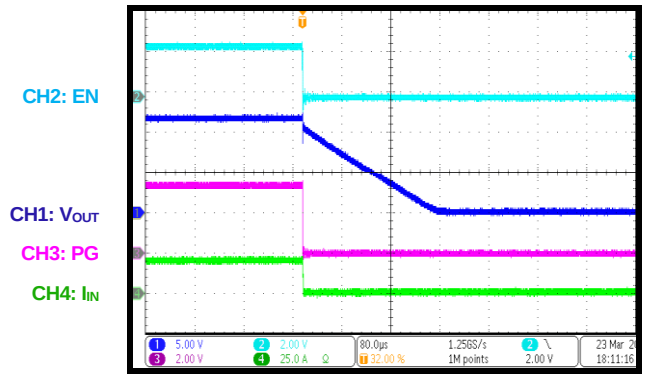
Shutdown via VIN
I_{OUT} = 20A



Start-Up via EN
I_{OUT} = 6A



Shutdown via EN
I_{OUT} = 20A

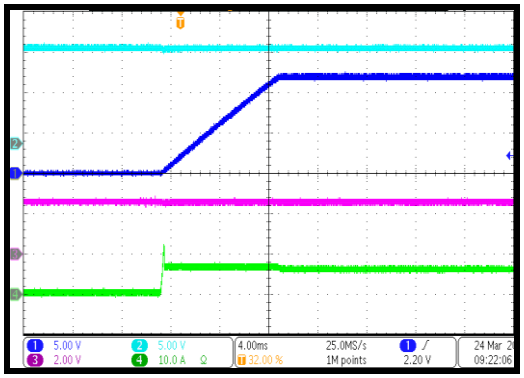


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, R_{IMON} = 2.49kΩ, R_{ISET} = 12kΩ, T_A = 25°C, unless otherwise noted.

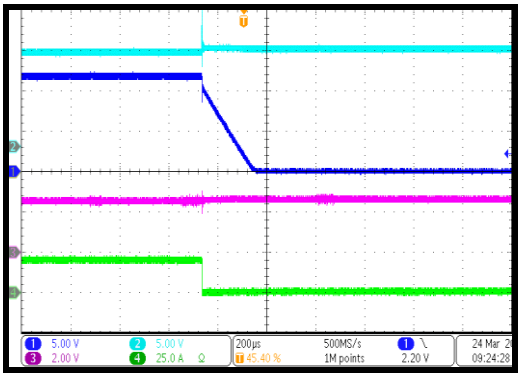
Start-Up via OPERATION Command

I_{OUT} = 6A



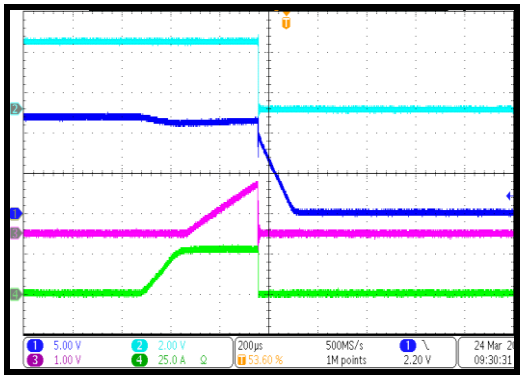
Shutdown via OPERATION Command

I_{OUT} = 20A



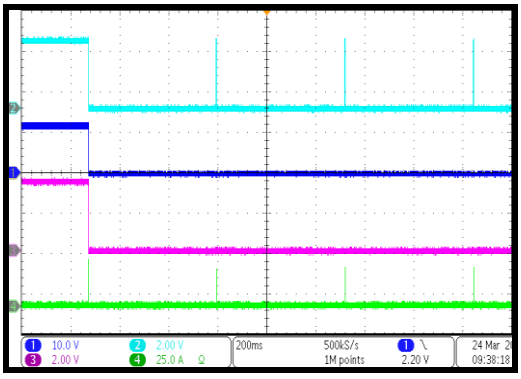
OCP

I_{LIMIT} = 25A, latch-off mode



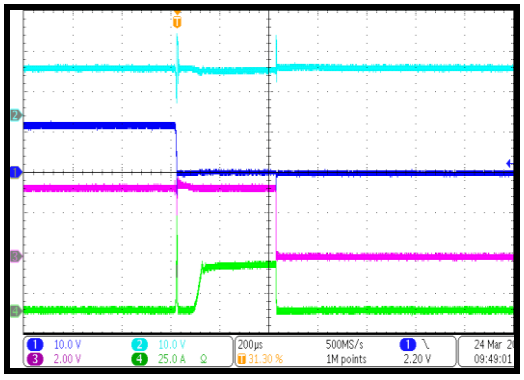
OCP

I_{LIMIT} = 25A, hiccup mode,
auto retry time = 500ms



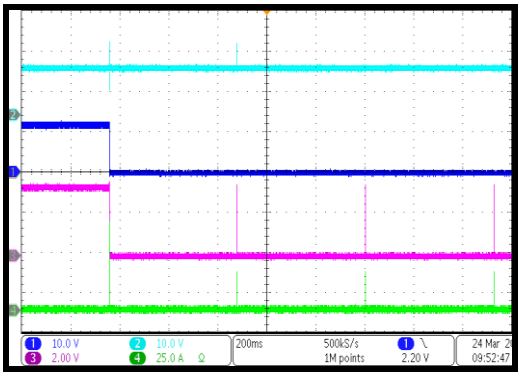
SCP

Latch-off mode



SCP

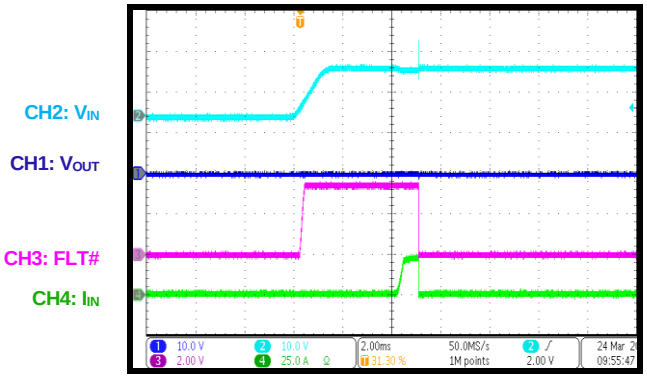
Hiccup mode



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

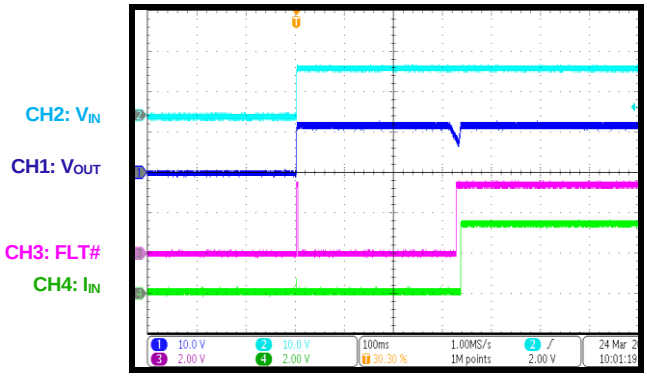
V_{IN} = 12V, R_{IMON} = 2.49kΩ, R_{ISET} = 12kΩ, T_A = 25°C, unless otherwise noted.

Short-Circuit Start-Up



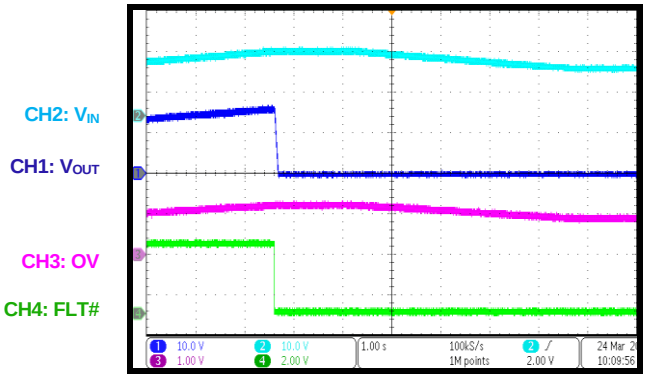
DS Short

IOUT = 0.1A, connect VOUT to VIN before start-up, then disconnect it after start-up



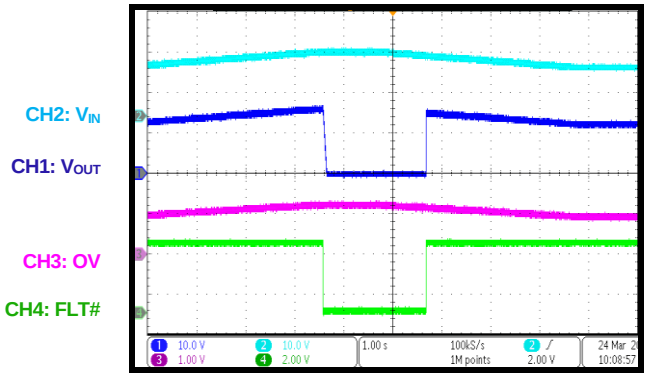
V_{IN} OVP in Latch-Off Mode

IOUT = 0.1A, apply VIN to trip OVP, then reduce VIN



V_{IN} OVP in Hiccup Mode

IOUT = 1A, apply 18.5V on VIN, then reduce VIN



FUNCTIONAL BLOCK DIAGRAM

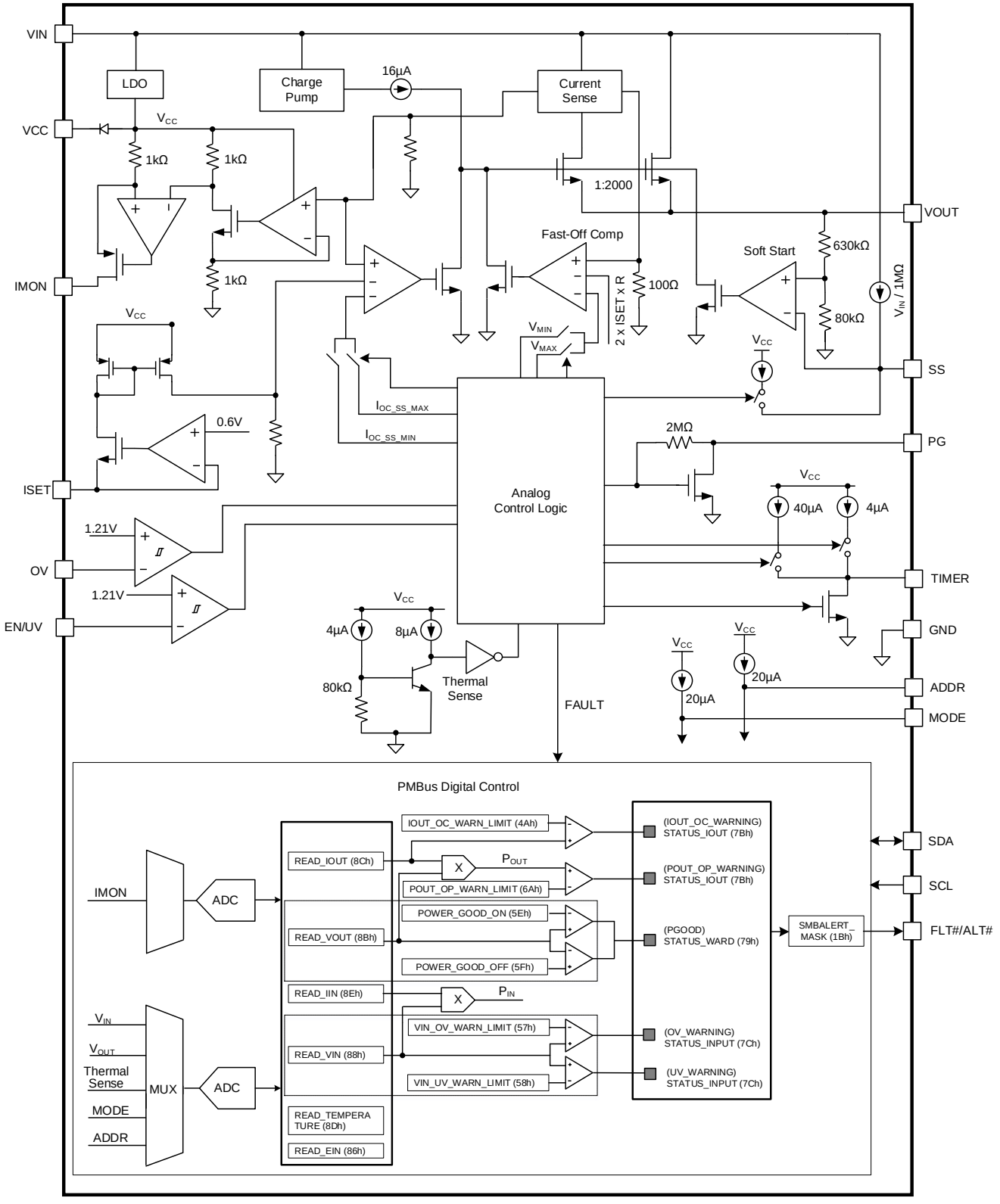


Figure 1: Functional Block Diagram

OPERATION

The MP5024 is designed to limit the inrush current to the load when a circuit card is inserted into a live backplane power source, limiting the backplane's voltage drop and the dV/dt of the voltage to the load. The MP5024 provides an integrated solution for monitoring the input voltage (V_{IN}), output voltage (V_{OUT}), output current (I_{OUT}), and die temperature to eliminate the need for an external current-sense power resistor, power MOSFET, and temperature-sensing device.

The MP5024 limits the internal MOSFET current (I_{FET}) by controlling the gate voltage through the current-limit reference input and soft-start ramp.

Start-Up Sequence

For hot-swap applications, the input of the MP5024 can experience a voltage spike or transient during the hot-plug procedure. This is caused by the parasitic inductance of the input trace and the input capacitor. To help stabilize V_{IN}, an insertion delay is implemented before the main MOSFET turns on (see Figure 2).

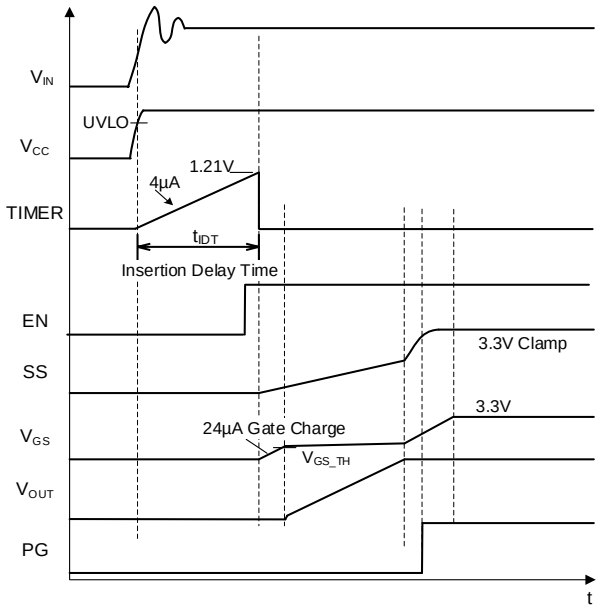


Figure 2: Start-Up Sequence

After VIN and VCC exceed their UVLO thresholds, the TIMER pin charges the external capacitor (C_{TMR}) through a 4µA constant current source.

The insertion delay time (t_{IDT}) is the time is takes for the TMR capacitor (C_{TMR}) to be charged from 0V to 1.21V by the internal 4µA current source. Select C_{TMR} (connected from the TIMER pin to ground) to set the insertion delay time. t_{IDT} can be calculated with Equation (1):

$$t_{IDT}(ms) = \frac{1.21}{4} \times C_{TMR}(nF) \quad (1)$$

For example, a 10nF capacitor results in an insertion delay time of 3.025ms.

Once the insertion delay time ends and the EN voltage exceeds 1.4V, the MOSFET is charged by the internal 24µA charge pump. The MOSFET turns on once the gate-to-source (GS) voltage (V_{GS}) exceeds its threshold (V_{GS_TH}), and V_{OUT} rises.

Soft Start (SS)

A capacitor (C_{SS}) connected to the SS pin determines the soft-start time (t_{SS}). When EN is pulled high and the insertion delay time ends, a constant current source proportional to V_{IN} charges up the SS voltage (V_{SS}). V_{OUT} rises at a similar slew rate to V_{SS}.

C_{SS} can be estimated with Equation (2):

$$C_{SS}(nF) = 9 \times \frac{t_{SS}(ms)}{R_{SS}(M\Omega)} \quad (2)$$

Where R_{SS} is 0.89MΩ. For example, a 100nF capacitance results in a t_{SS} of 9.9ms.

If the load capacitance is extremely large, the current required to maintain the preset t_{SS} exceeds the start-up current limit. In this scenario, the rising time is controlled by the load capacitor and the start-up current limit.

Float the SS pin to generate a fast ramp-up voltage. A 24µA current source pulls up the gate of the power FET. The gate charge current controls the V_{OUT} rising time. The approximate t_{SS} is about 1ms, which is the minimum V_{OUT} soft-start time.

Over-Current Protection (OCP)

The MP5024 provides a constant current limit that can be configured by an external resistor.

The Intelli-Fuse over-current limit (I_{LIMIT}) is a function of the ISET resistor (R_{ISET}). I_{LIMIT} can be calculated with Equation (3):

$$I_{LIMIT}(A) = \frac{0.3V}{R_{ISET}(k\Omega)} \times 10^3 \quad (3)$$

When V_{OUT} falls below the larger value between (V_{IN} - 0.5V) and (90% of V_{IN}), the MP5024 operates in start-up mode. To ensure that the device can start up normally with an output load, I_{LIMIT} has an internal lower current limit clamp at about 10A.

To protect the MP5024 from overheating during start-up, I_{LIMIT} has an internal upper current limit clamp at about 20A. When I_{LIMIT} is below 10A, I_{OC_SS} is clamped to 10A. When I_{LIMIT} exceeds 20A, I_{OC_SS} is clamped to 20A. I_{OC_SS} is equal to I_{LIMIT} under all other conditions (see Figure 3).

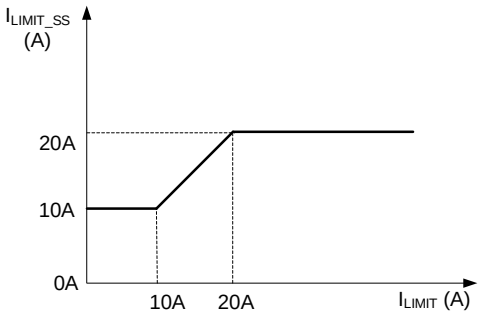


Figure 3: Start-Up Current Limit Compared to Normal Over-Current Limit

The device exits start-up mode when V_{OUT} exceeds the larger value between (V_{IN} - 0.5V) and (90% of V_{IN}), and V_{GS} is close to the internal charge pump voltage.

Once the MP5024 detects that start-up has finished, the internal current limit clamps are disabled. During normal operation, the current limit is determined by I_{LIMIT} only.

Once the device reaches its current limit threshold, the internal circuit regulates the gate voltage to hold the current in the power FET constant. The typical response time is about 20µs. I_{OUT} may have a small overshoot during this period.

Intelli-Fuse OCP during Start-Up

During start-up, if the current through the MP5024 is regulated by I_{OC_SS} for the soft-start OC regulation time (t_{OC_REG}), the gate stops regulating and pulls low. When a soft-start OC fault is triggered, the power MOSFET shuts down. The FLT#/ALT# pin drives low with an 8µs propagation delay to indicate a fault (see Figure 7). In addition, STATUS_IOUT (7Bh), bit[4] is also set 1 to indicate that a soft-start OC event has occurred.

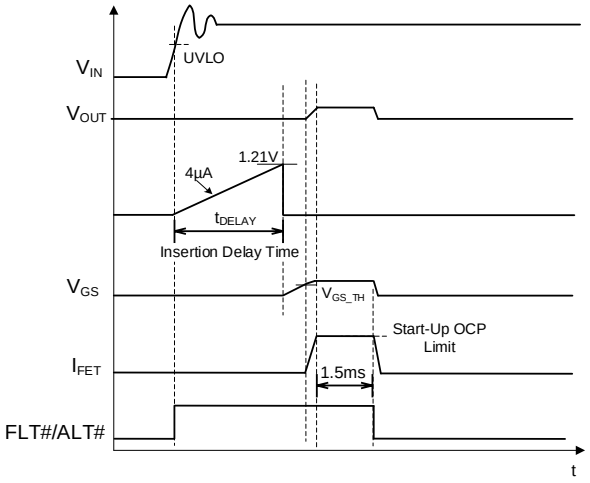


Figure 4: Start-Up OCP Behavior with Latch-Off Mode

The typical t_{OC_REG} time is 1.5ms, but the actual regulating time depends on the device's safe operation area (SOA). If over-temperature protection (OTP) is triggered during the soft-start OC regulation time, the power FET shuts down immediately.

OCP during Normal Operation

Once soft start is complete, the MP5024 enters normal operation. When I_{LIMIT} is triggered, the fault timer starts. If I_{FET} falls below I_{LIMIT} before the end of the fault timeout period, the MP5024 resumes normal operation. Otherwise, if the OC condition lasts for longer than the fault timeout period, the OC fault is triggered and the power MOSFET turns off. FLT#/ALT# is driven low with an 8µs propagation delay to indicate a fault. STATUS_IOUT (7Bh), bit[7] is also set 1 to indicate that an OC event has occurred.

The OCP fault timer (t_{OC}) can be estimated with Equation (4):

$$t_{OC}(ms) = \frac{1.21}{40} \times C_{TMR}(nF) \quad (4)$$

For example, a 10nF capacitor results in an OCP fault timer of 0.3ms.

Normal OCP can be configured to latch-off mode or auto-retry mode through the MODE pin's setting. The power MOSFET restarts immediately once the retry delay time ends. If the fault is not removed, the MP5024 triggers a start-up current limit and shuts down again (see Figure 5). The MP5024 resumes normal operation until the OC fault is removed.

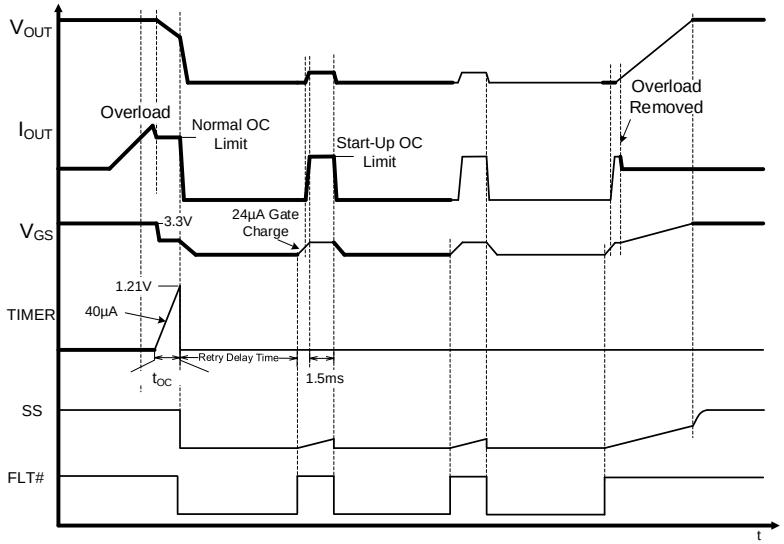


Figure 5: Normal OCP Behavior in Auto-Retry Mode

Short-Circuit Protection (SCP)

If I_{FET} increases rapidly due to a short-circuit event, the current may exceed the current limit by a significant amount before the hot-swap control loop can respond. If the Intelli-Fuse's current reaches the short-circuit current limit (I_{SC}), a fast turn-off circuit in the Intelli-Fuse is activated to turn off the power FET. This limits the peak current through the power MOSFET to limit the input voltage drop. The total short-circuit response time is about 200ns.

When I_{LIMIT} is below 10A, I_{SC} is clamped to 20A. When I_{LIMIT} exceeds 25A, I_{SC} is clamped to 50A. Under most conditions, I_{SC} is 2 times greater than I_{LIMIT} (see Figure 6).

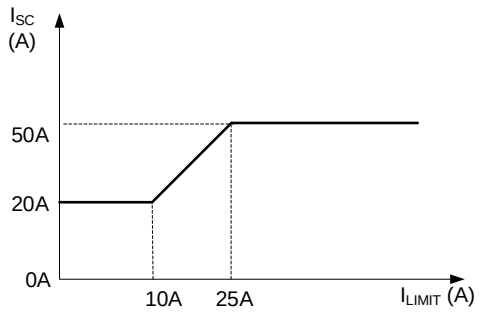


Figure 6: Short-Circuit Current Limit to Normal Over-Current Limit

If I_{FET} exceeds I_{SC}, the MP5024 turns off and V_{GS} drops low. Then the MP5024 attempts to start up again more rapidly to avoid an input voltage line transient issue. V_{GS} is charged up by an internal charge pump. When V_{GS} exceeds its threshold (V_{GS_TH}), the MP5024 turns on. If the short-circuit condition remains, the load current is limited by I_{LIMIT}. If the fault is not removed after t_{OC}, the power MOSFET turns off and the FLT#/ALT# pin switches low (see Figure 7 on page 19).

When a hard short occurs, if V_{IN} drops below the under-voltage lockout (UVLO) threshold quickly, the MP5024 triggers an under-voltage (UV) fault. The MP5024 shuts down immediately, regardless of whether the short-circuit current limit has been reached. If V_{IN} rises above the V_{IN} rising threshold again, the MP5024 retries while the short-circuit condition is present. The behavior is the same as start-up OCP (see Figure 4 on page 17).

The retry behavior is similar to a normal OCP event (see Figure 5).

Figure 7 on page 19 shows the SCP behavior during latch-off mode.

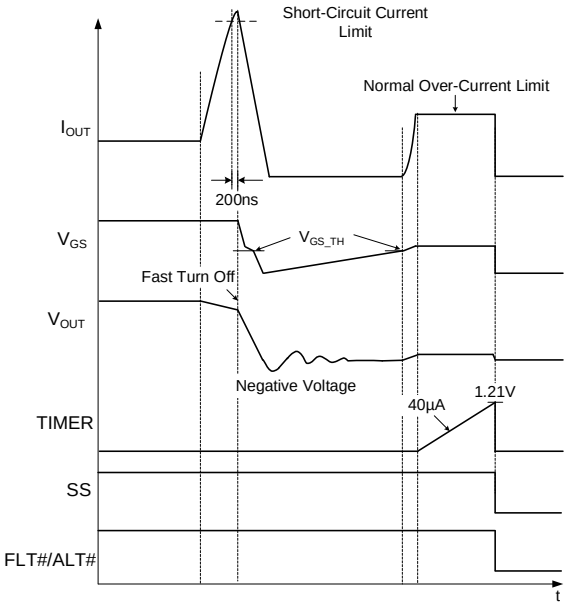


Figure 7: SCP Behavior in Latch-Off Mode

Power Good (PG)

The power good (PG) pin is an open-drain output that indicates whether V_{OUT} is in the normal range relative to V_{IN}. Pull PG up to the external power supply through a 10kΩ to 100kΩ resistor. During start-up, the PG pin's output is driven low. This instructs the system to remain off and minimize the load on V_{OUT} to reduce inrush current and power dissipation at start-up.

PG stays low until all of the following conditions are met:

1. V_{OUT} > PG rising threshold.
    a. If MFR_PRT_CONFIG (F1h), bit[11] is set to 0, the PG rising threshold is fixed at 90% of V_{IN}.
    b. If MFR_PRT_CONFIG (F1h), bit[11] is set to 1, the PG rising threshold is configured via POWER_GOOD_ON (5Eh).
2. V_{OUT} > V_{IN} - 0.5V.
3. V_{GS} > 2V.

PG pulls low if any of the following events occur:

1. V_{OUT} < PG falling threshold.
    a. If MFR_PRT_CONFIG (F1h), bit[11] is set to 0, the PG falling threshold is fixed at 75% of V_{IN}.
    b. If MFR_PRT_CONFIG (F1h), bit[11] is set to 1, the PG rising threshold is configured via POWER_GOOD_OFF (5Fh).
2. EN goes low.
3. The OPERATION (01h) command is set to 0x00.
4. A fault event occurs.

When there is no input, PG stays at a logic low level in the presence of a pull-up supply.

Output Current Monitor (IMON)

The MP5024 provides a high-accuracy MOSFET output current monitor (IMON). The current monitor gain is 20µA/A. Connect a 2.49kΩ resistor (R_{IMON}) between the IMON and GND pins to set the gain of the IMON output voltage (V_{IMON}), which is about 49.8mV per ampere. For the best accuracy, select resistors within 1%. Place a 100nF capacitor from IMON to GND to smooth the indicator voltage.

The recommended V_{IMON} range is between 0V and 1.23V, which is also within the internal analog-to-digital converter's (ADC) sensing limit.

To ensure that the PMBus reports I_{OUT} accurately, the MP5024 provides IOUT_CAL_GAIN_TUNE (38h) to store the IMON gain and R_{IMON}. The I_{OUT} telemetry reporting value can be calculated with Equation (5):

$$READ\_IOUT = \left(\frac{V_{IMON\_ADC}}{IOUT\_CAL\_GAIN}\right) \times 100 + IOUT\_CAL\_OFFSET \quad (5)$$

The default IOUT_CAL_GAIN is set to 0x00F9, which is calculated with a 2.49kΩ R_{IMON} and 20µA/A IMON sense gain.

Although IMON has no biased value as the load current, the MP5024 provides IOUT_CAL_OFFSET (39h) to quantify the error between IOUT_CAL_GAIN and the analog value. The default value of IOUT_CAL_OFFSET (39h) is 0x0000.

MODE

The MODE pin voltage is sampled and latched before the insertion delay time ends. The new MODE pin configuration does not take effect until the next insertion delay time.

The MODE pin serves three functions:

1. Sets the protection mode to latch-off or auto-retry mode.
2. Selects whether the FLT#/ALT# pin is set to FLT# or ALT#.
3. Works with the ADDR pin to determine the PMBus address (see Table 2 on page 22).

Table 1 shows the recommended R_{MODE} value for different function selections.

Table 1: Mode Configuration

Option	R_{MODE} (kΩ) (1%)	Protection Mode	FLT#/ ALT#	F0h, Bit[3]
1	0	Latch-off mode	FLT#	0
2	4.99			1
3	9.76		ALT#	0
4	15			1
5	21	Auto-retry mode (default 500ms)	ALT#	1
6	28.7			0
7	38.3		FLT#	1
8	>51.1			0

Auto-Retry or Latch-Off Mode Protection

The protection mode can be configured to latch-off mode or auto-retry mode via the MODE pin setting.

If a fault event (OVP, OCP, SCP or OTP) occurs, the power MOSFET turns off and the FLT#/ALT# pin pulls down.

In latch-off mode, the power MOSFET stays latched off until the fault event is removed and any of below conditions are met:

- Power is cycled on VIN
- Power is cycled on EN
- The OPERATION (01h) command is recycled

In auto-retry mode, the retry delay timer starts when the fault event occurs. When the retry delay time expires, the MP5024 attempts to restart. If the fault event is not removed, the MP5024 stays off and starts the next retry delay timer. If the fault event is removed, the MP5024 resumes normal operation.

The default retry delay time is 500ms, but it can be configured to 250ms or 1s via MFR_PRT_CONFIG (F1h), bits[10:9].

FLT#/ALT#

The FLT#/ALT# pin is an open-drain output that can indicate whether a fault/warning event has occurred. Pull FLT#/ALT# up to an external power supply through a 10kΩ to 100kΩ resistor. This pin is a multiplex pin that can be configured by the MODE pin's setting.

When this pin is configured as FLT#, it is driven low with an 8µs propagation delay if any of the following conditions occur:

- Over-current (normal OCP and start-up OCP) or an output short (SCP)
- Over-temperature (OT)
- Input over-voltage (V_{IN} OV)
- Internal MOSFET short (GS short, DS short)

The FLT# pin stays low until the power FET resumes normal operation, or if any of the below conditions are met:

- Power is cycled on VIN
- EN goes low
- OPERATION (01h) = 0x00
- The retry delay time is expired

If this pin is set to ALT#, it is driven low with an 8µs propagation delay under any fault and warning conditions. The ALT# pin stays low until any of the below conditions are met:

- Power is cycled on VIN
- EN goes low, then send a CLEAR_FAULT (03h) command
- OPERATION (01h) = 0x00, then send a CLEAR_FAULT (03h) command
- Resume normal operation then send a CLEAR_FAULT (03h) command

Thermal Protection

The MP5024 senses the junction temperature (T_J) internally on the power FET. If T_J exceeds the thermal shutdown threshold, the power MOSFET turns off. Meanwhile, the FLT#/ALT# and SS pins pull low.

The OTP threshold is typically fixed to 148°C.

If T_J exceeds the 148°C threshold, the MP5024 triggers thermal shutdown and the register

STATUS_TEMPERATURE (7Dh), bit[7] is set to 1 to indicate that an OT event has occurred.

The MP5024's thermal shutdown protection mode depends on the MODE pin configuration. If auto-retry mode is selected, the power MOSFET recovers after the temperature falls below the OT falling threshold. The OT hysteresis is 20°C.

Additional Protections

The MP5024 provides additional protections, described below.

V_{IN} Over-Voltage Protection (OVP)

The MP5024 has internal voltage sensing to monitor V_{IN}. Connect a resistor divider to the OV pin to set the input over-voltage threshold (V_{OV}) (see Figure 8).

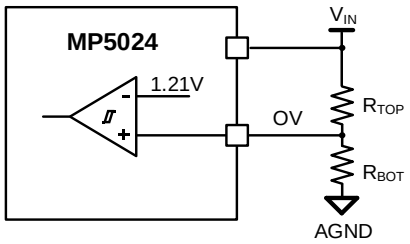


Figure 8: OV Connection

V_{OV} can be estimated with Equation (6):

$$V_{ov}(V) = 1.21 \times \left(1 + \frac{R_{TOP}}{R_{BOT}}\right) \quad (6)$$

Regardless of whether EN pin's voltage is high or low, OV detection and the OVP response action are always active. If the voltage on the OV pin exceeds the rising threshold (typically 1.21V), the power FET turns off, and the FLT# and SS pins pull low. If the OV pin's voltage drops below the falling threshold, the device can restart again by cycling power on VIN or EN (see Figure 9).

Connect the OV pin to GND to disable OVP.

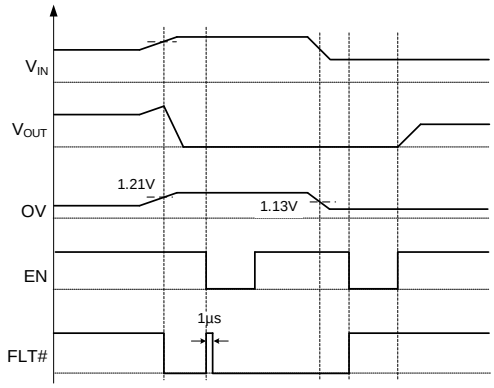


Figure 9: OVP Behavior

Drain-to-Source (DS) Short Detection

The internal drain-to-source (DS) short detection circuit starts to work when V_{IN} and V_{CC} reach their UVLO thresholds; DS short detection is no longer available once the device enters soft start. If V_{OUT} exceeds the smaller value between (V_{IN} - 0.5V) and (90% of V_{IN}) during the detection period, the internal DS short flag is set. STATUS_FET (80h), bit[0] is set to 1 to indicate a DS short has occurred.

The MP5024 determines that a real DS short event occurs when all the below conditions are met. Then FLT# pulls low and the GATE voltage stays low to disable the power FET.

- The internal DS short flag is set
- EN is high
- The insertion delay time ends

The DS short is a live protection. Once V_{OUT} drops below the smaller value between (V_{IN} - 0.7V) and (75% of V_{IN}), the device resumes normal operation and FLT# releases high,

Gate-to-Source (GS) Short Detection

If all of the following conditions are all met for 200ms, the device determines that a gate-to-source (GS) short event has occurred, and shuts off the power FET:

- V_{GS} < 2.4V
- V_{SS} > V_{CC} - 0.7V
- No OC fault has occurred

STATUS_FET (80h), bit[1] is set to 1 to indicate that a GS short has occurred.

PMBUS/I²C COMMUNICATION

General Description

The power management bus (PMBus) is an open-standard power-management protocol that defines a means of communicating with power conversion and other devices. It is a two-wire, bidirectional serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are externally pulled to a bus voltage when they are idle. Connecting to the line, a master device generates the SCL signal and device address, and arranges the communication sequence. It is based on the principles of I²C operation.

The MP5024 supports 100kHz, 400kHz, and 1MHz bus timing requirements. The timing and electrical characteristics of the PMBus can be found in the Electrical Characteristics section starting on page 6 or in the PMBus power system management protocol specification, part 1, revision 1.3, which is available at http://PMBus.org.

PMBus/I²C Address

To support multiple devices using the same PMBus/I²C interface, the MP5024 provides 16 sets of pin-configurable PMBus addresses, which are set by the ADDR pin and MODE pin. The PMBus address's bits[2:0] are determined by the ADDR pin, while bit[3] is determined by the MODE pin. Bits[6:4] are fixed to 4h, so the PMBus-configurable range is between 40h and 4Fh. Table 2 shows how the PMBus address is set.

Table 2: Pin-Configurable PMBus Address

Bit	6	5	4	3	2	1	0
Address	Fixed to 4h			MODE Pin	ADDR Pin		

Table 3 shows how to select the PMBus address.

Table 3: PMBus Address Selection

Address	V_{ADDR} (V)	R_{ADDR} (kΩ) (1%)	R_{MODE} (kΩ (1%) (8)
40h	0	0	0, 9.76, 28.7, or >51.1
41h	0.1	4.99	
42h	0.2	9.76	
43h	0.3	15	
44h	0.42	21	
45h	0.57	28.7	
46h	0.77	38.3	
47h	>1.02	>51.1	
48h	0	0	4.99, 15, 21, or 38.3
49h	0.1	4.99	
4Ah	0.2	9.76	
4Bh	0.3	15	
4Ch	0.42	21	
4Dh	0.57	28.7	
4Eh	0.77	38.3	
4Fh	>1.02	>51.1	

Note:

8) Table 1 on page 20 shows how to configure MODE.

Start and Stop Commands

Start and stop are signaled by the master device, which signifies the beginning and the end of the PMBus transfer. The start command is defined as the SDA signal transitioning from high to low while the SCL is high. The stop command is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 12).

The master then generates the SCL clocks and transmits the device address and the read/write (R/W) direction bit on the SDA line. Data is transferred in 8-bit bytes by the SDA line. Each byte of data must be followed by an acknowledge (ACK) bit.

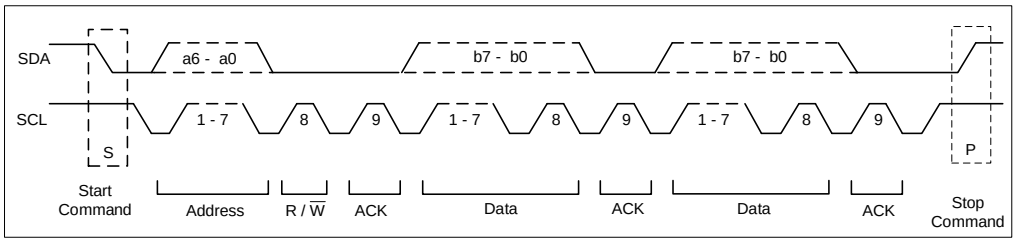


Figure 12: Data Transfer over the PMBus

PMBus Update Sequence

The MP5024 requires a start command, a valid PMBus address, a register address byte, and a data byte for a single data update. The MP5024 acknowledges the receipt of each byte by pulling the SDA line low during the high period of a single clock pulse. A valid PMBus address selects the MP5024, and the MP5024 performs an update on the falling edge of the least significant bit (LSB) byte.

Protocol Usage

All PMBus transactions on the MP5024 are done using defined bus protocols. The following protocols are implemented:

- Send byte with packet error checking (PEC)
- Receive byte with PEC
- Write byte with PEC
- Read byte with PEC
- Write word with PEC
- Read word with PEC
- Block read with PEC

PMBus Message Format

Figure 13 on page 24 shows the PMBus message format, where the unshaded cells indicate that the bus host is actively driving the bus. Shaded cells indicate that the MP5024 is driving the bus.

- S = start command
- Sr = repeated start command
- P = stop command
- R = read bit
- $\overline{W}$ = write bit
- A = acknowledge bit (0)
- $\overline{A}$ = acknowledge bit (1)

A represents the acknowledge (ACK) bit. The ACK bit is typically active low (logic 0) if the transmitted byte is received successfully by a device. However, when the receiving device is the bus master, the acknowledge bit for the last byte read is logic 1, indicated by $\overline{A}$.

Packet Error Checking (PEC)

The PMBus interface supports the use of a PEC byte. The PEC byte is transmitted by the MP5024 during a read transaction or sent by the bus host to the MP5024 during a write transaction.

The PEC byte is used by the bus host or the MP5024 to detect errors during a bus transaction, depending on whether the transaction is a read or a write. If the host determines that the PEC byte read during a read transaction is incorrect, it can decide to repeat the read if necessary. If the MP5024 determines that the PEC byte sent during a write transaction is incorrect, it ignores the command (it is not executed) and sets a status flag. Within a group command, the host can choose to send or not send a PEC byte as part of the message to the MP5024.

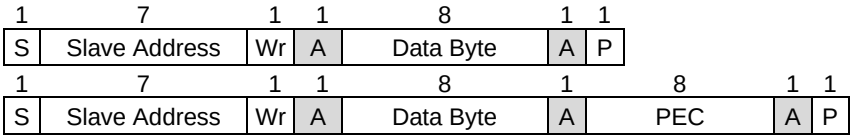
PMBus Alert Response Address (ARA)

The PMBus alert response address (ARA) is a special address that can be used by the bus host to locate any devices that need to talk to the bus host. A host typically uses a hardware interrupt pin to monitor the PMBus ALERT# pins of a number of devices. When a host interrupt occurs, the host issues a message on the bus using the PMBus receive byte or receive byte with the PEC protocol.

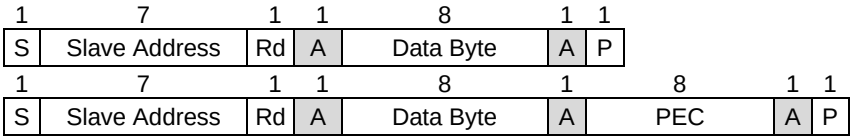
The special address used by the host is 0x0C. Any devices that have a SMBAlert signal return their own 7-bit address as the seven most significant bits (MSBs) of the data byte. The LSB value is not used and can be either 1 or 0. The host reads the device address from the received data byte and proceeds to handle the alert condition.

More than one device may have an active SMBAlert signal and attempt to communicate with the host. In this case, the device with the lowest address dominates the bus and succeeds in transmitting its address to the host. The device that succeeds disables its PMBus alert signal. If the host sees that the PMBus alert signal is still low, it continues to read addresses until all devices that need to talk to it have transmitted their addresses successfully.

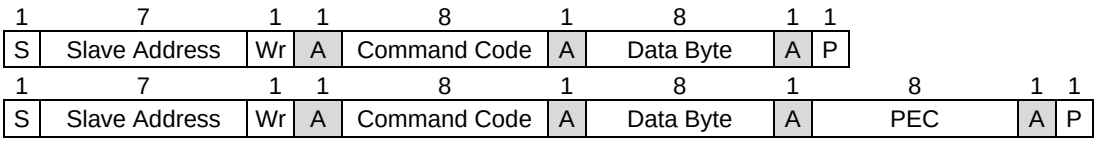
Send Byte and Send Byte with PEC



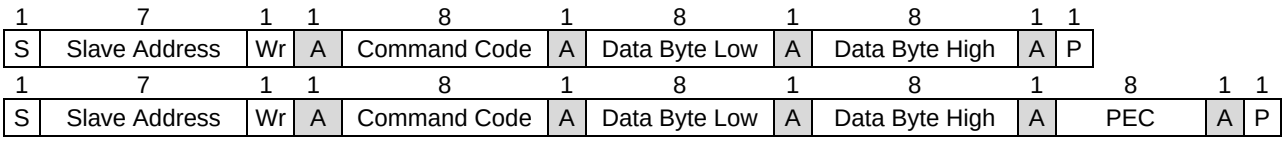
Receive Byte and Receive Byte with PEC



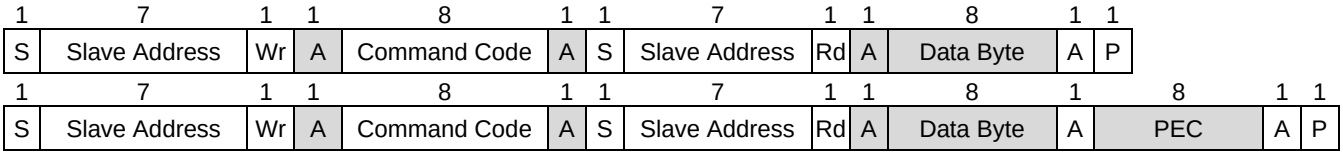
Write Byte and Write Byte with PEC



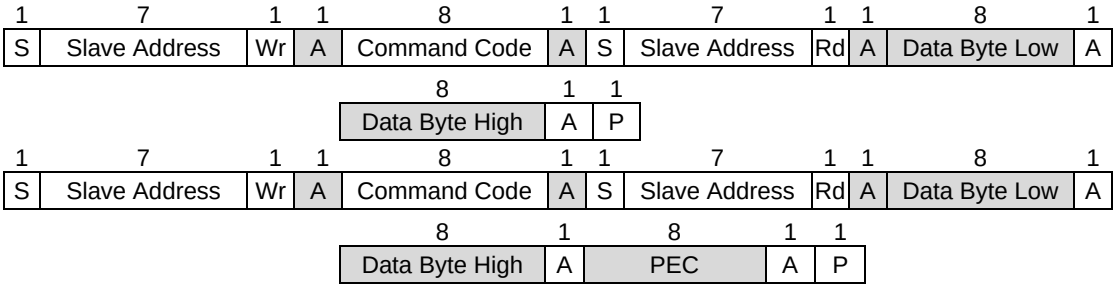
Write Word and Write Word with PEC



Read Byte and Read Byte with PEC



Read Word and Read Word with PEC



Block Read with PEC

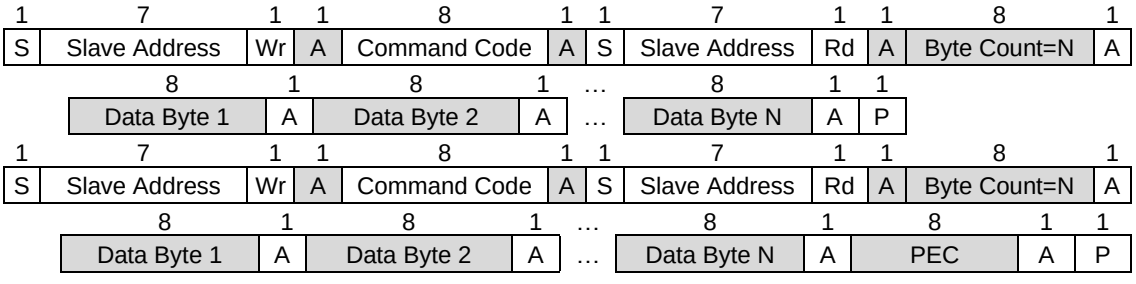


Figure 13: PMBus Message Format

Direct Format Conversion

The MP5024 uses an internal direct format to represent real-world values, such as voltage, current, power, and temperature. A direct format number takes the form of a 2-byte, two's complement, binary integer value.

The real-world values can be converted to direct format, calculated with Equation (7):

$$Y = (mX + b) \times 10^{R} \quad (7)$$

The direct format values can be converted to real-world values, estimated with Equation (8):

$$X = \frac{1}{m}(Y \times 10^{-R} - b) \quad (8)$$

Where *Y* is the value in direct format, *X* is the calculated real-world value (e.g. in A, V, W, and °C), *m* is the slope coefficient, *b* is the offset, and *R* is a scaling exponent.

The same equations are used for voltage, current, power, and temperature conversions, with the only difference being the values of the *m*, *b*, and *R* coefficients. Table 4 lists all the coefficients required for the MP5024.

V_{IN} and V_{OUT} Internal Sensing Ratio

To improve voltage reporting accuracy in different applications, the MP5024 provides an option to select a V_{IN} and V_{OUT} internal sensing divider ratio.

When MFR_TELEMETRY_CONFIG (F2h), bit[2] is set to 0 (the default setting), the internal sensing ratio is 1:12. The voltage reporting range can be up to 19V.

To improve voltage reporting accuracy for applications below 6V, the internal sensing ratio can be configured to 1:4 by setting F2h, bit[2] = 1.

Table 4: Direct Format Conversion to Real-Word Coefficients

Commands	*m*	*b*	*R*	Units
• READ_IOUT • READ_IIN • IOUT_OC_WARN_LIMIT	32	0	0	A
• READ_VIN • READ_VOUT • VIN_OV_WARN_LIMIT • VIN_UV_WARN_LIMIT • POWER_GOOD_ON • POWER_GOOD_OFF	160/3 when F2h, bit[2] = 0 160 when F2h, bit[2] = 1	0	0	V
• READ_PIN • READ_POUT • READ_EIN • POUT_OP_WARN_LIMIT	10/3 when F2h, bit[2] = 0 10 when F2h, bit[2] = 1	0	0	W
READ_TEMPERATURE	2	0	0	°C

SUPPORTED PMBUS COMMAND LIST

Name	Code	Type	Bytes	Default Value
OPERATION	01h	R/W with PEC	1	80h
CLEAR_FAULT	03h	Send byte with PEC	0	-
WRITE_PROTECT	10h	R/W with PEC	2	0080h
CAPABILITY	19h	Read with PEC	1	D0h
SMBALERT_MASK	1Bh	Read with PEC	2	FFFFh
IOUT_CAL_GAIN	38h	R/W with PEC	2	00F9h
IOUT_CAL_OFFSET	39h	R/W with PEC	2	0000h
IOUT_OC_WARN_LIMIT	4Ah	R/W with PEC	2	02A8h
VIN_OV_WARN_LIMIT	57h	R/W with PEC	2	0305h
VIN_UV_WARN_LIMIT	58h	R/W with PEC	2	0090h
POWER_GOOD_ON	5Eh	R/W with PEC	2	01E0h
POWER_GOOD_OFF	5Fh	R/W with PEC	2	01AAh
POUT_OP_WARN_LIMIT	6Ah	R/W with PEC	2	0535h
STATUS_BYTE	78h	Read with PEC	1	00h
STATUS_WORD	79h	Read with PEC	2	0000h
STATUS_IOUT	7Bh	Read with PEC	1	00h
STATUS_ INPUT	7Ch	Read with PEC	1	00h
STATUS_TEMPERATURE	7Dh	Read with PEC	1	00h
STATUS_CML	7Eh	Read with PEC	1	00h
STATUS_FET	80h	Read with PEC	1	00h
READ_EIN	86h	Block read with PEC	1 (byte) + 6 (data)	06h, 0000h, 00h, 000000h
READ_VIN	88h	Read with PEC	2	0000h
READ_VOUT	8Bh	Read with PEC	2	0000h
READ_IOUT	8Ch	Read with PEC	2	0000h
READ_TEMPERATURE	8Dh	Read with PEC	2	0000h
READ_IIN	8Eh	Read with PEC	2	0000h
READ_POUT	96h	Read with PEC	2	0000h
READ_PIN	97h	Read with PEC	2	0000h
PMBUS_REVISION	98h	Read with PEC	1	33h
MFR_ID	99h	Block read with PEC	3	ASCII “MPS”
MFR_MODEL	9Ah	Block read with PEC	6	ASCII “MP5024”
MFR_REVISION	9Bh	Read with PEC	1	00h
MFR_DATE	9Dh	Block read with PEC	6	ASCII “YYMMDD”
MFR_PMBUS_ADDR	F0h	Read with PEC	1	40h
MFR_PRT_CONFIG	F1h	R/W with PEC	2	0000h
MFR_TELEMETRY_CONFIG	F2h	R/W with PEC	2	0001h

REGISTER MAP

OPERATION (01h)

Format: Unsigned binary

The OPERATION command controls the power MOSFET, which provides another way to control the hot-swap on and off function via the PMBus. This command can turn the power MOSFET on and off under host control and re-enable the power MOSFET after a fault-triggered shutdown.

Bits	Access	Bit Name	Description
7	R/W	ON_OFF_STATE	1'b0: Turn off the power FET 1'b1: Turn on the power FET
6:0	R/W	RESERVED	Always write to 6'b 00 0000.

CLEAR_FAULT (03h)

The CLEAR_FAULT command clears all the status faults of the read-only STATUS registers (78h~80h). This command is write-only. There is no byte for this command.

WRITE_PROTECT (10h)

Format: Unsigned binary

The WRITE_PROTECTION command controls writing to the PMBus device. This provides protection against accidental changes. This command is not intended to provide protection against deliberate changes to a device's configuration or operation. All supported commands can have their parameters read, regardless of the WRITE_PROTECTION settings. The default setting is 0x0080, which disables all writes except the WRITE_PROTECTION command.

Bits	Access	Bit Name	Description
15:8	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R/W	WRITE_PROTECT	8'b 1000 0000: Disable all writes except to the WRITE_PROTECT command 8'b 0100 0000 and 0110 0000: Disable all writes except to WRITE_PROTECTION and OPERATION commands. 8'b 0000 0000: Enable writes to all commands Others: Writing error. Set the CML bit in STATUS_BYTE command and CML_OTHER_FAULTS bit in the STATUS_CML command

CAPABILITY (19h)

Format: Unsigned binary

The CAPABILITY command provides 1 byte to return the key capabilities that the PMBus device can support. The MP5024 always returns 0xD0.

Bits	Access	Bit Name	Description
7	R	PACKET_ERROR_ CHECKING	1'b1: Packet error checking (PEC) is supported
6:5	R	MAXIMUM_BUS_ SPEED	2'b10: The PMBus/I^2C maximum bus speed is 1MHz
4	R	SMBALERT#	1'b1: The MP5024 has an ALT_P# pin and supports the SMBus Alert Response protocol
3	R	NUMERIC_FORMAT	1'b0: Numeric data format is Linear 11, ULinear 16, SLinear 16, and direct format
2	R	AVSBUS_SUPPORT	1'b0: AVSBus is not supported
1:0	R	RESERVED	Reserved. Always returns 2'b00.

SMBALERT_MASK (1Bh)

Format: Unsigned binary

The SMBALERT_MASK command masks the faults or warnings to assert the ALT#.

Bits	Access	Bit Name	Description
15	R/W	VIN_OVP	1'b0: ALT# does not assert when a V_{IN} over-voltage (OV) fault occurs 1'b1: ALT# asserts when a V_{IN} OV fault occurs
14	R/W	VIN_OVW	1'b0: ALT# does not assert when a V_{IN} OV warning occurs 1'b1: ALT# asserts when a V_{IN} OV warning occurs
13	R/W	VIN_UVW	1'b0: ALT# does not assert when a V_{IN} under-voltage (UV) fault occurs 1'b1: ALT# asserts when a V_{IN} UV fault occurs
12	R/W	PEC	1'b0: ALT# does not assert when a packet error checking (PEC) error occurs 1'b1: ALT# asserts when a PEC error occurs
11	R/W	INVALID_CMD	1'b0: ALT# does not assert when the PMBus receives an invalid command 1'b1: ALT# asserts when the PMBus receives an invalid command
10	R/W	INVALID_DATA	1'b0: ALT# does not assert when the PMBus receives invalid data 1'b1: ALT# asserts when the PMBus receives invalid data
9	R/W	CML_OTHER_FLT	1'b0: ALT# does not assert when other PMBus communication faults occur 1'b1: ALT# asserts when other PMBus communication faults occur
8	R/W	GS_GD_ST	1'b0: ALT# does not assert when GS or GD faults occur 1'b1: ALT# asserts when GS or GD faults occur
7	R/W	DS_ST	1'b0: ALT# does not assert when a DS short fault occurs 1'b1: ALT# asserts when a DS short fault occurs
6	R/W	RESERVED	Unused.
5	R/W	OC_FAULT	1'b0: ALT# does not assert when an over-current (OC) fault occurs 1'b1: ALT# asserts when an OC fault occurs
4	R/W	OC_WARN	1'b0: ALT# does not assert when an OC warning occurs 1'b1: ALT# asserts when an OC warning occurs
3	R/W	OP_WARN	1'b0: ALT# does not assert when an over-power (OP) warning occurs 1'b1: ALT# asserts when an OP warning occurs
2:1	R/W	RESERVED	Unused.
0	R/W	OT_FAULT	1'b0: ALT# does not assert when an over-temperature (OT) fault occurs 1'b1: ALT# asserts when an OT fault occurs

IOUT_CAL_GAIN_TUNE (38h)

Format: Unsigned binary

The IOUT_CAL_GAIN_TUNE command provides 2 bytes to fine-tune the gain of the output current reported by the PMBus.

Bits	Access	Bit Name	Description
15:10	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R/W	IOUT_RPT_GAIN_TUNE	IOUT_PRT_GAIN_TUNE can be calculated with the IMON resistor and IMON gain: IOUT_RPT_GAIN_TUNE = R_{IMON} x G_{IMON} (0.05mΩ/LSB) The default is 0x00F9, which matches R_{IMON} = 2.49kΩ.

IOUT_CAL_OFFSET (39h)

Format: Two's complement

The IOUT_CAL_OFFSET command sets the I_{OUT} offset for the PMBus report.

Bits	Access	Bit Name	Description
15:9	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
8:0	R/W	IOUT_CAL_OFFSET	Sets the I_{OUT} report offset in two's complement data format. Bit[8] is the signed bit. The total offset only affects the final I_{OUT} PMBus report to READ_IOUT (8Ch). 31.25mA/LSB. The current list below shows the binary data and real-world value. 9'b 0 0000 0000: 0A 9'b 0 0000 0001: +(1/32)A 9'b 0 1111 1111: +(255/32)A 9'b 1 0000 0000: -8A 9'b 1 0000 0001: -(255/32)A 9'b 1 1111 1111: -(1/32)A

IOUT_OC_WARN_LIMIT (4Ah)

Format: Unsigned binary

The IOUT_OC_WARN_LIMIT command sets the over-current (OC) warning limit.

Bits	Access	Bit Name	Description
15:10	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R/W	IOUT_OC_WARN_ LIMIT	Sets the OC warning limit. 31.25mA/LSB

VIN_OV_WARN_LIMIT (57h)

Format: Unsigned binary

The VIN_OV_WARN_LIMIT command sets the input over-voltage (OV) warning threshold.

Bits	Access	Bit Name	Description
15:10	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R/W	VIN_OV_WARN_ LIMIT	Sets the input OV warning threshold. When F2h, bit[2] = 0: 18.75mV/LSB. Supports up to 19.18V When F2h, bit[2] = 1: 6.25mV/LSB. Supports up to 6.4V

VIN_UV_WARN_LIMIT (58h)

Format: Unsigned binary

The VIN_UV_WARN_LIMIT command sets the input under-voltage (UV) warning threshold.

Bits	Access	Bit Name	Description
15:10	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R/W	VIN_UV_WARN_ LIMIT	Sets the input under-voltage (UV) warning threshold. When F2h, bit[2] = 0: 18.75mV/LSB. Supports up to 19.18V When F2h, bit[2] = 1: 6.25mV/LSB. Supports up to 6.4V

POWER_GOOD_ON (5Eh)

Format: Unsigned binary

The POWER_GOOD_ON command sets the digital PG rising threshold. If MFR_PRT_CONFIG (F1h), bit[11] is set to 1, the PG rising threshold is configured via this command.

Bits	Access	Bit Name	Description
15:10	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R/W	POWER_GOOD_ON	Sets the digital PG rising threshold. When F2h, bit[2] = 0: 18.75mV/LSB. Supports up to 19.18V When F2h, bit[2] = 1: 6.25mV/LSB. Supports up to 6.4V

POWER_GOOD_OFF (5Fh)

Format: Unsigned binary

The POWER_GOOD_OFF command sets the digital PG falling threshold. If MFR_PRT_CONFIG (F1h), bit[11] is set to 1, the PG falling threshold is configured via this command.

Bits	Access	Bit Name	Description
15:10	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R/W	POWER_GOOD_OFF	Sets the digital PG falling threshold. When F2h, bit[2] = 0: 18.75mV/LSB. Supports up to 19.18V When F2h, bit[2] = 1: 6.25mV/LSB. Supports up to 6.4V

POUT_OP_WARN_LIMIT (6Ah)

Format: Unsigned binary

The POUT_OP_WARN_LIMIT sets the output over-power (OP) warning limit.

Bits	Access	Bit Name	Description
15:11	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
10:0	R/W	POUT_OP_WARN_ LIMIT	Sets the OP warning limit. When F2h, bit[2] = 0: 0.3W/LSB. Supports up to 599W When F2h, bit[2] = 0: 0.1W/LSB. Supports up to 199.7W

STATUS_BYTE (78h)

Format: Unsigned binary

The STATUS_BYTE command returns 1 byte of information with a summary of the most critical statuses and faults.

Bits	Access	Bit Name	Description
7	R	RESERVED	Unused. Writes are ignored and reads are always 0.
6	R	OFF	1’b0: GATE is high and V_{OUT} is on 1’b1: GATE is low and V_{OUT} is off
5	R	RESERVED	Always returns 0.
4	R	IOUT_OC_SC_ FAULT	Indicates whether an output over-current (OC) fault or short-circuit protection (SCP) were detected. Send a CLEAR_FAULTS (03h) command to reset this bit. 1’b0: No output OC or SC fault has occurred 1’b1: An output OC or SC fault has occurred
3	R	RESERVED	Always returns 0.

2	R	TEMPERATURE	Indicates whether an over-temperature (OT) fault has occurred. This bit is set and latched if OTP occurs. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No OT fault has occurred 1'b1: An OT fault has occurred
1	R	CML	Indicates whether a PMBus communication fault has occurred. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No communication, logic, and memory (CML) fault has occurred 1'b1: A CML fault has occurred
0	R	RESERVED	Always returns 0.

STATUS_WORD (79h)

Format: Unsigned binary

The STATUS_WORD (79h) command returns 2 bytes of information with a summary of the device's fault/warning conditions. The higher byte provides more detailed information of the fault conditions. The lower byte is same as the STATUS BYTE (78h) register.

Bits	Access	Bit Name	Description
15	R	RESERVED	Unused. Writes are ignored and reads are always 0.
14	R	IOUT/POUT	Indicates whether an I_{OUT}/P_{OUT} fault or warning has occurred. If an output current fault (over-current protection (OCP), short-circuit protection (SCP)), OC warning, or over-power (OP) warning occur, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No I_{OUT}/P_{OUT} fault and warning has occurred 1'b1: An I_{OUT}/P_{OUT} fault or warning has occurred
13	R	INPUT	Indicates whether an input voltage fault or warning has occurred. This includes over-voltage (OV) fault/warning and under-voltage (UV) warning. If any protection or warning occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No input fault or warning has occurred 1'b1: An input fault or warning has occurred
12	R	BAD_FET	Indicates whether the power FET has bad health. If a DS short or GS short occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No bad FET fault has occurred 1'b1: A bad FET fault has occurred
11	R	PGOOD	Indicates PG's live status. 1'b0: PG indicates high 1'b1: PG indicates low
10:8	R	RESERVED	Always returns 0.
7	R	RESERVED	Always returns 0.
6	R	OFF	1'b0: GATE is high and V_{OUT} is on 1'b1: GATE is low and V_{OUT} is off
5	R	RESERVED	Always returns 0.
4	R	IOUT_OC_SC_ FAULT	Indicates whether an output over-current (OC) fault or short-circuit protection (SCP) were detected. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No output OC or SC fault has occurred 1'b1: An output OC or SC fault has occurred

3	R	RESERVED	Always returns 0.
2	R	TEMPERATURE	Indicates whether an over-temperature (OT) fault has occurred. This bit is set and latched if OTP occurs. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No OT fault has occurred 1'b1: An OT fault has occurred
1	R	CML	Indicates whether a PMBus communication fault has occurred. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No communication, logic, and memory (CML) fault has occurred 1'b1: A CML fault has occurred
0	R	RESERVED	Always returns 0.

STATUS_IOUT (7Bh)

Format: Unsigned binary

The STATUS_IOUT command returns 1 byte of information with the detailed I_{OUT}/P_{OUT} fault and warning status.

Bits	Access	Bit Name	Description
7	R	IOUT_OC_SC_ FAULT	Indicates whether an output over-current (OC) or short-circuit (SC) fault has occurred. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No output OC fault or SC fault has occurred 1'b1: An output OC fault or SC fault has occurred
6	R	RESERVED	Always returns 0.
5	R	IOUT_OC_WARN	Indicates whether an OC warning has occurred. If an output OC warning occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No output OC warning has occurred 1'b1: An output OC warning has occurred
4	R	IOUT_SS_OC	Indicates whether an output soft start OC fault has occurred. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No output soft start OC fault has occurred 1'b1: An output soft start OC fault has occurred
3:1	R	RESERVED	Always returns 0.
0	R	POUT_OP_WARN	Indicates whether an over-power (OP) warning has occurred. If an output OP warning occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No output OP warning has occurred 1'b1: An output OP warning has occurred

STATUS_INPUT (7Ch)

Format: Unsigned binary

The STATUS_INPUT command returns 1 byte of information with detailed input fault and warning conditions.

Bits	Access	Bit Name	Description
7	R	VIN_OV_FAULT	Indicates whether a V_{IN} over-voltage (OV) fault has occurred. If the sensed V_{IN} exceeds the V_{IN} OV fault limit, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{IN} OV fault has occurred 1'b1: A V_{IN} OV fault has occurred

6	R	VIN_OV_WARN	Indicates whether a V_{IN} OV warning has occurred. If the sensed V_{IN} exceeds VIN_OV_WARN_LIMIT (57h), this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{IN} OV warning has occurred 1'b1: A V_{IN} OV warning has occurred
5	R	VIN_UV_WARN	Indicates whether a V_{IN} under-voltage (UV) warning has occurred. If the sensed V_{IN} is below VIN_UV_WARN_LIMIT (58h), this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No V_{IN} UV warning has occurred 1'b1: A V_{IN} UV warning has occurred
4:0	R	RESERVED	Always returns 0.

STATUS_TEMPERATURE (7Dh)

Format: Unsigned binary

The STATUS_TEMPERATURE command returns 1 byte of information with temperature-related fault and warning conditions.

Bits	Access	Bit Name	Description
7	R	OT_FAULT	Indicates whether an over-temperature (OT) fault has occurred. If an on-die OT fault occurs, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No OT fault has occurred 1'b1: An OT fault has occurred
6:0	R	RESERVED	Unused. Writes are ignored and reads are always 0.

STATUS_CML (7Eh)

Format: Unsigned binary

The STATUS_CML command returns 1 byte of information with communication-related fault conditions.

Bits	Access	Bit Name	Description
7	R	INVALID_CMD	Indicates whether an invalid PMBus command has been received. This bit is set and latched when the MP5024 receives an unsupported command code. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No invalid PMBus command has been received 1'b1: An invalid PMBus command has been received
6	R	INVALID_DATA	Indicates whether invalid PMBus data has been received. This bit is set and latched when the MP5024 receives unsupported data. Send a CLEAR_FAULTS (03h) command to reset this bit. 1'b0: No invalid PMBus data has been received 1'b1: Invalid PMBus data has been received
5	R	PEC_ERROR	Indicates whether a PMBus packet error checking (PEC) fault has been detected. The PMBus interface supports the use of a PEC byte that is defined in the SMBus standard. The PEC byte is transmitted by the MP5024 during a read transaction or sent to the MP5024 during a write transaction. If the PEC byte sent to the controller during a write transaction is incorrect, the command is not executed and PEC_FAULT is set and latched. Send a CLEAR_FAULTS (03h) command to clear the fault. 1'b0: No PEC fault has been detected 1'b1: A PEC fault has been detected
4:2	R	RESERVED	Always returns 0.

1	R	CML_OTHER_ FAULTS	If any faults listed below occur during PMBus communication, this bit is set and latched. Send a CLEAR_FAULTS (03h) command to clear the fault. 1) Sending too few bits 2) Reading too few bits 3) Host sends or reads too few bytes 4) Reading too many bytes 5) Writing error
0	R	RESERVED	Always returns 0.

STATUS_FET (80h)

Format: Unsigned binary

The STATUS_FET command returns 1 byte of information with the detailed bad FET health fault conditions.

Bits	Access	Bit Name	Description
7:3	R	RESERVED	Unused. Writes are ignored and reads are always 0.
2	R	GS_HIGH_FLT	Indicates whether a high gate-to-source (GS) fault has occurred, including gate-to-drain (GD) shorts and GS going high before turning on. 1'b0: No GD short or GS high fault have been detected 1'b1: A GD short or GS high fault have been detected
1	R	GS_SHORT	Indicates whether a GS short has been detected. The bit is set and latched when a GS short is detected. Send a CLEAR_FAULTS (03h) command to clear the fault. 1'b0: No GS short has been detected 1'b1: A GS short has been detected
0	R	DS_SHORT	Indicates whether a drain-to-source (DS) short has been detected. The bit is set and latched when a DS short is detected. Send a CLEAR_FAULTS (03h) command to clear the fault. 1'b0: No DS short has been detected 1'b1: A DS short has been detected

READ_EIN (86h)

Format: Unsigned binary

The READ_EIN command returns the 16 bits of the energy accumulator, the 8 bits of the rollover counter, and the 24 bits of the sample counter. This is the preferred command for supporting input power monitoring. This command provides a more flexible method for power sensing so that the system can supply faster or slower power data, depending on how fast the host polls the device.

The READ_EIN register sampling period is about 290µs, which is the same as the READ_IOUT register updating rate (3.4kHz). When READ_IOUT is sampled, the input energy (E_{IN}) and input power (P_{IN}) registers (READ_EIN (86h) and READ_PIN (97h), respectively) are updated simultaneously.

Byte	Access	Byte Name	Description
5	R	SAMPLE_CNT_HI	This is the total number of P_{IN} samples acquired and accumulated in the energy count accumulator. Byte[5] is the high byte, byte[4] is the middle byte, and byte[3] is the low byte. This is a straight 24-bit binary value.
4	R	SAMPLE_CNT_MID	Sample count middle byte.
3	R	SAMPLE_CNT_LO	Sample count low byte.

2	R	ROLLOVER_CNT	Returns the number of times that the energy count has rolled over from 0x7FFF to 0x0000. This is a straight 8-bit binary value.
1	R	EIN_HI	Returns the energy accumulator value in direct format. Byte[1] is the high byte, and byte[0] is the low byte. Internally, the energy accumulator is a 16-bit value.
0	R	EIN_LO	Returns the energy accumulator value in direct format. Byte[1] is the high byte, and byte[0] is the low byte. Internally, the energy accumulator is a 16-bit value.

READ_VIN (88h)

Format: Direct

The READ_VIN command returns the sensed V_{IN}. This value is also used internally for V_{IN} over-voltage (OV) and under-voltage (UV) warning detection.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R	READ_VIN	Returns the sensed V_{IN}. When F2h, bit[2] = 0: 18.75mV/LSB When F2h, bit[2] = 1: 6.25mV/LSB

READ_VOUT (8Bh)

Format: Direct

The READ_VOUT command returns the sensed V_{OUT}. This value is also used to determine the digital PG indication.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R	READ_VOUT	Return the sensed V_{OUT}. When F2h, bit[2] = 0: 18.75mV/LSB When F2h, bit[2] = 1: 6.25mV/LSB

READ_IOUT (8Ch)

Format: Direct

The READ_IOUT command returns the measured I_{OUT}.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R	READ_IOUT	Returns the sensed I_{OUT}. 31.25mA/LSB.

READ_TEMPERATURE (8Dh)

Format: Direct

The READ_TEMPERATURE command returns the sensed temperature.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R	READ_ TEMPERATURE	Returns the sensed temperature. Bit[9] = 0: Indicates a positive temperature Bit[9] = 1: Indicates a negative temperature Bits[8:0]: Indicates the absolute temperature. 0.5°C /LSB

READ_IIN (8Eh)

Format: Direct

The READ_IIN command returns the measured I_{IN}.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R	READ_IIN	Return the sensed I_{IN}. 31.25mA/LSB.

READ_POUT (96h)

Format: Direct

The READ_POUT command returns the sensed P_{OUT}.

Bits	Access	Bit Name	Description
15:11	R	RESERVED	Unused. Writes are ignored and reads are always 0.
10:0	R	READ_POUT	Returns the sensed P_{OUT}. When F2h, bit[2] = 0: 0.3W/LSB When F2h, bit[2] = 1: 0.1W/LSB

READ_PIN (97h)

Format: Direct

The READ_PIN command returns the total P_{IN}.

Bits	Access	Bit Name	Description
15:11	R	RESERVED	Unused. Writes are ignored and reads are always 0.
10:0	R	READ_PIN	Return the total P_{IN}. When F2h, bit[2] = 0: 0.3W/LSB When F2h, bit[2] = 1: 0.1W/LSB

PMBUS_REVISION (98h)

Format: Unsigned binary

The PMBUS_REVISION command reads the PMBus revision to which the device is compliant. It is read-only.

Bits	Access	Bit Name	Description
7:0	R	PMBUS_REVISION	Always returns 0x33. This means that the VR supports PMBus revision to 1.3.

MFR_ID (99h)

Format: Unsigned binary

The MFR_ID command sets the manufacturer's ID for users. The format is text (ISO/IEC 8859-1) characters (i.e. ASCII character array). This is a block read command with 3 bytes of data.

Byte	Access	Byte Name	Description
2	R	ID3	Returns the ASCII code of character "M" (i.e. 0x4D).
1	R	ID2	Returns the ASCII code of character "P" (i.e. 0x50).
0	R	ID1	Returns the ASCII code of character "S" (i.e. 0x53).

MFR_MODEL (9Ah)

Format: Unsigned binary

The MFR_MODEL command returns the part name (MP5024). The format is text (ISO/IEC 8859-1) characters (i.e. ASCII character array). This is a block read command with 6 bytes of data.

Byte	Access	Byte Name	Description
5	R	MODEL6	Returns the ASCII code of character "M" (i.e. 0x4D).
4	R	MODEL5	Returns the ASCII code of character "P" (i.e. 0x50).
3	R	MODEL4	Returns the ASCII code of character "5" (i.e. 0x35).
2	R	MODEL3	Returns the ASCII code of character "0" (i.e. 0x30).
1	R	MODEL2	Returns the ASCII code of character "2" (i.e. 0x32).
0	R	MODEL1	Returns the ASCII code of character "4" (i.e. 0x34).

MFR_REVISION (9Bh)

Format: Unsigned binary

The MFR_REVISION command provides 1 byte for users to track the product revision. It is read-only.

Bits	Access	Bit Name	Description
7:0	R	REVISION	Returns the silicon revision.

MFR_DATE (9Dh)

Format: Unsigned binary

The MFR_DATE command provides six bytes to return the part's manufacture date with the format ASCII "YYMMDD."

Byte	Access	Byte Name	Description
5	R	DATE6	YY. Identifies the year that the part is manufactured.
4	R	DATE5	YY. Identifies the year that the part is manufactured.
3	R	DATE4	MM. Identifies the month that the part is manufactured.
2	R	DATE3	MM. Identifies the month that the part is manufactured.
1	R	DATE2	DD. Identifies the date that the part is manufactured.
0	R	DATE1	DD. Identifies the date that the part is manufactured.

MFR_PMBUS_ADDR (F0h)

Format: Unsigned binary

The PMBUS_REVISION command returns the sensed PMBus address. It is read-only.

Bits	Access	Bit Name	Description
7	R	RESERVED	Unused. Writes are ignored and reads are always 0.
6:4	R	PMBUS_ADDR_ BASE	Always returns 3'b100.
3	R	PMBUS_ADDR_HIGH	Returns the sensed PMBus address set by the MODE pin.
2:0	R	PMBUS_ADDR_LOW	Returns the sensed PMBus address set by the ADDR pin.

MFR_PRT_CONFIG (F1h)

Format: Unsigned binary

The MFR_PRT_CONFIG command sets the protection related configurations.

Bits	Access	Bit Name	Description
15:12	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
11	R/W	PG_MODE	Selects whether the PG threshold is set by analog design or the digital register. See the Power Good (PG) section on page 19 for more details. 1'b0: PG threshold is set by analog design 1'b1: PG threshold is set by PMBus registers 5Eh and 5Fh
10:9	R/W	RETRY_DELAY_ TIME	Sets the retry delay time. 2'b00: 500ms 2'b01: 250ms 2'b10: 1s 2'b11: reserved
8:0	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.

MFR_TELEMETRY_CONFIG (F2h)

Format: Unsigned binary

The MFR_TELEMETRY_CONFIG sets the PMBus telemetry related configurations.

Bits	Access	Bit Name	Description
15:3	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
2	R/W	VIN_VOUT_SEN	Selects the V_{IN} and V_{OUT} internal sensing divider ratio. The input and output voltage digital-sensing gain changes automatically with the divider ratio. 1'b0: 1:12 1'b1: 1:4
1:0	R/W	FILTER	Select the VIN/VOUT/TEMPERATURE/IMON digital average filter. 2'b00 or 2b'11: 1 time 2'b01: 4 times 2'b10: 8 times

APPLICATION INFORMATION

Setting the Soft-Start Time (t_{SS})

A capacitor (C_{SS}) connected to the SS pin determines t_{SS}. V_{OUT} rises at a similar slew rate to V_{SS}.

C_{SS} can be calculated with Equation (7):

$$C_{SS}(nF) = 9 \times \frac{t_{SS}(ms)}{R_{SS}(M\Omega)} \quad (7)$$

Where R_{SS} is 0.89MΩ.

For example, placing a 100nF capacitor from SS to GND can achieve a 9.9ms soft-start time.

Setting the Current Limit

The MP5024's normal current limit value should exceed the normal maximum load current, allowing the tolerances within the current-sense value. The current limit can be estimated with Equation (8):

$$I_{LIMIT}(A) = \frac{0.3V}{R_{ISET}(k\Omega)} \times 10^3 \quad (8)$$

Insertion Delay and OC Fault Timer (C_{TMR})

The MP5024's TIMER pin serves two functions: it sets the insertion delay time and OCP timer.

The insertion delay time can be calculated with Equation (9):

$$t_{IDT}(ms) = \frac{1.21}{4} \times C_{TMR}(nF) \quad (9)$$

The fault timer can be estimated with Equation (10):

$$t_{OC}(ms) = \frac{1.21}{40} \times C_{TMR}(nF) \quad (10)$$

Where C_{TMR} is the timer capacitor (in nF). Placing a 10nF capacitor from TIMER to GND can achieve a 3ms insertion delay time and 300µs OCP fault timer.

PCB Layout Guidelines

Efficient PCB layout is critical for optimal IC performance. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 14 and follow the guidelines below:

1. Place the MP5024 close to the board's input connector to minimize trace inductance.
2. Place a small capacitor (C_{IN}, 100nF) close to VIN and GND to minimize transients, which may occur on the input supply line. Transients of several volts can occur easily when the load current is shut off.
3. Place a 1µF capacitor as close to VCC as possible.
4. Keep the high-current path from the board's input to load and the return path close to each other, and in parallel, to minimize loop inductance.
5. Place an analog signal ground (AGND) plane locally in the MP5024, and connect it to the PCB power ground planes at a single point.
6. Place the vias to improve thermal performance.
   a. Place 6 vias (or more) on the bottom VIN pad.
   b. Place 6 vias (or more) close to the MP5024's VOUT pads.
   c. Place 3 vias (or more) close to the input TVS diode's pads.
   d. Place 3 vias (or more) close to the output Schottky diode's pads.

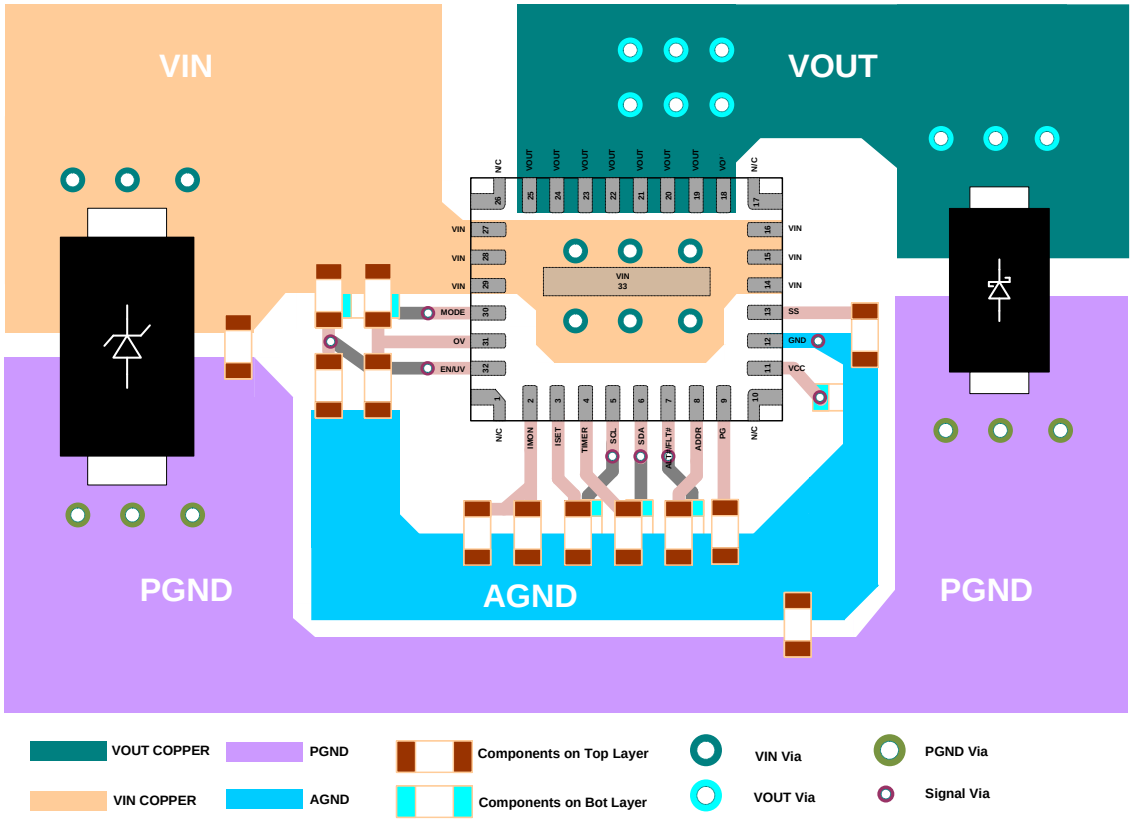


Figure 14: Example of PCB Layout (Placement and Top Layer PCB)

VIN TVS: SMDJ12A

VOUT Diode: B330A

TYPICAL APPLICATION CIRCUIT

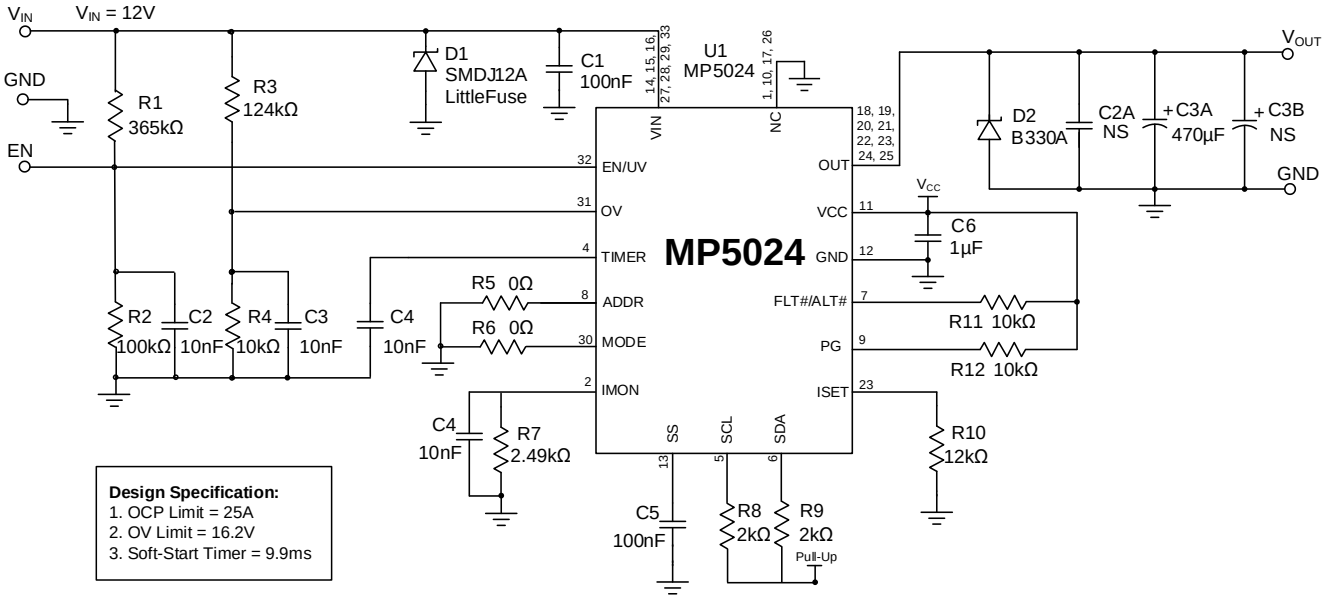
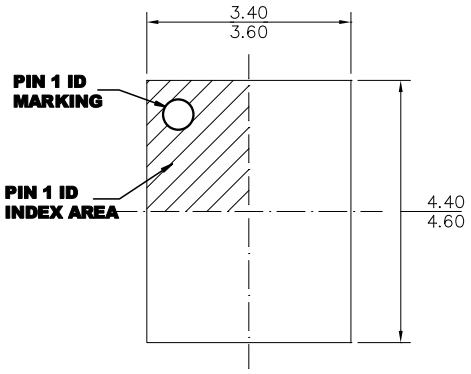


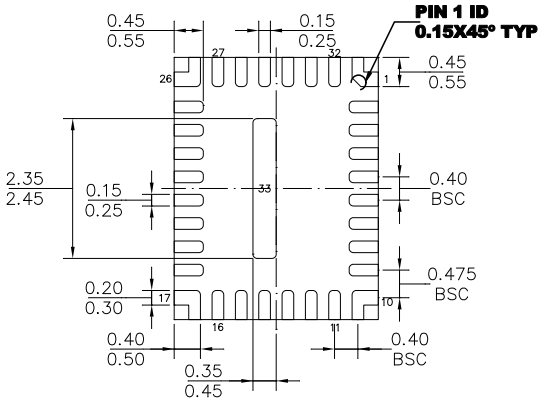
Figure 15: Typical Application Circuit (V_{IN} = 12V, OC Limit = 25A)

PACKAGE INFORMATION

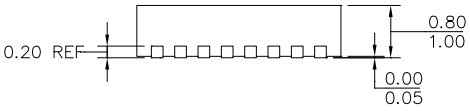
QFN-33 (3.5mmx4.5mm)



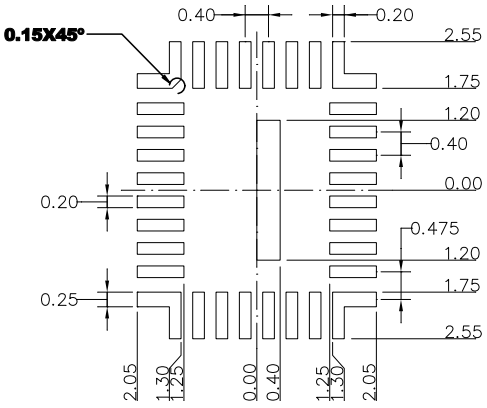
TOP VIEW



BOTTOM VIEW



SIDE VIEW

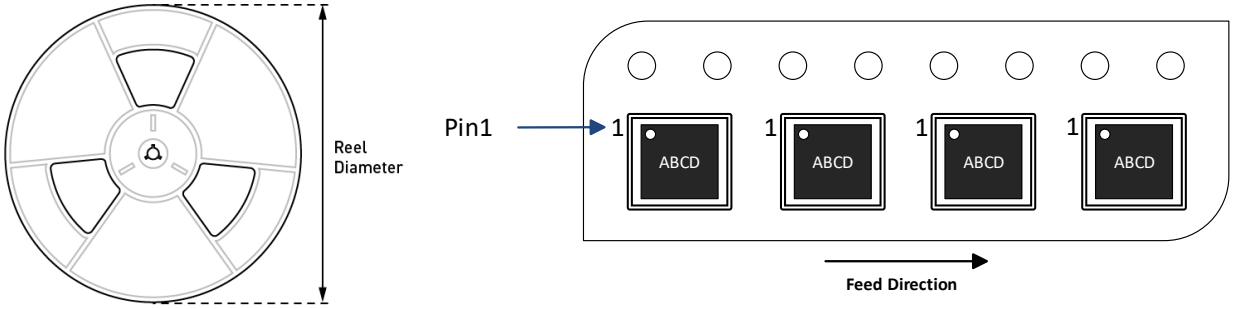


RECOMMENDED LAND PATTERN

NOTE:

1)ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP5024GRM-Z	QFN-33 (3.5mmx4.5mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	4/1/2024	Initial Release	-