MP5017A

3V to 5.5V, 1A to 5A Current Limit Switch with Over-Voltage Clamp and Reverse Blocking in a 2mmx3mm QFN Package

DESCRIPTION

The MP5017A is a protection device designed to protect circuitry on the output from transients from the input. It also protects the input from unwanted shorts and transients coming from the output.

During start-up, the inrush current is controlled by limiting the slew rate at the output. The slew rate is controlled with a small capacitor at the DV/DT pin.

The maximum load at the output is current-limited. The magnitude of the current limit is controlled by an external resistor placed between ILIMIT and GND. By controlling the gate voltages with a pair of N-channel MOSFETs, any current flowing from the output to the input is blocked.

Under-voltage lockout (UVLO) ensures that the input is above the minimum operating threshold before the device is turned on. If the input voltage (V_{IN}) exceeds 5.8V, the output voltage (V_{OUT}) is quickly limited to 5.8V. SAS/OV is used to program the input over-voltage protection (OVP) threshold. $\overline{FAULT}$ is an open-drain output that reports a fault (goes low) when any over-current, over-temperature, or output over-voltage fault is detected.

The MP5017A is available in a QFN-12 (2mmx3mm) package.

FEATURES

- 3V to 5.5V Continuous Operating Input Voltage (V_{IN}) Range
- 16V Absolute Maximum V_{IN}
- Output Discharge
- SAS/OV Disable to Support DEVSLP or POWER_DOWN
- 5.8V Fast Output OVP Response
- Reverse Current Blocking
- Integrated 45mΩ $R_{DS(ON)}$ Power MOSFET
- Adjustable Current-Limit through ILIMIT
- 210μA Low Quiescent Current (I_Q)
- Programmable Soft-Start Time (t_{SS}) via the DV/DT Pin
- Fast Response for Hard-Short Protection
- Fault Indication for Over-Current Protection (OCP), Over-Temperature Protection (OTP), and Output Over-Voltage Protection (OVP)
- OTP Auto-Retry with 76ms Recovery Delay
- Available in a QFN-12 (2mmx3mm) Package

APPLICATIONS

- HDDs and SSDs
- Hot Swap Devices
- Wireless Modem Data Cards
- PC Cards
- USB Power Distribution

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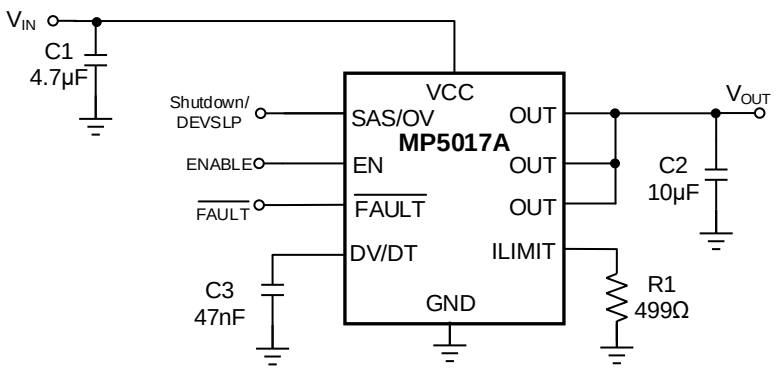
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP5017AGD	QFN-12 (2mmx3mm)	*See Below*	1

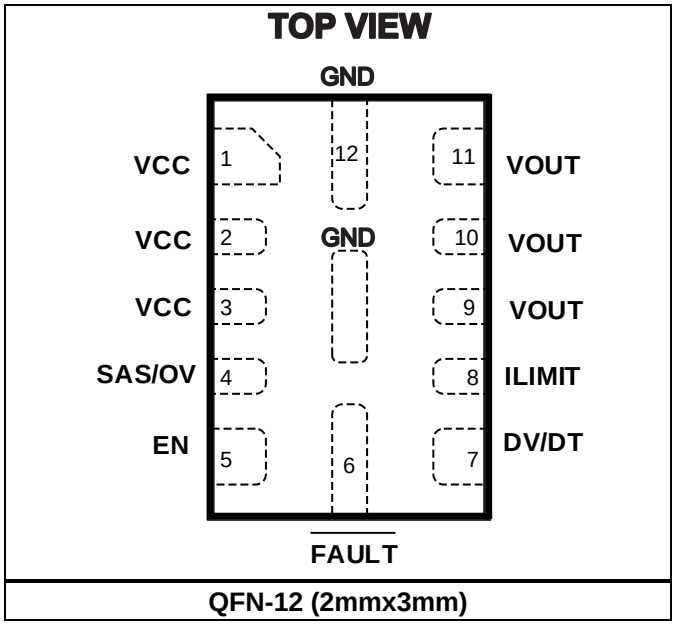
* For Tape & Reel, add suffix -Z (e.g. MP5017AGD-Z).

TOP MARKING

$\overline{\text{BTA}}$
YWW
LLLL

BTA: Product code of MP5017AGD
Y: Year code
WW: Week code
LLLL: Lot number

PACKAGE REFERENCE



QFN-12 (2mmx3mm)

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PIN FUNCTIONS

Pin #	Name	Description
1, 2, 3	VCC	**Supply voltage.** The MP5017A operates from a 3V to 5.5V continuous input voltage (V_{IN}) range, with up to 16V of maximum transient V_{IN}. Decouple the input rail with a 4.7µF ceramic capacitor. Use wide copper traces for all connections to VCC.
4	SAS/OV	**SAS disable pin.** Pull SAS/OV low to enable the part; pull SAS/OV high to disable the part. SAS/OV has an internal 1MΩ pull-down resistor connected to ground, so that the MP5017A can start up automatically when SAS/OV is floating. Connect SAS/OV to the tap of an external resistor divider, placed between the input and GND, to set the input over-voltage (OV) threshold.
5	EN	**Enable.** EN is a digital input pin that turns the regulator on and off. Float EN or pull EN high to turn on the regulator; pull EN low to turn off the regulator.
6	$\overline{\text{FAULT}}$	**Open-drain output.** If over-current protection (OCP), over-temperature protection (OTP), or output over-voltage protection (OVP) occurs, $\overline{\text{FAULT}}$ is pulled low.
7	DV/DT	**Slew rate.** The internal DV/DT circuit controls the output voltage (V_{OUT}) slew rate at start-up. An external capacitor from DV/DT to ground is requited to set the soft-start time (t_{SS}).
8	ILIMIT	**Current limit setting pin.** Place a resistor between ILIMIT and ground to set the current limit value.
9, 10, 11	VOUT	**Output voltage.** This pin is the output terminal of the IC. V_{OUT} is controlled by the IC.
12, exposed pad	GND	**System ground.**

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} .....-0.3V to +16V
V_{OUT}..... 6.3V
All other pins .....-0.3V to +6V
Junction temperature ..... -40°C to +150°C
Lead temperature .....260°C
Continuous power dissipation ... (T_A = 25°C) (2) (4)
QFN-12 (2mmx3mm) 3.125W

ESD Ratings

Human body model (HBM) ..... ±2000V
Charged device model (CDM) ..... ±750V

Recommended Operating Conditions (3)

Continuous operation (V_{IN}).....3V to 5.5V
Supply maximum transient (V_{IN}) 16V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance	θ_{JA}	θ_{JC}
EV5017A-D-00A (4)	40	7°C/W
JESD51-7 (5)	70	15°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on EV5017A-D-00A, 2-layer (64mmx64mm) PCB.
5) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, R_{LIMIT} = 499Ω, C_{OUT} = 10μF, T_J = -40°C to +125°C (6), typical value is tested at T_J = 25°C unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Quiescent current	I_Q	EN, no load		210	310	μA
		EN = 0, SAS/OV = 0V		10	15	μA
		SAS/OV = 3V, EN = 5V			120	μA
Power MOSFET						
On resistance	$R_{DS(ON)}$	T_J = 25°C		45		mΩ
On resistance (7)	$R_{DS(ON)}$	T_J = 80°C		54		mΩ
Turn-on delay	t_{DELAY}	I_{OUT} = 0A, $C_{DV/DT}$ = 1nF		160		μs
Off-state leakage current	I_{OFF}	V_{IN} = 14V, EN = 0V			1	μA
Under-Voltage Protection (UVP)/Over-Voltage Protection (OVP)						
Under-voltage lockout (UVLO) threshold	V_{UVLO}	UVLO rising threshold	2.45	2.7	2.95	V
UVLO hysteresis	$V_{UVLOHYS}$			250		mV
Output over-voltage (OV) clamp voltage	V_{OVLO}		5.5	5.8	6.1	V
Output OV response time (7)	t_{OUT_OV}	C_{OUT} = 10μF, add 10Ω load resistor, V_{IN} = 5V to 7V/20μs		10	20	μs
DV/DT						
DV/DT current	$I_{DV/DT}$	Short DV/DT to GND, or add DV/DT capacitor	4.5	6.5	8.5	μA
Current Limit						
Current limit at normal operation	I_{LIMIT_NO}	R_{LIMIT} = 499Ω, V_{OUT} drops 10%	2	2.4	2.8	A
		R_{LIMIT} = 1.4kΩ, V_{OUT} drops 10%		0.9		A
Current limit response time (7)	t_{CL}	I_{LIMIT} = 3A, add 1Ω load resistor		10		μs
Secondary current limit (7)	I_{LIMITH}	Any value of R_{LIMIT}		7.5		A
Reverse Current Limit						
Reverse current limit	$I_{REVERSE}$	Any value of R_{LIMIT}	-5	-50	-200	mA
Reverse current limit deglitch time (7)	$t_{REVERSE}$			80		μs
Secondary reverse current limit (7)	$I_{REVERSEH}$	Fast response		-1		A
Secondary reverse current limit response time (7)	t_{SC}	V_{IN}_DV/DT = -5V/100μs		8		μs
Enable						
EN rising threshold	V_{EN_RISING}		1.4	1.47	1.55	V
EN hysteresis	V_{EN_HYS}			200		mV
EN pull-up current	I_{EH_PL}	V_{ENABLE} = 0V		3.4		μA

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, R_{LIMIT} = 499Ω, C_{OUT} = 10μF, T_J = -40°C to +125°C (6), typical value is tested at T_J = 25°C unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
SAS/OV						
Rising threshold	V_{SAS/OV_RISING}	Output disabled	1.2	1.25	1.3	V
Hysteresis	V_{SAS/OV_HYS}			40		mV
Input OV deglitch time	$t_{IN_SAS/OV}$			5		μs
$\overline{FAULT}$						
$\overline{FAULT}$ output logic low voltage	V_{FAULT_L}	Sink 1mA			200	mV
$\overline{FAULT}$ output high leakage current	I_{FAULT_OFF}	V_{FAULT} = 5.5V			1	μA
$\overline{FAULT}$ deglitch time	$t_{FAULT_DEG_OC}$	Delay time for assertion or de-assertion due to an OCP fault condition		5		ms
	$t_{FAULT_DEG_OV_OUTPUT}$ (7)	Delay time for assertion or de-assertion due to an output OVP fault condition after soft start completes		10		μs
Output Discharge						
Discharge resistance	R_{DIS}	V_{CC} = 5V		130		Ω
OTP						
Thermal shutdown (7)	T_{SD}			175		°C
Thermal hysteresis (7)	T_{SD-HYS}			50		°C

Notes:

6) Not tested in production. Guaranteed by over-temperature correlation.
7) Guarantee by engineering sample characterization.

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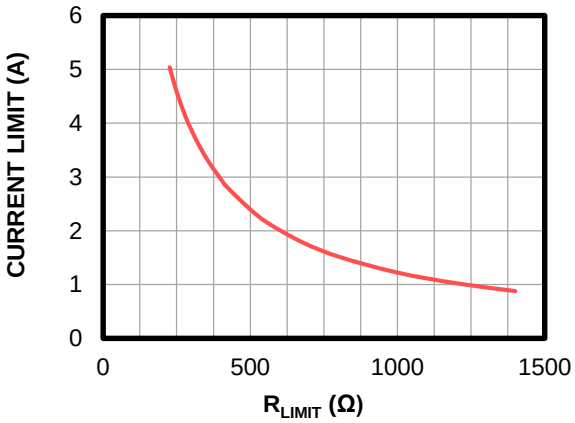
TYPICAL CHARACTERISTICS

Performance waveforms are tested on the evaluation board (see the Design Example section on page 14), V_{IN} = 5V, V_{EN} = 5V, R_{LIMIT} = 499Ω, SAS/OV floating, C_{OUT} = 10μF, T_A = 25°C, unless otherwise noted.

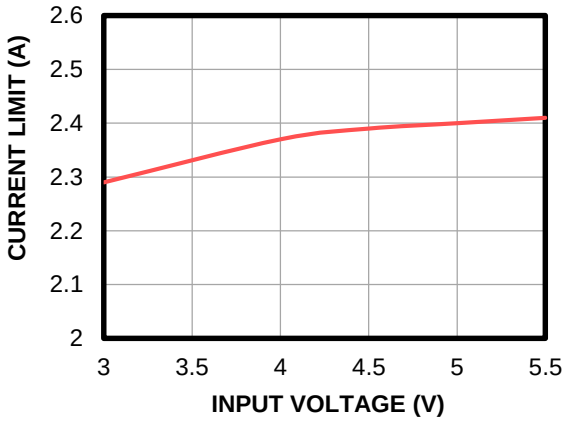
Current Limit vs. R_{LIMIT}

V_{OUT} drops 10%



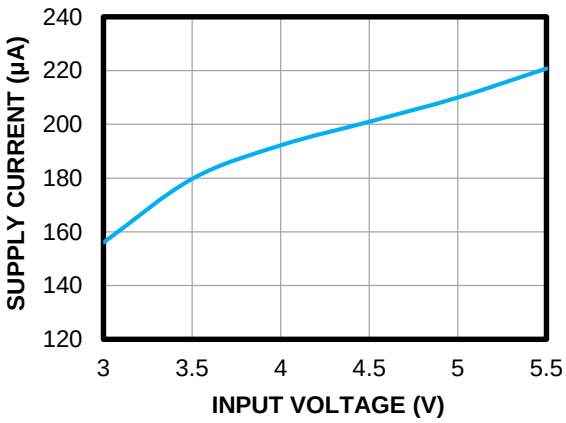
Current Limit vs. Input Voltage

R_{LIMIT} = 499Ω



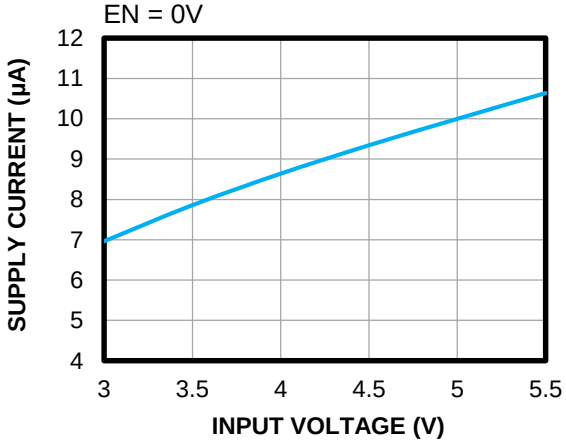
Supply Current vs. Input Voltage

EN = 5V



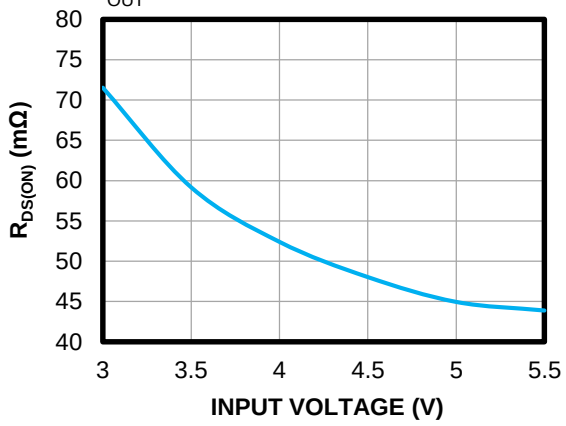
Supply Current vs. Input Voltage

EN = 0V



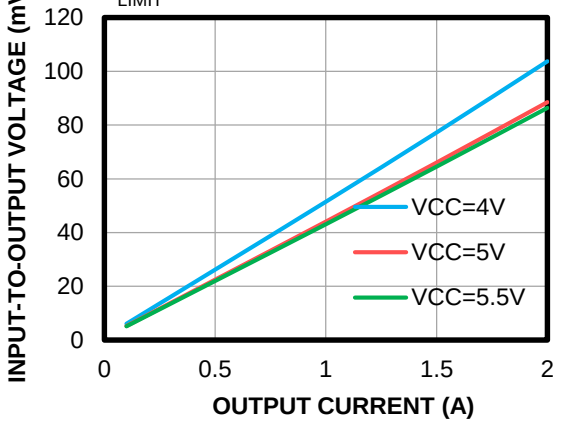
$R_{DS(ON)}$ vs. Input Voltage

I_{OUT} = 0.5A



Input-to-Output Voltage vs. Output Current

R_{LIMIT} = 499Ω



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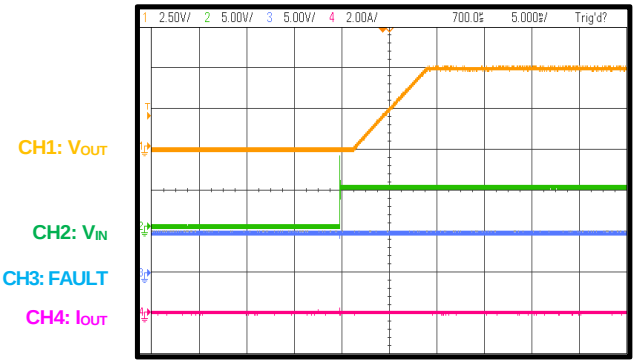
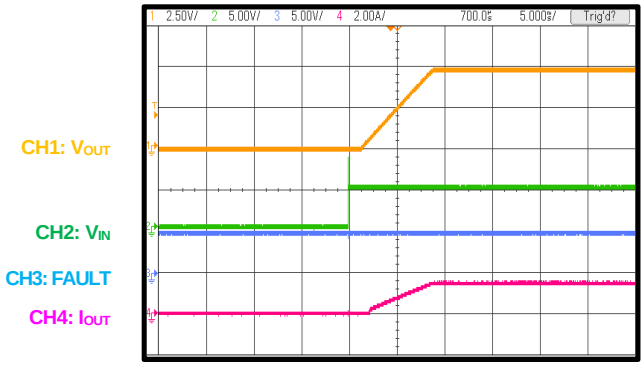
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board (see the Design Example section on page 14), V_{IN} = 5V, V_{EN} = 5V, R_{LIMIT} = 499Ω, SAS/OV floating, C_{OUT} = 10μF, T_A = 25°C, unless otherwise noted.

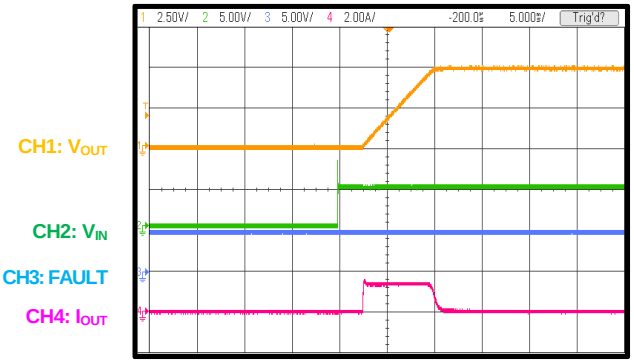
Start-Up through VIN
No load



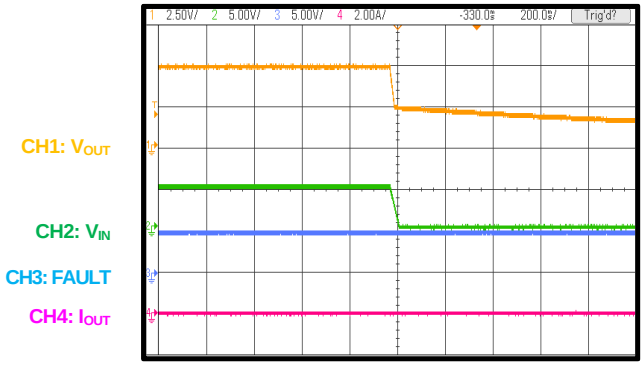
Start-Up through VIN
Load = 3.3Ω



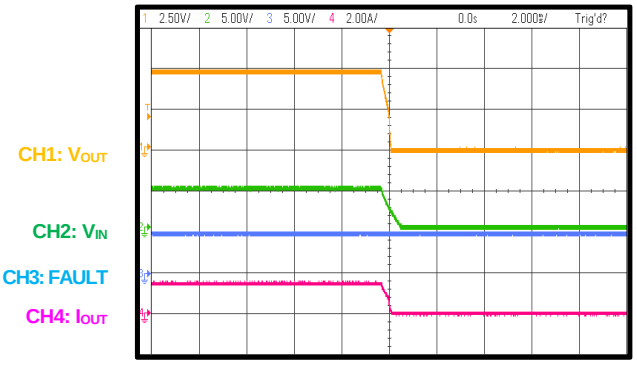
Start-Up through VIN
No load, C_{OUT} = 2200μF



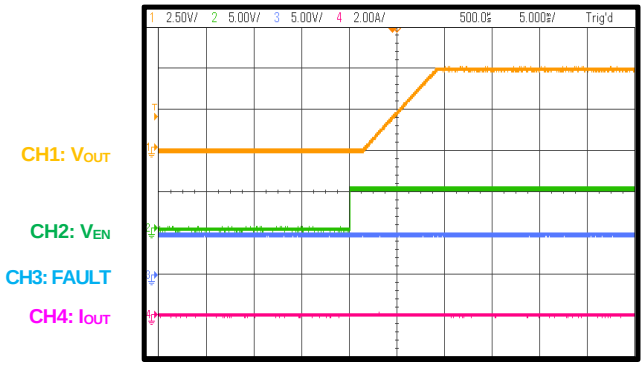
Shutdown through VIN
No load



Shutdown through VIN
Load = 3.3Ω



Start-Up through EN
No load



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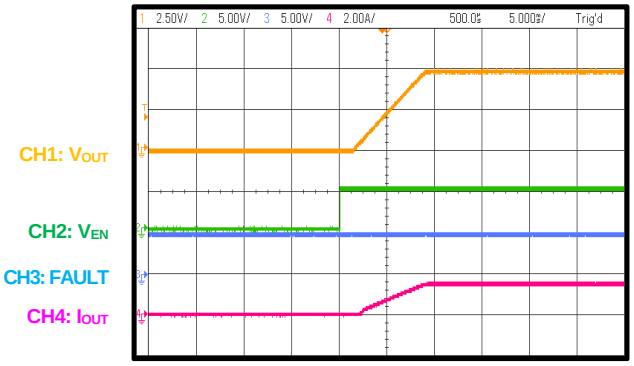
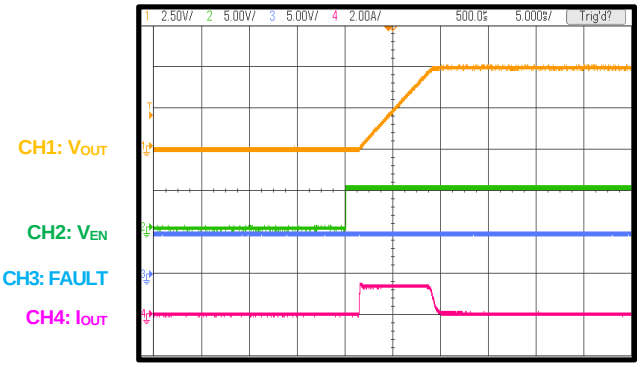
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board (see the Design Example section on page 14), V_{IN} = 5V, V_{EN} = 5V, R_{LIMIT} = 499Ω, SAS/OV floating, C_{OUT} = 10µF, T_A = 25°C, unless otherwise noted.

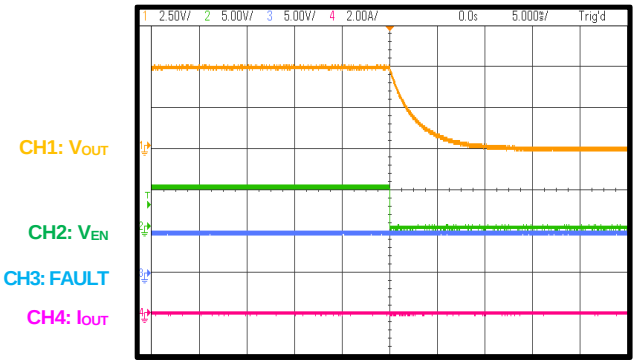
Start-Up through EN
Load = 3.3Ω



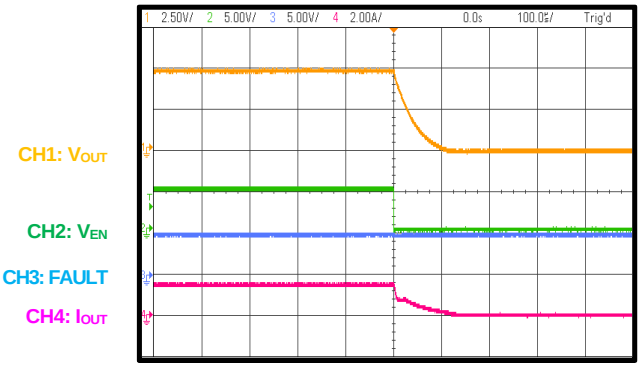
Start-Up through EN
No load, C_{OUT} = 2200µF



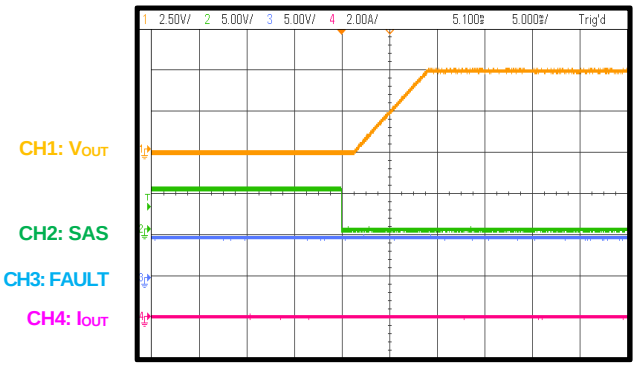
Shutdown through EN
No load



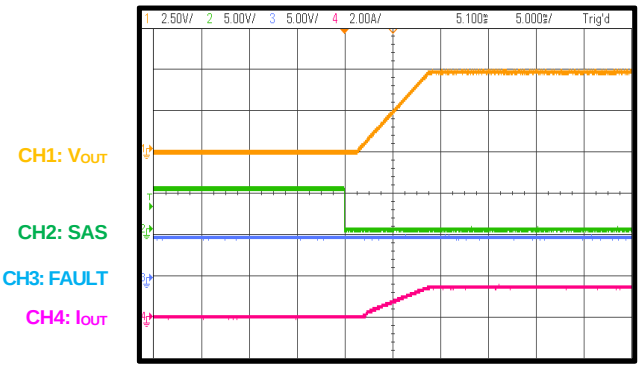
Shutdown through EN
Load = 3.3Ω



Start-Up through SAS
No load



Start-Up through SAS
Load = 3.3Ω



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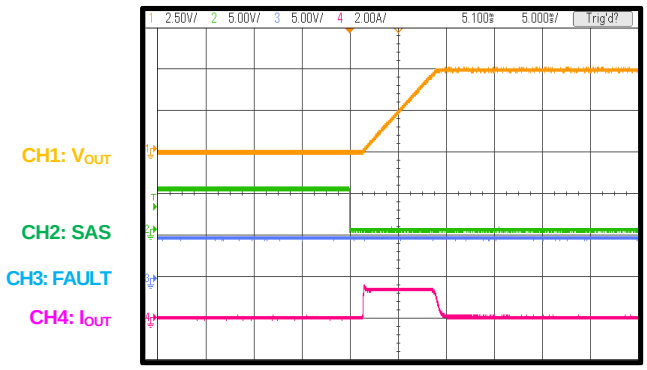
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board (see the Design Example section on page 14), V_{IN} = 5V, V_{EN} = 5V, R_{LIMIT} = 499Ω, SAS/OV floating, C_{OUT} = 10µF, T_A = 25°C, unless otherwise noted.

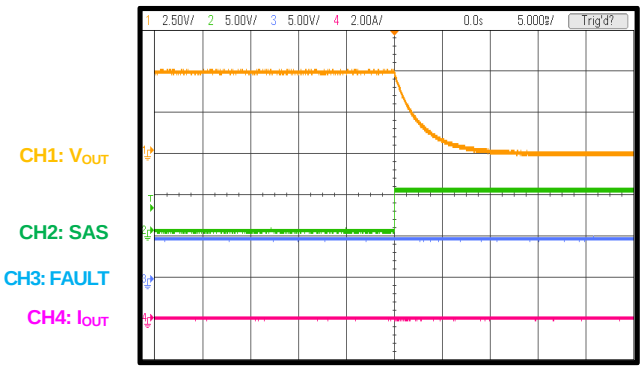
Start-Up through SAS

No load, C_{OUT} = 2200µF



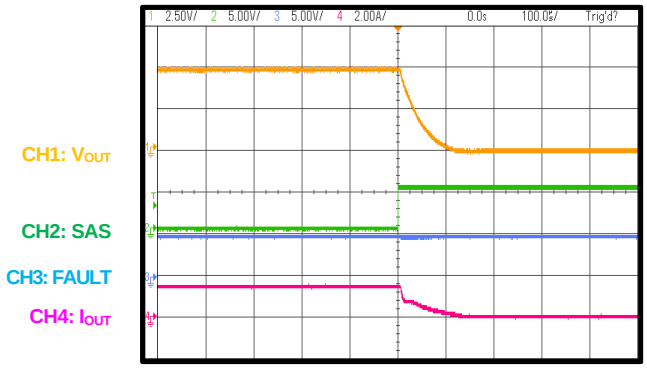
Shutdown through SAS

No load



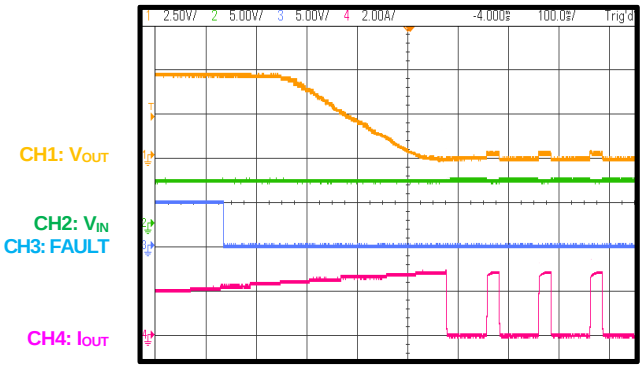
Shutdown through SAS

Load = 3.3Ω

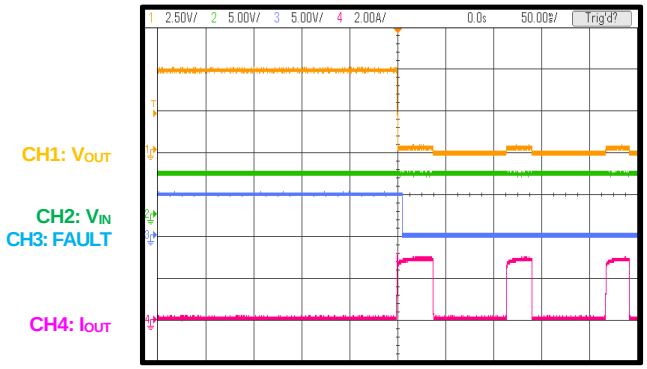


Over-Current Protection

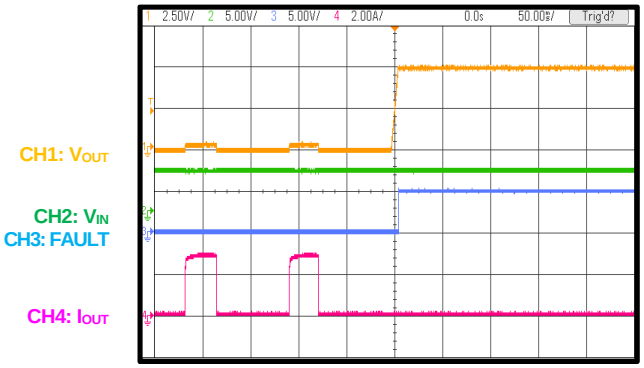
Load increases slowly



Short-Circuit Protection Entry



Short-Circuit Protection Recovery



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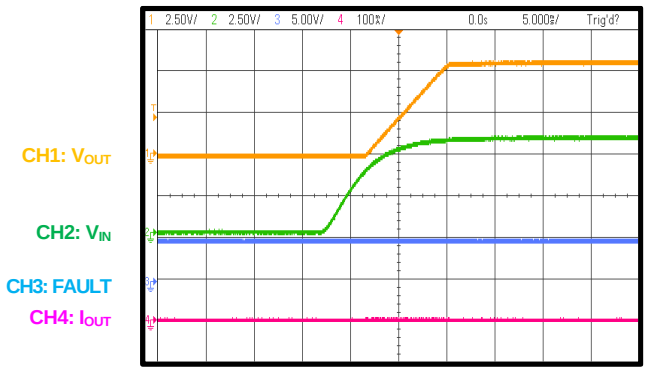
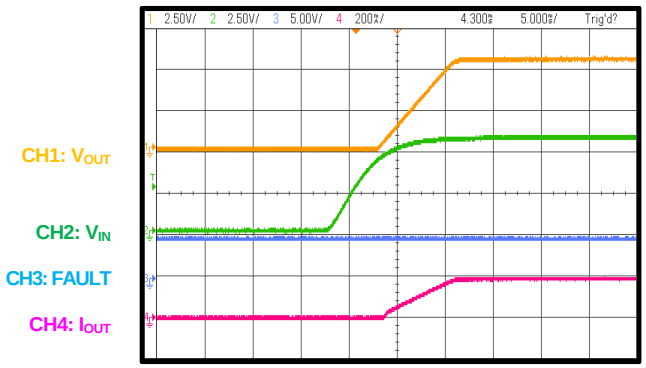
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board (see the Design Example section on page 14), V_{IN} = 5V, V_{EN} = 5V, R_{LIMIT} = 499Ω, SAS/OV floating, C_{OUT} = 10µF, T_A = 25°C, unless otherwise noted.

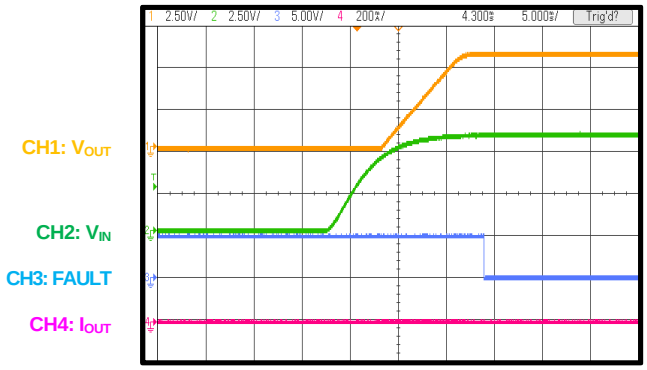
Start-Up
V_{IN} = 5.7V, no load



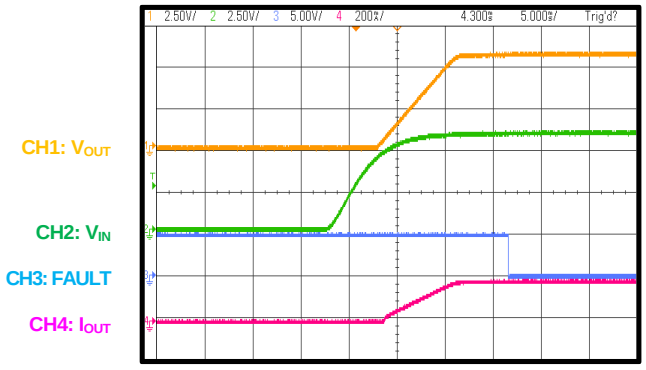
Start-Up
V_{IN} = 5.7V, load = 3.3Ω



Start-Up
V_{IN} = 5.8V, no load



Start-Up
V_{IN} = 5.8V, load = 3.3Ω



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FUNCTIONAL BLOCK DIAGRAM

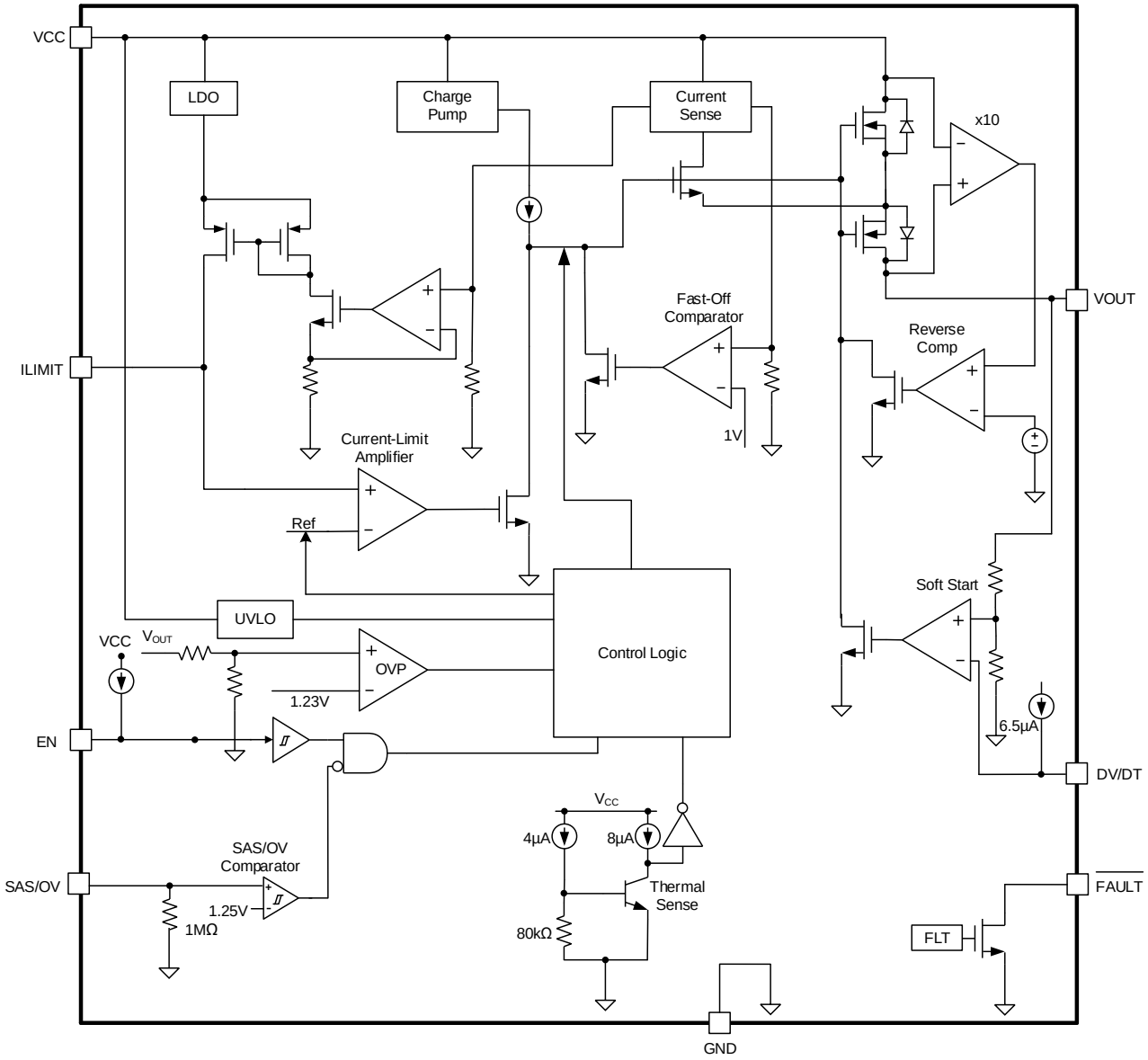

Figure 1: Functional Block Diagram

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OPERATION

The MP5017A is designed to limit the inrush current to the load when a circuit card is inserted into a live backplane power source. This limits the backplane voltage drop, as well as the dV/dt of the voltage to the load. It offers an integrated solution that monitors the input voltage (V_{IN}), output voltage (V_{OUT}), output current (I_{OUT}), and die temperature, eliminating the need for an external current-sense resistor, power MOSFET, and thermal sense device.

Under-Voltage Lockout (UVLO)

The nominal input supply voltage is 5V, but high energy transients can occur during normal operation or hot swap events. These transients depend on the parasitic inductance, the wire resistance, and the capacitor placed near VCC. If the power clamp (a TVS or Tranzorb diode) is not used, then the e-fuse must be able to withstand this transient voltage. The MP5017A uses a high-voltage MOSFET (up to 16V) and a high-voltage circuit on VCC to guarantee safe operation.

SAS/OV Control

The SAS/OV pin controls the part during start-up and shutdown. Float SAS/OV or pull it low to enable the part; pull it high to disable the part. SAS/OV also can be used as an input over-voltage protection (OVP) control. The V_{IN} OVP limit can be set by placing a divider between VCC and SAS/OV (see Figure 2). When the SAS/OV voltage exceeds 1.25V, the part shuts down. Once the voltage drops below 1.21V or if SAS/OV is floated, the part is enabled again.

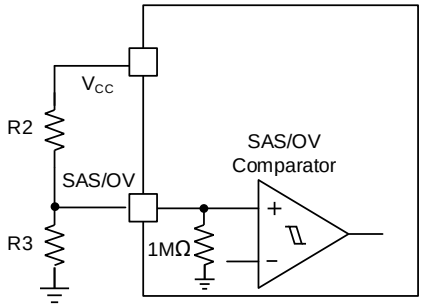

Figure 2: Adjustable Input OVP

Soft Start (SS)

The soft-start (SS) time is a function of the capacitor ($C_{DV/DT}$). The soft-start time (t_{SS}) can be calculated with Equation (1):

$$t_{SS}(ms) = \frac{1V \times C_{DV/DT}(nF)}{6.5\mu A} \quad (1)$$

For example, a 47nF capacitor generates a soft-start time of approximately 7.2ms.

Fast Output Over-Voltage Protection (OVP)

The MP5017A uses an output OVP function to protect the downstream load when there is a voltage surge at the input. A fast, accurate comparator monitors the over-voltage (OV) condition on the output. If V_{OUT} exceeds the threshold (typically 5.8V), then the internal MOSFET's gate is pulled down quickly and is regulated to a specific value to keep V_{OUT} clamped at 5.8V. The rapid loop response speed (typically 10µs) keeps the OV overshoot small.

Current Limit

The MP5017A provides a constant current limit, which can be configured by an external resistor. Once the current limit threshold is reached, the internal circuit regulates the gate voltage to hold the current in the power MOSFET. To limit the current, the gate-to-source voltage must be regulated from 5V to about 1V. The typical response time is about 10µs. During this period, I_{OUT} may have a small overshoot.

The desired current limit is a function of the external current-limit resistor.

Reverse Current Blocking

The MP5017A uses a pair of back-to-back N-channel MOSFETs for reverse current protection. Once the reverse current limit threshold (about -50mA) is reached and the 80µs deglitch time passes, the internal circuit pulls the gate voltage down to shut down the MOSFETs. If the reverse current reaches its threshold (about -1A), then the part shuts the MOSFETs down immediately to prevent V_{OUT} from being pulled down.

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$\overline{\text{FAULT}}$ does not change its state during the reverse current limit. The reverse current is blocked, and this state continues until V_{CC} > V_{OUT} - 2mV. When V_{CC} > V_{OUT} - 2mV, the part restarts. If V_{IN} drops below the UVLO threshold, then the back-to-back MOSFETs are turned off, eliminating any reverse current.

$\overline{\text{FAULT}}$

$\overline{\text{FAULT}}$ is an open-drain configuration pin. If an over-current (OC) condition is detected, then $\overline{\text{FAULT}}$ reports a fault (low level) after a 5ms deglitch timeout. There is a 10µs deglitch timeout if output OVP is triggered. This ensures that no false fault signals are accidentally reported. The internal deglitch circuit eliminates the need for external components. $\overline{\text{FAULT}}$ does not deglitch during an over-temperature (OT) condition (see Table 1).

Table 1: $\overline{\text{FAULT}}$ Function Truth Table

Description	$\overline{\text{FAULT}}$	E-Fuse State	Latch	Output Discharge
Under-voltage lockout (UVLO)	High	Off	No	No
EN low	High	Off	No	Yes
SAS/OV high	High	Off	No	Yes
V_{OUT} OVP clamp	Low (10µs deglitch time)	Hi-Z	No	No
Thermal shutdown	Low	Off	No	No
Current limit	Low (5ms deglitch time)	Hi-Z	No	No
Fast current limit	Low	Off	No	No
Reverse current protection	High	Off	No	No
SAS/OV floating	High	On	No	No
SAS/OV low	High	On	No	No

Short-Circuit Protection

If the load current increases too rapidly due to a short-circuit event, the current may exceed the current limit threshold before the control loop is able to respond. If the current reaches 7.5A, a secondary current-limit level from a fast turn-off circuit is activated. The power MOSFET then turns off with a 100mA pull-down gate discharge current. This helps limit the peak current through the MOSFET, keeping V_{IN} from dropping excessively. After the MOSFET is switched off, the part restarts. If the short remains once the part restarts, then the MP5017A regulates the gate voltage to hold the current at a normal current-limit level.

Output Discharge

The MP5017A uses a discharge function to provide a resistive discharge path for the external output capacitor. The function is active when the part is disabled (EN low or SAS high).

EN Control

EN enables the part when it is pulled high, and disables the part when it is pulled low. Floating EN automatically starts the part because an internal current source pulls EN up to the internal supply. The maximum internal pull-up voltage source is about 5V.

Thermal Shutdown (OTP Auto-Retry)

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds about 175°C, the entire chip shuts down and the $\overline{\text{FAULT}}$ pin reports the fault. Once the temperature drops below its lower threshold (typically 125°C), there is a 76ms delay and then the chip is enabled again and resumes normal operation.

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APPLICATION INFORMATION

Setting the Current Limit

The MP5017A current limit value should exceed the normal maximum load current to account for the variations in the current sense value. The current limit is a function of the external current-limit resistor. The current limit (I_{LIMIT}) can be estimated with Equation (2):

$$I_{LIMIT}(A) = \frac{1.16V \times 10^3}{R_{LIMIT}(\Omega)} \quad (2)$$

Table 2 and Figure 3 show examples of current limit values as a function of the resistor value.

Table 2: Current Limit vs. Current Limit Resistor

Current Limit Resistor (Ω)	1400	806	499	324	226
Current Limit (A)	0.9	1.51	2.4	3.61	5.04

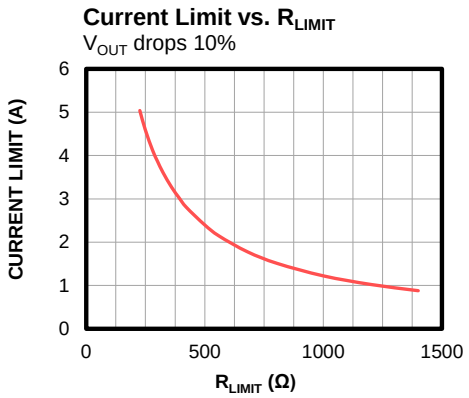


Figure 3: Current Limit vs. Current Limit Resistor

Design Example

Table 3 shows a design example following the application guidelines for the given specifications:

Table 3: Design Example

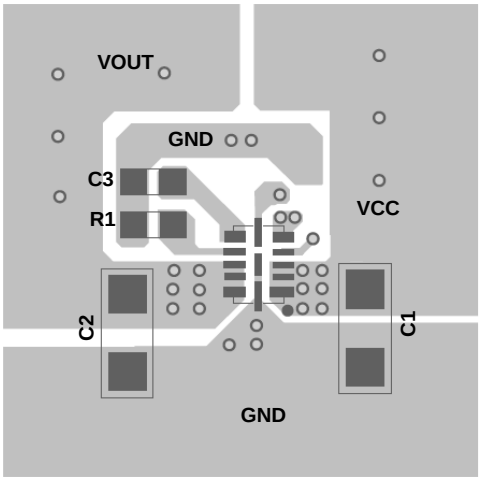
V_{IN}	5V
Current Limit	2.4A
Soft-Start Time	7.2ms

Figure 5 on page 15 shows the detailed application schematic. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section on page 7. For more detailed device applications, refer to the related evaluation board datasheets.

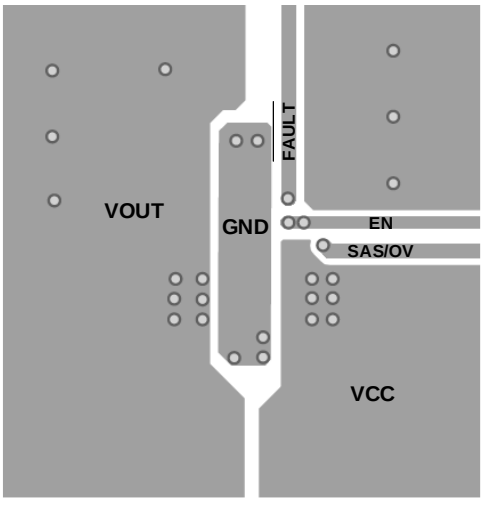
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 4 and follow the guidelines below:

1. Place the high-current paths (VCC and VOUT) close to the device using short, direct, and wide traces.
2. Place the input capacitor (C1) as close to VCC and GND as possible.
3. Connect the VCC and VOUT pads to large copper traces for better thermal performance.
4. Place R_{LIMIT} (R1) close to ILIMIT.
5. Place DV/DT capacitor (C3) close to DV/DT.



Top Layer



Bottom Layer

Figure 4: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS

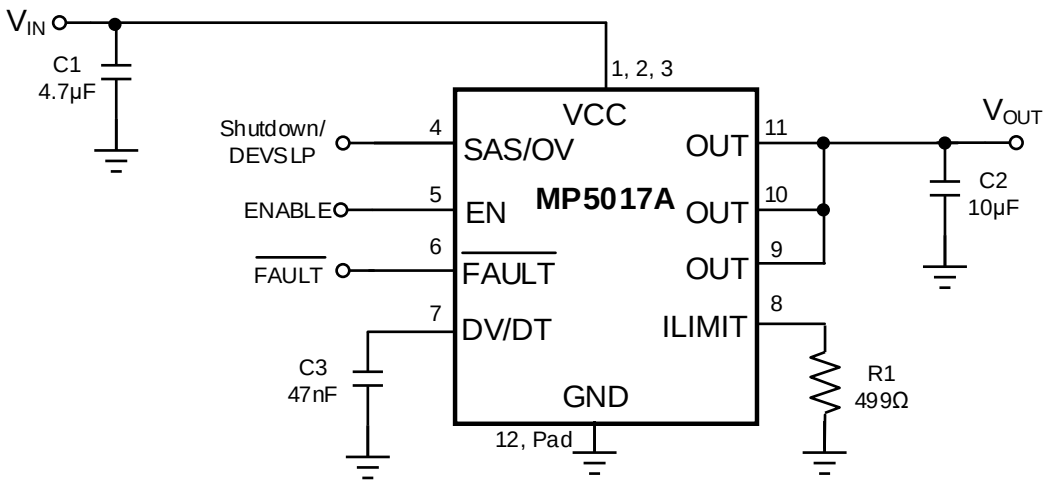

Figure 5: Typical Application Circuit (V_{IN} = 5V)

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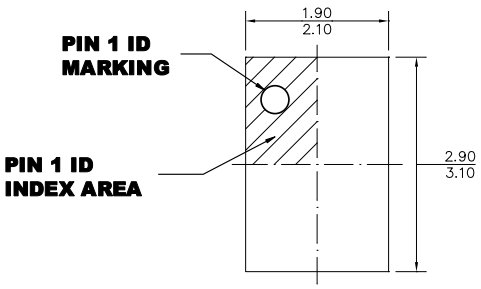
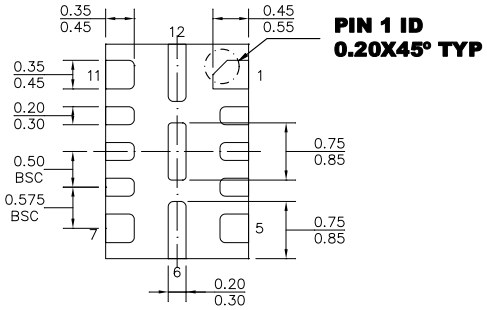
PACKAGE INFORMATION

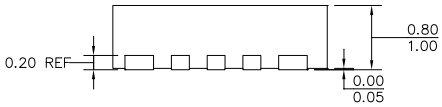
QFN-12 (2mmx3mm)



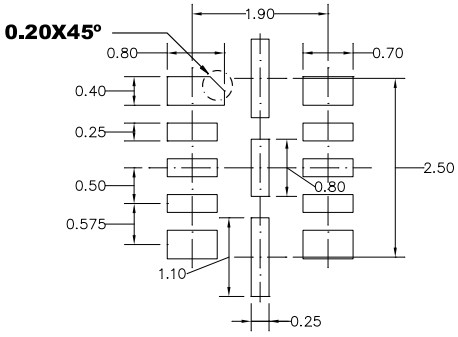
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.1 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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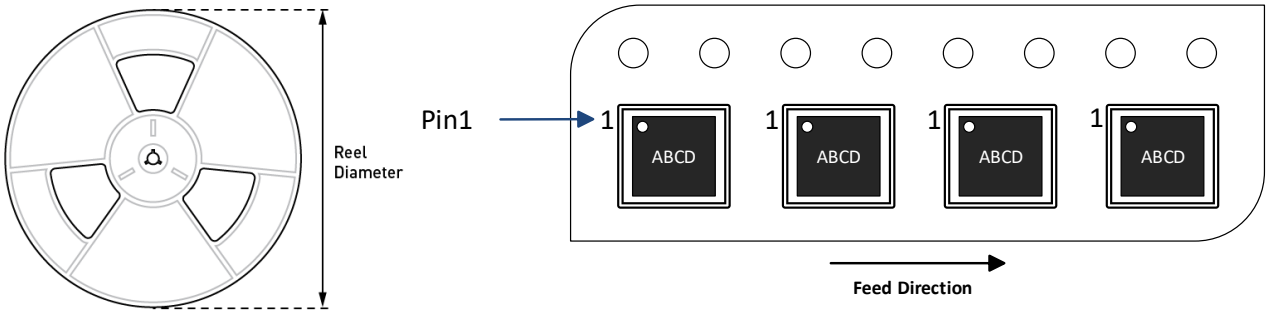
CARRIER INFORMATION



Part Number	Package Description	Quantity /Reel	Quantity /Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP5017AGD-Z	QFN-12 (2mmx3mm)	5000	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	10/19/2021	Initial Release	-

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