MP5016

2.7 - 15V, 0.7 - 5A, Current Limit Switch with Over-Voltage Clamp and Reverse Blocking

The Future of Analog IC Technology

DESCRIPTION

The MP5016 is a protection device designed to protect circuitry on the output from transients on the input. The MP5016 also protects the input from undesired shorts and transients coming from the output.

During start-up, the inrush current is limited by limiting the slew rate at the output. The slew rate is controlled by the DV/DT pin setting and MODE pin setting.

The maximum load at the output is current-limited. The magnitude of the current limit is controlled by an external resistor from ILIMIT to GND. There is a fixed 2.5A current limit when ILIMIT is floating.

The output voltage is limited by the output over-voltage protection (OVP) function. The clamp voltage can be set by the MODE connection.

The MP5016 offers a GATE drive signal connected to an external N-channel MOSFET gate to block current flowing from the output to the input when the IC is in enable off, power shutdown, or thermal shutdown.

The MP5016 is available in a QFN-10 (1.5mmx2mm) package.

FEATURES

- Wide 2.7V to 15V Operating Input Range
- 26V Absolute Maximum Transient Input Voltage
- Selectable Over-Voltage Clamp Threshold
- Fast Output Over-Voltage Protection (OVP) Response
- Integrated 43mΩ Power MOSFET
- Adjustable Current Limit or Fixed Current Limit when Floating ILIMIT
- Reverse-Blocking MOSFET Driver
- Soft-Start Time Programmable through DV/DT and MODE
- Fast Response for Hard Short Protection
- Over-Current Protection (OCP) Hiccup Protection
- Thermal Shutdown and Auto-Retry
- Available in a QFN-10 (1.5mmx2mm) Package

APPLICATIONS

- HDD, SSD
- Hot Swaps
- Wireless Modem Data Cards
- PC Cards
- USB Power Distribution
- USB Protection
- USB3.1 Power Delivery

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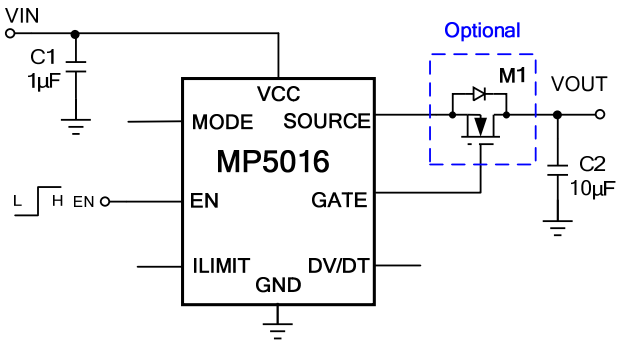
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP5016GQH	QFN-10 (1.5mmx2mm)	*See Below*

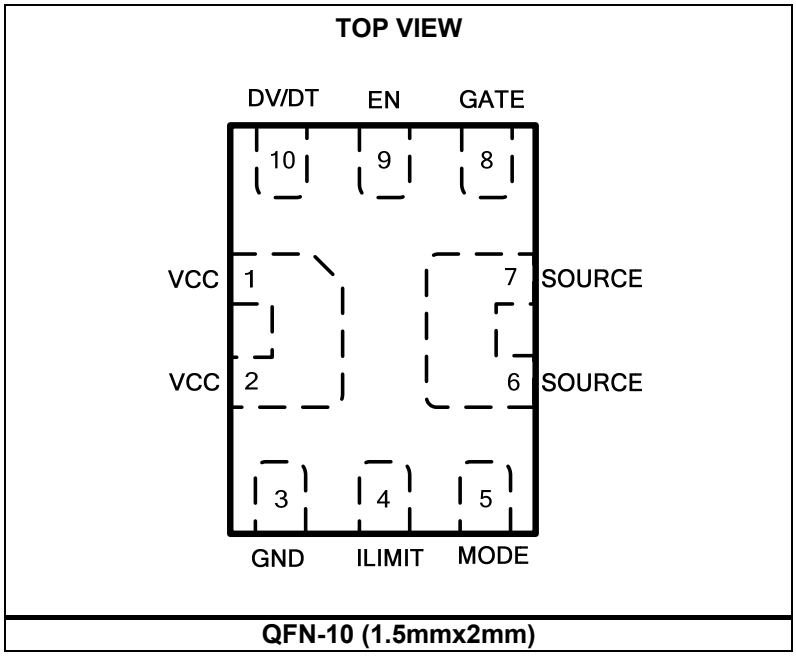
* For Tape & Reel, add suffix –Z (e.g.MP5016GQH-Z)

TOP MARKING

EK
LL

EK: Product code of MP5016GQH
LL: Lot number

PACKAGE REFERENCE



QFN-10 (1.5mmx2mm)

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ABSOLUTE MAXIMUM RATINGS (1)

VCC, SOURCE ..... -0.3V to 26V
MODE..... -0.3V to 26V
GATE..... SOURCE+ 5.5V
All other pins ..... -0.3V to +5.5V
Junction temperature ..... -40°C to +150°C
Lead temperature..... 260°C
Continuous power dissipation (T_A = +25°C) **(2) (4)**
QFN-10 (1.5mmx2mm)..... 2.23W

Recommended Operating Conditions (3)

Supply voltage (VCC) ..... 2.7V to 15V
Output voltage (SOURCE)..... 2.7V to 15V
Operating junction temp. (T_J)....-40°C to +125°C

Thermal Resistance	***θ_{JA}***	***θ_{JC}***	
QFN-10 (1.5mmx2mm)			
EV5016H-QH-00A **(4)**	56	18	°C/W
JESD51-7 **(5)**	130	25	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces the excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on EV5016-QH-00A, 2-layer PCB, 50mmx50mm.
5) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

VCC = 5V, R_{LIMIT} = NS, C_{OUT} = 10µF, T_J = -40°C + 125°C [6], typical value is tested at T_J = +25°C unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Supply current (quiescent)	I_Q	EN = high, MODE = VCC/GND/float		50		µA
		EN = high, MODE connect resistor to GND		90		µA
Supply current (shutdown)	I_S	EN = GND		9		µA
Power MOSFET						
On resistance	R_{DSon}	I_{OUT} = 1A		43		mΩ
Turn-on delay	T_{delay}	DV/DT float, MODE float		500		µs
Off-state leakage current	I_{OFF}	V_{IN} = 12V, EN = 0V		0.1	1	µA
Under-/Over-Voltage Protection (UVP, OVP)						
Under-voltage lockout rising threshold	V_{UVLO}		2.38	2.53	2.68	V
UVLO hysteresis	$V_{UVLOHYS}$			200		mV
Output over-voltage clamp voltage	V_{CLAMP}	V_{MODE} = GND, T_J = 25°C	5.5	5.75	6	V
		V_{MODE} = VCC, T_J = 25°C	14.2	15.2	16.2	V
		R_{MODE} = 76.8kΩ, VCC = 5V, T_J = 25°C	3.71	3.95	4.19	V
		R_{MODE} = 115kΩ, T_J = 25°C	5.3	5.7	6.1	V
		R_{MODE} = 324kΩ, T_J = 25°C	14.2	15.5	16.7	V
DV/DT						
DV/DT slew rate	dv/dt	DV/DT float, V_{MODE} = GND	0.4	0.8	1.2	V/ms
		DV/DT float, V_{MODE} = VCC	1.3	2	2.7	
		DV/DT float, MODE float	2.8	3.8	4.8	
DV/DT current	$I_{DV/DT}$	$V_{DV/DT}$ = 0.5V	4.5	6.5	8.5	µA
Current Limit						
Current limit at normal operation	I_{Limit_NO}	Float ILIMIT, T_J = 25°C	2.3	2.5	2.7	A
		R_{LIMIT} = 604Ω, T_J = 25°C	3.3	3.5	3.7	A
		R_{LIMIT} = 3kΩ, T_J = 25°C	0.6	0.75	0.9	A
Enable (EN)						
Enable rising threshold	V_{EN_RISING}		1.86	2	2.16	V
Enable hysteresis	V_{EN_HYS}			350		mV
Enable pull-down resistor	R_{EN_DOWN}			2.2		MΩ
GATE						
GATE maximum source current	$I_{G_SOURCE_MAX}$	I_{OUT} = 1A	7	12		µA
GATE maximum sink current	$I_{G_SINK_MAX}$	VCC = V_{SOURCE} = 5V, V_{GATE} = 10.5V		1.3		mA
Output Discharge						
Discharge resistance	R_{DIS}	VCC = 5V		540		Ω

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ELECTRICAL CHARACTERISTICS *(continued)*

VCC = 5V, R_{LIMIT} = NS, C_{OUT} = 10µF, T_J = -40°C + 125°C [6], typical value is tested at T_J = +25°C unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
OTP						
Thermal shutdown [7]	T_{SD}			175		°C
Thermal hysteresis [7]	T_{SD_HYS}			50		°C

NOTES:

6) Not tested in production, guaranteed by over-temperature correlation.
7) Guaranteed by engineering sample characterization.

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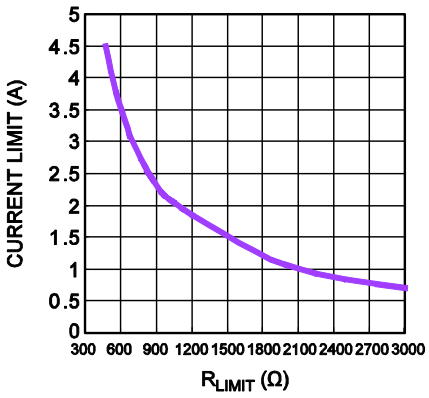
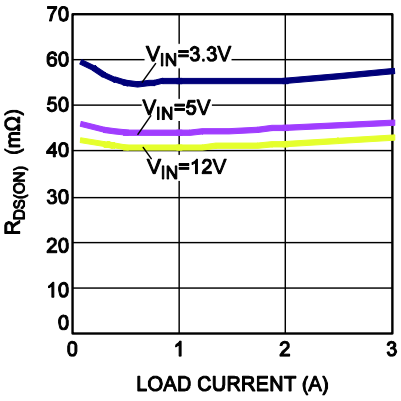
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = VCC = 5V, V_{EN} = 5V, R_{LIMIT} = 604Ω, C_{OUT} = 10µF, T_A = 25°C, unless otherwise noted.

Current Limit vs. R_{LIMIT}

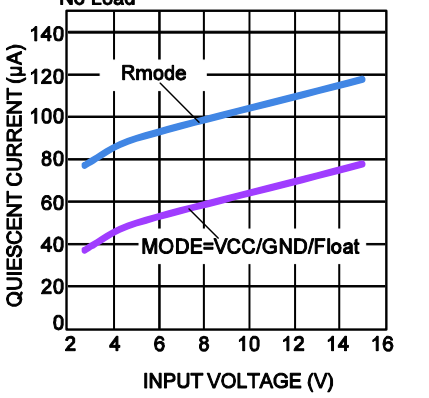


$R_{DS(ON)}$ vs. Load Current



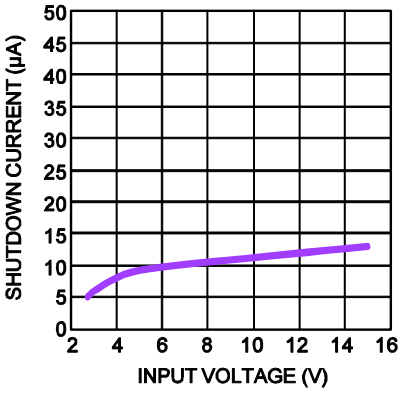
Quiescent Current vs. Input Voltage

EN=3V, Remove the EN Pull-Up Risistor, No Load



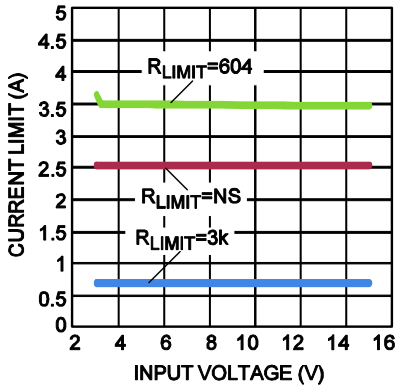
Shutdown Current vs. Input Voltage

V_{EN}=0V



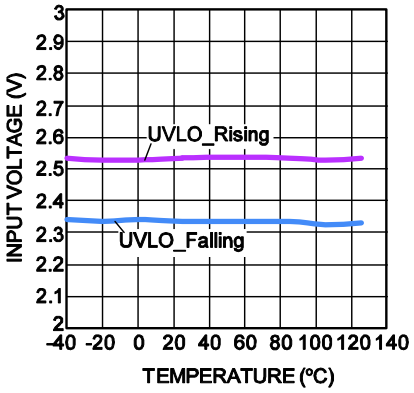
Current Limit vs. Input Voltage

V_{IN}=3V to 22V



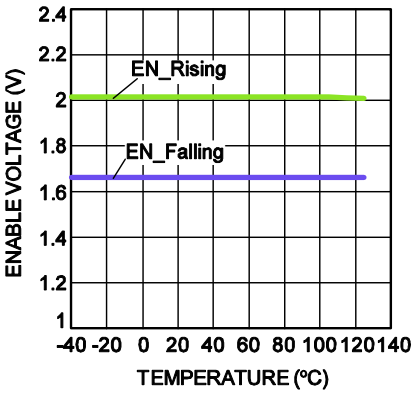
VIN UVLO Rising/Falling Threshold vs. Temperature

T_A=-40°C to +125°C



EN Rising/Falling Threshold vs. Temperature

T_A=-40°C to +125°C



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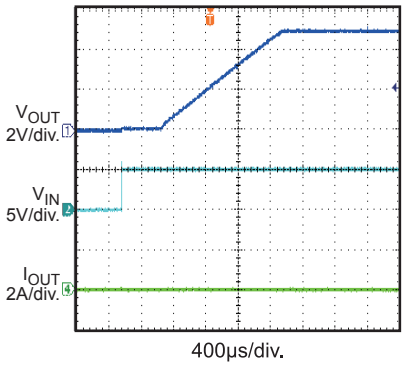
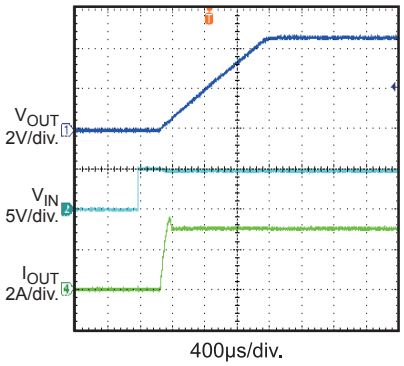
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = VCC = 5V, V_{EN} = 5V, R_{LIMIT} = 604Ω, MODE floating, DV/DT floating, C_{OUT} = 10µF, T_A = 25°C, unless otherwise noted.

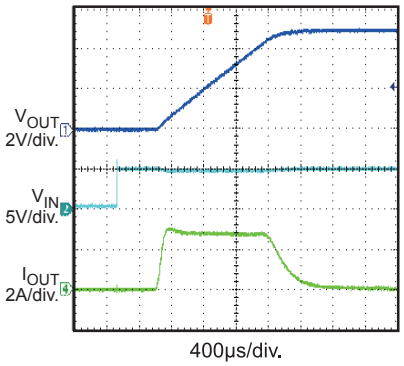
Start-Up through Input Voltage
No Load



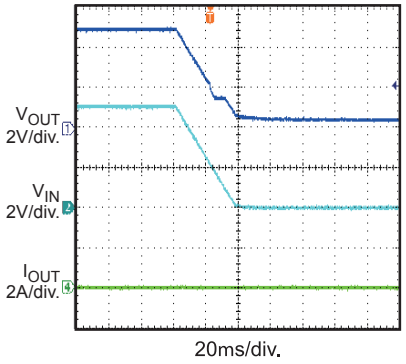
Start-Up through Input Voltage
CC Load =3A



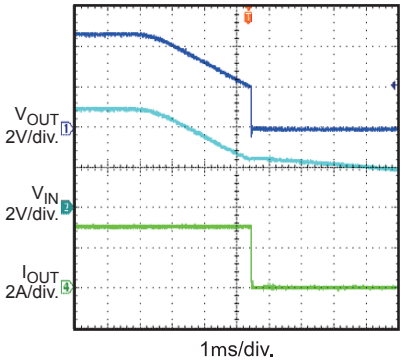
Start-Up through Input Voltage
No Load, C_{OUT} = 1000µF



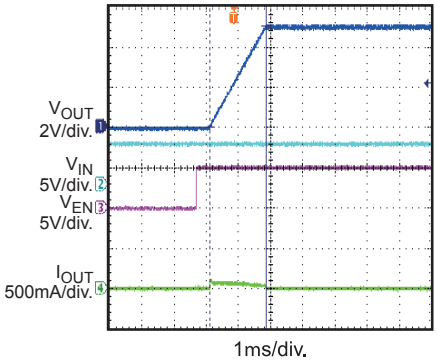
Shutdown through Input Voltage
No Load



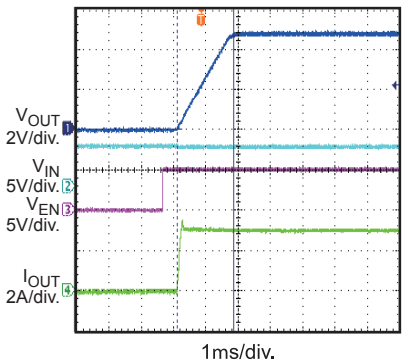
Shutdown through Input Voltage
CC Load =3A



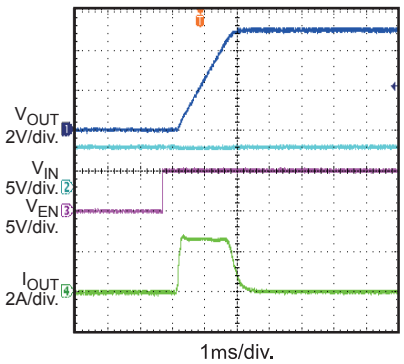
Start-Up through Enable
No Load



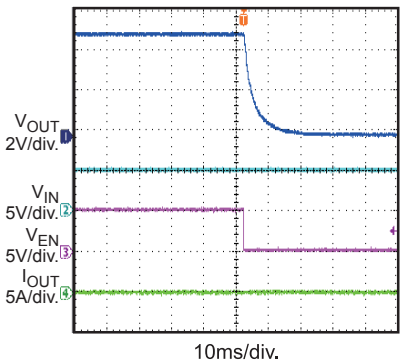
Start-Up through Enable
CC Load =3A



Start-Up through Enable
No Load, C_{OUT} =1000µF



Shutdown through Enable
No Load



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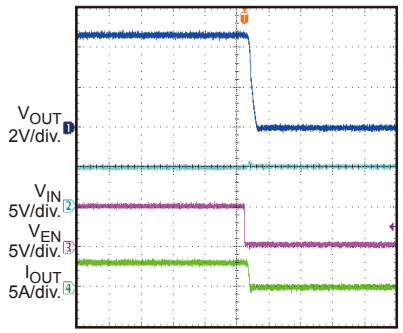
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = VCC = 5V, V_{EN} = 5V, R_{LIMIT} = 604Ω, MODE floating, DV/DT floating, C_{OUT} = 10µF, T_A = 25°C, unless otherwise noted.

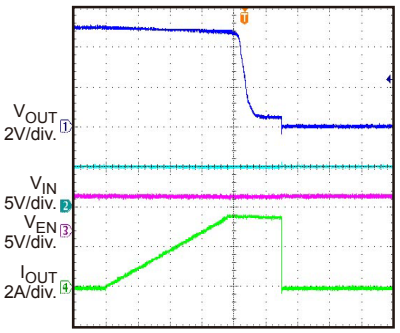
Shutdown through Enable

CC Load = 3A

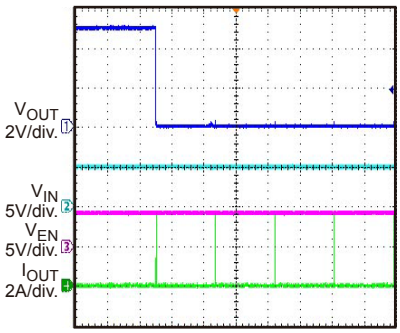


Current Limit

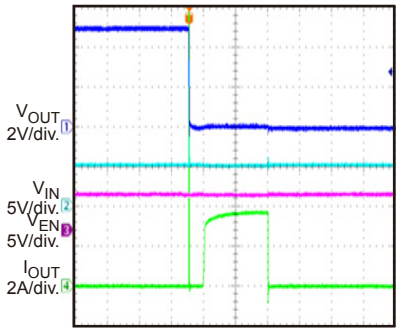
Increase I_{OUT} Slowly



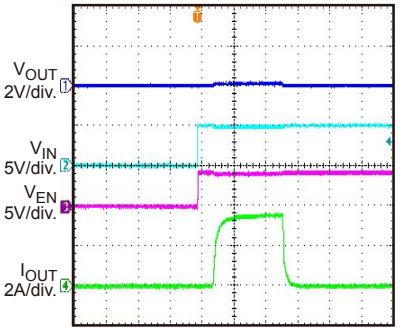
Short Circuit during Normal Operation and Hiccup



Short Circuit Entry during Normal Operation

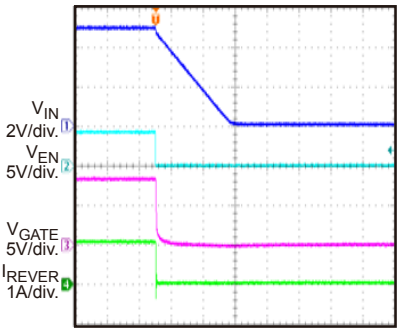


Short Circuit before Input Voltage Start-Up



Reverse Current Protection during EN Shutdown

V_{OUT} = 5V, Pull EN Low



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PIN FUNCTIONS

Pin #	Name	Description
1, 2	VCC	**Supply voltage.** The MP5016 operates from a 2.7V to 15V input rail. A ceramic capacitor is required to decouple the input rail. Connect VCC using a wide PCB trace.
3	GND	**System ground.**
4	ILIMIT	**Current limit set.** Place a resistor between ILIMIT and ground to set the value of the current limit. Float ILIMIT to achieve a 2.5A fixed current limit.
5	MODE	**Output over-voltage protection (OVP) clamp voltage select.** The output OVP clamp voltage is selected by the MODE connection. A resistor connected from MODE to ground sets the OVP threshold voltage. Three digital inputs are provided for MODE. Drive MODE high to VCC to set the output OVP clamp voltage at 15.2V. Drive MODE low to GND to set the output OVP clamp voltage at 5.75V. Float MODE for no OVP clamp protection.
6, 7	SOURCE	**Source of the internal power MOSFET and the output terminal of the IC.**
8	GATE	**Gate driver for the reverse-current block MOSFET.** A 100pF capacitor is required on GATE if the reverse-current block MOSFET is not being used.
9	EN	**Enable.** Force EN high to enable the MP5016. Float EN or pull EN to ground to disable the IC. For quick start-up, pull EN up to VCC through a 300kΩ resistor.
10	DV/DT	**DV/DT.** Connect a capacitor from DV/DT to ground to set the DV/DT slew rate.

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BLOCK DIAGRAM

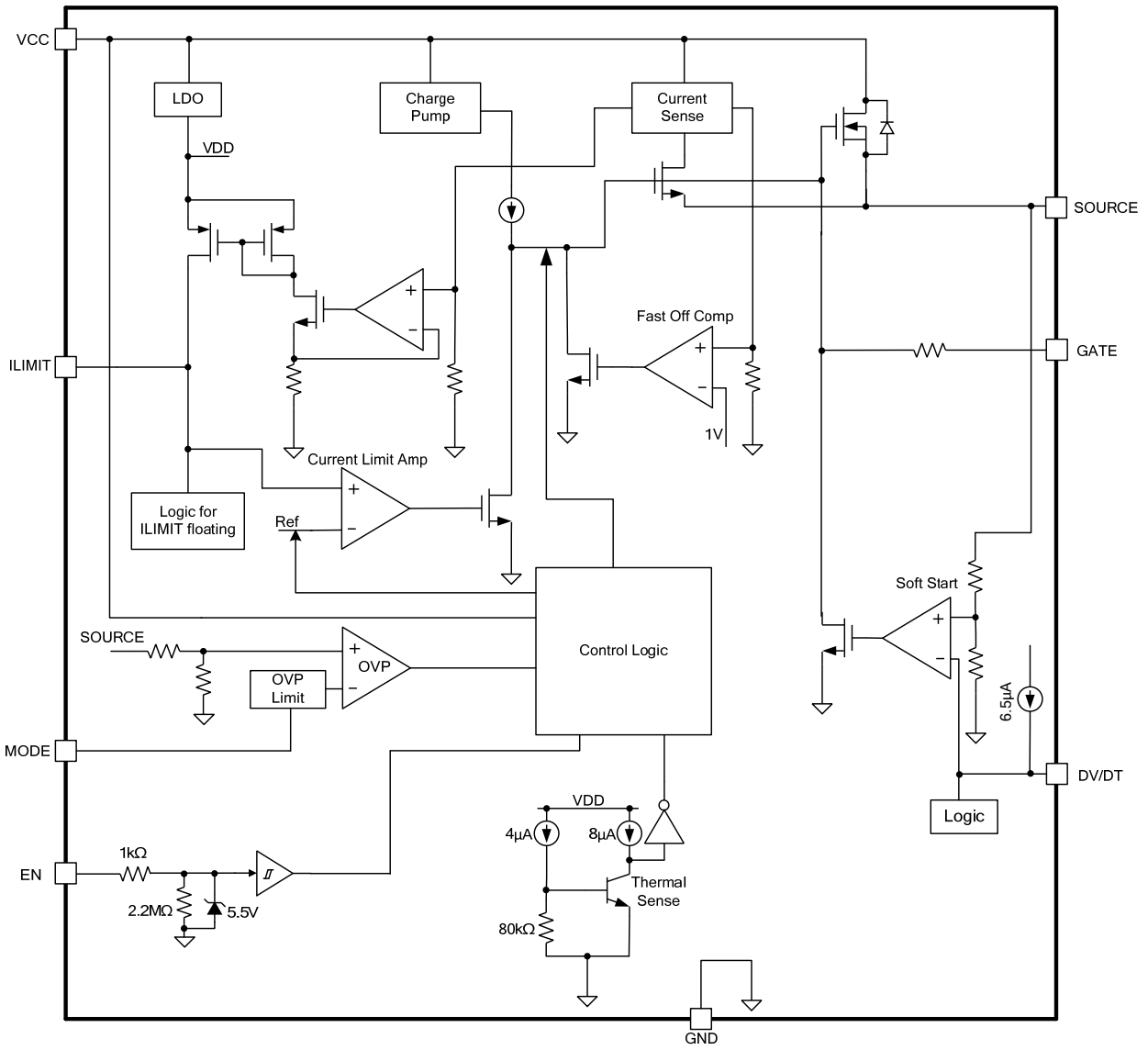

Figure 1: Functional Block Diagram

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OPERATION

The MP5016 is designed to limit the inrush current to the load when a circuit card is inserted into a live backplane power source, thereby limiting the backplane's voltage drop and the dV/dt of the voltage to the load. The MP5016 offers an integrated solution that monitors the input voltage, output voltage, output current, and die temperature, which eliminates the requirement of an external current sense power resistor, power MOSFET, and thermal sense device.

Under-Voltage Lockout (UVLO)

The MP5016 can be used in the 2.7V to 15V input supply system. There are high-energy transients during normal operation or hot swaps. These transients depend on the parasitic inductance and resistance of the wire and the capacitor at the VCC node. If a power clamp (TVS, Tranzorb) diode is not used, the E-fuse must be able to withstand this transient voltage. The MP5016 integrates a high-voltage MOSFET with up to 15V of continuous voltage and 26V of maximum transient input voltage. The MP5016 also uses a high-voltage circuit for the VCC node to guarantee safe operation.

MODE

MODE is used to select the output over-voltage protection (OVP) threshold.

Three digital inputs are provided for MODE. Drive MODE high to VCC to set the output OVP clamp voltage at 15.2V. Drive MODE low to GND to set the output OVP clamp voltage at 5.75V. Float MODE for no OVP clamp protection. The OVP threshold can be set by connecting a resistor from MODE to ground. For more details, refer to the Application Information section on page 14.

Soft Start (SS)

The soft-start time is related to the dV/dt slew rate and input voltage and can be calculated with Equation (1):

$$t_ss(ms) = \frac{Vin(V)}{dv/dt\ (V/ms)} \quad (1)$$

The dV/dt slew rate is controlled by an external DV/DT capacitor setting and the MODE setting.

Fast Output and Input OVP

To protect the downstream load when there is a surge voltage at the input, the MP5016 provides an output OVP function. An accurate and fast comparator monitors the over-voltage condition of the output. If the output voltage rises above the threshold set by MODE, the gate of the internal MOSFETs is pulled down quickly and is regulated to a certain value to keep the output voltage clamped at the OVP threshold. The fast loop response speed keeps the over-voltage overshoot small.

Current Limit

The MP5016 provides a constant current limit, and the current limit can be programmed by an external resistor.

The desired current limit is a function of the external current limit resistor and can be approximated with Equation (2):

$$I_{LIMIT}(A) = \frac{0.55(V)}{R_{LIMIT}(\Omega)} \times 3870 \quad (2)$$

Where 3870 is the current sense ratio.

Once the current limit threshold is reached, the internal circuit regulates the gate voltage to hold the current in the power MOSFET constant. To limit the current, the gate to the source voltage must be regulated from 5V to around 1V. The typical response time is about 15μs. During this period, the output current may have a small overshoot.

If the current limit condition lasts longer than 2ms, the IC enters hiccup mode with 2ms of on time and 700ms of off time.

The MP5016 allows ILIMIT to be floated during operation. If ILIMIT is floating, the current limit is set at a fixed 2.5A internally.

When shorting ILIMIT to GND, the normal current limit is disabled, but the secondary current limit still works. The secondary current limit is set to 8A internally. When the secondary current limit is triggered, the IC shuts down the power MOSFET.

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Short-Circuit Protection (SCP)

If the load current increases rapidly due to a short-circuit event, the current may exceed the current-limit threshold before the control loop can respond. If the current reaches the 8A secondary current limit level, a fast turn-off circuit activates to turn off the power MOSFET. This can help limit the peak current through the switch, keeping the input voltage from dropping too much. The total short-circuit response time is about 1µs. After the MOSFET has switched off, the part restarts. During the restart process, if the short still exists, the MP5016 regulates the gate voltage to hold the current at a normal current limit level. The IC enters hiccup mode with 2ms of on time and 700ms of off time.

To prevent safe operating area (SOA) damage during a high input voltage short-circuit protection (SCP) condition, the IC current limit folds back when the power MOSFET V_{DS} voltage is above the typical 11V and the junction temperature is over 110°C.

Reverse Blocking MOSFET Driver

The MP5016 has a GATE pin to provide an external N-channel MOSFET gate drive signal for reverse-current protection (RCP). Three events can pull down the GATE voltage: V_{IN} below the under-voltage lockout (UVLO), the enable (EN) voltage below the low-level threshold, or thermal shutdown. If any of these conditions occur, GATE sinks the current from the gate of the external MOSFET to initiate a fast turn-off.

For 3.3V low input voltage applications, choose an external reverse blocking MOSFET with a small gate threshold voltage (V_{GSth} < 1.6V) to reduce the voltage drop caused by the reverse-blocking MOSFET.

Setting an appropriate OVP threshold also can protect the reverse voltage (from the output to the input) when using an external N-channel MOSFET. When V_{OUT} rises too high during normal operation, the MP5016 SOURCE voltage is higher than the OVP threshold. In this case, the GATE voltage is regulated to maintain the SOURCE clamped at the OVP threshold. This action protects the reverse current from the high V_{OUT} to the low V_{IN}.

A 100pF capacitor is required on GATE if it is not connected to the external MOSFET.

Output Discharge

The MP5016 involves a discharge function that provides a resistive discharge path for the external output capacitor. The function is active when the part is disabled (V_{IN} UVLO, EN shutdown) and is done in a very limited amount of time. When using the external reverse-current block MOSFET, the output discharge path is blocked by the reverse current block MOSFET. Therefore, the output cannot be discharged when the reverse-current block MOSFET is used.

Enable (EN)

The MP5016 is enabled when EN is high. The MP5016 is disabled when EN is low. Floating EN shuts down the MP5016 because there is an internal 2.2MΩ resistor pulling EN down to ground. For automatic start-up, connect a pull-up resistor from VCC to EN.

EN is clamped internally using a 5.5V Zener diode (see Figure 2). Connecting the EN input through a pull-up resistor to VCC limits the EN input current below 100µA to prevent damage to the Zener diode. For example, when connecting a 300kΩ pull-up resistor to 15V VCC, I_{Zener} = (15V - 5.5V) / 300kΩ - 5.5V / 2.2MΩ = 29µA.

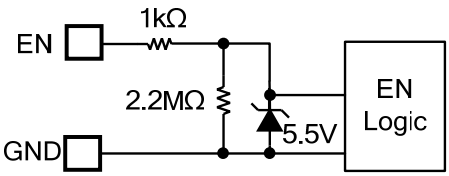

Figure 2: Zener Diode between EN and GND

When using a pull-up resistor to set the power-on threshold, avoid using a pull-up resistor that is too small to increase the operational quiescent current.

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Thermal Shutdown – Auto-Retry

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 175°C, the entire chip shuts down, and EN reports a fail mode. When the temperature drops below its lower threshold (typically 125°C), the chip is enabled again after a 700ms delay, typically.

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APPLICATION INFORMATION

Setting the Current Limit

The MP5016 current limit value should exceed the normal maximum load current, allowing for tolerances in the current sense value. The current limit is a function of the external current limit resistor. Table 1 and Figure 3 list examples of typical current limit values as a function of the resistor value.

Table 1: Typical Current Limit vs. Current Limit Resistor (8)

R_{LIMIT} (Ω)	3000	1050	604	470	422
I_{LIMIT} (A)	0.75	2	3.5	4.5	5

NOTE:

8) The current limit in Table 1 is a typical value for the reference design.

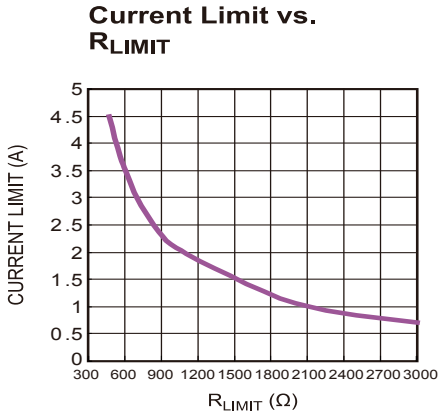

Figure 3: Current Limit vs. Current Limit Resistor

The MP5016 current limit can be programmed from 0.7A to 5A by connecting the correct resistor (R_{LIMIT}). The current limit cannot be set too low, because the MP5016 works in sleep mode when the load is lower than 0.38A, typically. The current limit logic is disabled in sleep mode, also.

Setting the Over-Voltage Clamp Threshold

Drive MODE high to VCC to set the output OVP clamp voltage at 15.2V. Drive MODE low to GND to set the output OVP clamp voltage at 5.75V.

Refer to Table 2 to set the MODE high/low digital voltage.

Table 2: MODE High/Low Digital Voltage

	Min.	Max.
V_{MODE}_HIGH	VCC - 0.2V	
V_{MODE}_LOW		0.2V

The OVP threshold can also be set by connecting a resistor from MODE to ground. In this case, the OVP clamp threshold is given by Equation (3):

$$V_{clamp}(V) = 0.047 \times R_{MODE}(K\Omega) + 0.3(V) \quad (3)$$

R_{MODE} should be above 68kΩ. For example, an R_{MODE} value of 76.8kΩ can set the OVP clamp threshold to 3.9V.

When R_{MODE} is used, place a 39pF capacitor from MODE to GND.

Setting the Soft-Start Time

The soft-start time is related to the dV/dt slew rate and input voltage and can be calculated with Equation (4):

$$t_ss(ms) = \frac{Vin(V)}{dv/dt\ (V/ms)} \quad (4)$$

The dV/dt slew rate is controlled by external DV/DT capacitor setting and MODE setting.

Table 3 shows the dV/dt slew rate when DV/DT is floating.

Table 3: dV/dt Slew Rate Value when DV/DT is Floating

MODE Connection	dV/dt Slew Rate (V/ms)
Low	0.8
High	2
Float	3.8
R_{MODE}	$\frac{V_{clamp}(V)}{7ms}$

For cases with an external DV/DT capacitor, the dV/dt slew rate can be calculated with Equation (5):

$$dv/dt\ (V/ms) = \frac{6.5(\mu A) \times K1}{C_{DV/DT}(nF)} \quad (5)$$

See Table 4 for the K1 factor value.

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Table 4: K1 Factor Value at External DV/DT Capacitor

MODE Connection	K1
Low	5.75
High	15.2
Float	27
R_{MODE}	$\frac{V_{clamp}}{7\mu * R_{MODE}}$

For example, when the external DV/DT cap is 47nF and R_{MODE} = 76.8kΩ, the dV/dt slew rate is 1V/ms.

Large Output Capacitor

With large output capacitor, if the charge current during soft start triggers the current limit, the MP5016 enters hiccup when the current limit is triggered for 2ms. To avoid start-up failure with a large output capacitor, a proper dV/dt slew rate must be set during the soft start to avoid triggering the current limit.

PCB Layout Guide

Efficient PCB layout is critical for stable operation. For best results, refer to Figure 4 and follow the guidelines below.

1. Place the high-current paths (VCC, VOUT) close to the device using short, direct, and wide traces.
2. Place the input capacitors close to the VCC and GND.
3. Connect the VCC and VOUT pads to large VCC and VOUT planes respectively to achieve better thermal performance.
4. Place a current-limit resistor close to ILIMIT.
5. Place a DV/DT capacitor close to DV/DT.

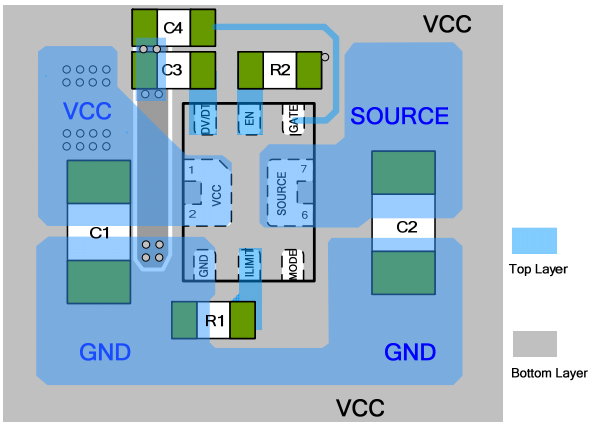

Figure 4: Recommended Layout

Design Example

Table 5 is a design example following the application guidelines for the given specifications.

Table 5: Design Example

V_{IN} (V)	2.7 to 15
Current Limit (A)	3.5
DV/DT Slew Rate (V/ms)	3.8

The detailed application circuits are shown in Figure 5 and Figure 6. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section. For more detailed device applications, please refer to the related evaluation board datasheet.

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TYPICAL APPLICATION CIRCUITS

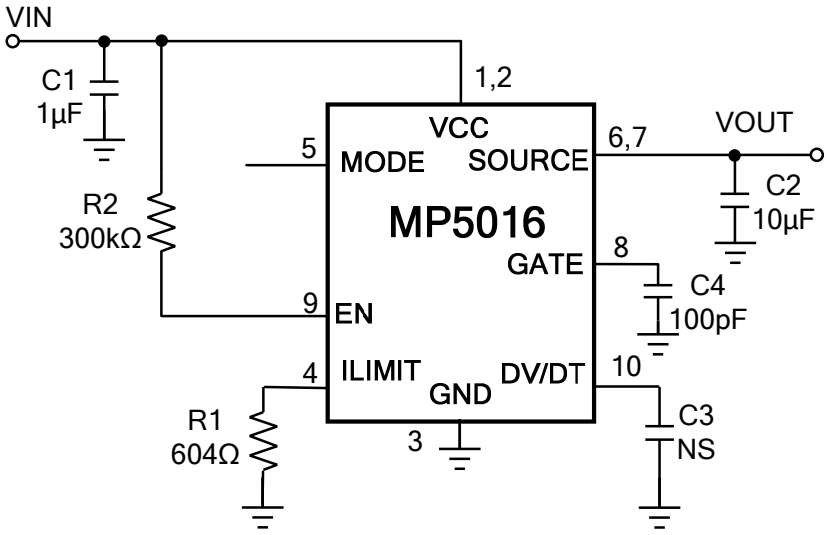

Figure 5: Typical Application Circuit without Reverse-Current Blocking MOSFET

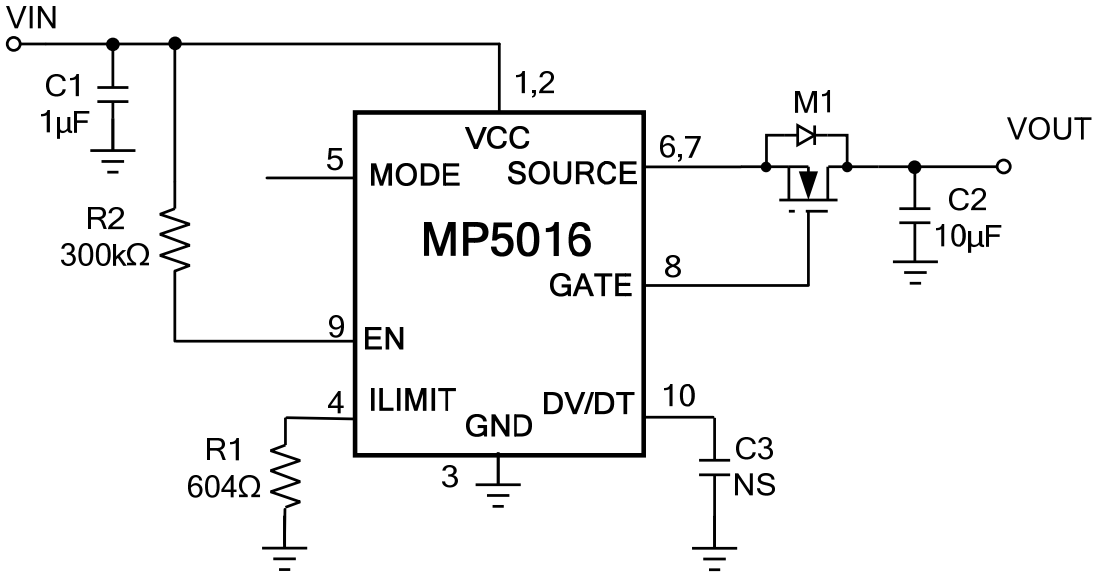

Figure 6: Typical Application Circuit with Reverse-Current Blocking MOSFET (9)

NOTE:

9) For 3.3V low input voltage applications, it is recommended to choose an external reverse-blocking MOSFET with a small gate threshold voltage (V_{GSth} < 1.6V) to reduce the voltage drop caused by the reverse-blocking MOSFET.

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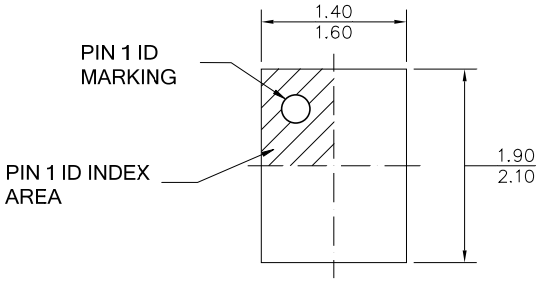
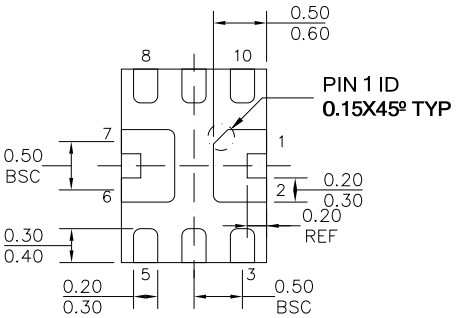
PACKAGE INFORMATION

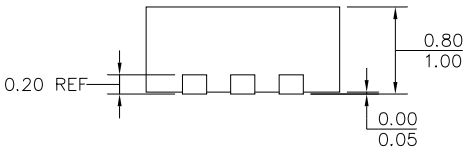
QFN-10 (1.5mmx2mm)



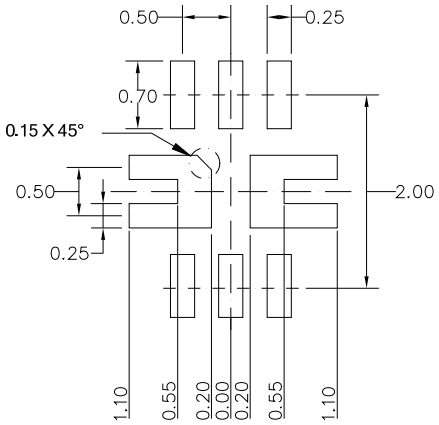
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIM MAX.
3) JEDEC REFERENCE IS MO-220.
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