MP5013E

5V, 2A, Programmable Current-Limit Switch with Over-Voltage Clamp and Slew Rate Control in a TSOT23-8

The Future of Analog IC Technology

DESCRIPTION

The MP5013E is a protection device designed to protect circuitry on the output (source) from transients on the input (VCC). It also protects the input from unwanted shorts and transients coming from the source.

A small capacitor on DV/DT controls the slew rate that limits the inrush current at the source. An internal circuit in DV/DT allows it to be floated (no connection) and still receive 1.2ms of ramp time at the source. The maximum load at the source is current-limited using sense FET topology. An external resistor between I-Limit and SOURCE controls the magnitude of the current limit.

An internal charge pump drives the gate of the power device, allowing the DMOS power FET to have a very low on resistance of only 36mΩ.

The MP5013E protects the source from the input being too low or too high. Under-voltage lockout (UVLO) ensures that the input remains above the minimum operating threshold before the power device turns on. If the input rises above the high output threshold, the MP5013E limits the source voltage.

FEATURES

- 3V to 5.5V Operating Input Range
- 2A DC, 5A Peak Current
- 5.7V Typical Output Over-Voltage Clamp
- 22V Absolute Maximum Voltage
- Input Under-Voltage Lockout (UVLO)
- Low Inrush Current during Start-Up
- Integrated 36mΩ Power FET
- ENABLE/FAULT Pin
- Adjustable Output Voltage Slew Rate
- Adjustable Current Limit
- Thermal Shutdown Protection
- Available in a TSOT23-8 Package

APPLICATIONS

- Storage (HDDs, SSDs)
- Hot-Swap Systems
- Set-Top Boxes
- USB Ports/Hubs
- Gaming

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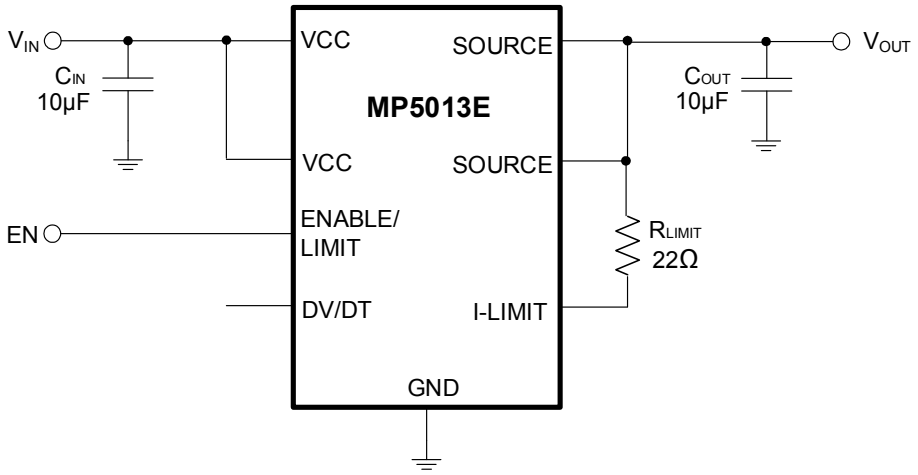
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP5013EGJ	TSOT23-8	*See Below*

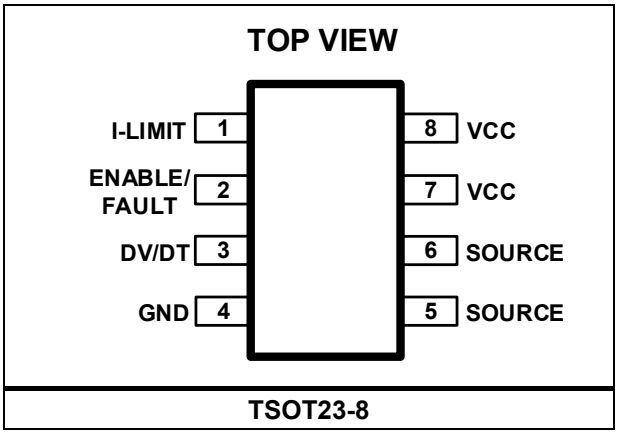
* For Tape & Reel, add suffix -Z (e.g. MP5013EGJ-Z)

TOP MARKING

|AWBY

AWB: Product code of MP5013EGJ
Y: Year code

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

VCC, SOURCE, I-LIMIT ..... -0.3V to 22V
DV/DT, ENABLE/FAULT ..... -0.3V to 6V
Storage temperature .....-65°C to +155°C
Junction temperature ..... +150°C
Lead temperature..... +260°C
Continuous power dissipation (T_A = +25°C) (2)
.....1.25W

Recommended Operating Conditions (3)

Input voltage operating range..... 3V to 5.5V
Current capability .....2A/5A peak
(100% duty cycle, and <1s response time)
Operating junction temp (T_J).....-40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TSOT23-8 ..... 100 ..... 55 ... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. the maximum allowable power dissipation at any ambient temperature is calculated using: $P_D(MAX)=(T_J(MAX)-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
Reduce 0.1W for every 10°C ambient temperature increase.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7 4-layer board.

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ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, R_{LIMIT} = 22Ω, capacitive load = 10µF, T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Power FET						
Delay time	t_{DLY}	Enable chip to I_D = 40mA with a 5Ω resistive load, float DV/DT		0.2		ms
On resistance	$R_{DS(ON)}$	T_J = 85°C (5)			65	mΩ
Off state output voltage	V_{OFF}	V_{CC} = 18V, V_{EN} = 0V, R_L = 500Ω			120	mV
Thermal Latch						
Shutdown temperature(5)	T_{SD}			175		°C
Under-Voltage (UV) and Over-Voltage Protection (OVP)						
Output clamp voltage	V_{CLAMP}	Over-voltage protection, V_{CC} = 8V	5.5	5.7	5.9	V
Under-voltage lockout	V_{UVLO}	Rising edge	2.5	2.7	2.9	V
Under-voltage lockout hysteresis	V_{HYST}			0.13		V
Current Limit (5)						
Hold current	I_{LIM-SS}	0Ω short resistance, R_{LIM} = 22Ω	2.7	3.5	4.3	A
Trip current	I_{LIM-OL}	R_{LIM} = 22Ω		6.5		A
DV/DT Circuit						
Rise time	τ_r	Float DV/DT, output rises from 10% to 90%	0.84	1.2	2.75	ms
ENABLE/FAULT						
Low-level input voltage	V_{IL}	Output disabled			0.5	V
Intermediate-level input voltage	$V_{I (INT)}$	Thermal fault, output disabled	0.82	1.3	1.95	V
High-level input voltage	V_{IH}	Output enabled	2.5			V
High-state maximum voltage	$V_{I (MAX)}$			4.95		V
Pull-up current (source)	I_{IL}	V_{ENABLE} = 0V	15	25	35	µA
Maximum fan-out for ENABLE/FAULT signal		Maximum number of chips for simultaneous shutdown			3	units
Maximum voltage on enable (EN) (6)	V_{MAX}				VCC	V
Total Device						
Bias current	I_{BIAS}	Device operational		890	950	µA
		Enable shutdown		580	650	
		Thermal shutdown		600	700	
Minimum operating voltage for under-voltage lockout	V_{MIN}	Enable < 0.5V			2.5	V

Notes:

5) Guaranteed by characterization test.
6) Maximum input voltage on ENABLE/FAULT is ≤6V if V_{CC} ≥ 6V. Maximum input voltage on ENABLE/FAULT is V_{CC} if V_{CC} ≤ 6V.

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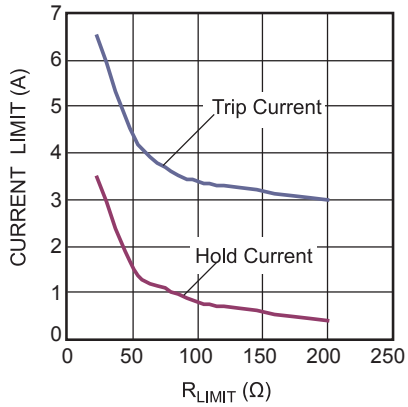
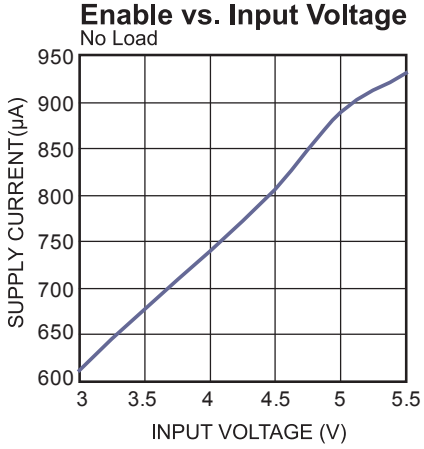
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{EN} = 5V, R_{LIMIT} = 22Ω, C_{OUT} = 10μF, $C_{DV/DT}$ = float, T_A = 25°C, unless otherwise noted.

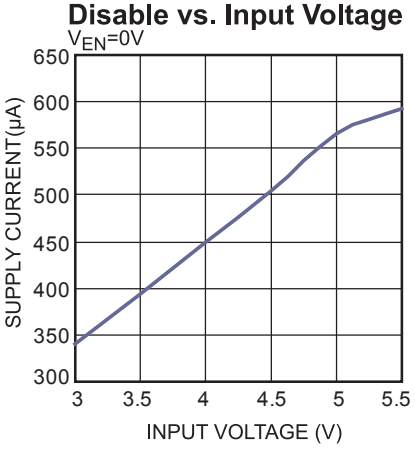
Trip Current & Hold Current vs. R_{LIMIT}



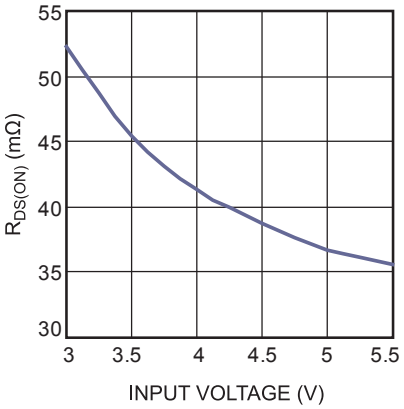
Supply Current, Output Enable vs. Input Voltage



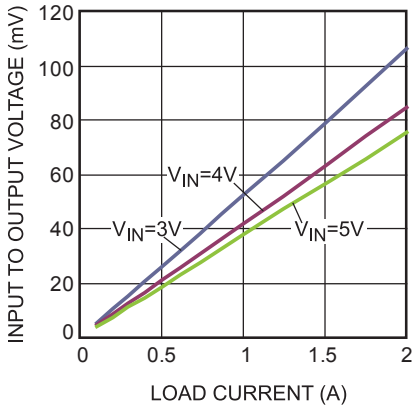
Supply Current, Output Disable vs. Input Voltage



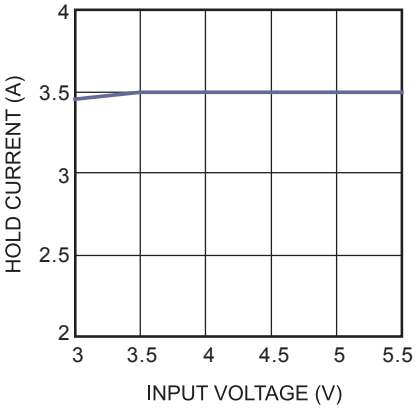
$R_{DS(ON)}$ vs. Input Voltage



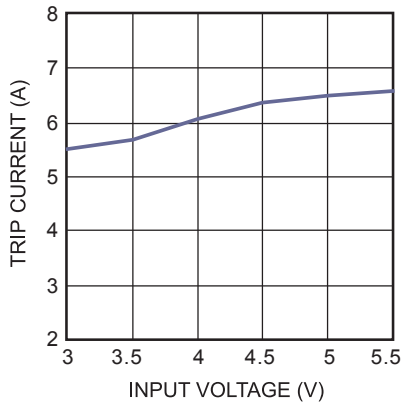
Input to Output Voltage vs. Load Current



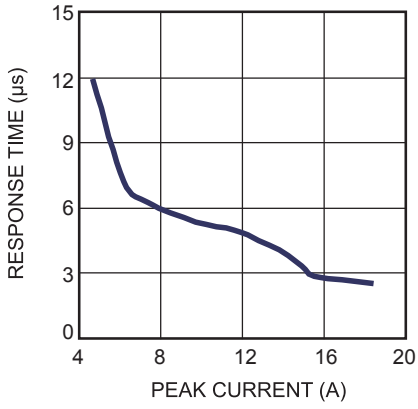
Hold Current vs. Input Voltage



Trip Current vs. Input Voltage



Current Limit Response vs. Peak Current



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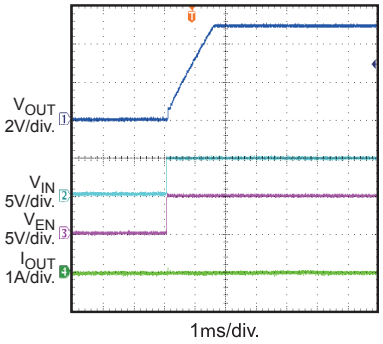
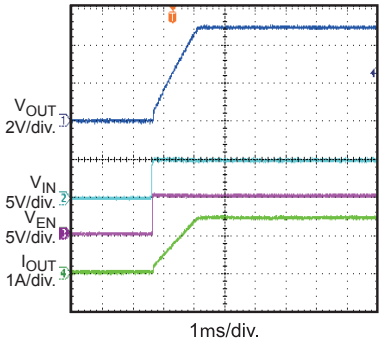
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{EN} = 5V, R_{LIMIT} = 22Ω, C_{OUT} = 10µF, $C_{DV/DT}$ = float, T_A = 25°C, unless otherwise noted.

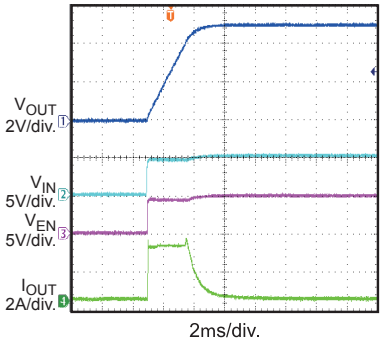
Start-Up through Input Voltage
No Load



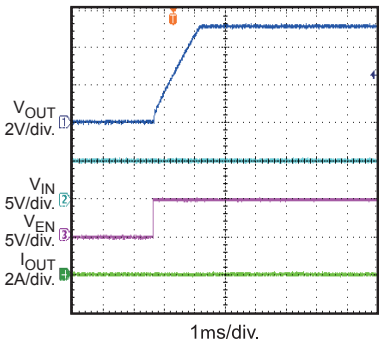
Start-Up through Input Voltage
R_{LOAD} = 3.3Ω



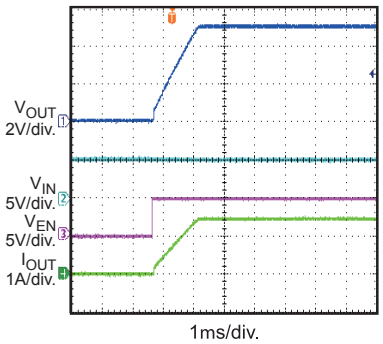
Start-Up through Input Voltage
C_{OUT} = 2200µF



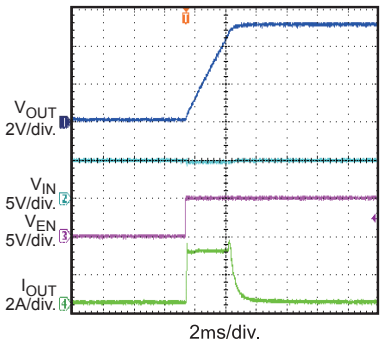
Start-Up through Enable/Fault
No Load



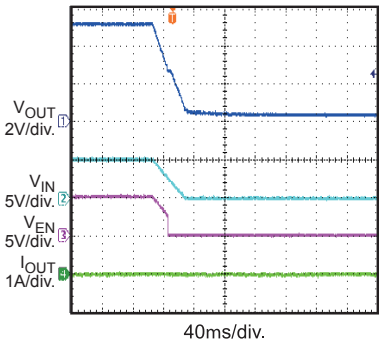
Start-Up through Enable/Fault
R_{LOAD} = 3.3Ω



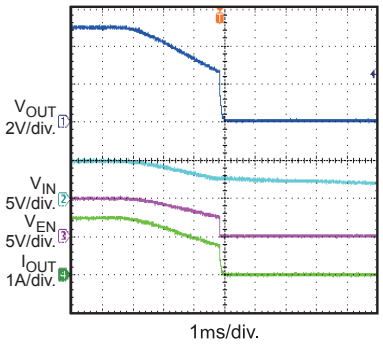
Start-Up through Enable/Fault
C_{OUT} = 2200µF



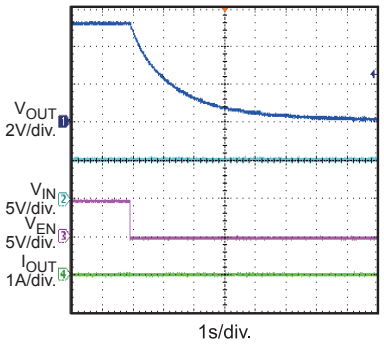
Shutdown through Input Voltage
No Load



Shutdown through Input Voltage
R_{LOAD} = 3.3Ω



Shutdown through Enable/Fault
No Load



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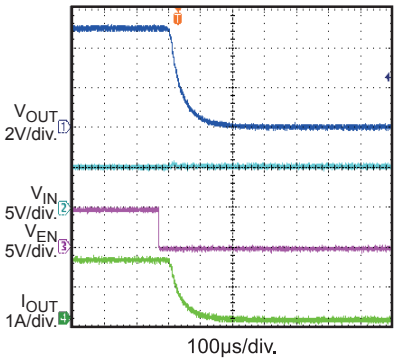
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

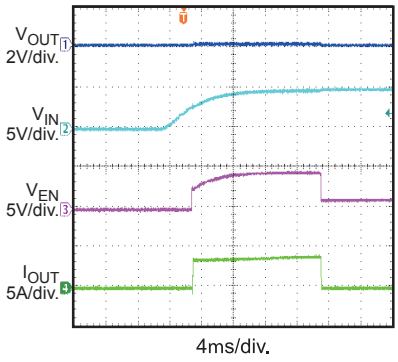
V_{IN} = 5V, V_{EN} = 5V, R_{LIMIT} = 22Ω, C_{OUT} = 10µF, $C_{DV/DT}$ = float, T_A = 25°C, unless otherwise noted.

Shutdown through Enable/Fault

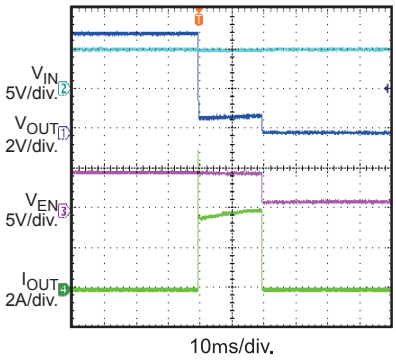
R_{LOAD} = 3.3Ω



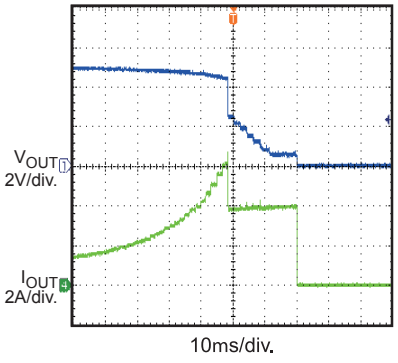
Short Circuit before Input Voltage Start-Up and Thermal Shutdown



Short Circuit during Normal Operation and Thermal Shutdown

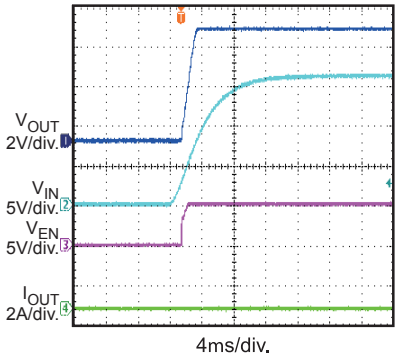


Current Limit



Start-Up into OVP

V_{IN} = 16V



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PIN FUNCTIONS

Pin #	Name	Description
1	I-LIMIT	**Current limit.** Use a resistor between I-LIMIT and SOURCE to set the overload and short circuit current-limit levels.
2	ENABLE/ FAULT	**Enable/fault.** ENABLE/FAULT is a tri-state, bidirectional interface. Leave ENABLE/FAULT floating to enable the output. Pull ENABLE/FAULT to ground using an open drain or open collector device to disable the output. If a thermal fault occurs, ENABLE/FAULT enters an intermediate state to signify that the device is in thermal shutdown.
3	DV/DT	**Output voltage slew rate.** The internal DV/DT circuit controls the slew rate of the output voltage during start-up. DV/DT has an internal capacitor that allows it to ramp up in 1.2ms. An external capacitor can be added to DV/DT to increase the ramp time. If an additional time delay is not required, leave DV/DT open.
4	GND	**Ground.** GND is the internal IC reference.
5, 6	SOURCE	**Source.** SOURCE is the internal power FET source. SOURCE is an IC output.
7, 8	VCC	**Input.** VCC is the positive input voltage.

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FUNCTIONAL BLOCK DIAGRAM

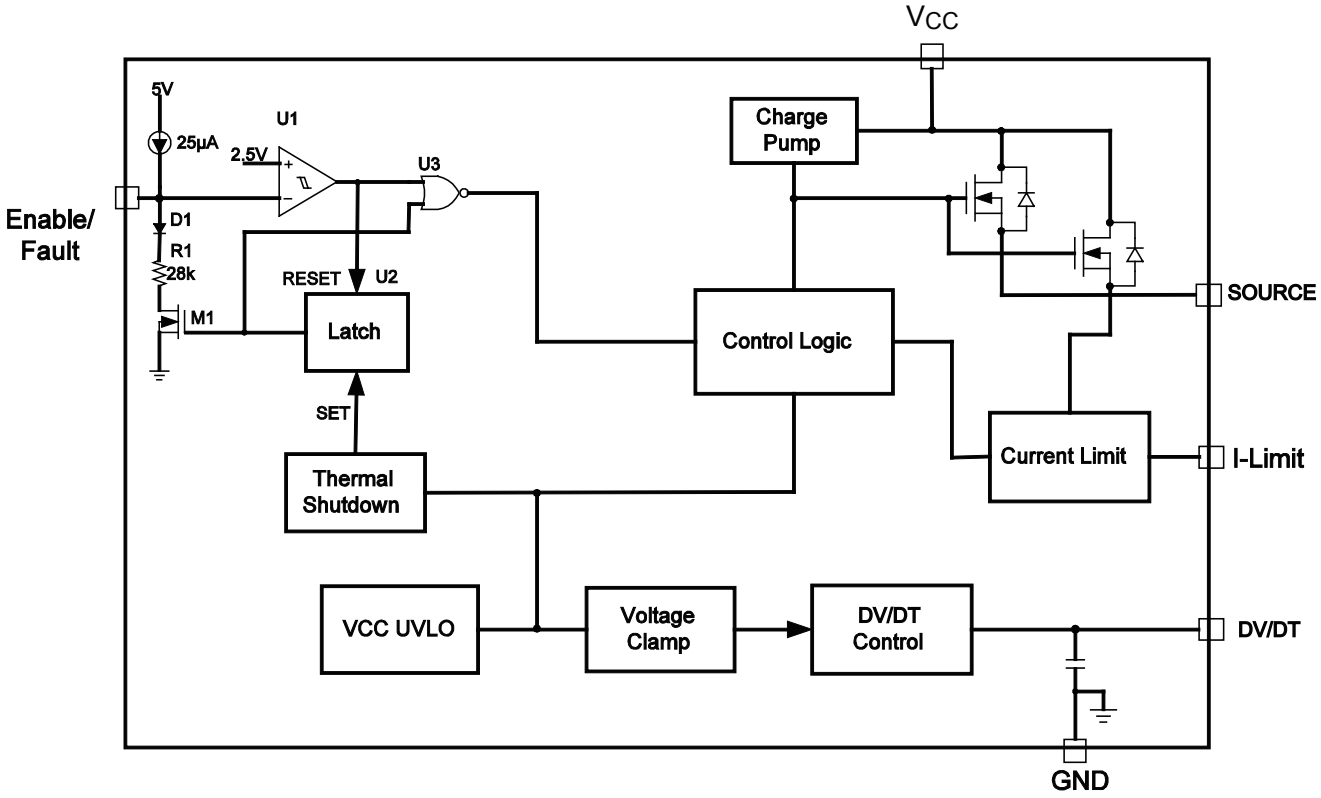

Figure 1: Functional Block Diagram

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OPERATION

The MP5013E limits the inrush current to the load when a circuit card connects to a live backplane power source, thereby limiting the backplane's voltage drop and the DV/DT of the voltage to the load. the MP5013E offers an integrated solution to monitor the input voltage, output voltage, output current, and die temperature while eliminating the external current-sense power resistor, power MOSFET, and thermal sensor.

Under-Voltage Lockout (UVLO) Operation

If the supply (input) is below the under-voltage lockout (UVLO) threshold, the output is disabled, and the ENABLE/FAULT line is driven low. When the supply rises above the UVLO threshold, the output is enabled, and ENABLE/FAULT is pulled high through a 25μA current source without an external pull-up resistor. The pull-up voltage is limited to 4.95V.

Output Over-Voltage Protection (OVP)

If the input voltage exceeds the over-voltage protection (OVP) threshold, the output is clamped at 5.7V, typically.

Current Limiting

When the chip is active, if the load reaches the over-current protection (OCP) threshold (trip current) or a short is present, the MP5013E switches to constant-current mode (hold current). The MP5013E shuts down only if the over-current condition triggers thermal protection. However, when the MP5013E is powered up by VCC or enable (EN), the load current should be smaller than the hold current. Otherwise, the part cannot be fully turned on.

In a typical application with a 22Ω current-limiting resistor, the trip current is 6.5A, and the hold current is 3.5A. If the MP5013E is in normal operation and exceeds 2.0A, it only needs to dissipate 144mW with a low 36mΩ on resistance. For a package dissipation of 100°C/W, the temperature rise is 14°C. Given a 25°C ambient temperature, the typical package temperature is 39°C.

The MP5013E requires a heat sink during constant-current mode (i.e.: from a short circuit) to prevent an unwanted shutdown. During a short-circuit condition, the MP5013E must dissipate the power from a 5V drop. Without additional heat dissipation at 100°C/W, the temperature exceeds the thermal threshold (+175°C), and the MP5013E shuts down to force the temperature to drop.

Thermal Protection

If the temperature exceeds the thermal threshold, the MP5013E disables its output and drives the ENABLE/FAULT line to middle (mid) level (see the ENABLE/FAULT section below for more details). The thermal fault condition is latched, and the MP5013E remains in a latched-off state until the power is restarted or ENABLE/FAULT is reset.

ENABLE/FAULT

ENABLE/FAULT is a bidirectional, three-level I/O pin with a weak pull-up current (typically 25μA). The three levels are low, mid, and high. The ENABLE/FAULT functions enable or disable the MP5013E and relay fault information.

When ENABLE/FAULT functions as an input, low and mid levels disable the MP5013E. A low level can also clear the fault flag. A high level enables the MP5013E if the fault flag is clear.

When ENABLE/FAULT functions as an output, the pull-up current allows a wired-NOR pull-up to enable the MP5013E if the current is not overridden. An under-voltage condition causes a low level on ENABLE/FAULT and clears the fault flag. A thermal fault sets a mid level on ENABLE/FAULT and sets the fault flag.

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The ENABLE/FAULT line must remain high for the output to turn on.

The fault flag is an internal flip-flop that can be set or reset under the following conditions:

- Thermal shutdown: set fault flag.
- Under-voltage: reset fault flag.
- Low on ENABLE/FAULT: reset fault flag.
- Mid on ENABLE/FAULT: no effect.

Under thermal shutdown, ENABLE/FAULT is driven to mid level.

There are four types of faults. Each fault has a direct and indirect effect on ENABLE/FAULT and the internal fault flag (see Table 1). In a typical application, there are one or more MP5013E chips in a system. The ENABLE/FAULT lines are connected together, typically.

Table 1: Fault Function Influence in Application

Fault Description	Internal Action	Effect on ENABLE/FAULT	Effect on Flag	Effect on Secondary Part
Short/over-current	Limit current	None	None	None
Under-voltage	Output turns off	Internally drives ENABLE/FAULT to logic low	Flag is reset	Disables secondary output and resets fault flag
Over-voltage	Limit output voltage	None	None	None
Thermal shutdown	Shut down. The MP5013E is latched off or until UVLO is driven to ground externally.	Internally drives ENABLE/FAULT to mid	Flag is set	Disables secondary part output

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APPLICATION INFORMATION

Current Limit

The current limit is a function of the external current-limit resistor (R_{LIMIT}). Table 2 lists current trip values based on R_{LIMIT}.

Table 2: Current Limit Trip Value vs. Current Limit Resistor (V_{CC} = 5V)

R_{LIMIT} (Ω)	22	51	75	100	220
Trip Current (A) (Load ramp up with 50mA/μs)	6.5	4.3	3.7	3.3	3
Trip Current (A) (DC load)	5.7	3.4	3	2.8	2.4

Table 3 lists hold current values based on R_{LIMIT}.

Table 3: Current Limit Hold Value vs. Current Limit Resistor (V_{CC} = 5V)

R_{LIMIT} (Ω)	22	51	75	100	220
Hold Current (A)	3.5	1.5	1.1	0.81	0.4

Rise Time

The rise time is a function of the capacitor ($C_{DV/DT}$) on DV/DT. Table 4 lists typical rise times as a function of the capacitance.

Table 4: Rise Time vs. $C_{DV/DT}$

$C_{DV/DT}$	None	150pF	470pF	1nF
Rise Time (ms)	1.2	5.7	15.3	31.2

Calculate the rise time with Equation (1):

$$\text{Rise time (ms)} = 0.03\text{ms} * C_{DV/DT}\text{(pF)} + 1.2\text{ms} \quad (1)$$

The rise time is measured from 10% to 90% of the output voltage (see Figure 2).

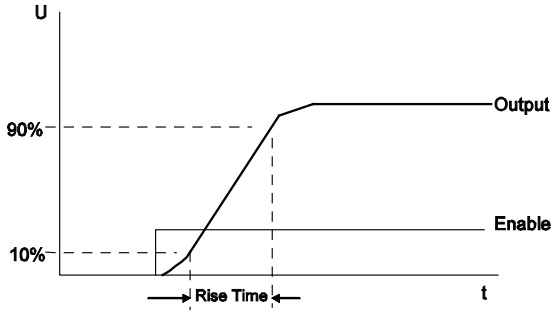
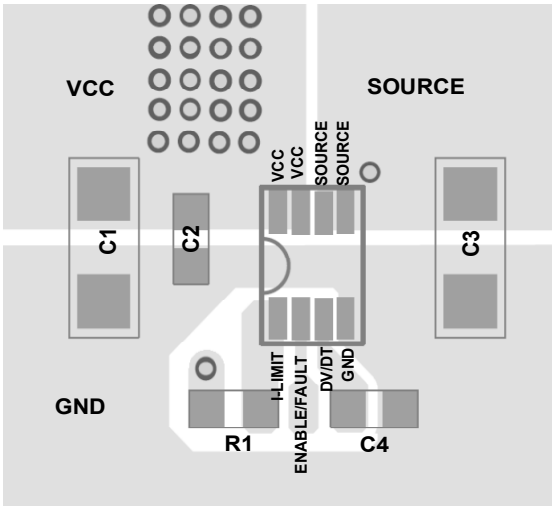


Figure 2: Rise Time

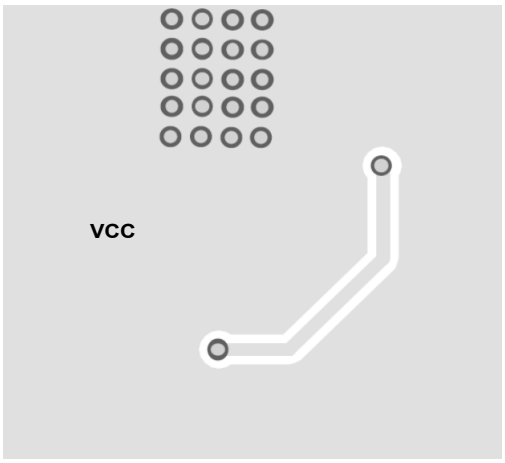
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 3 and follow the guidelines below.

1. Place R_{LIMIT} close to I-Limit.
2. Place $C_{DV/DT}$ close to DV/DT.
3. Place the input capacitor close to VCC.
4. Place enough copper area near VCC and SOURCE for thermal dissipation.



Top Layer



Bottom Layer

Figure 3: Recommended PCB Layout

Design Example

Table 5 is a design example following the application guidelines for the specifications below.

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Table 5: Design Example

V_{IN}	5V
Trip Current	6.5A
Hold Current	3.5A

Figure 4 shows the typical application schematic. The Typical Performance Characteristics section shows the circuit waveforms. For more device applications, please refer to the related evaluation board datasheet.

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TYPICAL APPLICATION CIRCUIT

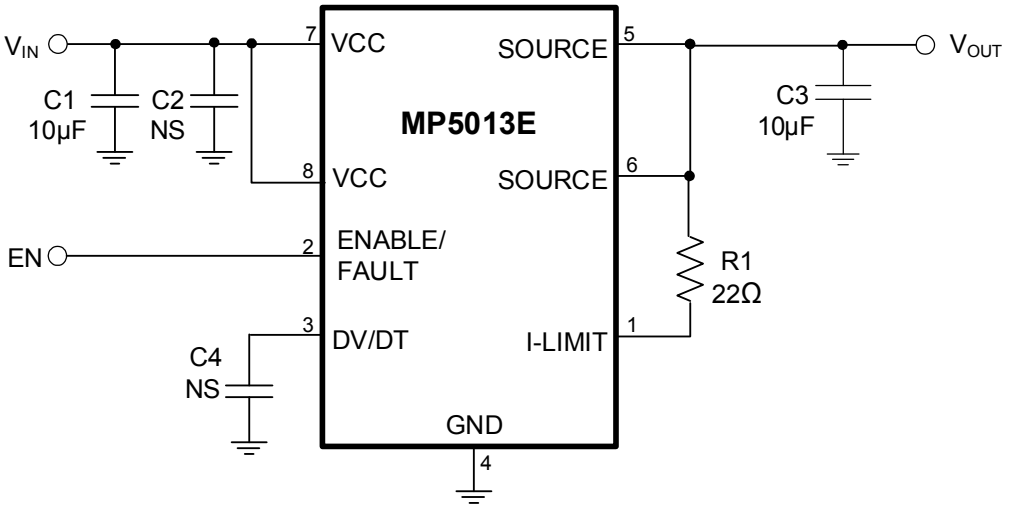

Figure 4: Typical Application Schematic

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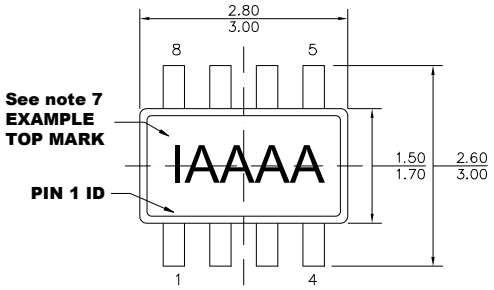
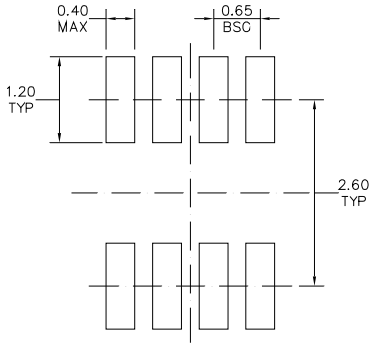
PACKAGE INFORMATION

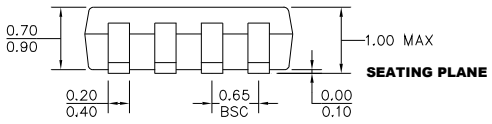
TSOT23-8



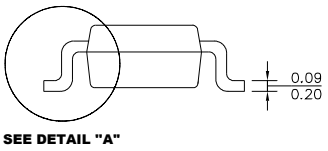
TOP VIEW



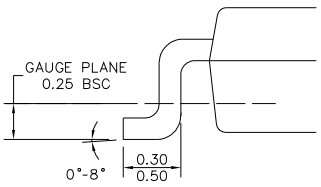
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-193, VARIATION BA.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	09/26/2016	Initial Release	-
1.1	07/13/2021	• Table 2 is updated to Current Limit Trip Value vs. Current Limit Resistor with different load conditions • Table 3 is updated to Current Limit Trip Value vs. Current Limit Resistor	11

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