MP5013A

5 V, 5 A Programmable Current-Limit Switch with Over-Voltage Clamp and Slew-Rate Control in TSOT23-8

The Future of Analog IC Technology

DESCRIPTION

The MP5013A is a protection device designed to protect circuitry on the output (source) from transients on the input (V_{CC}). Also, it protects the input from undesired shorts and transients coming from the source.

A small capacitor on DV/DT controls the slew rate that limits the inrush current at the source. DV/DT has an internal circuit that allows the customer to float this pin (no connection) and still receive 1.4 ms ramp time at the source. The maximum load at the source is current limited using a sense FET topology. An external resistor between I-LIMIT and SOURCE controls the magnitude of the current limit.

An internal charge pump drives the gate of the power device, allowing the DMOS power FET to have a very low on resistance of just 36 mΩ.

The MP5013A protects the source from the input becoming too low or too high. Under-voltage lockout ensures that the input remains above the minimum operating threshold before the power device turns on. If the input rises above the high output threshold, the MP5013A limits the source voltage.

FEATURES

- 3 V to 5.5 V Operating Input Range
- 5.7 V Typical Output Over-Voltage Clamp
- Absolute Maximum Voltage of 22 V
- Input Under-Voltage Lockout
- Low Inrush Current during Start-Up
- Integrated 36 mΩ Power FET
- Enable/Fault Pin
- Adjustable Output Voltage Slew Rate
- Adjustable Current Limit
- Thermal Shutdown Protection
- TSOT23-8 Package

APPLICATIONS

- Storage (HDDs, SSDs)
- Hot-Swap Systems
- Set-Top Boxes
- USB Ports/Hubs
- Gaming

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance.

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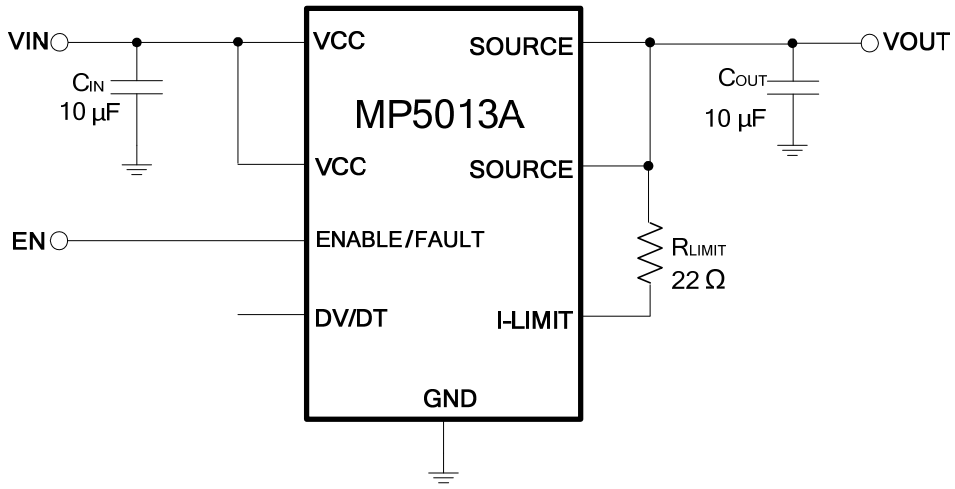
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP5013AGJ	TSOT23-8	*See Below*

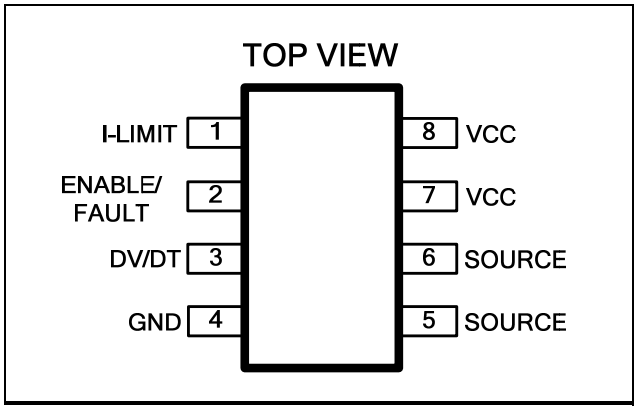
* For Tape & Reel, add suffix –Z (e.g. MP5013AGJ–Z)

TOP MARKING

|AMKY

AMK: Product code of MP5013AGJ
Y: Year code

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

VCC, SOURCE, I-LIMIT.....–0.3 V to 22 V
DV/DT, ENABLE/FAULT.....–0.3 V to 6 V
Storage temperature..... –65°C to +155°C
Junction temperature..... +150°C
Lead temperature..... +260°C
Continuous power dissipation (T_A=+25°C) (2)
..... .1.25 W

Recommended Operating Conditions (3)

Input voltage operating range ..... 3 V to 5.5 V
0.5 in^2 pad ..... 4.2 A
For minimum copper, T_A = 80°C ..... 2.3 A
Operating junction temp. (T_J)..... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TSOT23-8 .....100 ..... 55 ... °C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. the maximum allowable power dissipation at any ambient temperature is calculated using: $P_D(MAX)=(T_J(MAX)-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will produce an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
   Reduce 0.1 watts for every 10°C ambient temperature increase.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7 4-layer board.

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ELECTRICAL CHARACTERISTICS

V_{CC} = 5 V, R_{LIMIT} = 22 Ω, Capacitive Load = 10 µF, T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Power FET						
Delay time	t_{DLY}	Enabling of chip to I_D = 40 mA with a 5 Ω resistive load, float DV/DT		37		µs
On resistance	R_{DSon}	T_J = 25°C		36		mΩ
		T_J = 85°C(5)		48		
Off-state output voltage	V_{OFF}	V_{CC} = 18 V, V_{EN} = 0 V, R_L = 500 Ω			120	mV
Thermal latch						
Shutdown temperature(5)	T_{SD}			175		°C
Under/over-voltage protection						
Output clamp voltage	V_{CLAMP}	Over-voltage protection V_{CC} = 8 V	5.5	5.7	5.9	V
Under-voltage lockout	V_{UVLO}	Rising edge	2.5	2.7	2.9	V
Under-voltage lockout (UVLO) Hysteresis	V_{HYST}			0.13		V
Current limit (5)						
Hold current	I_{LIM-SS}	0 Ω short resistance, R_{LIM} = 22 Ω	2.1	2.8	3.5	A
Trip current	I_{LIM-OL}	R_{LIM} = 22 Ω		5		A
DV/DT circuit						
Rise time	t_r	Float DV/DT, Output rises from 10% to 90%		1.4		ms
Enable/fault						
Low-level input voltage	V_{IL}	Output disabled			0.5	V
Intermediate-level input voltage	$V_{I (INT)}$	Thermal fault, output disabled	0.82	1.3	1.95	V
High-level input voltage	V_{IH}	Output enabled	2.5			V
High-state maximum voltage	$V_{I (MAX)}$			4.95		V
Pull-up current (source)	I_{IL}	V_{ENABLE} = 0 V	15	25	35	µA
Maximum fanout for fault signal		Maximum number of chips for simultaneous shutdown			3	Units
Maximum voltage on EN(6)	V_{MAX}				VCC	V
Total device						
Bias current	I_{BIAS}	Device operational		890	950	µA
		Enable shutdown		580	650	
		Thermal shutdown		600	700	
Minimum operating voltage for UVLO	V_{MIN}	Enable < 0.5 V			2.5	V

NOTES:

5) Guaranteed by characterization test.

6) Maximum input voltage on ENABLE/FAULT is ≤ 6 V if VCC ≥ 6 V. Maximum input voltage on ENABLE/FAULT is VCC if VCC ≤ 6 V.

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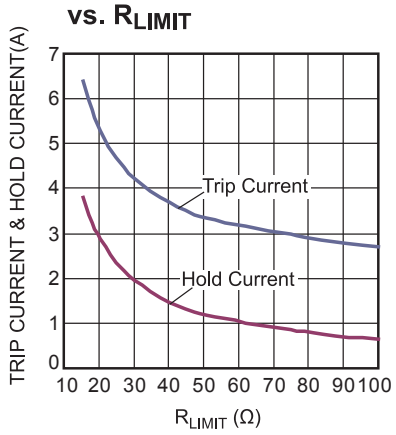
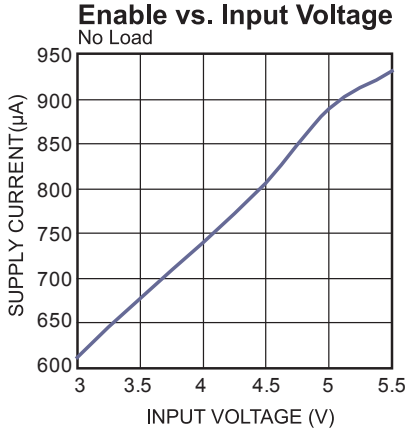
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5 V, V_{EN} = 5 V, R_{LIMIT} = 22 Ω, C_{OUT} = 10 µF, $C_{DV/DT}$ = float, T_A = 25°C, unless otherwise noted.

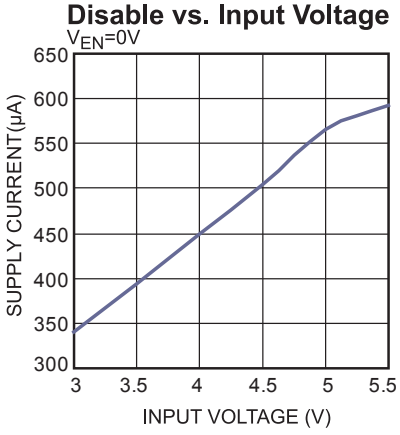
Trip Current & Hold Current vs. R_{LIMIT}



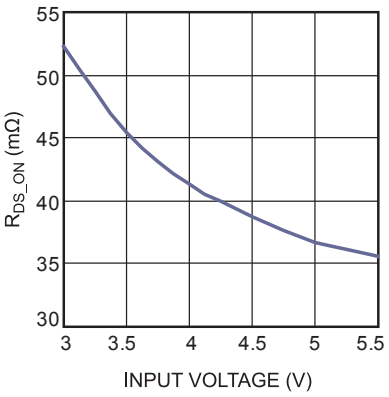
Supply Current, Output Enable vs. Input Voltage



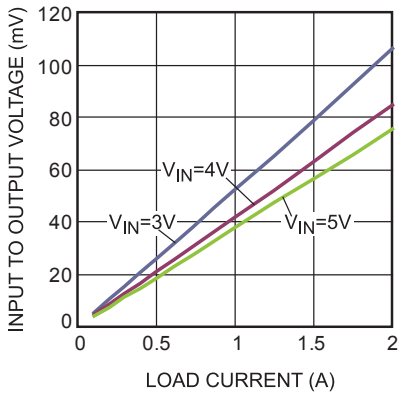
Supply Current, Output Disable vs. Input Voltage



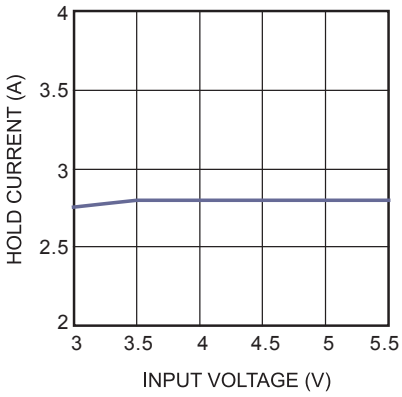
R_{DS_ON} vs. Input Voltage



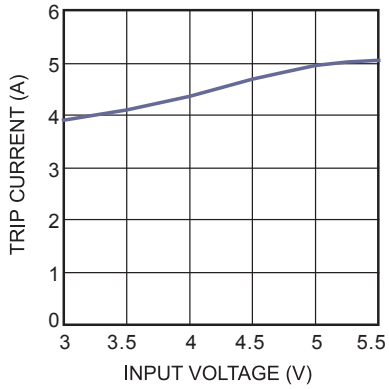
Input to Output Voltage vs. Load Current



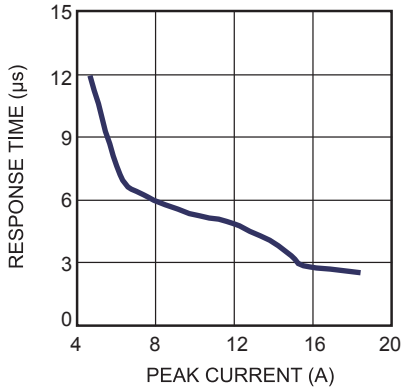
Hold Current vs. Input Voltage



Trip Current vs. Input Voltage



Current Limit Response vs. Peak Current



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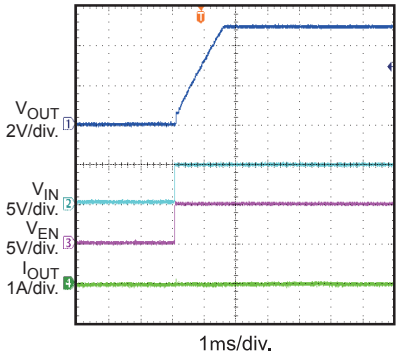
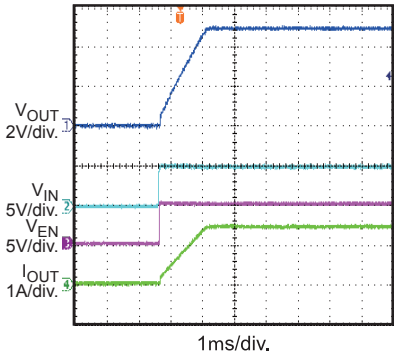
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5 V, V_{EN} = 5 V, R_{LIMIT} = 22 Ω, C_{OUT}= 10 µF, $C_{DV/DT}$ = Float, T_A = 25°C, unless otherwise noted.

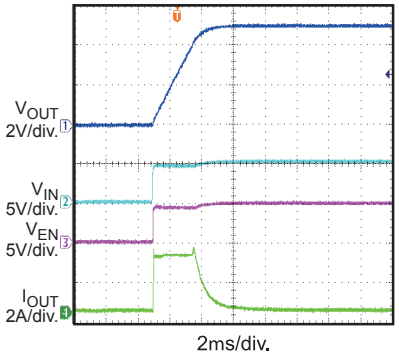
Start-Up through Input Voltage
No Load



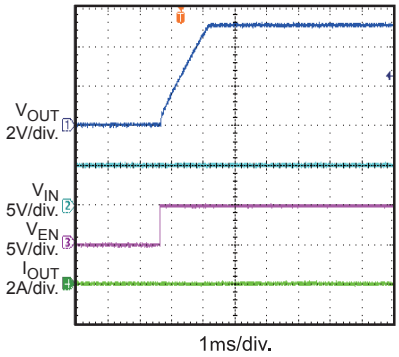
Start-Up through Input Voltage
R_{LOAD} = 3.3Ω



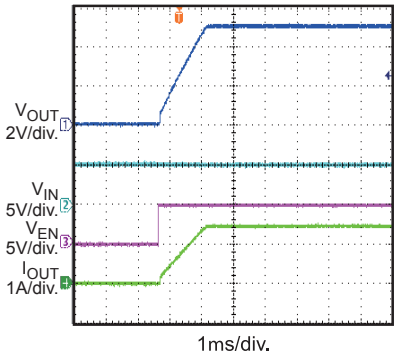
Start-Up through Input Voltage
C_{OUT} = 2200µF



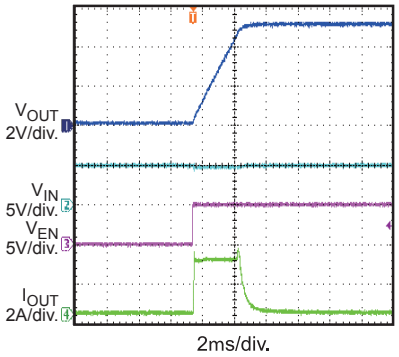
Start-Up through Enable
No Load



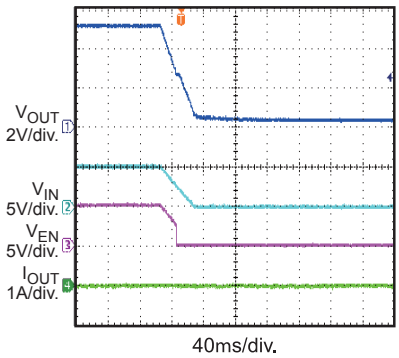
Start-Up through Enable
R_{LOAD} = 3.3Ω



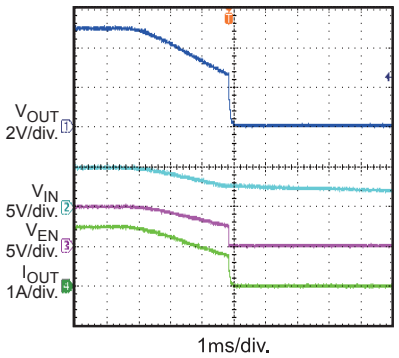
Start-Up through Enable
C_{OUT} = 2200µF



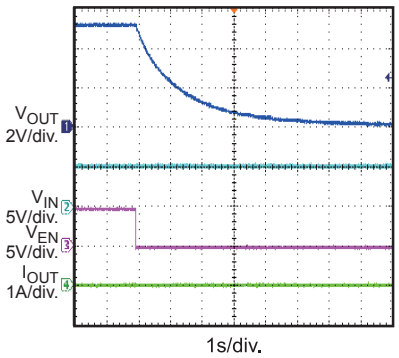
Shutdown through Input Voltage
No Load



Shutdown through Input Voltage
R_{LOAD} = 3.3Ω



Shutdown through Enable
No Load



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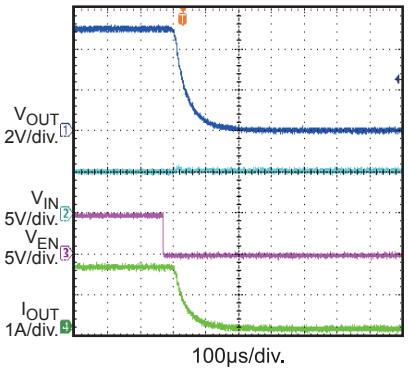
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

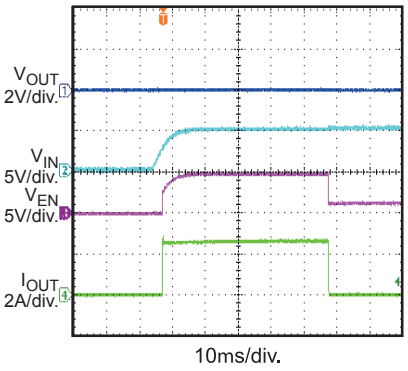
V_{IN} = 5 V, V_{EN} = 5 V, R_{LIMIT} = 22 Ω, C_{OUT} = 10 µF, $C_{DV/DT}$ = float, T_A = 25°C, unless otherwise noted.

Shutdown through Enable

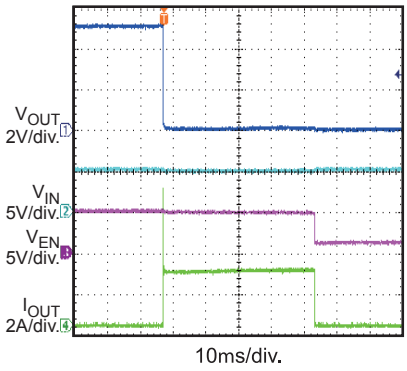
R_{LOAD} = 3.3Ω



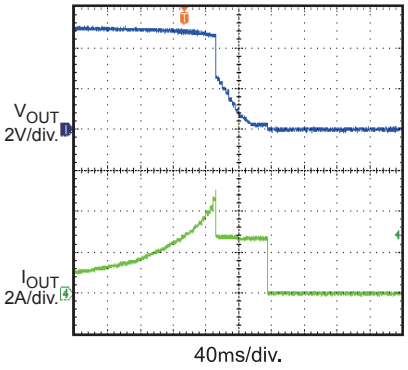
Short Circuit before Input Voltage Start-Up and Thermal Shutdown



Short Circuit during normal Operation and Thermal Shutdown

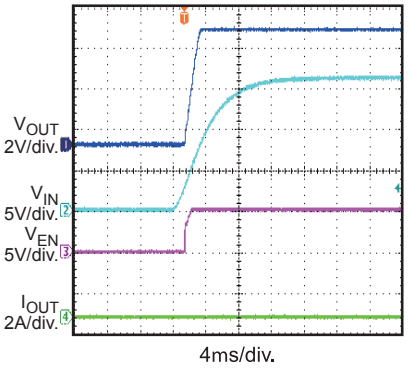


Current Limit



Start-Up into OVP

V_{IN} = 16V



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PIN FUNCTIONS

Pin #	Name	Description
1	I-LIMIT	**Current limit.** Use a resistor between I-LIMIT and the SOURCE pins to set the overload and short-circuit current-limit levels.
2	ENABLE/FAULT	**A tri-state, bi-directional interface**. Leave ENABLE/FAULT floating to enable the output. Pull ENABLE/FAULT to ground (using an open drain or open collector device) to disable the output. If a thermal fault occurs, this voltage enters an intermediate state to signal that the device is in thermal shutdown.
3	DV/DT	**Controls the slew rate of the output voltage at turn on**. DV/DT has an internal capacitor that allows it to ramp up over a period of 1.4 ms. An external capacitor can be added to DV/DT to increase the ramp time. If an additional time delay is not required, DV/DT should be left open.
4	GND	**Ground.** Internal IC reference.
5,6	SOURCE	**Source.** Internal power FET source. IC output.
7,8	VCC	**Input**. Positive input voltage.

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FUNCTIONAL BLOCK DIAGRAM

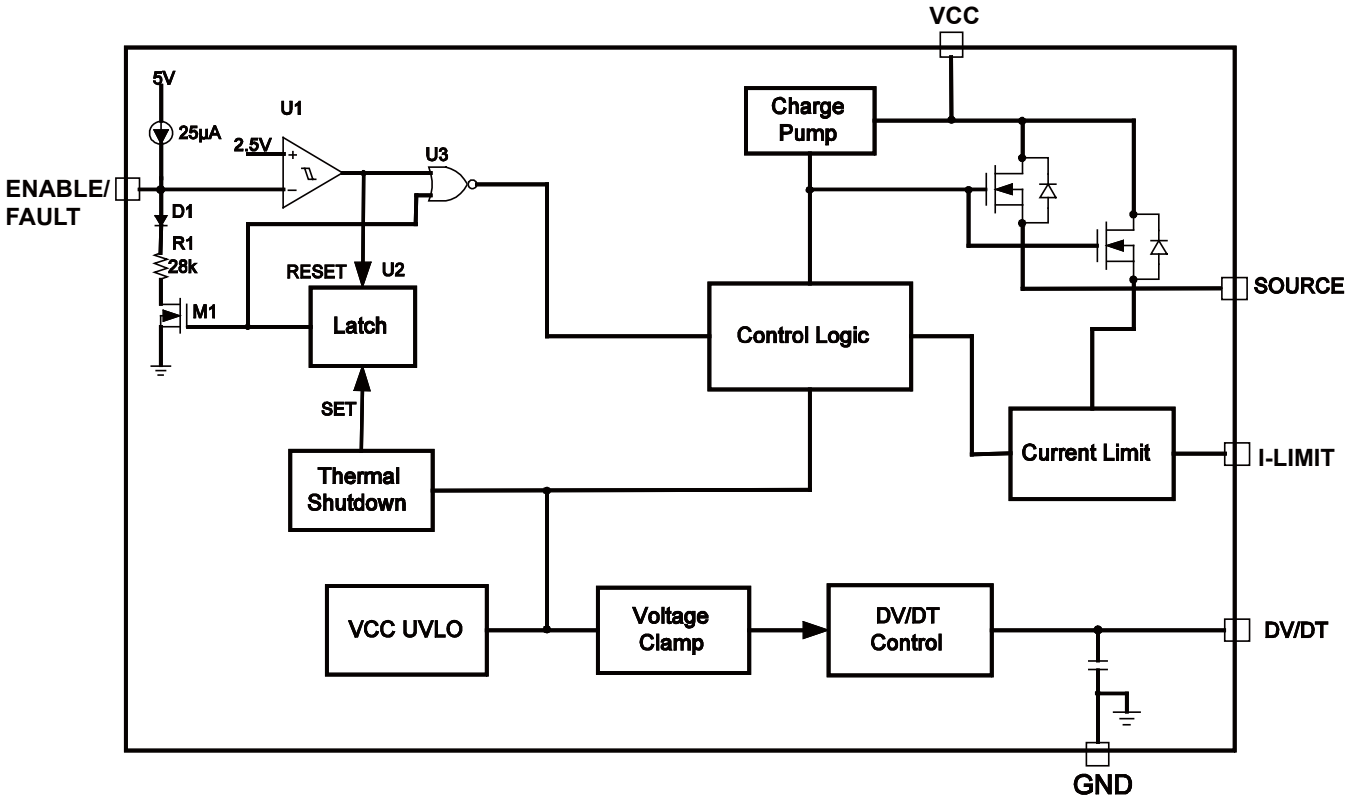

Figure 1—Functional block diagram

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OPERATION

The MP5013A limits the inrush current to the load when a circuit card connects to a live backplane power source, thereby limiting the backplane's voltage drop and the dv/dt of the voltage to the load. It offers an integrated solution to monitor the input voltage, output voltage, output current, and die temperature, eliminating the external current-sense power resistor, power MOSFET, and thermal sensor.

Under-Voltage Lockout Operation

If the supply (input) is below the UVLO threshold, the output is disabled, and the ENABLE/FAULT line is driven low.

When the supply rises above the UVLO threshold, the output is enabled, and ENABLE/FAULT is pulled high through a 25 μA current source without an external pull-up resistor. The pull-up voltage is limited to 4.95 V.

Output Over-Voltage Protection (OVP)

If the input voltage exceeds the over-voltage protection (OVP) threshold, the output is clamped at 5.7 V (typically).

Current Limiting

When the chip is active, if the load reaches the over-current protection (OCP) threshold (trip current), or a short is present, the part switches to constant-current mode (hold current). The chip shuts down only if the over-current condition eventually triggers thermal protection. However, when the part is powered up by VCC or EN, the load current should be less than the hold current. Otherwise, the part cannot be turned on fully.

In a typical application with a current-limiting resistor of 22 Ω, the trip current is 5 A, and the hold current is 2.8 A. If the device is in normal operation and passing 2 A, it will only need to dissipate 144 mW with the low on resistance of 36 mΩ. For a package dissipation of 100°C/W, the temperature rise is +14°C. Given a 25°C ambient temperature, the typical package temperature is 39°C.

The MP5013A requires a heat sink during constant-current mode (e.g., from a short circuit) to prevent an unwanted shutdown. (During a short-circuit condition, the chip must dissipate the power from a 5 V drop.) Without an additional heat dissipation at 100°C/W, the temperature will exceed the thermal threshold (+175°C), and the MP5013A will shut down to force the temperature to drop.

Thermal Protection

If the temperature exceeds the thermal threshold, the MP5013A disables its output and drives the ENABLE/FAULT line to the middle (mid) level (see the following "ENABLE/FAULT" section for more information). The thermal fault condition is latched, and the part will remain in a latched-off state until the power is re-started, or ENABLE/FAULT is re-set.

ENABLE/FAULT

ENABLE/FAULT is a bi-directional, three-level I/O with a weak pull-up current (25 μA, typically). The three levels are low, mid, and high. It functions to enable/disable the part and to relay fault information.

ENABLE/FAULT as an input:

1. Low and mid disable the part.
2. Low, in addition to disabling the part, clears the fault flag.
3. High enables the part (if the fault flag is clear).

ENABLE/FAULT as an output:

1. The pull-up current will allow a "wired nor" pull-up to enable the part (if not overridden).
2. An under-voltage condition will cause a low on ENABLE/FAULT and will clear the fault flag.
3. A thermal fault will set a mid on the ENABLE/FAULT and will set the fault flag.

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The ENABLE/FAULT line must remain at a high level for the output to turn on.

The fault flag is an internal flip-flop that can be set or re-set under the following conditions:

1. Thermal Shutdown: sets fault flag.
2. Under-Voltage: re-sets fault flag.
3. Low on ENABLE/FAULT: re-sets fault flag.
4. Mid on ENABLE/FAULT: no effect.

During a thermal shutdown, ENABLE/FAULT is driven to the mid level.

There are 4 types of faults, and each fault has a direct and indirect effect on EANBLE/FAULT and the internal fault flag (see Table 1). In a typical application, there are one or more of the MP5013A chips in a system. ENABLE/FAULT lines are connected together typically.

Table 1—Fault function influence in application

Fault Description	Internal Action	Effect on Fault Pin	Effect on Flag	Effect on Secondary Part
Short/over current	Limits current	None	None	None
Under voltage	Output turns off	Internally drives ENABLE/FAULT to logic low	Flag is re-set	Disables secondary output and re-sets fault flag
Over voltage	Limits output voltage	None	None	None
Thermal shutdown	Shutdown. The part is latched off until a UVLO or externally driven to ground.	Internally drives ENABLE/FAULT to mid level	Flag is set	Disables secondary part output

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APPLICATION INFORMATION

Current Limit

The current limit is a function of the external current-limit resistor. Table 2 lists examples of current values as a function of the resistor value.

Rise Time

The rise time is a function of the capacitor ($C_{DV/DT}$) on DV/DT. Table 3 lists the typical rise time as a function of capacitance.

Table 2—Current limit vs. current limit resistor (V_{CC} = 5 V)

R_{LIMIT} (Ω)	22	51	75	100	220
Trip current (A)	5	3.4	2.98	2.7	2.43
Hold current (A)	2.8	1.2	0.84	0.65	0.33

Table 3—Rise time vs. $C_{DV/DT}$

$C_{DV/DT}$	None	150 pF	470 pF	1 nF
Rise time (ms, typically)	1.4	5.9	15.5	31.4

* **NOTE:** Rise time(ms) = 0.03ms*$C_{DV/DT}$(pF)+1.4ms

The rise time is measured from 10% to 90% of the output voltage (see Figure 2).

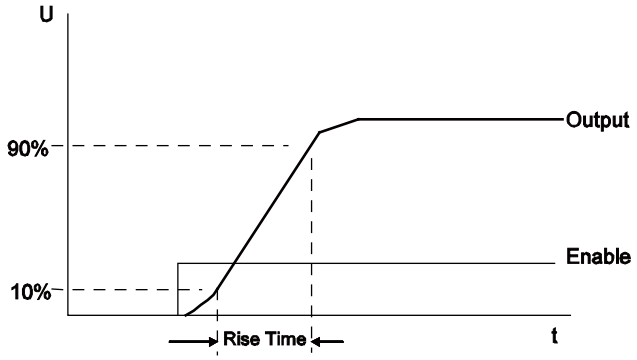

Figure 2—Rise time

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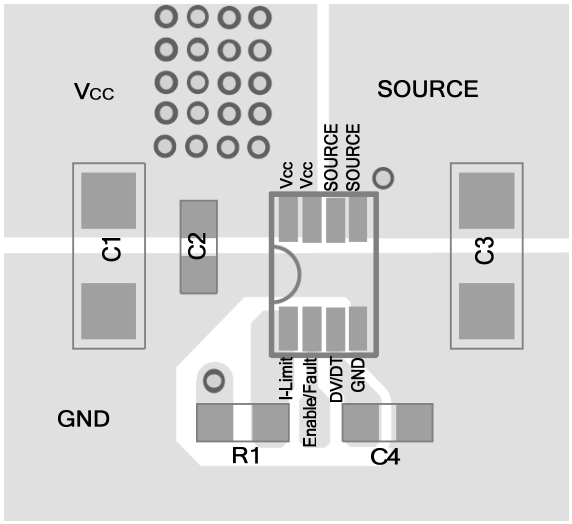
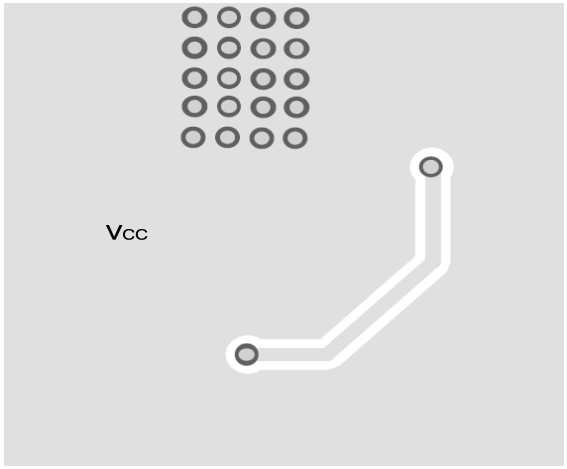
PCB Layout Guidelines

Efficient PCB layout is critical to achieve stable operation. For best results, please refer to Figure 3 and follow the guidelines below:

1. Place R_{LIMIT} close to the I-LIMIT.
2. Place $C_{DV/DT}$ close to DV/DT.
3. Place the input capacitor close to VCC.
4. Place enough copper area near VCC and SOURCE for thermal dissipation.



Top Layer



Bottom Layer

Figure 3—Sample PCB layout

Design Example

Table 4 shows a design example following the application guidelines for the given specifications:

Table 4—Design example

V_{IN}	5 V
Trip current	5 A
Hold current	2.8 A

Figure 4 shows the application schematic. The “Typical Performance Characteristics” section shows the circuit waveforms. For more device applications, please refer to the related evaluation board datasheet.

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TYPICAL APPLICATION CIRCUITS

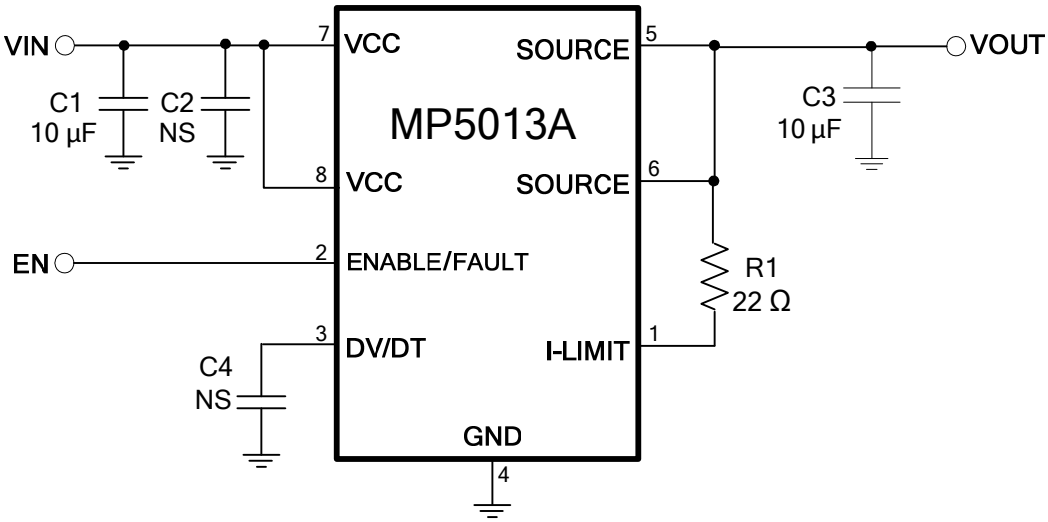

Figure 4—Typical application schematic

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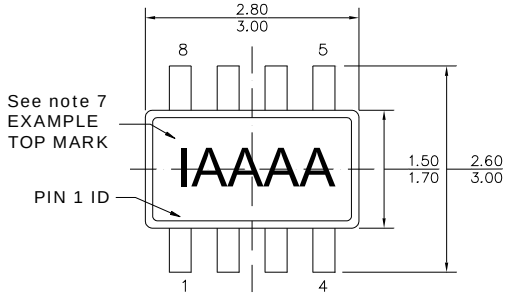
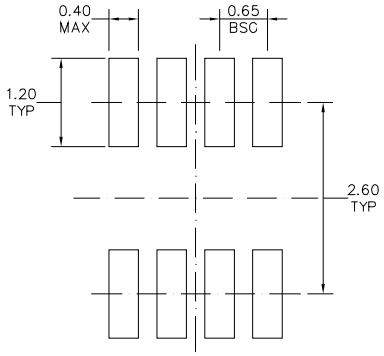
PACKAGE INFORMATION

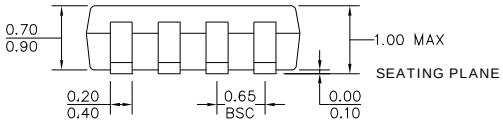
TSOT23-8



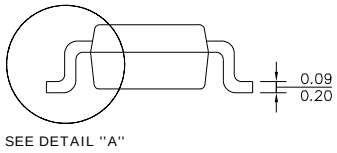
TOP VIEW



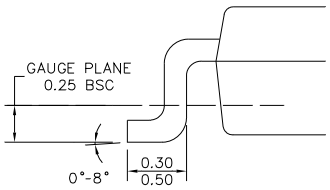
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-193, VARIATION BA.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

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