MP4651

Off Line LED Driver

The Future of Analog IC Technology

DESCRIPTION

The MP4651 is a high performance off-line LED driver designed for powering the LEDs especially for high power isolated application.

The MP4651 utilizes fixed operating frequency PWM control. It outputs two 180 degree phase shifted driving signals for various external power stages. Its enhanced 9V gate driver provides adequate driving capability for the external MOSFETs and directly drives the external gate driving transformer.

The MP4651 implements fast and high contrast ratio PWM dimming to the LEDs. PWM dimming is controlled with either an external DC voltage or PWM signal. The burst dimming frequency can be synchronized to an external synchronizing signal.

The Built-in fault management features include open LED protection, short LED protection, over voltage protection, and over temperature protection. The protection interface is flexible for various setups and is easy to use. MP4651 integrates a delay timer to recover the system.

The MP4651 is available in a 16-pin SOIC package.

FEATURES

- 9V Enhanced Gate Driver
- Programmable Fixed Operating Frequency
- Input Voltage Range from 9V to 30V
- DC or PWM Input Dimming Control
- Burst Dimming Frequency Synchronization
- Smart Fault Protection Interface
- Built-in Fault Management
- Built-in Delay Timer for System Recovery
- Available in a SOIC16 Package

APPLICATIONS

- LCD TV and LCD Monitor
- Flat Panel Video Displays
- LED Lighting Applications

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The MP4651 is covered by US Patents 6,683,422, 6,316,881, and 6,114,814. Other Patents Pending.

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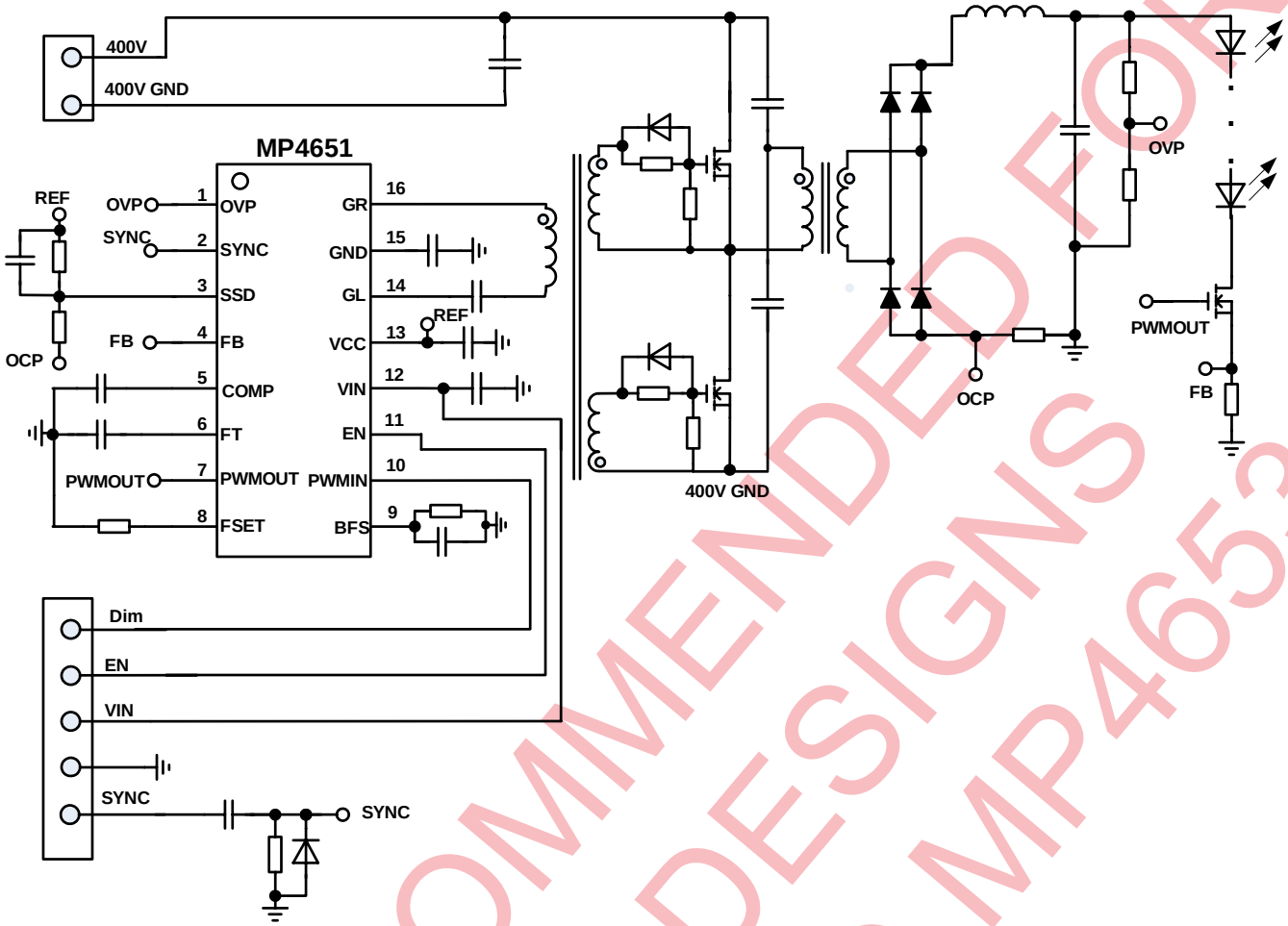
SIMPLIFIED TYPICAL APPLICATION CIRCUIT



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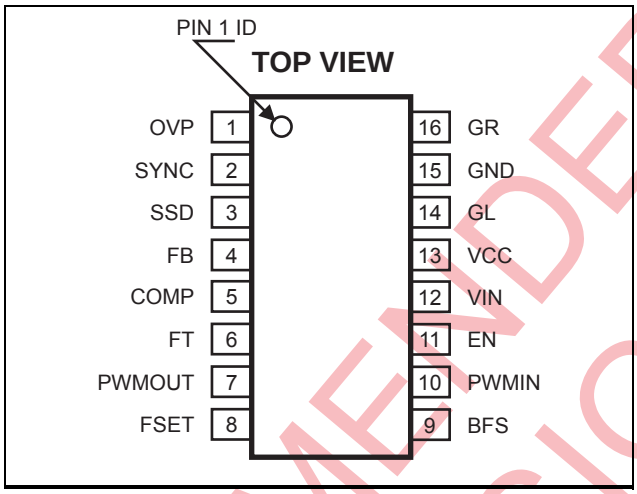
ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature (T_A)
MP4651ES	SOIC16	MP4651ES	-20°C to +85°C

* For Tape & Reel, add suffix –Z (e.g. MP4651ES–Z)
For RoHS Compliant Packaging, add suffix –LF (e.g. MP4651ES–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Input Voltage V_{IN} 35V
GL, GR ..... -0.3V to 10.7V
FB, SSD ..... -5.8V to +5.8V
Other Pins ..... -0.3V to +6.5V
Continuous Power Dissipation (T_A = +25°C)(2) 2.5W
Junction Temperature ..... 150°C
Lead Temperature (Solder) ..... 260°C
Operating Frequency ..... 20kHz to 150kHz
Storage Temperature ..... -55°C to +150°C

Recommended Operating Conditions (3)

Input Voltage V_{IN} ..... 9V to 30V
Operating Frequency (Typical) 50kHz
Maximum Junction Temp. (T_J) ..... +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
SOIC16	80	30	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/ θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Gate driver GL, GR						
Gate Pull-Down	R_{GD}			2		Ω
Gate Pull-Up	R_{GU}			4		Ω
Output Source Current	I_{SOURCE}			1		A
Output Sink Current	I_{SINK}			2		A
Maximum Duty Cycle	D_{MAX}			46%		
EN						
EN Turn On Threshold	V_{EN-ON}		2			V
EN Turn Off Threshold	V_{EN-OFF}				1	V
Internal Pull-down Resistor	R_{EN-IN}			60		kΩ
Brightness Dimming Control Range						
PWM Full Scale	V_{PWM}	DC input burst dimming	1.1	1.2	1.3	V
PWM Logic Input Threshold	V_{TH-PWM}	PWM dimming	1.6	1.9	2.2	V
PWM Logic Input Hysteresis	$V_{TH-PWM-Hyst}$	PWM dimming		0.1		V
Burst Frequency Set (BFS)						
Source Current	$I_{SRC(BFS)}$	V_{BFS} = 2V	120	140	170	μA
Lower Threshold	$V_{V(BFS)}$		2.2	2.4	2.6	V
Upper Threshold	$V_{P(BFS)}$		3.3	3.55	3.8	V
Supply Current						
Supply Current (Enabled)	I_{IN-EN}	No driver output		1.5	2.5	mA
Supply Current (Disabled)	I_{IN-OFF}	V_{IN}=30V			1	μA
Operating Frequency	f_O	25kΩ FSET to GND	46.5	50	53.5	kHz
Frequency Set Voltage	V_{FSET}		1.14	1.2	1.25	V
Output PWM Dimming Signal for LED (PWMOUT)						
Logic High Voltage	$V_{H-PWMOUT}$	Normal Operation	5V	6	6.5V	V
Logic Low Voltage	$V_{L-PWMOUT}$	At Fault Condition, 25kΩ FSET to GND		0.1	0.6V	V
Output PWM Source Current	I_{SOURCE_PWMOUT}	100pF on PWMOUT pin		3		mA
Output PWM Sink Current	I_{SINK_PWMOUT}	100pF on PWMOUT pin		20		mA
LED Current Feedback (FB)						
Magnitude	$\|V_{FB}\|$		0.57	0.6	0.63	V
Input resistance	R_{FB_IN}			30		kΩ
Over Voltage Protection (OVP)						
Over Voltage Protection Threshold	$V_{TH(OVP)}$		2.22	2.38	2.55	V

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Fault Timer (FT)						
Threshold	$V_{th(FT)}$		2.2	2.4	2.6	V
Source Current	$I_{SOURCE(FT)}$			8		µA
Comp						
Clamp Voltage	V_{COMP}			0.60		V
Reference Current	I_{COMP+}			20		µA
Pull Down Current at Fault Condition	$I_{COMP-FAULT}$	Fault Mode is triggered		30		µA
Burst Frequency Synchronization (SYNC)						
High logic level	V_{SYNC-H}		1.4			V
Low logic level	V_{SYNC-L}				0.7	V
Pulse width	t_{sync}		6	10	20	µs
Synchronizing Frequency	f_{SYNC}	DC input burst dimming, Compared to the frequency f_{BFS} set by BFS pin R and C	110%	120%		
Fault Detection Threshold (SSD, FB)						
SSD Threshold	V_{SSD}		2.22	2.36	2.55	V
SSD Detection Delay Time	$T_{D\ SSD}$			7		µs
FB threshold	$V_{FB\ th}$		1.1	1.2	1.3	V
FB Detection Delay Time	$T_{D\ FB}$			7		µs
Output Gate Driver (VCC)						
Voltage	V_{VCC}	No load	8.7	9.7	10.5	V
Current	I_{VCC}			20		mA

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PIN FUNCTIONS

Pin #	Name	Description
1	OVP	Over Voltage Protection. The output voltage is sensed by this pin through a voltage divider from the anode of the LED to ground. If the voltage at OVP exceeds 2.38V for 7us, the Fault Mode is triggered.
2	SYNC	Synchronization for the burst dimming frequency. Applying a synchronizing signal with a narrow pulse on this pin will synchronize the burst frequency on BFS pin. The frequency of the synchronizing signal should be higher than the frequency set by BFS pin.
3	SSD	Short String Detection. A comparator is integrated in this pin for short string protection. If the voltage on this pin gets lower than 2.36V for 7us, the Fault Mode is triggered.
4	FB	LED Current Feedback Input. Connect this pin to the cathode of the LED and shunt a sense resistor to ground. The internal error amplifier sinks a current from the COMP pin proportional to the absolute value of the voltage at this pin. The average voltage at this pin is regulated to 0.6V reference voltage. The voltage on this pin is also used for short string detection. When the voltage on this pin gets higher than 1.2V for 7us, the IC recognizes this as short string condition and triggers the Fault Mode.
5	COMP	Feedback Compensation Node. Connect a compensation capacitor or a R-C network from this pin to GND.
6	FT	Fault Timer. Connect a timing capacitor from this pin to GND to set the fault timer to recover the system. When the voltage on this pin gets higher than the 2.38V threshold, the IC recovers.
7	PWMOUT	This pin outputs the PWM dimming signal to LED for fast dimming. At Fault Mode, the PWMOUT is pulled down.
8	FSET	Frequency Set. Connect a resistor from this pin to GND. This resistor sets the operating frequency of the MP4651. A 25kOhm resistor sets the operating frequency at typical 50kHz.
9	BFS	Burst Frequency Set. Connect a resistor in parallel with a capacitor from BFS to GND. The resistor and capacitor programs the burst dimming frequency. If the burst dimming is to be controlled by an external PWM signal, pull up BFS to VCC through a 20kΩ resistor and apply the PWM signal to the PWMIN pin.
10	PWMIN	Burst-Mode (Digital) Brightness Control Input. For DC input burst dimming, the voltage range from 0 V to 1.2V at PWMIN linearly sets the burst-mode duty cycle from 0 to 100%. For external PWM input dimming, directly apply the logic signal on this pin. The MP4651 has positive dimming polarity.
11	EN	Enable Input. Pull EN high to turn on the chip, and pull EN low to turn it off.
12	VIN	Supply voltage input.
13	VCC	Linear Regulator Output and Bias Supply of the Gate Driver. It provides the supply for the gate driver and also the external control circuit, the typical value is 9.7V. Bypass VCC with a 1μF or larger ceramic capacitor.
14	GL	Driving signal output, 180 degree phase shifted of GR
15	GND	Ground.
16	GR	Driving signal output, 180 degree phase shifted of GL

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BLOCK DIAGRAM

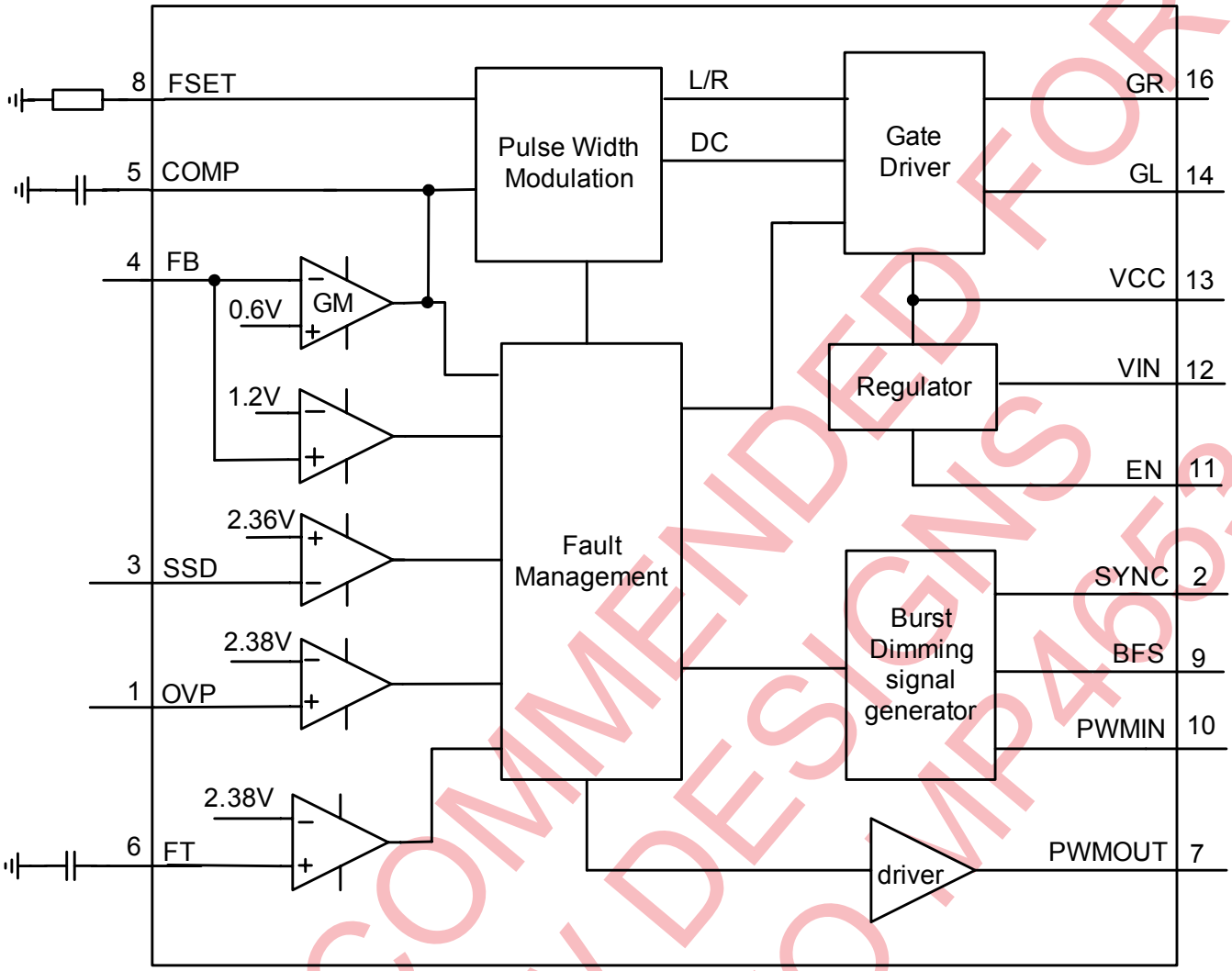

Figure 1—MP4651 Block Diagram

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DESIGN INFORMATION

Steady State and Enable Control

The MP4651 is a fixed operating frequency off-line LED driver, specifically designed for the high power isolated applications. Powered by 9V to 30V input supplies, the MP4651 outputs two 180 degree phase shifted driving signals for the external power stages. Its enhanced 9V gate driver provides adequate driving capability to the external MOSFETs and directly drives the external gate driving transformer.

The MP4651 utilizes Pulse Width Modulation control to the system. The operating frequency is set by an external resistor connected from FSET pin to GND. The LED current is fed back to FB pin and compared with internal 0.6V reference voltage. Together with the integrator compensation network on COMP pin, which is connected to the output of the error amplifier, the output LED current is accurately regulated. The voltage on COMP pin is compared with the internal oscillator and generates duty cycle modulated signals to control the external power switches.

The system power is controlled by EN pin. When the chip is enabled, the built-in regulator for VCC is powered up and the internal circuit starts.

Brightness Control

MP4651 implements burst dimming (digital brightness) of the LED. The MP4651 has a built-in burst oscillator which can generate a triangle waveform on the BFS pin. Burst dimming can be achieved by either a DC voltage input or external PWM signal.

When burst dimming with a DC input voltage, add a capacitor in parallel with a resistor on BFS pin to set the burst frequency and apply the DC voltage on the PWMIN pin to program the burst duty cycle.

The burst frequency can be synchronized to an external frequency. Applying a synchronizing frequency signal with narrow pulse on SYNC pin can synchronize the burst frequency. The synchronizing frequency should be higher than the burst frequency set by the BFS pin. Please refer to SYNC pin description for details.

When burst dimming with external PWM signal, pull up BFS pin to VCC through a 20kΩ resistor and apply the PWM signal on PWMIN pin.

Fast and High Contrast Ratio PWM Dimming

The MP4651 implements fast and high contrast ratio PWM dimming to the WLED. The PWM dimming signal (controlled by a DC input voltage or direct PWM signal) is outputted on PWMOUT pin to drive the external MOSFET in series with the LEDs, therefore the LED current rises up immediately when PWM dimming signal is effective.

The PWM dimming signal is also used to disconnect the compensation network (on comp pin, a capacitor or a R-C network) from the error amplifier at PWM off interval, and so that the compensation network voltage is hold at this interval and gets nearly immediately to the steady state value when PWM signal is effective. It eliminates the control loop response time and realizes fast dimming.

The MP4651 strictly controls the sequence of the driving signals. Both the sequence of GL and GR signals and the delay time between PWM dimming signal and driving signals are accurately fixed. Therefore, for each time of PWM dimming, the driving signals are exactly the same and so does the output power delivered to the load. It eliminates the possibility of flicker at small PWM dimming pulse and thus realizes the high contrast ratio PWM dimming.

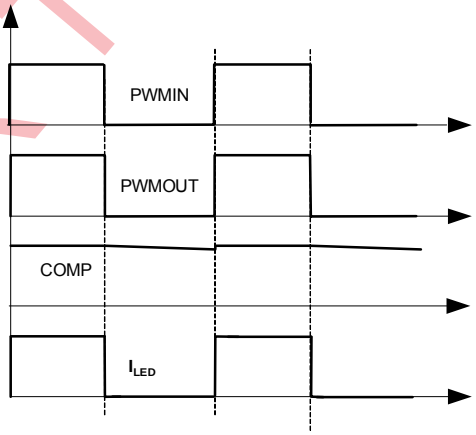

Figure 2—Fast and High Contrast Ratio PWM Dimming

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Fault Protection

System fault management facilities include the over voltage protection, short string protection and a delay timer for system recovery.

The output voltage is monitored by the OVP pin through a voltage divider. Once the voltage on OVP pin exceeds 2.38V for 7us, the MP4651 recognizes this as open condition and triggers Fault Mode.

The SSD pin is used for short string detection. When the voltage on SSD pin gets lower than 2.36V for 7us, the MP4651 recognizes this as short string condition and triggers the Fault Mode.

FB pin also functions as short string protection. When the voltage on FB pin is higher than 1.2V for 7us, the IC triggers the Fault Mode.

At Fault Mode, the outputs of the gate drivers GL and GR are disabled, the PWMOUT signal is pulled down and the COMP capacitor is discharged by a 30uA sourcing current. The fault timer is started. An 8uA current source charges the FT capacitor, and when FT voltage hits 2.38V, system recovers. It enables the output driving signals, releases the COMP, resets the fault flag and pulls down the FT pin.

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APPLICATION INFORMATION

Pin 1 (OVP):

Over Voltage Protection: This pin is used for over voltage protection. The output voltage is monitored by this pin and when the voltage on this pin exceeds 2.38V for 7us, the Fault Mode is triggered.

Pin 3 (SSD):

Short String Detection: This pin is used for short string protection, when the voltage on this pin gets lower than 2.36V for 7us, the IC treats it as short string condition and triggers the Fault Mode.

Pin 4 (FB):

LED Current Feedback. This pin is used for LED current regulation. The voltage on this pin is regulated with 0.6V average value.

FB pin also functions as short sting protection. When the voltage on FB gets higher than 1.2V for 7us, the IC triggers the Fault Mode.

Pin 5 (COMP):

This pin is used for compensation. Connect a 1~47nF capacitor from COMP to GND. This cap should be X7R ceramic. The value of this cap determines the stability of the LED current regulation.

Pin 6 (FT):

Connect a capacitor from this pin to GND to set the fault timer. It sets the time to recover the system when a fault condition is detected.

$$T_{FT} = \frac{2.38V \times C_{FT}}{8uA}$$

A 10nF capacitor on FT sets the delay time around 3ms

Pin 8 (FSET):

Connect a resistor from this pin to GND to set the operating frequency (f_o). The value for this resistor R1 is calculated by

$$R1 = \frac{1.25 \times 10^9}{f_o}$$

For R1 = 25kΩ, operating frequency will be 50kHz.

Pin 7 (PWMOUT):

This pin outputs the burst dimming signal to the LED for fast PWM dimming. Connect this pin directly to the gate of the dimming MOSFET in series of the LED.

Pin 10 (PWMIN):

This pin is used for burst brightness control. For DC input burst dimming, the DC voltage on this pin controls the burst percentage on the output. The signal is filtered for optimal operation. A voltage ranging from 0 to 1.2V on PWMIN programs the burst dimming duty cycle from 0 to 100%.

For direct PWM burst dimming, Pull BFS high to VCC through a 20kΩ resistor and connect PWMIN pin to a logic level PWM signal. Logic High is Burst On and a logic Low is Burst Off.

Pin 9 (BFS):

BFS pin is used to set the burst dimming frequency. Connect a resistor (R_{BFS}) in parallel with a capacitor (C_{BFS}) on this pin to set the burst dimming frequency, as shown in figure 3.

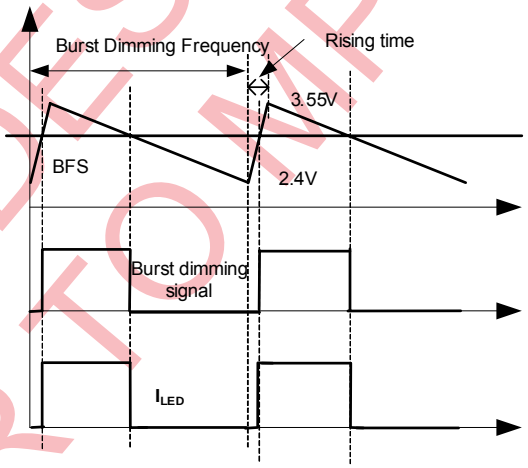

Figure 3—Burst Mode with DC Input Voltage at PWMIN Pin

These values are determined as follows:

Set a percentage of the rising time, where:

$$D_{rise} = t_{rise} \times f_{Burst}$$

R_{BFS} and C_{BFS} are determined by:

$$R_{BFS} \approx 21.16k\left(\frac{1}{D_{rise}} - 1\right) + 21.43k$$

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$$C_{BFS} = \frac{1 - D_{rise}}{f_{Burst} \times R_{BFS} \times 0.405}$$

For D_{rise}= 0.1, f_{Burst} = 200Hz, then R_{BFS} = 212k, C_{BFS} = 52nF

For direct PWM burst dimming, pull BFS high to VCC through a 20kΩ resistor and apply the PWM signal to PWMIN pin.

Pin 2 (SYNC):

Burst frequency synchronization. This pin is used to synchronize the burst dimming frequency. Applying a synchronizing frequency signal with small pulse will synchronize the burst frequency.

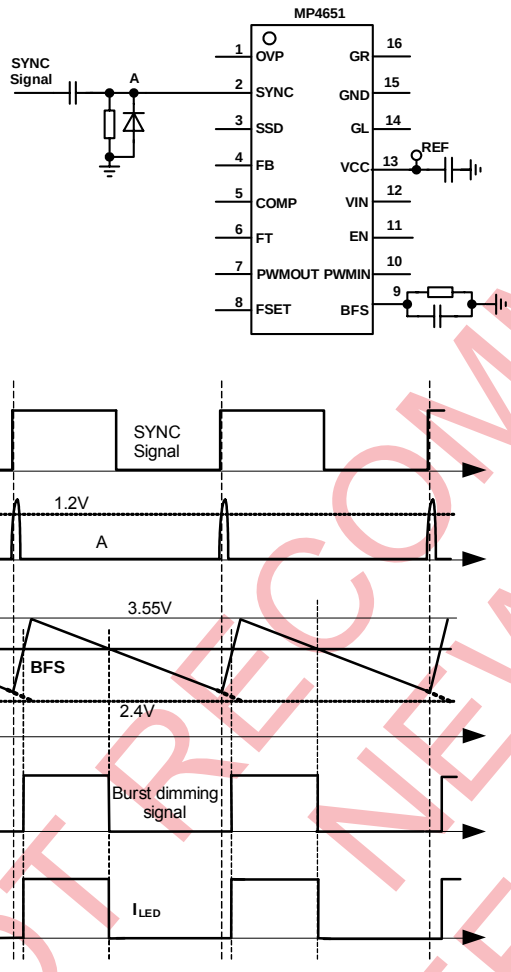

Figure 4—Synchronized DC Input Burst Dimming

Figure 4 shows the synchronized DC input burst dimming. The synchronizing signal is filtered by a high pass filter. Its rising edge is caught and used for synchronizing the triangle waveform on BFS pin. The synchronizing frequency should be higher than that set by BFS pin and the amplitude of the synchronizing signal should be higher than 1.4V.

Table 1—Function Mode

Function	Pin Connection		
	PWM	BFS	SYNC
Burst Mode with DC Input Voltage	0V to 1.2V	C_{BFS}, R_{BFS}	GND
Burst Mode with DC Input Voltage and Synchronizing frequency	0V to 1.2V	C_{BFS}, R_{BFS}	R,C,D network
Burst Mode with External PWM Source	PWM	To VCC through 20kΩ resistor	GND

Burst Brightness Polarity: 100% duty cycle at PWM voltage 1.2V.

Pin 11 (EN):

Pull this pin high to enable the chip, and pull it low to disable the chip.

Pin 12 (VIN):

Supply voltage input. Bypass the supply voltage with a 0.1uF or greater ceramic cap. This cap should be placed close to the IC.

Pin 13 (VCC):

This pin provides the gate driver supply voltage, its typical value is 9.7V. Connect a 1uF or greater ceramic capacitor on this pin to bypass the supply voltage. This voltage is also used to supply the external control circuit.

Pin 14(GL), Pin 16 (GR):

Gate driving signals output. GL and GR are 180 degree phase shifted driving signals. With its enhanced driving capability, GL and GR are able to directly drive the externally MOSFET in the off-line system through a gate driving transformer. Connect two 5Ω resistors in series with GL and GR to reduce the EMI noise.

A 2.2nF Y capacitor is recommended to be placed between the primary reference ground and secondary reference ground.

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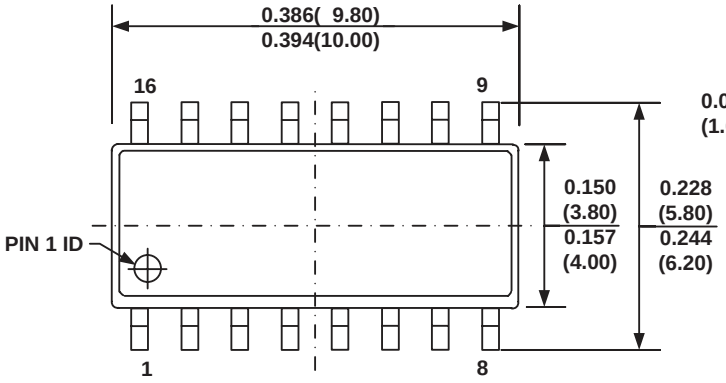
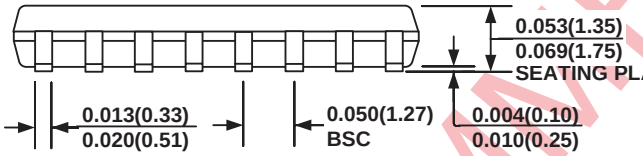
PACKAGE INFORMATION

SOIC16

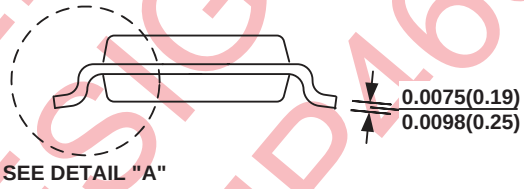


TOP VIEW

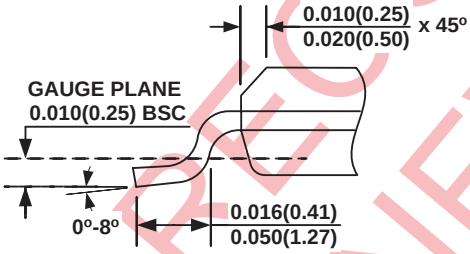
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AC.
6) DRAWING IS NOT TO SCALE.

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