MP4582

100V, 2A, 8µA I_Q, Synchronous Step-Down DC/DC Converter

DESCRIPTION

The MP4582 is an 8µA quiescent current (I_Q), synchronous step-down converter with integrated high-side and low-side MOSFETs (HS-FET and LS-FET, respectively). It supports up to 2A of output current (I_{OUT}) with internal compensation.

High power conversion efficiency across a wide load range is achieved through power-save mode (PSM) and low I_Q under light-load conditions to reduce the switching and gate driver losses.

To achieve a small output ripple at light loads, pull the MODE/SYNC pin high to set the part to forced continuous conduction mode (FCCM). The switching frequency (f_{SW}) is always fixed at 400kHz for all load conditions.

Full protection features include over-current protection (OCP), short-circuit protection (SCP) with hiccup mode, input voltage (V_{IN}) and output (V_{OUT}) over-voltage protection (OVP), and over-temperature protection (OTP).

The MP4582 is available in a QFN-19 (3mmx5mm) package.

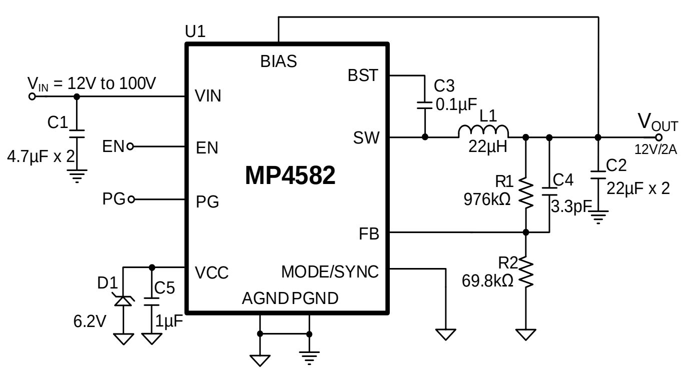
FEATURES

- 4.5V to 100V Input Voltage (V_{IN}) Range
- 8µA Quiescent Current (I_Q)
- Fixed 400kHz Switching Frequency (f_{SW})
- Selectable Power-Save Mode (PSM) or Forced Continuous Conduction Mode (FCCM)
- 0.8V to 35V Output Voltage (V_{OUT}) Range
- 180mΩ/90mΩ Internal MOSFETs
- Power Good (PG) Indication
- Additional BIAS Pin for High-Efficiency VCC (V_{CC}) Regulator
- Internal Loop Compensation and Soft Start (SS)
- Available in a QFN-19 (3mmx5mm) Package

APPLICATIONS

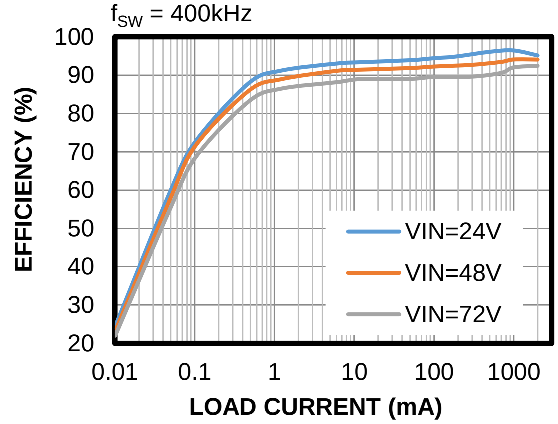
- Power Tools
- Solar Inverters/Optimizers
- Portable Power Stations
- Battery Management Systems (BMS)
- Server Power/Telecom Power Units

TYPICAL APPLICATION



Efficiency vs. Load Current

V_{OUT} = 12V, L = 22µH, DCR = 50mΩ, f_{SW} = 400kHz



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP4582GQVE	QFN-19 (3mmx5mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MP4582GQVE-Z).

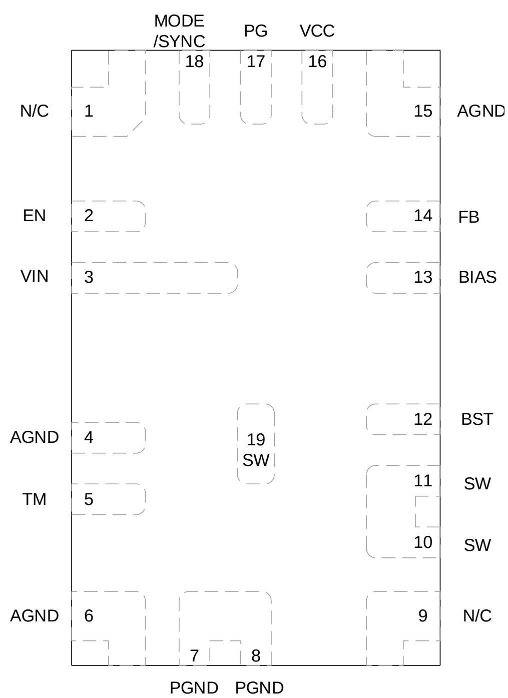
TOP MARKING

MPYW
4582
LLL
E

MP: MPS prefix
Y: Year code
W: Week code
4582: Part number
LLL: Lot number
E: Wettable flank

PACKAGE REFERENCE

TOP VIEW



QFN-19 (3mmx5mm)

PIN FUNCTIONS

Pin #	Name	Description
1, 9	NC	**No connection.** Connect the NC pin to PGND to improve thermal performance.
2	EN	**Power enable pin.** Pull the EN pin high to enable the MP4582; pull it low to disable the MP4582. This pin is floated internally, and must be pulled high or low externally in application.
3	VIN	**Power supply input pin.** Place a decoupling capacitor between the VIN pin and PGND, as close to VIN as possible, to minimize switching spikes.
4, 6, 15	AGND	**Signal ground.** Reference ground of the regulated output voltage (V_{OUT}). Use a single-point connection between AGND and PGND.
5	TM	**Test mode pin.** The TM pin must be floated in application.
7, 8	PGND	**Power ground pin.**
10, 11, 19	SW	**Switch node of converter.** The SW pin is connected to the source of the high-side MOSFET (HS-FET) and the drain of the low-side MOSFET (LS-FET).
12	BST	**Bootstrap power pin.** Connect a 0.1μF capacitor between the BST and SW pins.
13	BIAS	**External power bias supply pin.** It is recommended to connect the BIAS pin to V_{OUT} or another voltage rail if the voltage >4.4V. It is recommended to decouple with one ≥0.1μF ceramic capacitor placed close to the BIAS pin. Float this pin if BIAS is not required.
14	FB	**V_{OUT} feedback pin.** Connect a resistor divider from V_{OUT} to the FB pin.
16	VCC	**Internal 5V LDO output.** The VCC pin supplies power to the internal control circuit. Decouple this pin with a ≥1μF ceramic capacitor. Must connect one 6.2V Zener diode from the VCC pin to AGND.
17	PG	**Power good output pin.** The PG pin's output is an open drain. If enable (EN) under-voltage lockout (UVLO), input voltage (V_{IN}) UVLO, or over-temperature protection (OTP) is triggered, the PG output is pulled low.
18	MODE/ SYNC	**MODE/SYNC pin.** Pull the MODE/SYNC pin low to set the MP4582 to power-save mode (PSM) mode; pull it high to set the MP4582 to forced continuous conduction (FCCM) mode. Apply an external clock to MODE/SYNC to change the switching frequency (f_{SW}).

ABSOLUTE MAXIMUM RATINGS (1)

VIN, EN .... -0.3V to +105V
SW .... -0.3V to V_{IN} + 0.3V
SW (<10ns) .... -4V to V_{IN} + 4V
BIAS .... -0.3V to +14V
BST to SW .... -0.3V to +6.5V
All other pins .... -0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2) (4)
.... 3.9W
Junction temperature (T_J) .... 150°C
Lead temperature .... 260°C
Storage temperature .... -65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .... 4.5V to 100V
Output voltage (V_{OUT}) .... 0.8V to 35V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance	θ_{JA}	θ_{JC}	
EV4582-QVE-00A (4)	32	8	°C/W
QFN-19 (3mmx5mm) (5)	48	38	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on the EV4582-QVE-00A, a 64mmx64mm, 1OZ, 4-layer PCB.
5) The value of θ_{JA} given in this table is only valid for comparison with other packages, and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 48V, T_J = -40°C to +125°C [(6)], typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Input voltage (V_{IN}) under-voltage lockout (UVLO) rising threshold	$V_{IN\_UVLO\_R}$		4	4.2	4.4	V
V_{IN} UVLO threshold hysteresis	V_{IN_HYS}			350		mV
VCC voltage (V_{CC}) UVLO rising threshold	$V_{CC\_UVLO\_R}$	V_{CC} rising	3.7	3.85	4.1	V
V_{CC} UVLO threshold hysteresis	V_{CC_HYS}			350		mV
V_{CC} regulation voltage		V_{IN} = 12V or V_{BIAS} = 12V, 5mA	4.5	4.85	5.1	V
		V_{IN} = 4.5V, 4mA		4.1		V
		BIAS voltage (V_{BIAS}) = 4.5V, 4mA		4.3		V
BIAS power supply threshold		V_{BIAS} rising, override V_{IN} supply		4.25	4.4	V
		V_{BIAS} falling, recover to V_{IN} supply		4.05	4.2	V
Supply Current						
Shutdown current	I_{SD}	EN voltage (V_{EN}) = 0V, measured on the VIN pin		1		μA
Quiescent current	I_Q	FB voltage (V_{FB}) = 0.82V, V_{BIAS} = 0V, V_{BST} = 5V, no switching, measured on the VIN pin, T_J < 85°C		8	12	μA
		V_{FB} = 0.82V, V_{BIAS} = 5V, V_{BST} = 5V, no switching, measured on the VIN pin		0.5		μA
		V_{FB} = 0.82V, V_{BIAS} = 5V, V_{BST} = 5V, no switching, measured on the BIAS pin, T_J < 85°C		8	12	μA
Enable (EN) Control						
EN input high threshold	V_{EN_ON}	V_{EN} rising	1.1	1.2	1.3	V
EN hysteresis	V_{EN_H}	V_{EN} rising		225		mV
EN input current	I_{EN}	V_{EN} = 5V		0		μA
EN turn-on delay		EN on to MOSFET switching		700		μs
Switching Frequency						
Switching frequency	f_{SW}		360	400	440	kHz
Minimum off time [(7)]	t_{MIN_OFF}			120		ns
Minimum on time [(7)]	t_{MIN_ON}			40		ns
Reference Voltage						
Feedback (FB) reference voltage	V_{REF}	4.5V to 100V, T_J = 25°C	0.792	0.8	0.808	V
		4.5V to 100V, T_J = -40°C to +125°C	0.788	0.8	0.812	V
FB input current	I_{FB}	V_{FB} = 1.05V	-100	-50	-10	nA
Internal soft-start time	t_{SS}	10% to 90% of V_{REF}		3.7		ms

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 48V, T_J = -40°C to +125°C (6), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
FB under-voltage protection (UVP) threshold	V_{UVP}		55%	60%	65%	V_{REF}
FB over-voltage protection (OVP) threshold	V_{OVP}		105%	108%	111%	V_{REF}
FB OVP recovery hysteresis				1%		V_{REF}
MODE/SYNC Setting						
MODE/SYNC input signal high voltage	V_{MODE_H}		1.3			V
MODE/SYNC input signal low voltage	V_{MODE_L}				0.8	V
Clock SYNC range	f_{SYNC_RANGE}	Add an external clock	400		2200	kHz
Power MOSFET						
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_L}$			90		mΩ
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_H}$			180		mΩ
Current Limit						
High-side (HS) peak current limit	I_{H_LIMIT}		2.75	3.1	3.65	A
Low-side (LS) valley current limit	I_{L_LIMIT}		1.8	2.1	2.5	A
Inductor current (I_L) zero-current detection (ZCD) threshold	I_{ZCD}			50		mA
Power Good (PG)						
PG upper threshold		FB rising, PG falling	105%	108%	111%	V_{FB}
		FB falling, PG rising	104%	107%	110%	V_{FB}
		Hysteresis		1%		V_{FB}
PG lower threshold		FB falling, PG falling	89%	92%	95%	V_{FB}
		FB rising, PG rising	90%	93%	96%	V_{FB}
		Hysteresis		1%		V_{FB}
PG low-to-high delay				380		us
PG high-to-low delay				150		us
PG sink current capability		Sink 4mA			0.4	V
PG leakage current		V_{PG} = 5V		1		µA
Thermal Protection (7)						
Thermal shutdown rising threshold	T_{SD}			150		°C
Thermal shutdown hysteresis	T_{SD-HYS}			20		°C

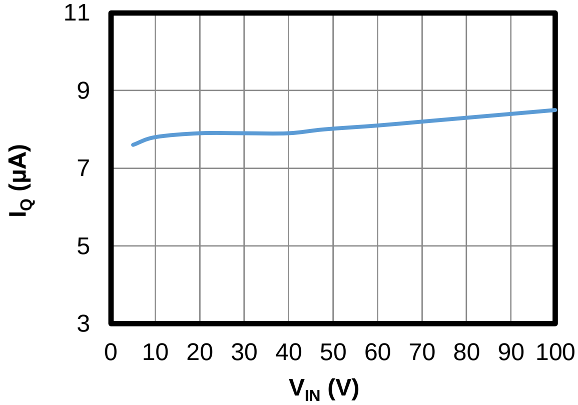
Notes:

6) Not tested in production. Guaranteed by over-temperature correlation.
7) Guaranteed by engineering sample characterization.

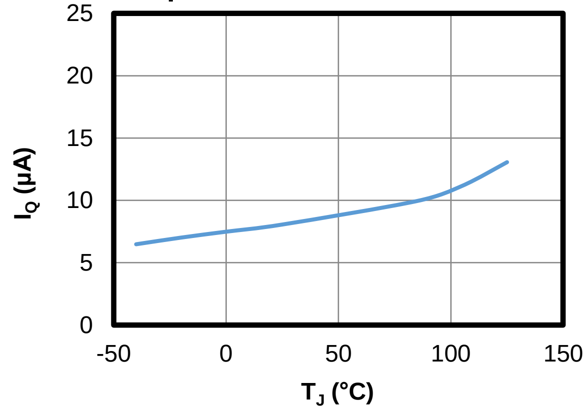
TYPICAL CHARACTERISTICS

V_{IN} = 48V, T_A = 25°C, unless otherwise noted.

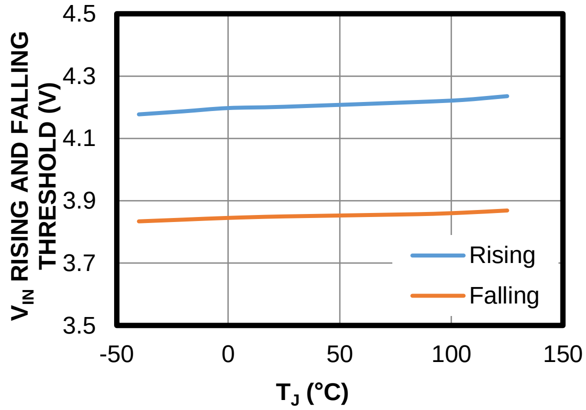
Quiescent Current vs. Input Voltage



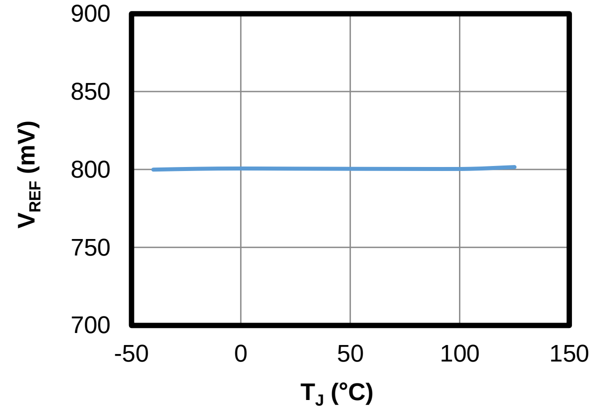
Quiescent Current vs. Junction Temperature



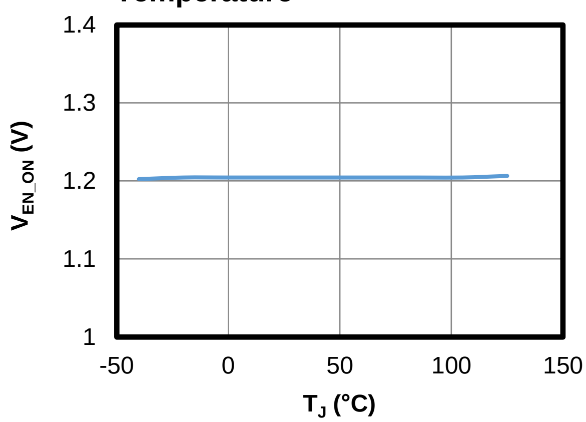
V_{IN} Rising and Falling Threshold vs. Junction Temperature



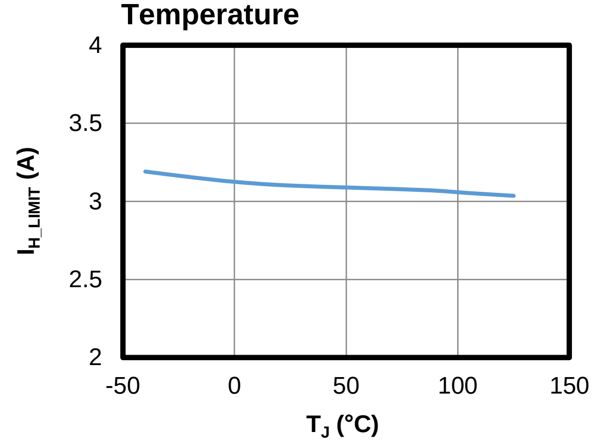
Feedback Reference Voltage vs. Junction Temperature



EN Threshold vs. Junction Temperature

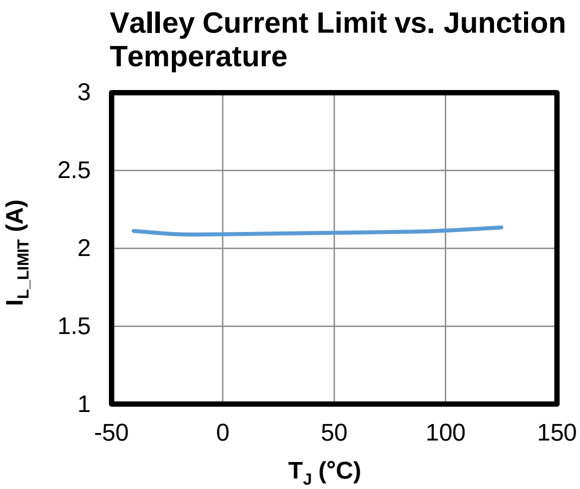


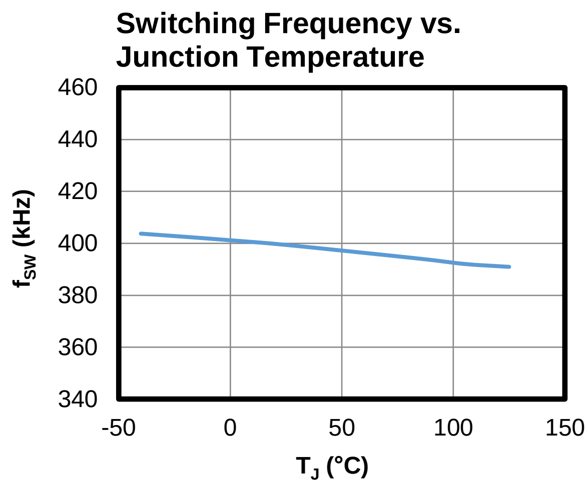
Peak Current Limit vs. Junction Temperature



TYPICAL CHARACTERISTICS *(continued)*

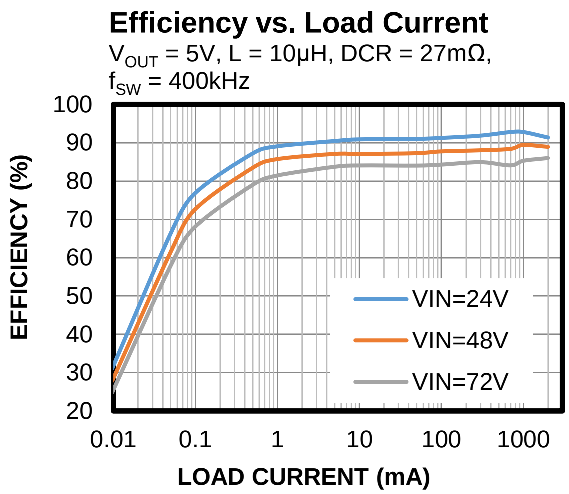
V_{IN} = 48V, T_A = 25°C, unless otherwise noted.

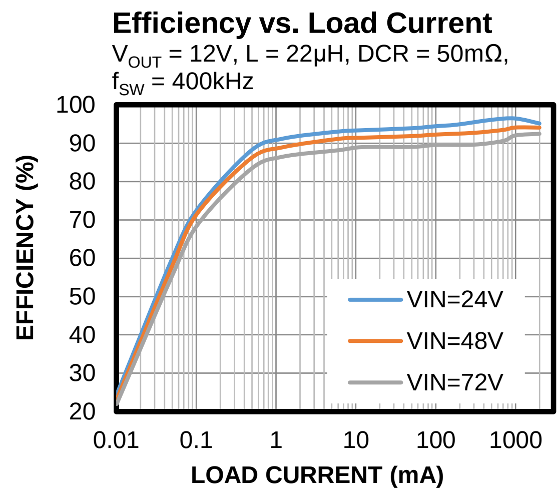


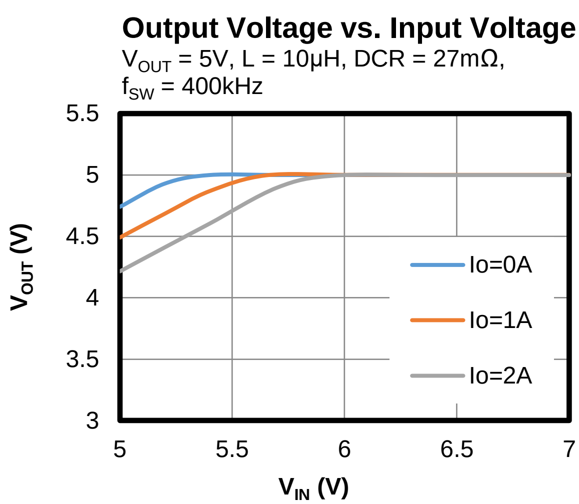


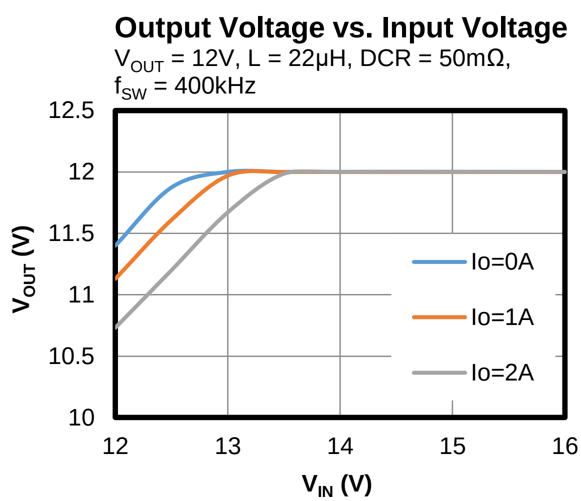
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 48V, V_{OUT} = 12V, L = 22μH, T_A = 25°C, unless otherwise noted.







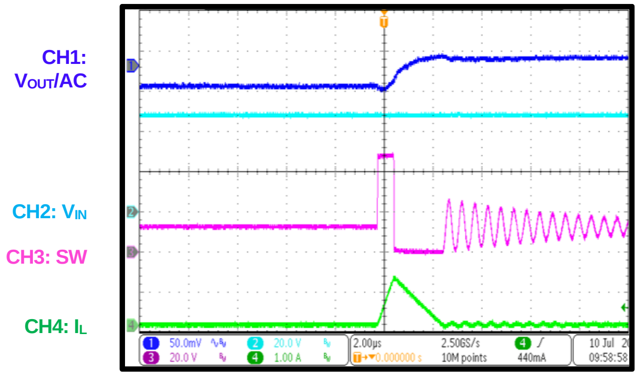


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 48V, V_{OUT} = 12V, L = 22µH, T_A = 25°C, unless otherwise noted.

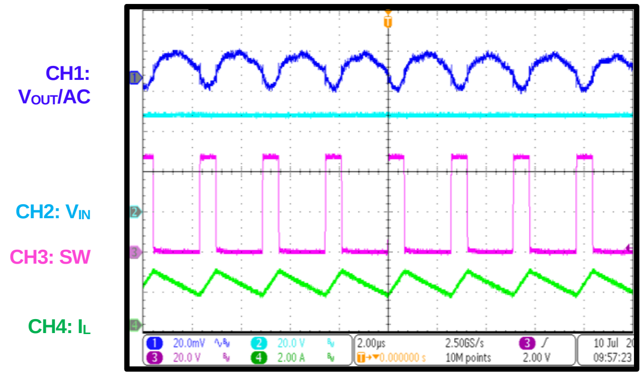
Steady State

I_{OUT} = 0A



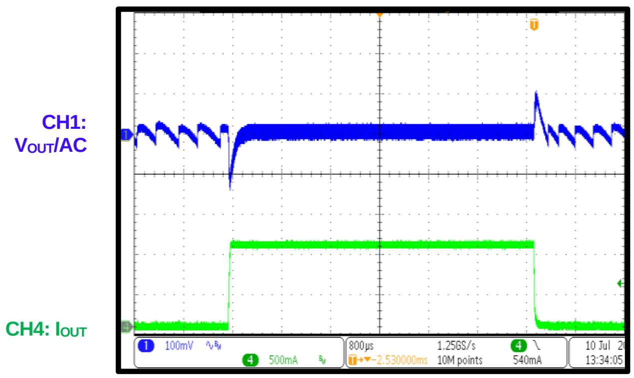
Steady State

I_{OUT} = 2A



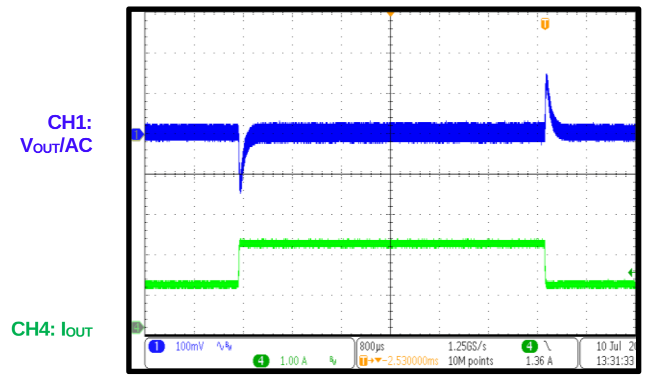
Load Transient Response

I_{OUT} = 0A to 1A



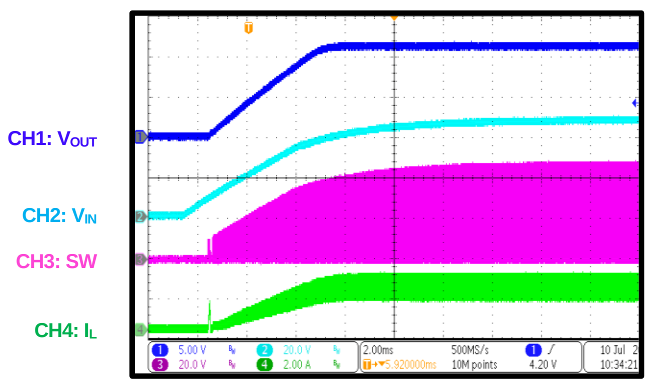
Load Transient Response

I_{OUT} = 1A to 2A



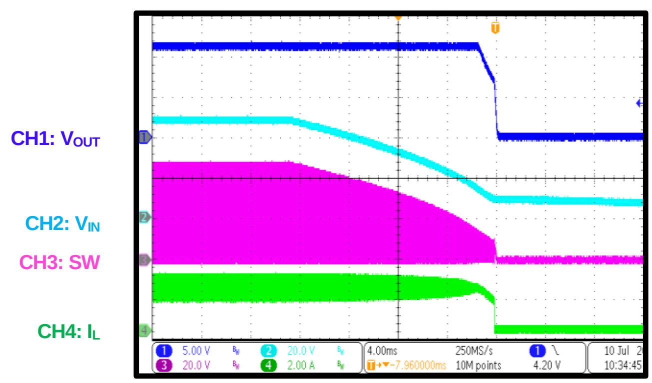
Start-Up through VIN

I_{OUT} = 2A



Shutdown through VIN

I_{OUT} = 2A

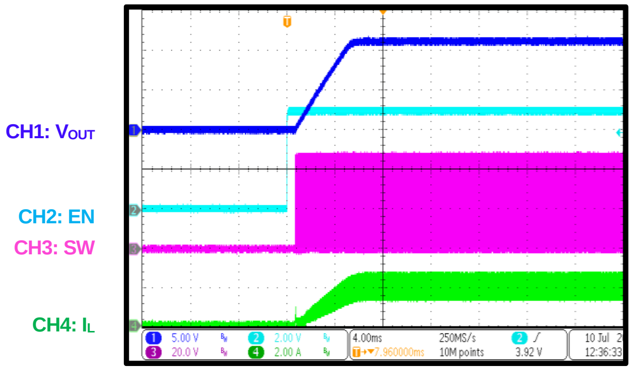


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 48V, V_{OUT} = 12V, L = 22µH, T_A = 25°C, unless otherwise noted.

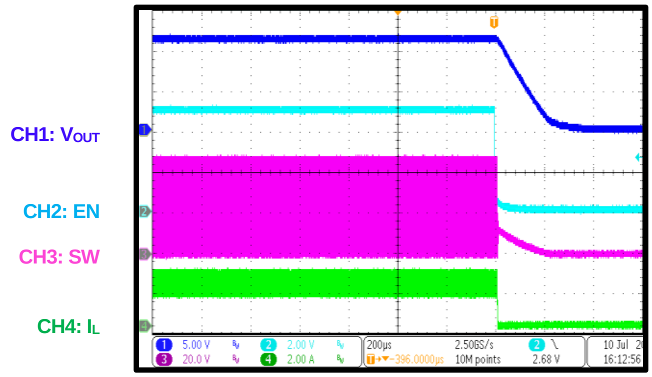
Start-Up through EN

I_{OUT} = 2A



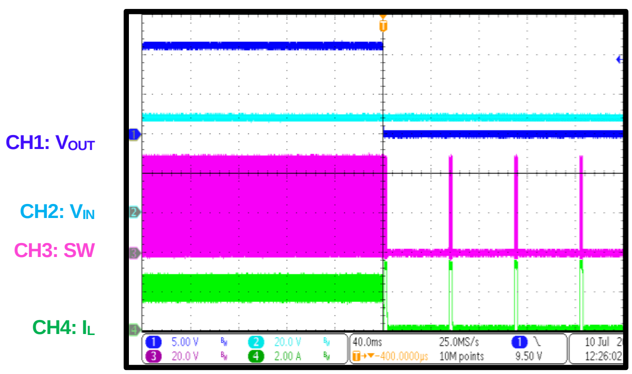
Shutdown through EN

I_{OUT} = 2A



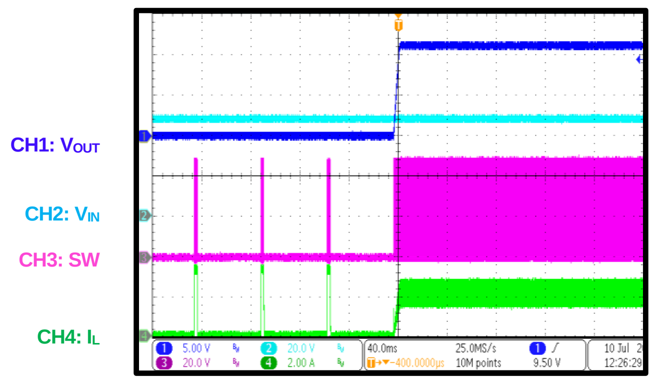
SCP Entry

I_{OUT} = 2A to SCP



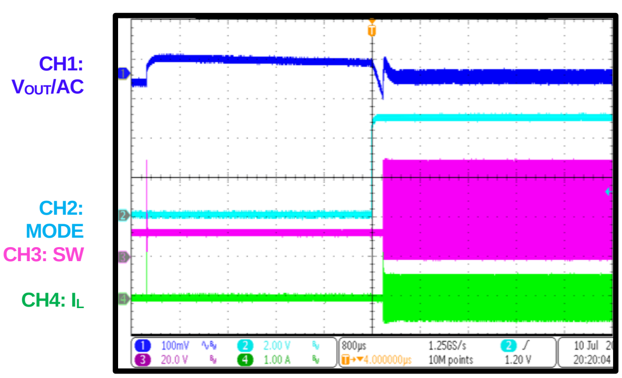
SCP Recovery

I_{OUT} = SCP to 2A



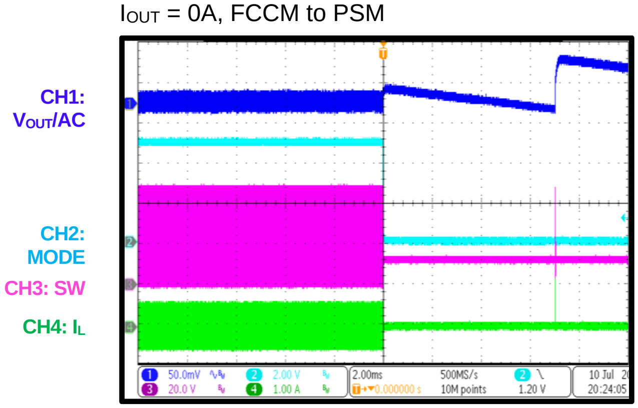
Mode Transient

I_{OUT} = 0A, PSM to FCCM



Mode Transient

I_{OUT} = 0A, FCCM to PSM



FUNCTIONAL BLOCK DIAGRAM

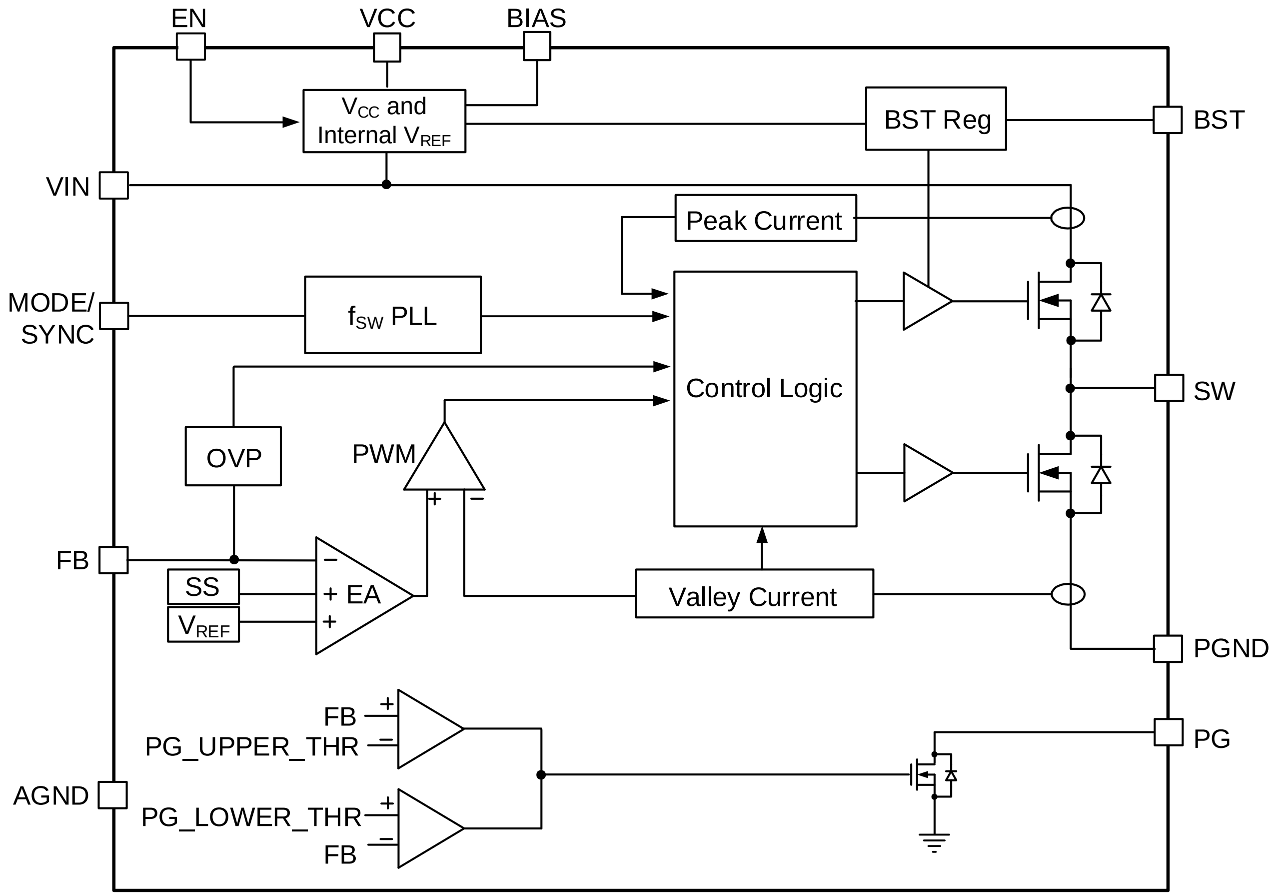


Figure 1: Functional Block Diagram

OPERATION

The MP4582 is a synchronous, step-down, switching converter with integrated high-side and low-side power MOSFETs (HS-FET and LS-FET, respectively). It provides a highly efficient solution with internal compensation, featuring a wide input voltage (V_{IN}) range, internal soft-start (SS) control, and precise current limiting. Its low operational quiescent current (I_Q) makes it suitable for high efficiency in light-load applications. Figure 1 on page 11 shows the internal block diagram, and the following sections describe the MP4582's detailed functionality.

Buck Operation

The MP4582 works in fixed-frequency, valley current control mode to regulate the output voltage (V_{OUT}). At the beginning of each cycle, the HS-FET turns on once the feedback (FB) voltage (V_{FB}) drops below the reference voltage (V_{REF}). Once the HS-FET turns off, the LS-FET turns on to conduct the inductor current (I_L) until it triggers the COMP control signal. By repeating operation in this way, the MP4582 regulates V_{OUT}. When the HS-FET switches off, it remains off for at least 120ns before the next cycle begins.

If the current in the LS-FET does not trigger the error amplifier (EA) output value within one pulse-width modulation (PWM) period, the LS-FET remains on until the EA output value is triggered. Then the HS-FET turns on again.

If the HS-FET and LS-FET are turned on at the same time, a dead short occurs between the VIN and PGND pins. This is called shoot-through. To avoid shoot-through, a dead time is generated internally between the HS-FET and LS-FET on and off periods. The dead time occurs between the HS-FET off time and the LS-FET on time, or vice versa.

Heavy-Load Operation

The MP4582 operates in continuous conduction mode (CCM) when the output current (I_{OUT}) is high and I_L is above 0A. In CCM, the HS-FET turns on, then turns off once the on period is complete. Once the HS-FET turns off, the LS-FET turns on to conduct I_L. The part operates in PWM mode when the switching frequency (f_{SW}) remains constant while the part is in CCM.

Light-Load Operation

The MP4582 can work in power-save mode (PSM) under light-load conditions. In PSM, the LS-FET goes into tri-state (Hi-Z) when I_L drops close to 0A, and the output capacitors discharge slowly to GND through the FB pin's resistor. If V_{OUT} drops and the internal EA output voltage rises, the MP4582 starts the next switching cycle by turning on the HS-FET. The MP4582 automatically reduces f_{SW} and I_Q when the device is not switching. This improves the device's efficiency when I_{OUT} is low. When in PSM under light-load conditions, the HS-FET does not turn on as frequently as it does under heavy-load conditions. The frequency at which the HS-FET turns on is a function of I_{OUT}. As I_{OUT} increases, the HS-FET turns on more frequently. In turn, f_{SW} also increases. I_{OUT} exceeds the upper boundary level when the valley I_L reaches 0A.

VCC Power Supply

The MP4582's control circuit is powered by the VCC pin, which is regulated by V_{IN} and BIAS. VCC requires one ≥1μF, 16V ceramic capacitor and one 6.2V Zener diode connected from VCC to AGND for proper operation.

The V_{CC_UVLO} and V_{IN_UVLO} thresholds protect the chip from operating at an insufficient supply voltage. The MP4582's under-voltage lockout (UVLO) comparator monitors V_{IN} and V_{CC}. When both V_{IN} and V_{CC} are high enough, the device begins operation.

When V_{IN} exceeds V_{IN_UVLO} and EN is high, the MP4582 regulates V_{CC} from V_{IN} first. If BIAS is exceeds its 4.25V typical value and V_{IN} is above its UVLO threshold, the MP4582 switches the power source from V_{IN} to BIAS to achieve higher efficiency for internal driver loss. BIAS requires one ≥0.1μF ceramic capacitor for decoupling. If V_{OUT} is above 14V, a Zener diode is required to decrease V_{OUT} for the BIAS pin's power supply by inserting the Zener diode between V_{OUT} and the BIAS pin.

Start-Up

When the EN pin is high and V_{CC} and V_{IN} have exceeded their respective UVLO thresholds, the MP4582 starts up via an internal soft start (SS) signal. Once the MP4582 starts switching, the SS signal ramps up from 0V and is compared to V_{REF}. The lower voltage feeds the EA to control V_{OUT}. After the SS signal exceeds V_{REF}, SS completes and the internal reference block takes charge of the FB loop regulation. The MP4582 is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, neither the HS-FET nor LS-FET turns on until the soft-start voltage (V_{SS}) exceeds V_{FB}.

Enable (EN) and Configurable Under-Voltage Lockout (UVLO)

The EN pin turns the MP4582 on and off. When the EN voltage (V_{EN}) rises to the EN high threshold, the MP4582 enables all functions and starts switching. Once V_{EN} falls below its lower threshold, switching is disabled. EN is compatible with voltages up to 100V.

There is no internal resistor on EN. For automatic start-up, connect EN to V_{IN} through a resistor.

MODE/SYNC Control

Pull the MODE/SYNC pin low to set the MP4582 to PSM; pull MODE/SYNC high to set it to FCCM. PSM and FCCM can transition back and forth when the MP4582 is switching. Connect an external clock to sync the internal f_{SW} from 400kHz to 2.2MHz (sync the SW rising to the external signal's rising edge).

Switching Current Limit

The MP4582 supports a cycle-by-cycle switching current limit. When the LS-FET is on, I_L is monitored. If the sensed I_L exceeds the valley current limit threshold (I_{L_LIMIT}, 2.1A), the HS-FET waits until I_L falls below the valley current limit to turn on again (see Figure 2).

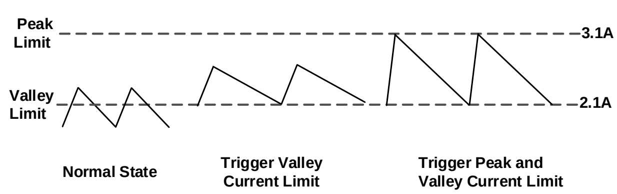


Figure 2: Current Limit Schematic

The MP4582 also supports a switching peak current limit during the HS-FET on period. When the peak current limit is triggered, the HS-FET shuts down immediately and the LS-FET turns on after a dead time. The HS-FET turns on again during the next switching period.

Overload Protection and Short-Circuit Protection (SCP)

During an overload or output short-circuit condition, V_{OUT} drops due to the cycle-by-cycle switching current limit. Once V_{FB} drops below the under-voltage (UV) threshold, the MP4582 enters hiccup mode to periodically restart the part. During the SS time (t_{SS}), hiccup mode is disabled.

During hiccup over-current protection (OCP), the MP4582 turns off the output power stage and discharges the SS capacitor (C_{SS}). Then the IC automatically initiates another SS. If the over-current (OC) condition remains after SS ends, the device repeats this hiccup operation until the OC condition is removed. Once the OC condition has been removed, V_{OUT} returns to its regulation level.

Input Over-Voltage Protection (OVP)

The MP4582 constantly monitors V_{IN}. If V_{IN} exceeds the V_{IN} over-voltage protection (OVP) threshold (about 103V) due to negative I_L, the controller switches from FCCM to discontinuous conduction mode (DCM). Once V_{IN} drops to a normal voltage (about 100V), the MP4582 recovers and resumes normal operation.

Output OVP

The MP4582 constantly monitors V_{OUT}. If V_{OUT} exceeds 108% of the V_{REF} threshold, the HS-FET turns off immediately and the V_{OUT} discharge function turns on (via a 1kΩ resistor between SW and PGND). Once V_{OUT} drops to a normal voltage (less than 107% of V_{REF}), the MP4582 recovers and resumes normal operation.

Bootstrap (BST) Power Supply

An external bootstrap (BST) capacitor (C_{BST}) powers the floating power MOSFET driver. This floating driver has its own UVLO protection. V_{CC} regulates the C_{BST} voltage (V_{BST}) internally through D1, M1, C3, L1, and C2 (see Figure 3

on page 14). If (V_{IN} - V_{SW}) exceeds 5V, then U1 regulates M1 to maintain a 5V V_{BST} across C3.

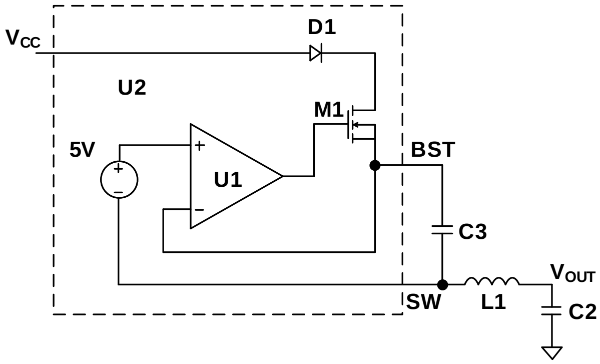


Figure 3: Internal Bootstrap Charger

Thermal Protection

The MP4582 has one temperature-monitoring circuit. If the junction temperature (T_J) exceeds 150°C, the MP4582 shuts down. Once the temperature drops below 130°C, the device resumes normal operation.

Power Good (PG)

The power good (PG) signal indicates whether V_{OUT} is within its normal range compared to the internal V_{REF}. The PG pin is an open-drain output.

When V_{OUT} is above 93% and below 107% of the internal V_{REF} and the SS is complete, the PG signal is pulled high. When the V_{OUT} is below 92% or above 108% of the internal V_{REF} after SS completes, the PG signal is pulled low.

The PG output is also pulled low if EN UVLO, V_{IN} UVLO, or OTP is triggered.

APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

The external resistor divider is used to set V_{OUT}. First, choose a value for the resistor (R1). Too small of a value for R1 can lead to considerable I_Q loss, while too large of a value can make FB noise-sensitive. It is recommended to choose an R1 value between 100kΩ and 1MΩ. Then R2 can be calculated with Equation (1):

$$R2 = \frac{R1}{\frac{V_{OUT}}{V_{REF}} - 1} \quad (1)$$

Where V_{REF} is the reference voltage (typically 0.8V).

Figure 4 shows a typical feedback circuit.

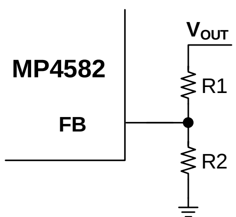


Figure 4: Feedback Network

Selecting the Inductor

A larger-value inductor provides less ripple current, which results in a lower V_{OUT} ripple (ΔV_{OUT}). However, a larger-value inductor also has a larger physical footprint, higher series resistance, and lower saturation current. The inductance (L) can be calculated with Equation (2):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (2)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

It is recommended to choose an inductor ripple current range of 30% to 60% of the maximum I_{OUT}. The inductor should not saturate under the maximum peak inductor current. The peak inductor current (I_{L_PEAK}) can be calculated with Equation (3):

$$I_{L\_PEAK} = I_{OUT} + \frac{V_{OUT}}{2 \times f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (3)$$

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the step-down converter while maintaining the DC V_{IN}. For the best results, it is recommended to use ceramic capacitors placed as close to VIN as possible. X5R and X7R capacitors with ceramic dielectrics are recommended for their stability amid temperature fluctuations.

The capacitors must also have a ripple current rating above the converter's maximum input ripple current. The input ripple current (I_{CIN}) can be estimated with Equation (4):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (4)$$

The worst-case scenario occurs at V_{IN} = 2 x V_{OUT}, calculated with Equation (5):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (5)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance (C_{IN}) determines the converter's V_{IN} ripple (ΔV_{IN}). If there is a ΔV_{IN} requirement in the system, choose C_{IN} to meet the relevant specifications. ΔV_{IN} can be estimated with Equation (6):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

The worst-case scenario occurs at V_{IN} = 2 x V_{OUT}, calculated with Equation (7):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (7)$$

Selecting the Output Capacitor

The output capacitor (C_{OUT}) is required to maintain the DC V_{OUT}. It is recommended to use ceramic or POSCAP capacitors.

ΔV_{OUT} can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right) \quad (8)$$

With ceramic capacitors, the capacitance dominates the impedance at f_{SW} and causes the majority of ΔV_{OUT}. For simplification, ΔV_{OUT} can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f^2_{SW} \times C_{OUT} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

With POSCAP capacitors, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (10)$$

Selecting a larger-value C_{OUT} provides faster load transient response. However, the maximum C_{OUT} limit should be also considered when designing for application. If the output capacitance is too high, V_{OUT} cannot reach the desired value during t_{SS}, and the capacitor fails to regulate. The maximum output capacitor value (C_{OUT_MAX}) can be estimated with Equation (11):

$$C_{OUT\_MAX} = (I_{LIM\_AVG} - I_{OUT}) \times t_{SS} / V_{OUT} \quad (11)$$

Where t_{SS} is the SS time, and I_{LIM_AVG} is the average start-up current during SS. I_{LIM_AVG} can be approximately estimated with Equation (12):

$$I_{LIM\_AVG} \approx I_{L\_LIMIT} + \Delta I_L / 4 \quad (12)$$

Where I_{L_LIMIT} is the valley current limit, and ΔI_L is the inductor ripple current.

Design Example

Table 1 shows a design example following the application guidelines for the provided specifications.

Table 1: Design Example

V_{IN}	12V to 100V
V_{OUT}	12V/2A
f_{SW}	400kHz

Figure 6 and Figure 7 on page 17 show the detailed application schematics. For the typical performance and circuit waveforms, see the Typical Performance Characteristics section on page 8. For more device applications, refer to the related evaluation board datasheet.

PCB Layout Guidelines

Efficient layout is critical for stable operation. For the best results, refer to Figure 5 and follow the guidelines below:

1. Place the high-current paths (PGND, VIN, and SW) as close to the device as possible using short, direct, and wide traces.
2. Place the input capacitor (C_{IN}) as close to the VIN and PGND pins as possible.
3. Place the external FB resistors close to the FB pin.
4. Keep the switching node (SW) short, and as far away from the FB network as possible.
5. Connect the NC pin to PGND, and place as many vias as possible next to the PGND and NC pins for better thermal performance.

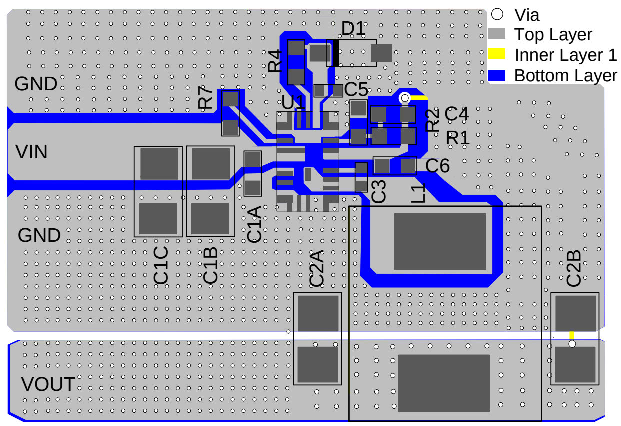


Figure 5: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

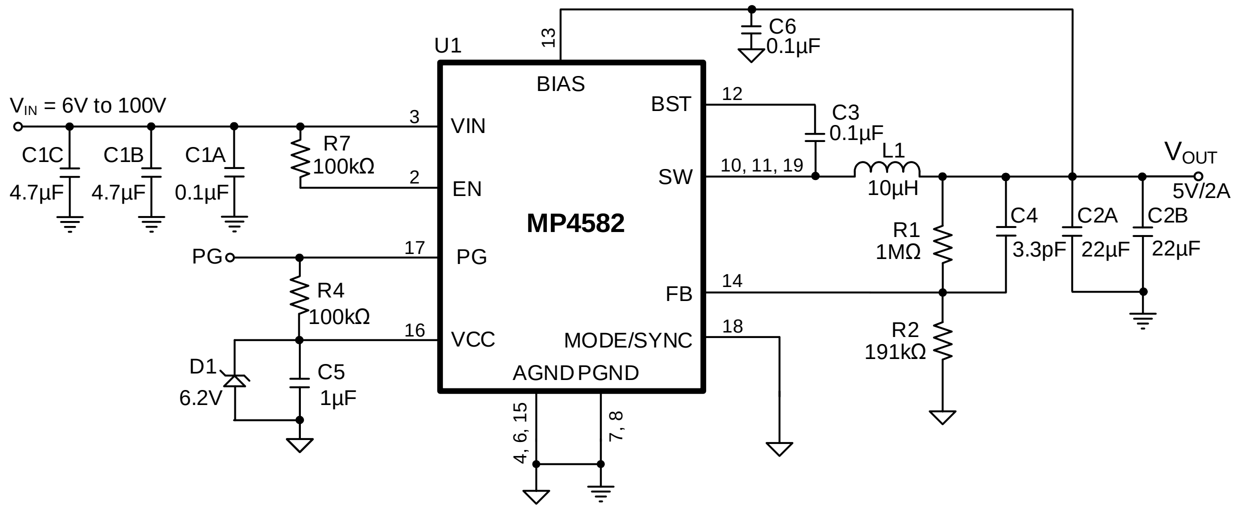


Figure 6: Typical Application Circuit (5V Output)

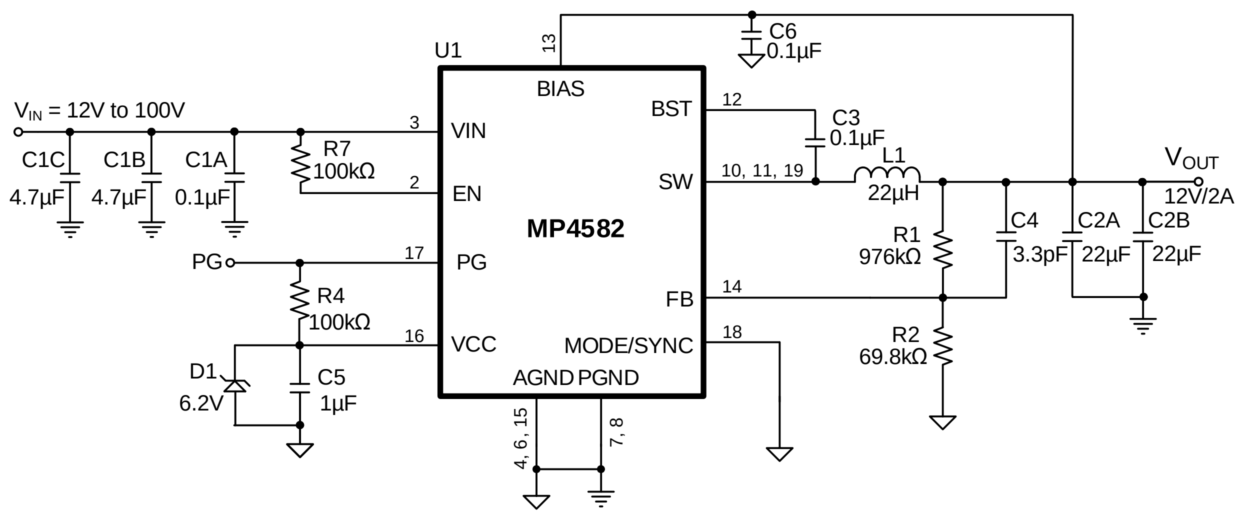
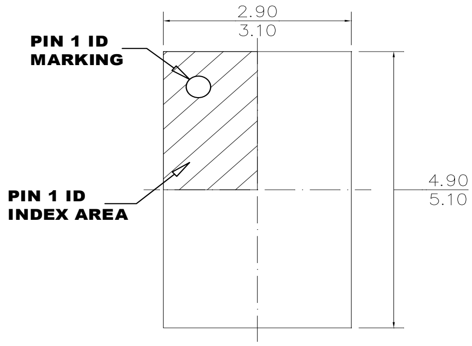


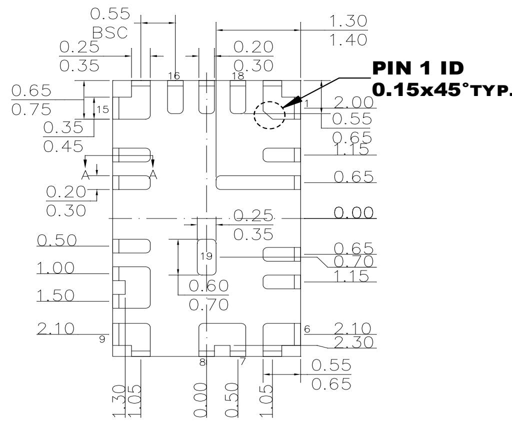
Figure 7: Typical Application Circuit (12V Output)

PACKAGE INFORMATION

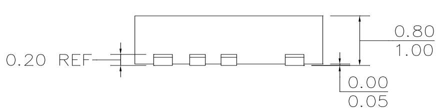
QFN-19 (3mmx5mm)



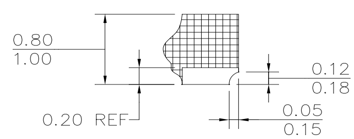
TOP VIEW



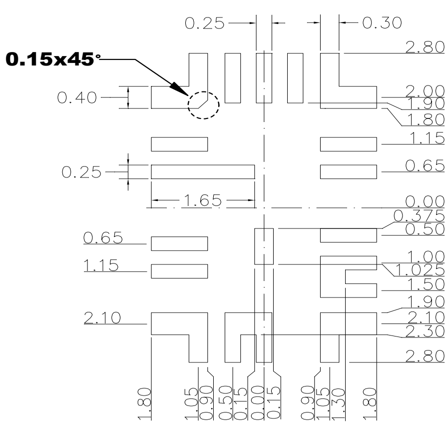
BOTTOM VIEW



SIDE VIEW



SECTION A-A

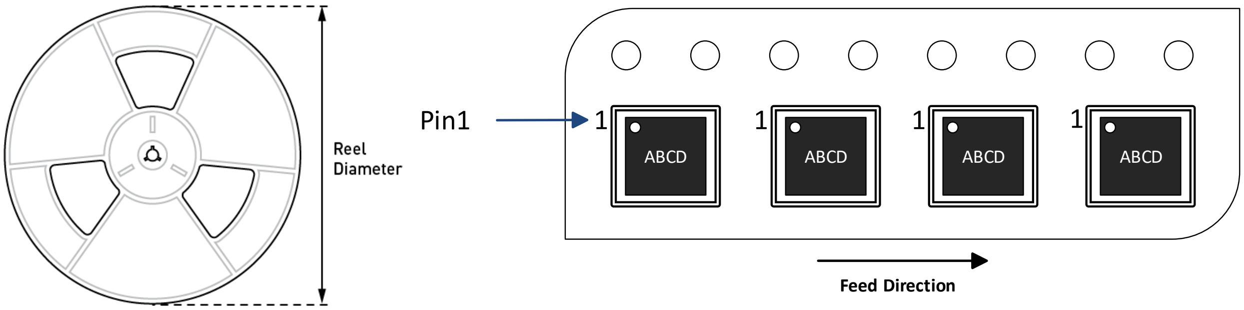


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP4582GQVE-Z	QFN-19 (3mmx5mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/11/2025	Initial Release	-