The Future of Analog IC Technology

MP4059

Single-Stage PFC Flyback Controller with Primary-Side Feedback, for LED Drivers Down to 1% Dimming

DESCRIPTION

The MP4059 is a single-stage PFC flyback controller for LED deep-dimming applications. The MP4059 can regulate constant current to an LED load over a wide 1% to 100% dimming range without flickering or shimmering. The MP4059 is a primary-side controller without any secondary-side feedback components or optocouplers, simplifying the LED driver design significantly. The MP4059 integrates power factor correction and works in valley switching mode to achieve high efficiency.

The MP4059 achieves ultra-low power consumption and can shut off the LED in standby mode, making it suitable for smart lighting applications.

The MP4059's multiple protection features enhance system reliability and safety greatly. Protection features include over-voltage protection (OVP), short-circuit protection (SCP), primary-side over-current protection (OCP), brown-out protection, cycle-by-cycle current limit protection, under-voltage lockout (UVLO), and auto-restart over-temperature protection (OTP).

The MP4059 is available in a SOIC-8 package.

FEATURES

- 1% to 100% PWM Dimming Range
- Ultra-Low Standby Loss, Typically Less than 50mW at $230V_{AC}$
- Universal Input
- Fast Start-Up
- No Flicker
- Low Audible Noise
- Valley Switching Mode for Good Efficiency
- Good PF (Typically >0.9)
- Primary-Side Over-Current Protection (OCP)
- Output Over-Voltage Protection (OVP)/Short-Circuit Protection (SCP)
- Under-Voltage Lockout (UVLO)
- Thermal Shutdown (160°C/100°C)
- Available in a SOIC-8 Package

APPLICATIONS

- LED PWM Dimming

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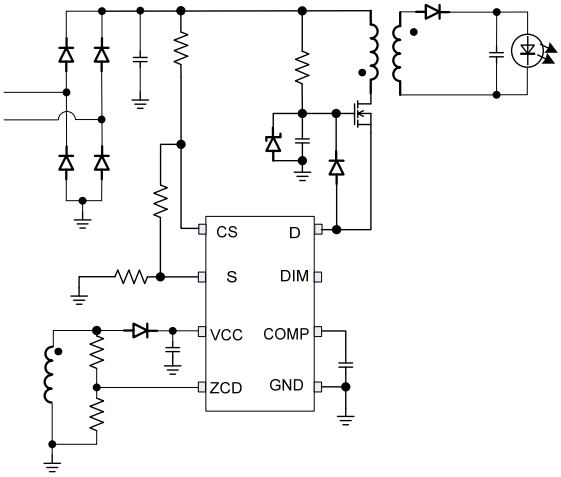
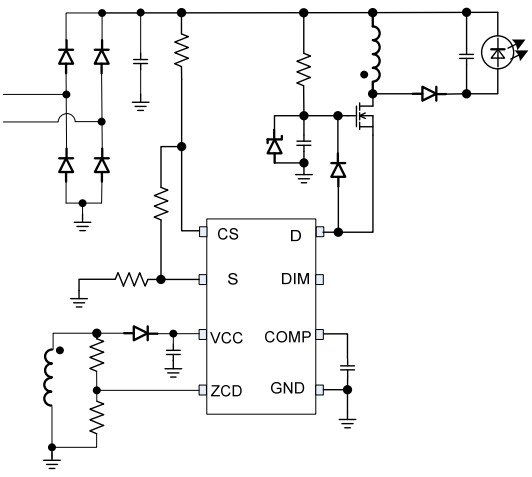
TYPICAL APPLICATION



Isolated Flyback Application



Non-Isolated Buck-Boost Application

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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP4059GS	SOIC-8	*See Below*

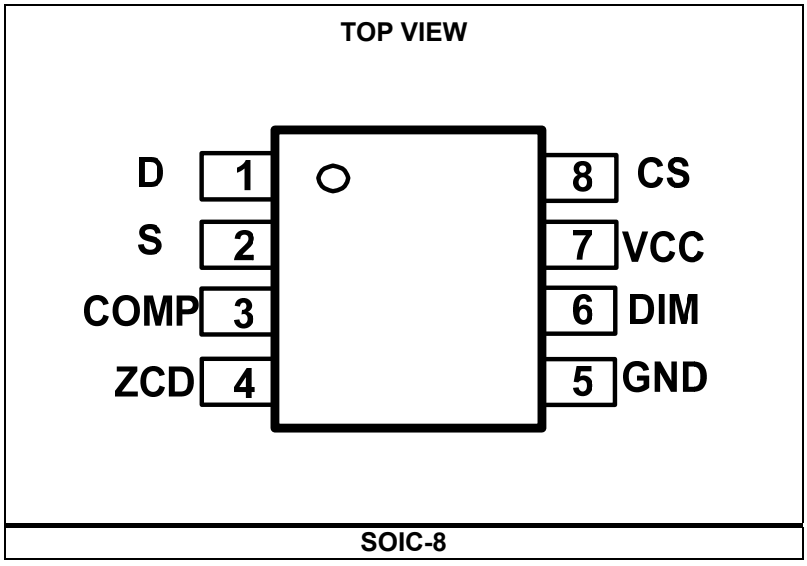
* For Tape & Reel, add suffix –Z (e.g.: MP4059GS–Z).

TOP MARKING

MP4059
LLLLLLLL
MPSYWW

MP4059: Part number
LLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code

PACKAGE REFERENCE



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ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (VCC) ..... -0.3V to 28V
ZCD ..... -0.3V to 6.5V
Low-side MOSFET drain-to-source voltage ..... -0.7V to 28V
All other pins ..... -0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2)
SOIC-8 ..... 1.3W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (VCC) ..... 6V to 27V
Operating junction temp. (T_J) ..... -40°C to 125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
SOIC-8	96	45	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

Typical values are tested at VCC = 12V, T_A = +25°C, unless otherwise noted. Minimum and maximum values are at VCC = 12V, T_J = -40°C~ + 125°C, unless otherwise noted, guaranteed by characterization.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Voltage VCC Section						
Operating range	VCC	After turn on	6		27	V
VCC LFM level: LFM is triggered	VCC_{LFM}	VCC falling edge	7.95	8.25	8.5	V
VCC regulate value at CV	$VCC_{regulate}$		7.1	7.5	7.9	V
VCC upper level: internal charging stops and IC turns on	VCC_H	VCC rising edge	10	10.5	11	V
VCC lower level: internal charging circuit triggers	VCC_L	VCC falling edge	5.2	5.5	5.8	V
VCC hysteretic	$VCC_{_HYS}$			5		V
Supply Current						
VCC charging current from D	$I_{D\text{-}charge}$	V_D = 16V, VCC = 10.5V	3.7	5.7	7.2	mA
Operating current	$I_{operating}$	CV, VCC=7.8V,COMP = V_{COMP_L}		100		µA
		Switch frequency is 60kHz, CC operation	370	440	620	µA
Operating current under fault condition	I_{fault}	Fault condition, IC latch, VCC = 15V	205	265	360	µA
Pull-down current during UVLO	$I_{pull_down_UVLO}$	VCC = 5V	0.85	1.25	1.8	mA
Leakage current on D	$I_{leakage\text{-}D}$	Refer operation current test condition V_D = 30V			1	µA
DIM Section						
High level	V_{dim_H}		1.08	1.2	1.33	V
Low level	V_{dim_L}		0.26	0.3	0.33	V
Maximum DIM detect time, to determine the frequency of PWM dimming signal	t_{dim_detect}	PWM dimming frequency should be higher than 200Hz	8	9.4	12	ms
Error Amplifier (EA)						
Feedback voltage	V_{FB}		0.186	0.193	0.2	V
Transconductance @ CC (6)	G_{EA_CC}			265		µA/V
Max source current (6)	I_{COMP+}	CC		50		µA
Max sink current (6)	I_{COMP-}			-200		µA
Transconductance @ CV (6)	G_{EA_CV}			50		µA/V
Transconductance for fast loop @ CV (6)	G_{EA}_fast	|VCC - VCC_regulate|>1V		640		µA/V
Upper clamp voltage for CV	$V_{COMP_H_CV}$		2.5	2.65	2.8	V
Lower clamp voltage	V_{COMP_L}		1.15	1.21	1.27	V
Comp voltage where min-off time changes	V_{COMP_MID}		1.3	1.39	1.47	V

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ELECTRICAL CHARACTERISTICS *(continued)*

Typical values are tested at VCC = 12V, T_A = +25°C, unless otherwise noted. Minimum and maximum values are at VCC = 12V, T_J = -40°C~+125°C, unless otherwise noted, guaranteed by characterization.

Parameter	Symbol	Condition	Min	Typ	Max	Units
PWM Comparator						
Slope rate of normal operation	α		0.24	0.28	0.3	V/μs
Minimum on time	$T_{min_ON_time}$	CV	310	480	620	ns
		CC	900	1100	1400	
Zero-Current Detector (ZCD)						
Bias current of ZCD	I_{bias_ZCD}	During turn on	255	315	355	μA
Brown-out protection threshold	$V_{brown\ out}$		0.16	0.185	0.21	V
Brown-out detection time	$T_{brown\ out}$		11	18.5	33	ms
Zero-current detect threshold	V_{ZCD_T}	V_{ZCD} falling edge	0.265	0.29	0.32	V
Zero-current hysteresis for CV	V_{ZCD_hys}		0.26	0.3	0.34	V
Zero-current hysteresis for CC	V_{ZCD_hys}		0.56	0.6	0.64	V
ZCD blanking time	t_{LEB_ZCD}	CC, after turn off, Vs_peak > 0.15V	1.2	1.6	2	μs
		CC and CV, after turn off, Vs_peak < 0.15V	0.6	0.8	1.1	
Over-voltage blanking time	t_{LEB_OVP}	CC, after turn off, Vs_peak > 0.15V	1.2	1.6	2	μs
		CC and CV, after turn off, Vs_peak < 0.15V	0.6	0.8	1.1	
Over-voltage threshold	V_{ZCD_OVP}	1.6μs delay after turn-off	4.7	4.9	5.2	V
OVP detect switching pulse	N_{pulse_OVP}	To count uninterrupted		5		
Fault Pull-Up MOSFET						
Breakdown voltage	$BV_{DSS_D_VCC}$		30			V
Continue drain current	$I_{D_D_VCC}$		9.5	13.5	18.5	mA
CC Minimum Off Time Section						
Minimum off time in CC mode	$T_{min_OFF_CC}$		4.4	5	6.2	μs
Maximum min off time depending on COMP	$T_{max_OFF_CC}$	COMP = V_{COMP_L}	165	210	270	μs
LFM Minimum Off Time Section						
Minimum off time in LFM (5)	$T_{min_OFF_LFM}$			4.8		ms
S Pin Section						
Blanking time for short inductor/transformer	$T_{blank_S_short}$			275		ns

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ELECTRICAL CHARACTERISTICS *(continued)*

Typical values are tested at VCC = 12V, T_A = +25°C, unless otherwise noted. Minimum and maximum values are at VCC = 12V, T_J = -40°C ~ +125°C, unless otherwise noted, guaranteed by characterization.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Starter						
Start timer period	t_{START}	ZCD not detected in CC	150	175	215	μs
Current Limit Section						
CV mode current limit	V_{cv_limit}	With S pin blanking 450ns	0.38	0.45	0.5	V
CC mode current limit	$VCC_{_limit}$	With S pin blanking 450ns	1.4	1.47	1.55	V
CV mode current limit foldback	$V_{cv_limit_foldback}$	With S pin blanking 450ns	0.15	0.2	0.235	V
Primary over-current protection	$V_{primary_OCP}$	With S pin blanking 350ns	1.9	2	2.1	V
CS						
Leading edge blanking time	T_{blank_S}		310	480	620	ns
Internal Main MOSFET						
Break down voltage	BV_{DSS_Main}	Vgs = 0	30			V
Drain-source on resistor	$R_{DS(ON)_Main}$	I_D = 500mA		315	480	mΩ
Thermal Shutdown						
Thermal shutdown threshold	T_{SD}			160		°C
Thermal shutdown recovery hysteresis	T_{hys}			60		°C

NOTE:

5) Guaranteed by design.

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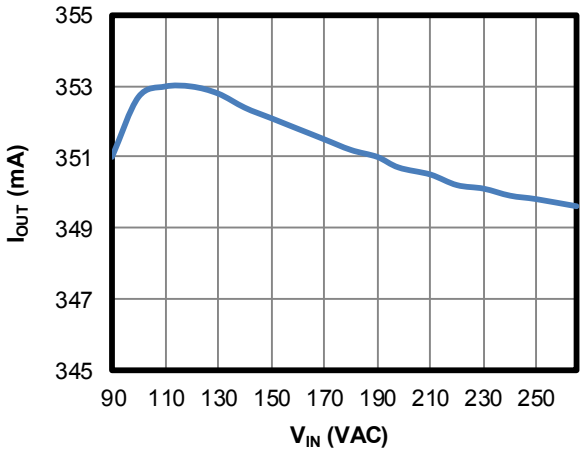
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board. V_{IN} = (90 - 265)V_{AC}/50Hz, 7LEDs in series, I_{LED} = 350mA, V_{LED} = 21V, Lp = 2.15mH.

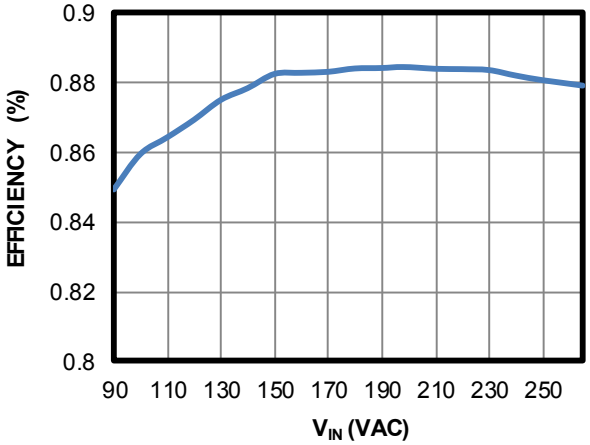
Line Regulation

V_{IN} = (90 - 265)V_{AC}/50Hz, full load



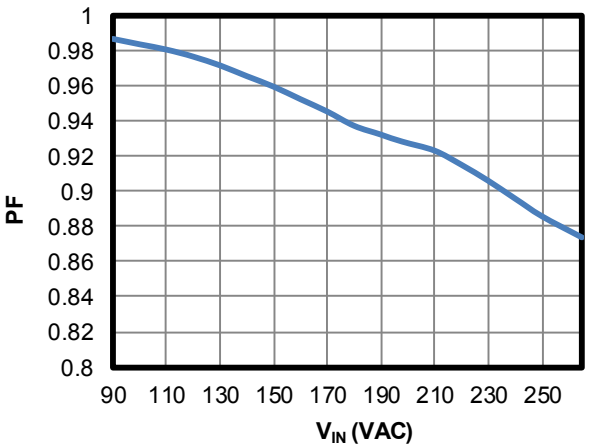
Efficiency

V_{IN} = (90 - 265)V_{AC}/50Hz, full load



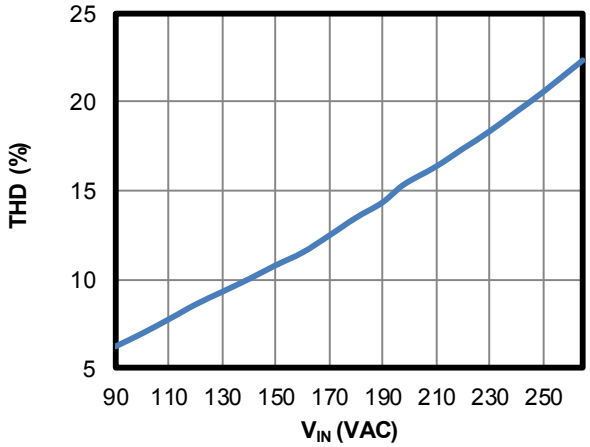
PF

V_{IN} = (90 - 265)V_{AC}/50Hz, full load



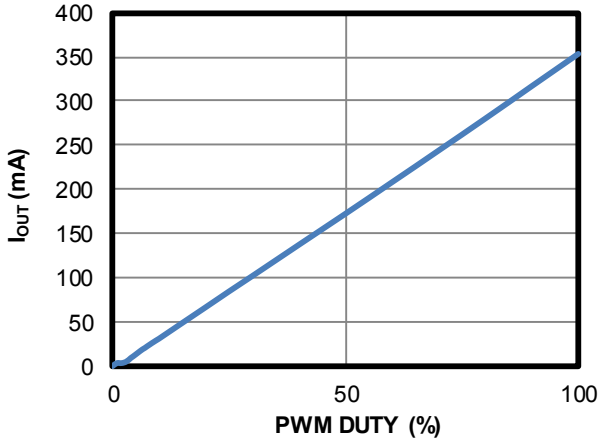
THD

V_{IN} = (90 - 265)V_{AC}/50Hz, full load



5kHz PWM Dimming Curve

V_{IN} = 220V_{AC}, 7 LED output



1kHz PWM Dimming Curve

V_{IN} = 220V_{AC}, 7 LED output

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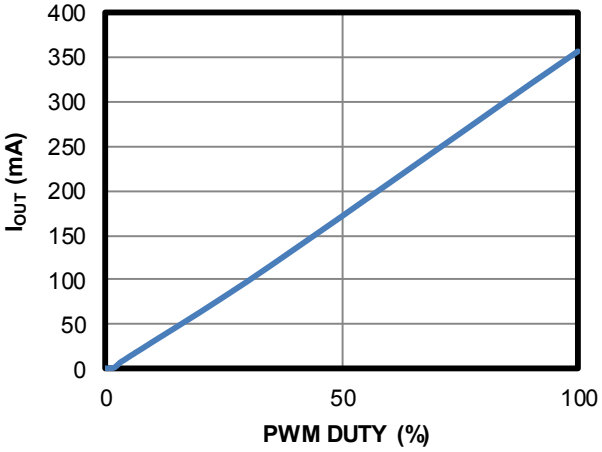
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. V_{IN} = (90 - 265)V_{AC}/50Hz, 7LEDs in series, I_{LED} = 350mA, V_{LED} = 21V, Lp = 2.15mH.

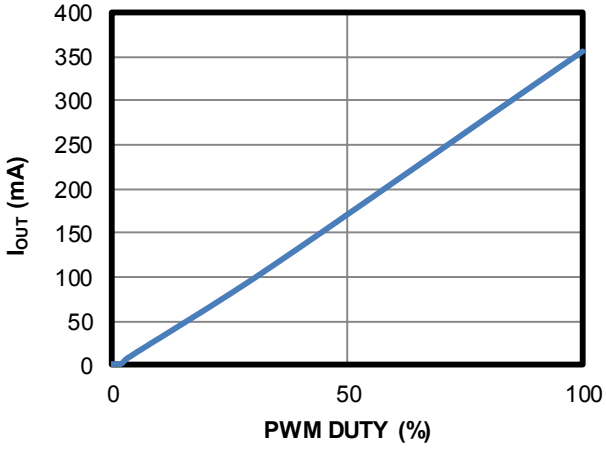
5kHz PWM Dimming Curve

V_{IN} = 120V_{AC}, 7 LED output



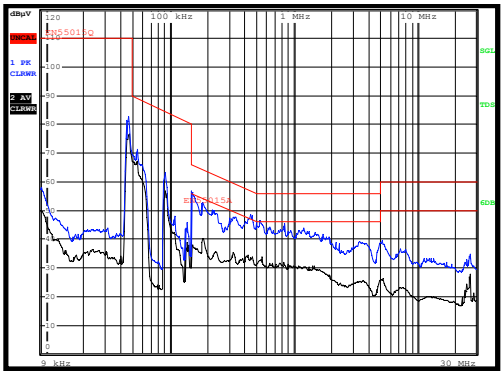
1kHz PWM Dimming Curve

V_{IN} = 120V_{AC}, 7 LED output



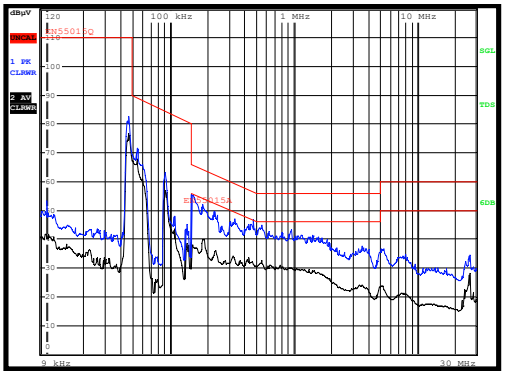
Conduct EMI-L Line

V_{IN} = 120V_{AC}, 7 LED output



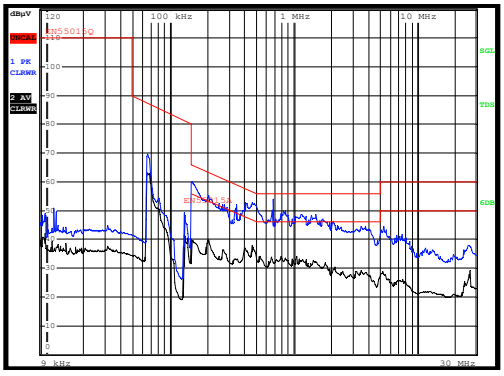
Conduct EMI-N Line

V_{IN} = 120V_{AC}, 7 LED output



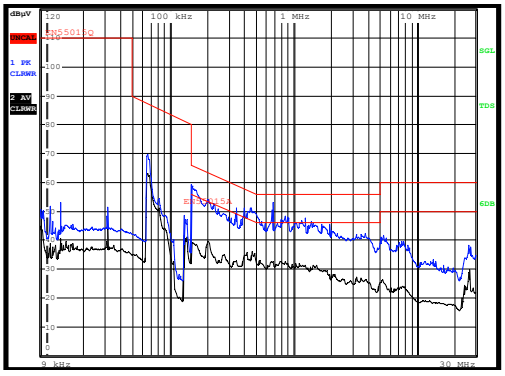
Conduct EMI-L Line

V_{IN} = 230V_{AC}, 7 LED output



Conduct EMI-N Line

V_{IN} = 120V_{AC}, 7 LED output



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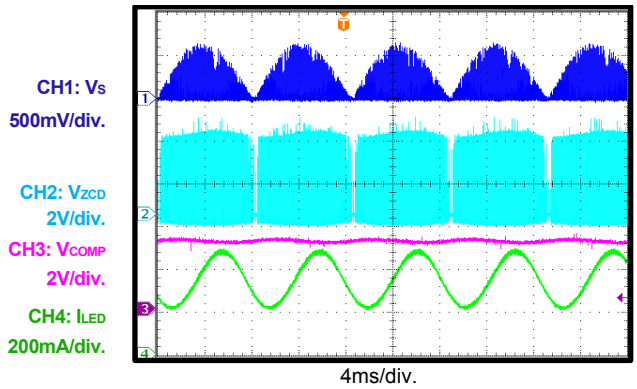
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. V_{IN} = (90 - 265)V_{AC}/50Hz, 7LEDs in series, I_{LED} = 350mA, V_{LED} = 21V, Lp = 2.15mH.

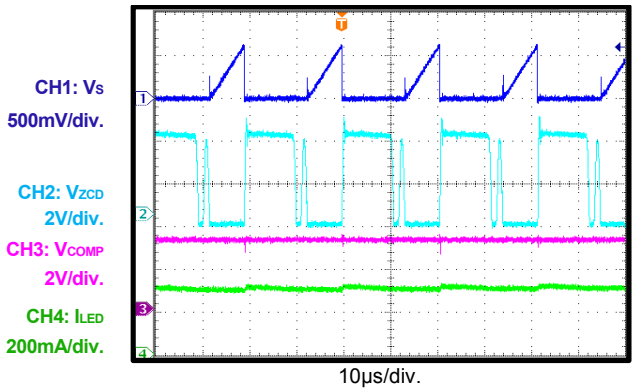
Steady State

V_{IN} = 120V_{AC}, 7 LED output



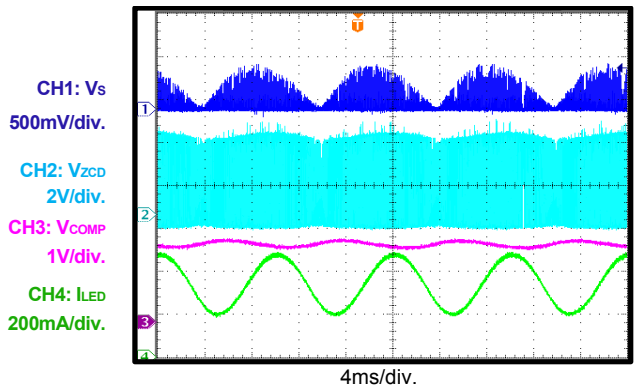
Steady State

V_{IN} = 120V_{AC}, 7 LED output



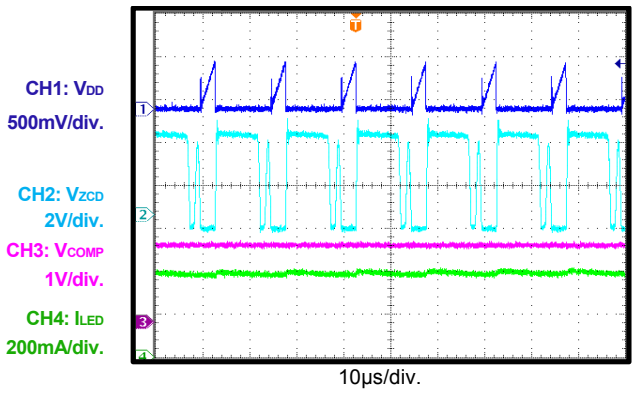
Steady State

V_{IN} = 230V_{AC}, 7 LED output



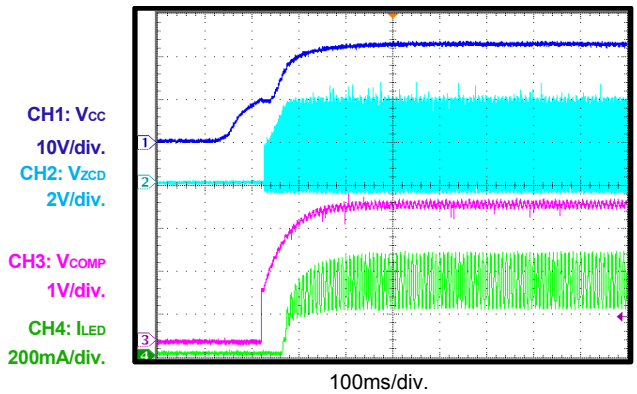
Steady State

V_{IN} = 230V_{AC}, 7 LED output



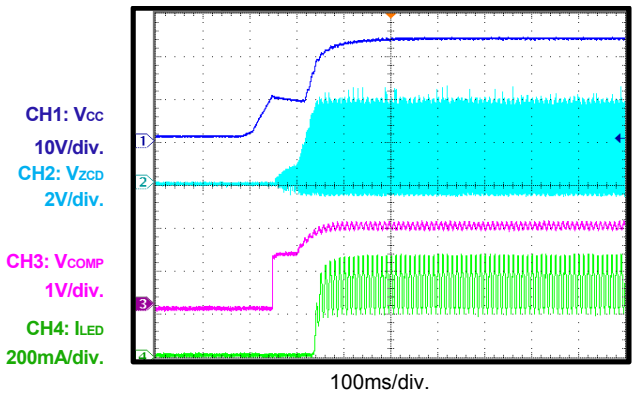
Start-Up

V_{IN} = 120V_{AC}, 7 LED output



Start-Up

V_{IN} = 230V_{AC}, 7 LED output



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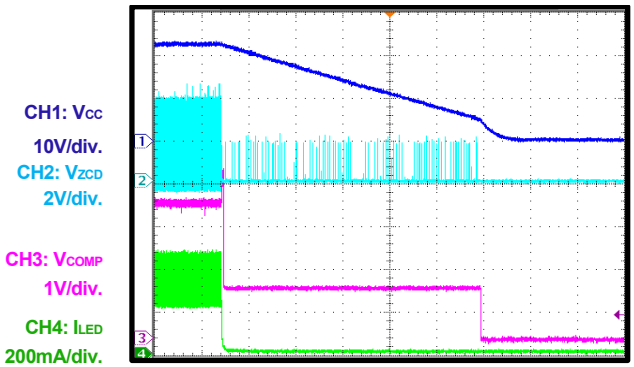
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. V_{IN} = (90 - 265)V_{AC}/50Hz, 7LEDs in series, I_{LED} = 350mA, V_{LED} = 21V, Lp = 2.15mH.

Shutdown

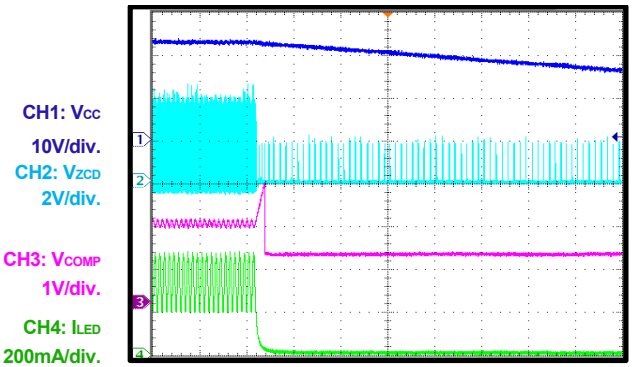
V_{IN} = 120V_{AC}, 7 LED output



400ms/div.

Shutdown

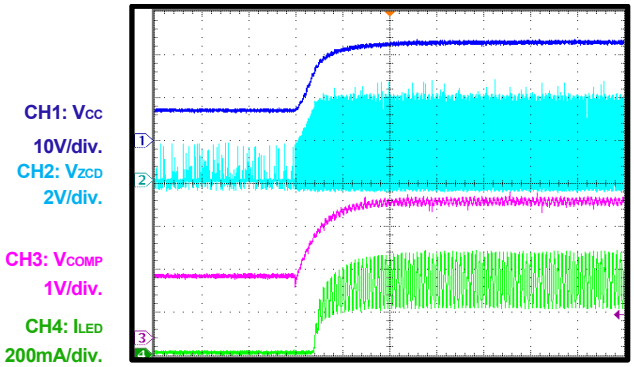
V_{IN} = 230V_{AC}, 7 LED output



100ms/div.

CV-CC

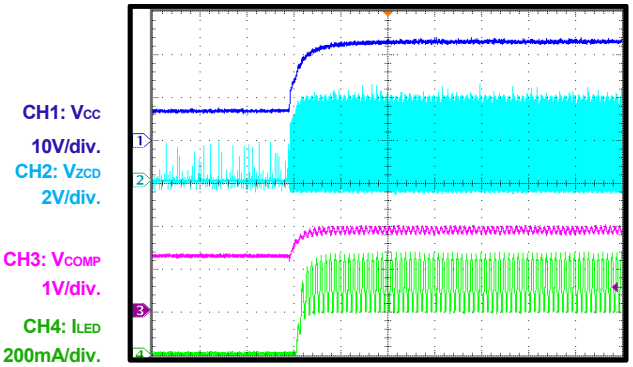
V_{IN} = 120V_{AC}, 7 LED output



100ms/div.

CV-CC

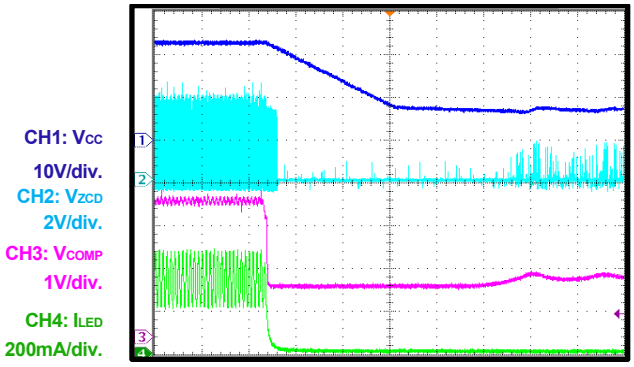
V_{IN} = 230V_{AC}, 7 LED output



100ms/div.

CC-CV

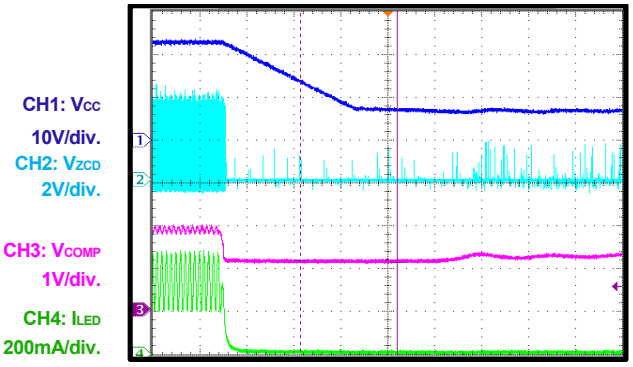
V_{IN} = 120V_{AC}, 7 LED output, full load



100ms/div.

CC-CV

V_{IN} = 230V_{AC}, 7 LED output, full load



100ms/div.

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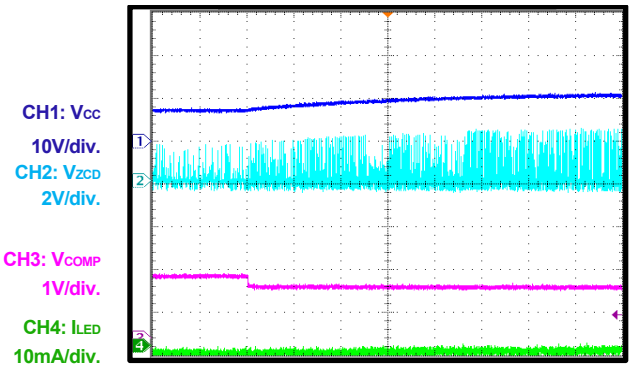
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. V_{IN} = (90 - 265)V_{AC}/50Hz, 7LEDs in series, I_{LED} = 350mA, V_{LED} = 21V, Lp = 2.15mH.

CV-CC

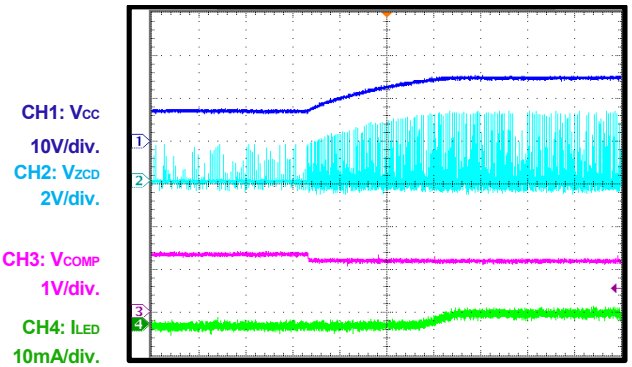
V_{IN} = 120V_{AC}, 7 LED output, DIM = 1%



400ms/div.

CV-CC

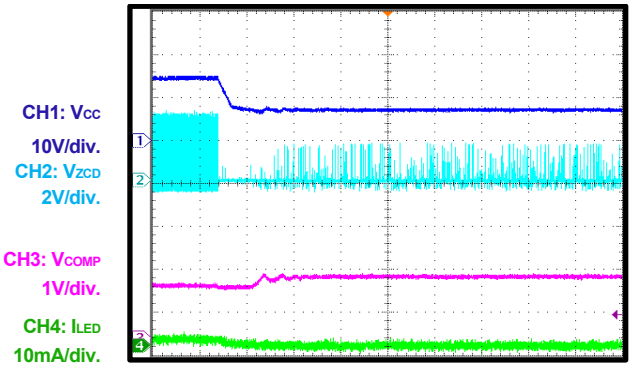
V_{IN} = 230V_{AC}, 7 LED output, DIM = 1%



400ms/div.

CC-CV

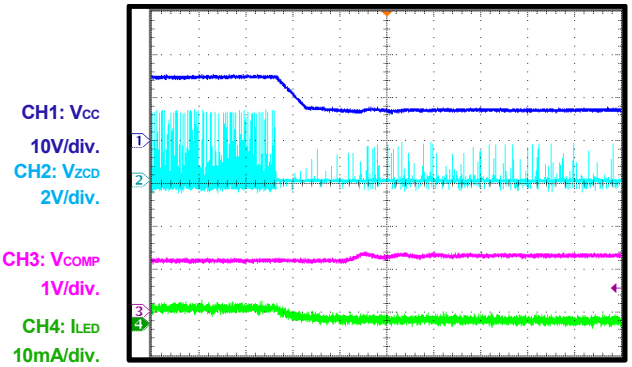
V_{IN} = 120V_{AC}, 7 LED output, DIM = 1%



400ms/div.

CC-CV

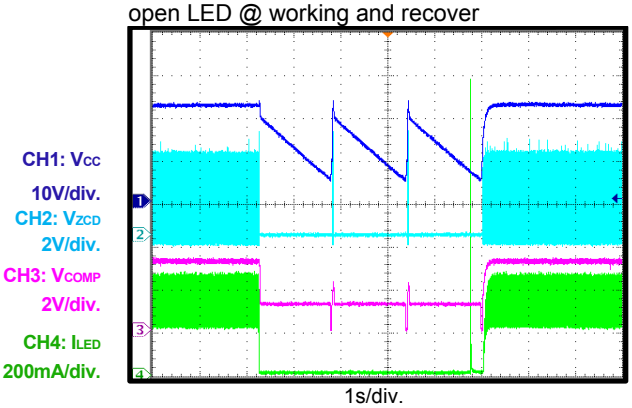
V_{IN} = 230V_{AC}, 7 LED output, DIM = 1%



200ms/div.

OVP

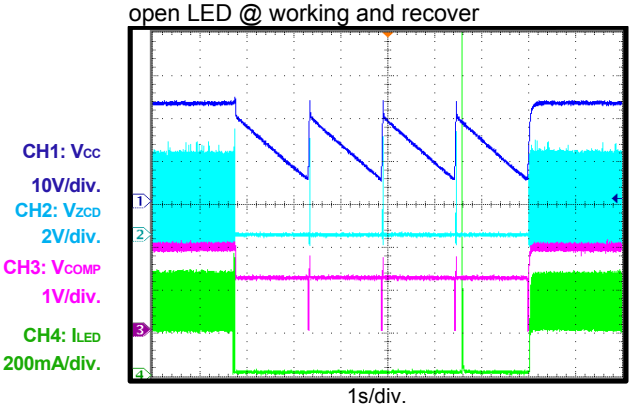
V_{IN} = 120V_{AC}, 7 LED output,
open LED @ working and recover



1s/div.

OVP

V_{IN} = 230V_{AC}, 7 LED output,
open LED @ working and recover



1s/div.

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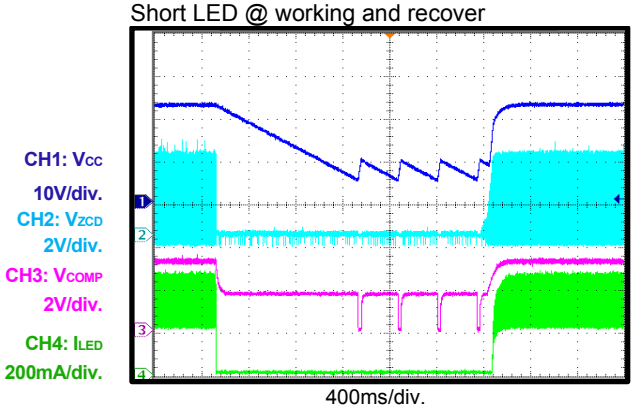
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. V_{IN} = (90 - 265)V_{AC}/50Hz, 7LEDs in series, I_{LED} = 350mA, V_{LED} = 21V, Lp = 2.15mH.

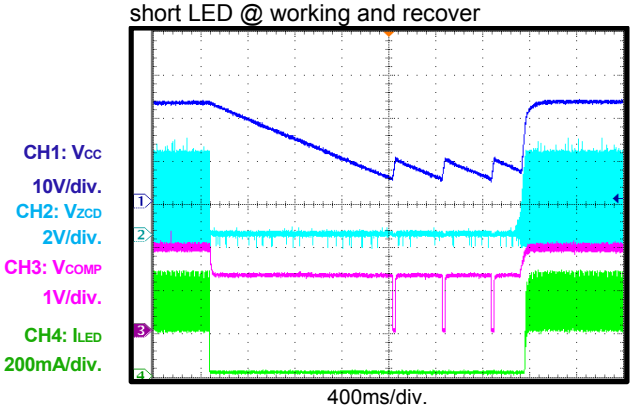
SCP

V_{IN} = 120V_{AC}, 7 LED output,
Short LED @ working and recover



SCP

V_{IN} = 230V_{AC}, 7 LED output,
short LED @ working and recover



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PIN FUNCTIONS

Pin #	Name	Description
1	D	**Internal low-side main MOSFET drain.** D is connected to the source of the external high-side main MOSFET. D is also connected to VCC internally through a diode and a JFET to form an internal charging circuit for VCC.
2	S	**Internal low-side main MOSFET source.** Connect a resistor from S to GND to sense the internal MOSFET current. In CV mode, the system is protected by a current limit function via S.
3	COMP	**Loop compensation.** Both CC and CV use COMP as the loop compensation. Connect a compensation network to COMP to stabilize the loop.
4	ZCD	**Zero-current detection.** Connect ZCD to a resistor divider between the auxiliary winding and GND. Over-voltage conditions are detected through ZCD. For every turn-off interval, if the ZCD voltage exceeds the over-voltage protection (OVP) threshold after the 1.6μs (Vs_peak > 0.15V) or 0.8μs (Vs_peak ≤ 0.15V) blanking time in four consecutive periods, OVP triggers, and the system stops switching until an auto-restart occurs. The input voltage is also detected by ZCD. For every turn-on interval, if ZCD is higher than 0.2V during the turn-on and remains higher for at least 22ms, the MP4059 recognizes this as a brown-out event.
5	GND	**Ground.** GND is the current return for the control signal and the gate-drive signal.
6	DIM	**Dimming.** Apply an external PWM signal on DIM to dim the LED. Apply a low-level (<0.3V) signal to force the chip to enter CV operation mode.
7	VCC	**Power supply input.**
8	CS	**Current sense.** In CC mode, the primary side real-current control is calculated via CS. The line regulation can be compensated by connecting a resistor from the line bus to CS.

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BLOCK DIAGRAM

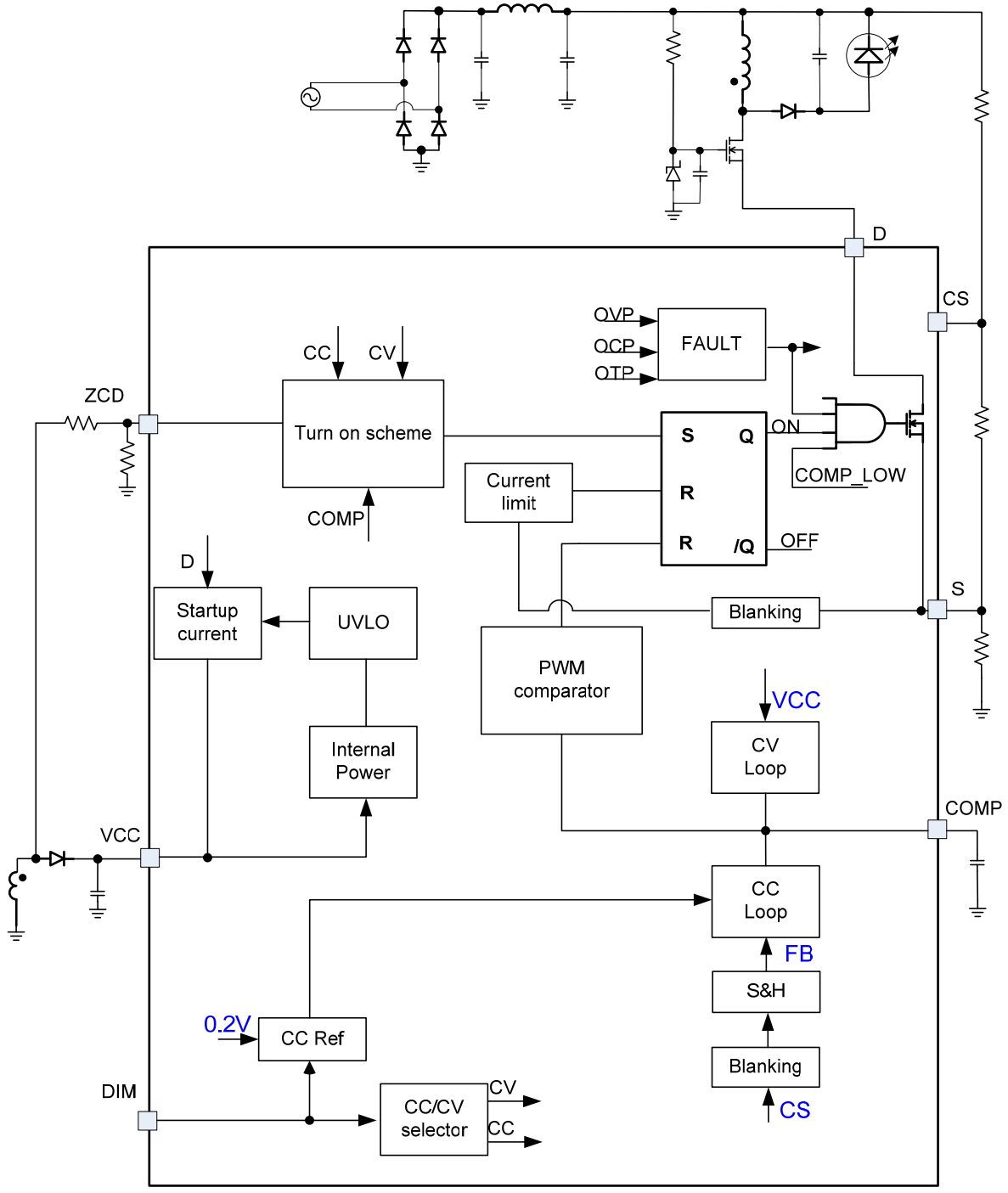

Figure 1: Functional Block Diagram

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OPERATION

The MP4059 can be configured as either a single-stage PFC flyback or buck-boost solution for LED dimming applications. According to the DIM pin setting, the MP4059 can operate in either constant-current (CC) or constant-voltage (CV) mode. In CC mode, the MP4059 can regulate a constant current to an LED load across a 1 - 100% dimming range without flickering or shimmering. In CV mode, the MP4059 can shut off the LED and achieve ultra-low standby power.

Start-Up

Initially, VCC is charged through the internal charging circuit from the AC line. When VCC reaches the VCC upper threshold (VCC_H), the under-voltage lockout (UVLO) logic switches low and the internal main MOSFET begins to switch.

CC Mode Valley Switching Operation

During the external MOSFET on time (t_{ON}), the rectified input voltage (V_{BUS}) is applied to the primary-side inductor (Lm), and the primary current (I_{pri}) increases linearly from zero to the peak value (I_{pk}). When the external MOSFET turns off, the energy stored in the inductor is transferred to the secondary-side and turns on the secondary-side diode to power the load. The secondary current (I_{sec}) begins to decrease linearly from the peak value to zero. When the secondary current decreases to zero, the primary-side leakage inductance, magnetizing inductance and all parasitic capacitances decrease the MOSFET drain-source voltage. This decrease is also reflected on the auxiliary winding. During CC operation, the MP4059 monitors ZCD when it falls to zero twice before the next switching period begins. The zero-current detector from the ZCD pin generates the gate turn-on signal when the ZCD voltage falls below 0.295V the second time (see Figure 2).

This virtually eliminates switch turn-on and diode reverse-recovery losses, ensuring high efficiency and low EMI noise.

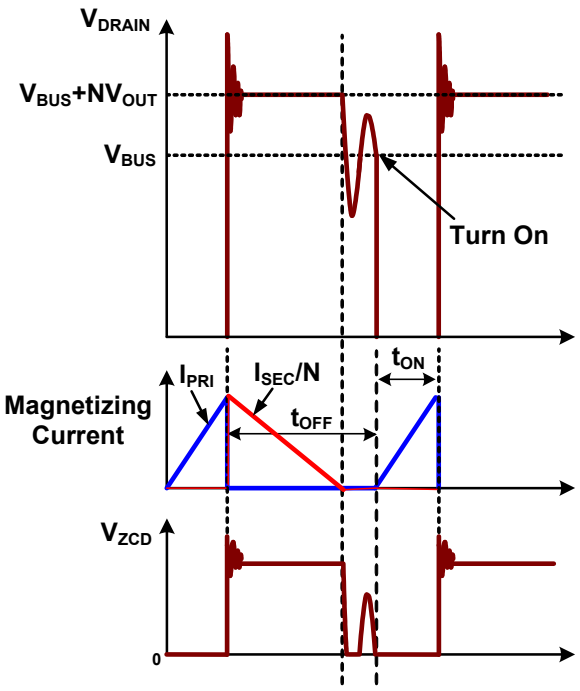

Figure 2: Valley Switching Mode

Real-Current Control

The proprietary real-current control method allows the MP4059 to control the secondary-side LED current from the primary side. The means that the output LED current can be calculated approximately with Equation (1):

$$I_o \approx \frac{N \cdot V_{FB}}{2 \cdot R_s} \quad (1)$$

Where N is the turn ratio of the primary side to secondary side, V_{FB} is the feedback reference voltage (typical 0.2V), and R_s is the sensing resistor connected between the MOSFET source and GND.

Minimum Off Time

The MP4059 operates with a variable switching frequency. The frequency changes with the input instantaneous line voltage. To limit the maximum frequency and achieve good EMI performance, the MP4059 employs an internal minimum off time limit of 5.5μs.

By increasing the minimum off time in deep dimming conditions, the MP4059 can achieve 1% dimming depth.

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Power Factor Correction

The high power factor is guaranteed by the constant-on-time (COT) theory. Use a fixed slope triangle to compare with the COMP voltage (V_{COMP}) and get the constant T_{ON} in certain V_{IN} and output loads. COT forces the primary peak current to follow the track of the input voltage, which achieves the high power factor (see Figure 3).

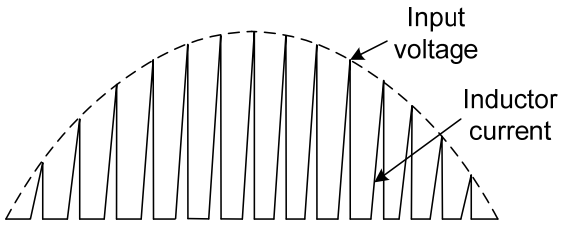

Figure 3: Constant T_{ON} for PFC

Low Frequency Mode (LFM) Operation

The MP4059 enter into low-frequency mode (LFM) operation when VCC is higher than V_{LFM} in a CV condition. In LFM, the minimum off time increases to 4ms to drop the switching frequency, which improves light-load efficiency.

Deep Dimming

To achieve deep dimming in CC mode, a special design is integrated into the MP4059.

V_{COMP} drops as the dimming depth increases. When V_{COMP} is lower than V_{COMP_MID}, the minimum off time increases with the falling V_{COMP}. When V_{COMP} reaches its low clamp value (V_{COMP_L}), the minimum off time reaches its maximum value ($t_{off_max_cc}$). This can help improve dimming depth greatly.

Auto-Starter

The MP4059 integrates an auto-starter, which starts timing when the MOSFET is turned off. If ZCD fails to send out another turn-on signal after 130μs, the starter automatically sends out the turn-on signal, which can prevent the IC from shutting down unnecessarily because of a ZCD missing detection.

Under-Voltage Lockout (UVLO)

If VCC drops below the UVLO threshold of 5.5V, the MP4059 stops switching and shuts down. VCC begins charging again via the internal current source from the AC line.

Leading-Edge Blanking (LEB)

To avoid a premature termination of the switching pulse due to the parasitic capacitance discharging when the MOSFET turns on, an internal leading-edge blanking (LEB) unit is employed between the S pin and the current comparator input. During the blanking time, the path (S to the current comparator input) is blocked. Figure 4 shows the leading-edge blanking.

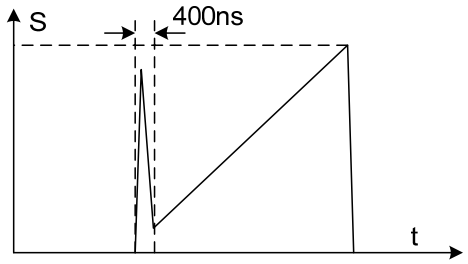

Figure 4: Leading-Edge Blanking

Output Over-Voltage Protection (OVP)

In CC mode, output over-voltage protection (OVP) can prevent the components from damage in an over-voltage condition. The positive plateau of the auxiliary winding voltage is proportional to the LED output voltage. OVP uses the auxiliary winding voltage instead of monitoring the output voltage directly. Once the ZCD voltage is higher than 4.5V within four consecutive periods, the OVP signal is triggered and latched, gate driver is turned off, and the IC works in quiescent mode (see Figure 5). VCC drops below UVLO, which makes the IC shut down and the system restart again. The output OVP setting point can be calculated with Equation (2):

$$V_{OUT_OVP} \cdot \frac{N_{Vcc}}{N_{SEC}} \cdot \frac{R_{ZCD2}}{R_{ZCD1} + R_{ZCD2}} = 4.5V \quad (2)$$

Where V_{OUT_OVP} is the output OVP point, N_{VCC} is the number of VCC winding turns, and N_{SEC} is the number of secondary winding turns.

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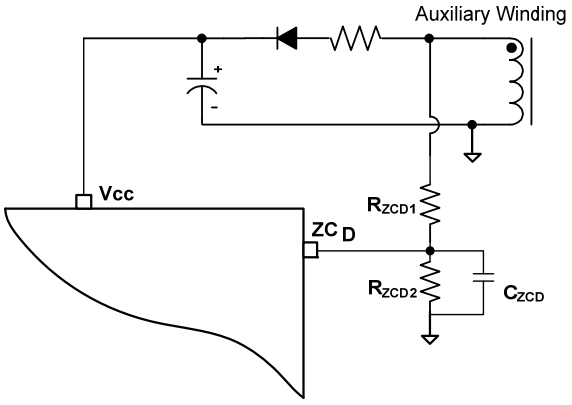

Figure 5: Zero-Current Detection

To avoid mistriggering OVP because of the oscillation spike that occurs after the switch turns off, the OVP sampling has a t_{LEB_OVP} blanking period (typically 1.6μs) (see Figure 6).

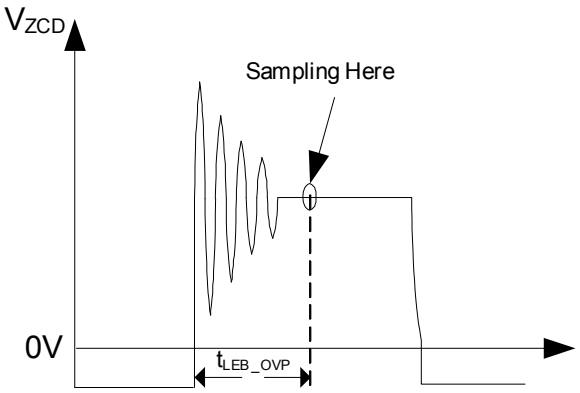

Figure 6: OVP Sample Blanking Time

Output Short-Circuit Protection (SCP)

In CC mode, if an output short circuit occurs, ZCD cannot detect the zero current crossing point of the transformer, so the 130μs auto-restart timer triggers the turn-on signal of the power MOSFET. In this situation, the switching frequency of the power circuit is reduced to about 8kHz, and the output current is limited to its nominal current. This makes the output power in the output short-circuit condition very small, and the temperature rise of the components is sufficiently low.

If an output short occurs in CV mode, for the first several pulses, the ZCD may still be detected by the chip, and the system can be protected by the current limit (typically 0.45V). Afterward, if the ZCD cannot be detected, the 130μs auto-restart timer determines the turn-off time, and the foldback value of the current limit determines the turn-on time.

Brown-Out Protection

Brown-out protection is integrated into the MP4059. During a turn-on, the ZCD voltage can reflect the input voltage. Connect a 300μA current source on the ZCD pin and compare it with 0.2V. If ZCD is higher than 0.2V during the turn-on and lasts for at least 22ms, the MP4059 recognizes that a brown-out has occurred.

Thermal Protection

The chip integrates a thermal protection. When the junction temperature reaches 160°C, the entire chip shuts down. When the temperature drops back to 90°C, the MP4059 resumes normal operation.

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APPLICATION INFORMATION

Select the sensing resistor and turn ratio between the primary and forward winding using Equation (3):

$$I_o \approx \frac{N_p \cdot 0.2}{2 \cdot R_s \cdot N_s} \quad (3)$$

Selecting the Turn Ratio and Primary Inductance

For the same LED output voltage, a small turns ratio between the primary and secondary sides means lower voltage spikes for the primary MOSFET but higher voltage spikes for the secondary rectifier diode. Similarly, a small turns ratio leads to poor PF/THD due to a smaller duty cycle operation and also results in a smaller inductance, which leads to a smaller transformer and worse efficiency.

For the auxiliary winding turns number, ensure that the LED will not light up during CV operation and will not trigger OVP in CC heavy-load operation.

The maximum inductance with a minimum working frequency occurs at the peak of the minimum input voltage. By integrating the secondary current into one line cycle to get the average constant current (Io), the relationship between Lp and Io can be set. The real inductance should be smaller than or equal to the calculated value to ensure a minimum working frequency.

Selecting the Input Capacitor

The input capacitor is used for the high frequency working current loop. A larger capacitor means better voltage ripple on the capacitor and better EMI performance but worse power factor. Typically, a 68 ~ 330nF capacitor is recommended.

Selecting the Output Capacitor

The output voltage contains two components: the switching frequency ripple associated with the flyback converter and the low frequency ripple associated with the input line voltage. Selecting the output bulk capacitor depends on the output current, output voltage, desired voltage ripple, and the LED current ripple.

ZCD Section

The conditions below must be considered when selecting the divider ratio and value.

1. Negative current limit: In the worst-case scenario, the maximum negative current should not be larger than 5mA; otherwise, a diode must be paralleled between ZCD and GND.
2. OVP detection: The resistor divider ratio can be calculated according to the setting value of the OV point. This ratio is also associated with the turns ratio between the VCC winding and secondary winding.
3. Brown-out detection: The resistors can be selected based on the required input brown-out voltage and turns ratio.
4. Normal working check: This is to ensure that ZCD can be detected in the worst-case scenario of CV normal operation.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For best results, refer to Figure 7 and follow the guidelines below.

1. Design the main power flow path to be as short as possible with wide wires.
2. Connect the low-side sensing resistor directly to the GND of the input CBB capacitor to minimize the current loop.
3. Design the high-frequency current loop to be as short as possible using heavy copper wires to minimize the voltage drop.

   This is for the forward winding loop due to some cases having a small on time but very high peak current.
4. Separate the power GND and analog GND.
5. Connect the power GND and analog GND with a single-point connection in the IC GND or input capacitor GND.

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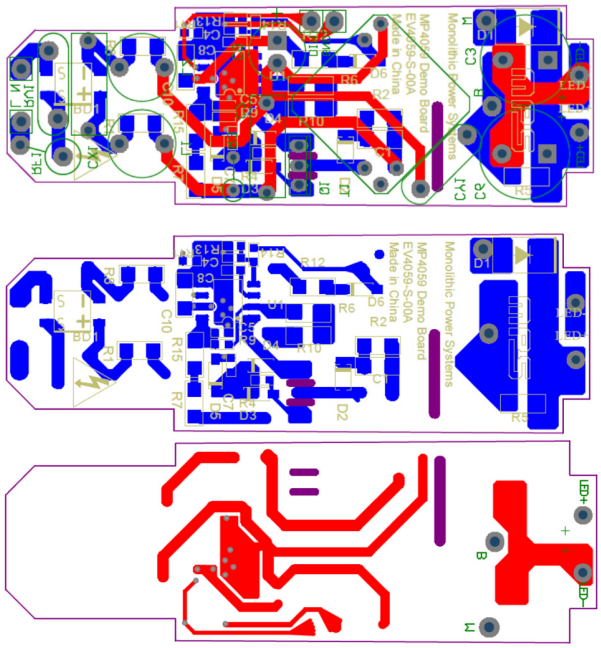

Figure 7: Recommended PCB Layout

Analog Dimming

If an analog signal is applied, the interface circuit shown in Figure 8 is recommended to convert the analog signal into a PWM signal.

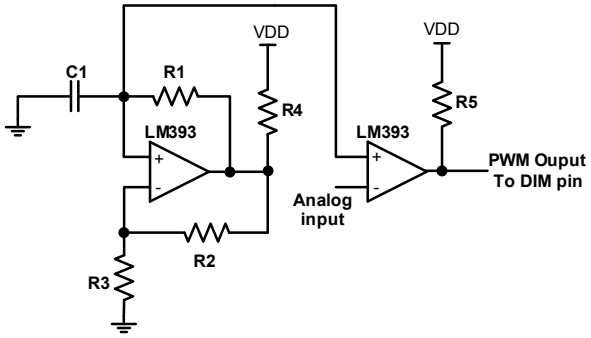

Figure 8: Analog to PWM Interface Circuit

The PWM frequency can be calculated with Equation (4):

$$f=\frac{1}{2*R1*C1*\ln\left(\frac{R3}{R2}+1\right)} \quad (4)$$

The analog dimming signal amplitude can be calculated with Equation (5):

$$V=\frac{R3}{R2+R3}*VDD \quad (5)\ (5)$$

PWM Dimming

Apply a 200Hz - 20kHz PWM dimming signal on DIM to configure the system into pulse-width modulation (PWM) dimming mode (see Figure 9). The amplitude of the PWM signal should be higher than 1.5V. A paralleled 100kΩ resistor is recommended if the system must work in CV mode at start-up and wait for the PWM signal. A 10kΩ resistor in series is recommended to protect the system from any noise caused by a poor layout.

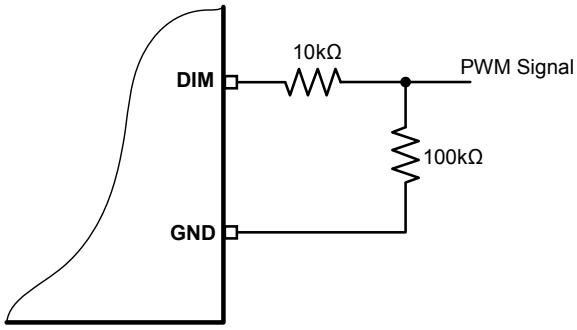

Figure 9: DIM Pin Connection

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TYPICAL APPLICATION CIRCUIT

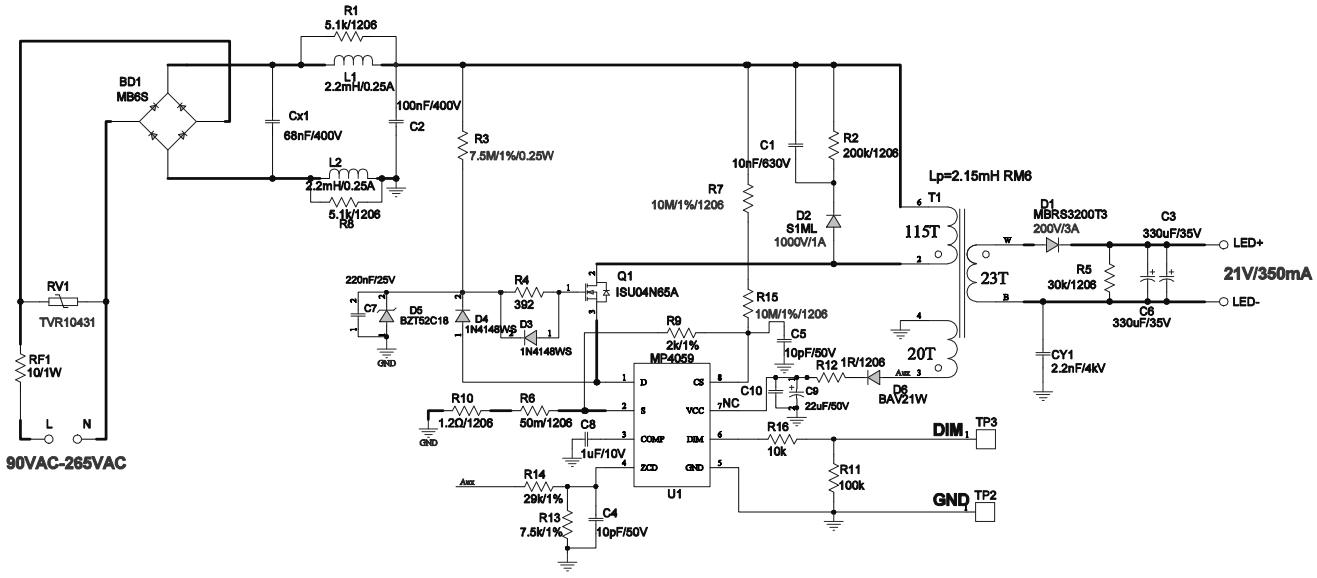

Figure 10: Typical Application Circuit

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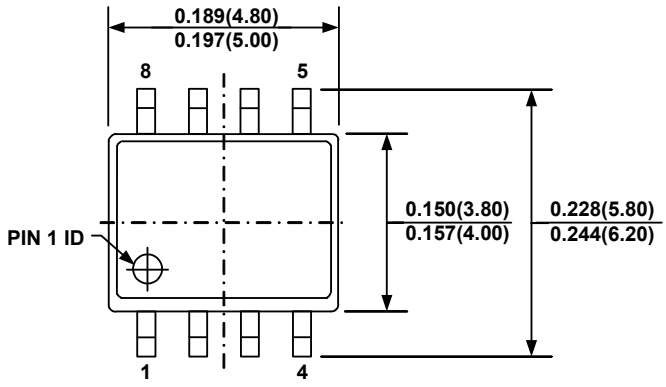
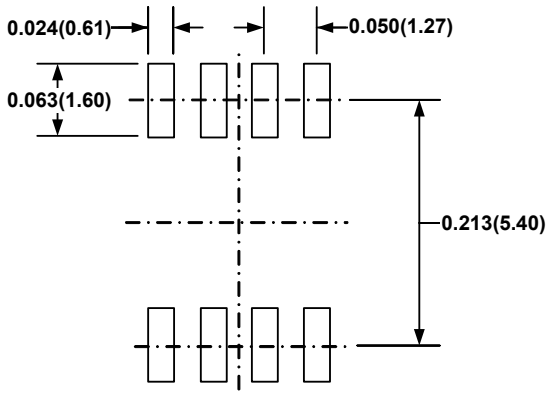
PACKAGE INFORMATION

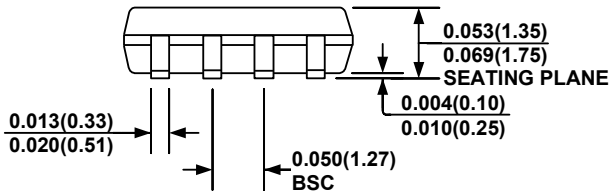
SOIC-8



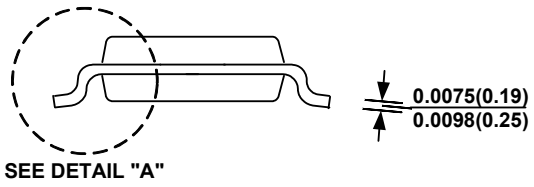
TOP VIEW



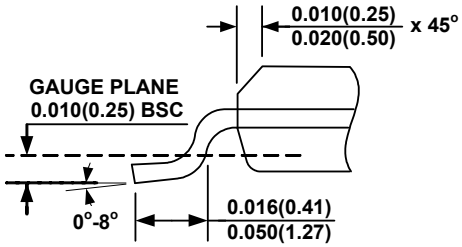
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

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