MP3385

4-String, 80V Output WLED Controller with I²C Interface

The Future of Analog IC Technology

DESCRIPTION

The MP3385 is a step-up controller with 4 regulated current channels designed to drive WLED arrays for middle and large-size LCD panel backlighting applications.

The MP3385 uses peak current mode, PWM control architecture for system loop regulation. It drives an external MOSFET to boost up the output voltage from a 4.5V to 33V input supply.

It employs an I²C digital interface and can flexibly set the operation and protection modes, including dimming mode, dimming current and dimming ratio, OCP, OVP, LED short protection threshold, and the switching frequency. For easy application use and board debugging, the MP3385 detects and automatically disables the unused LED strings during start-up to avoid charging the output to the OVP threshold.

The MP3385 achieves 1.8% current matching between each string. The low regulation voltage on the LED current sources improves efficiency and reduces power loss in order to achieve a higher current output.

The MP3385 supports analog, PWM, and combined analog and PWM dimming modes to meet different application requirements. Full protection features include OCP, OTP, UVP, OVP, LED short/open protection, and inductor/diode short protection.

The MP3385 is available in a QNF-20 (4mm x 4mm) and a TSSOP20-EP package.

FEATURES

- 4-String, Max 300mA/String WLED Driver
- 4.5V to 33V Input Voltage Range
- 80V Abs. Rating for Each String
- 1.8% Current Matching Accuracy for Each String
- Unused Channel Auto-Detection Function during Start-Up
- 100kHz-900kHz Programmable Switching Frequency
- Multiple Dimming Modes Selected by I²C Interface:
  1. Direct PWM Dimming Mode
  2. Internal Fixed 23kHz PWM Dimming Mode
  3. Analog Dimming Mode by Input Pulse
  4. Internal Analog Dimming Mode
  5. Mixed Dimming Mode by Input Pulse
  6. Internal Mixed Dimming Mode
- 2%-100% Programmable Full Scale Current with 8-Bit Resolution
- 0%-100% LED Dimming Range with 10-Bit Resolution for Internal Dimming Mode
- Cascading Capability with a Single Power Source
- 18V to 80V Over-Voltage Protection, 2V/Step
- 0.15V to 0.5V Latch-Off/Recoverable OCP Protection Threshold, 50mV/Step
- Recoverable Thermal Shutdown Protection

APPLICATIONS

- Desktop LCD Flat Panel Displays
- All-in-One
- 2D/3D LCD TV

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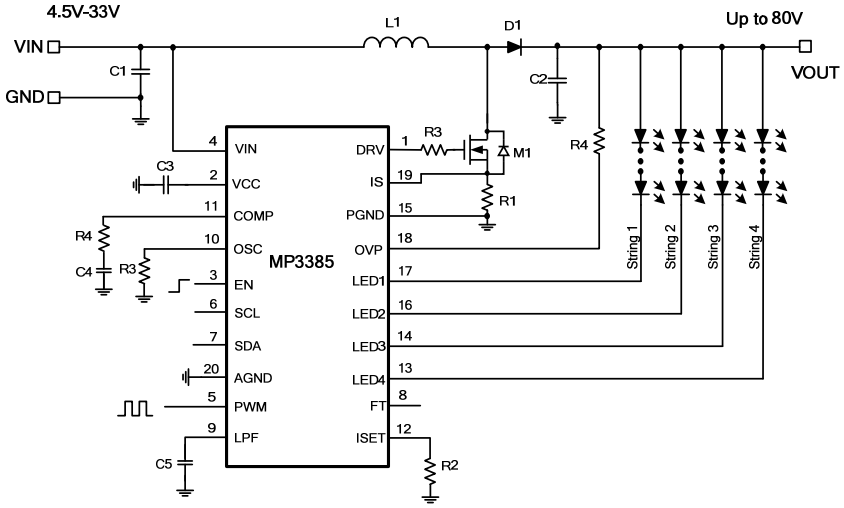
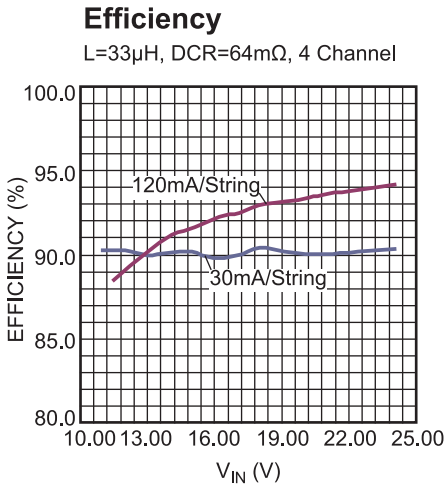
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number	Package	Top Marking
MP3385GR*	QFN-20 (4mm x 4mm)	*See Below*
MP3385GF**	TSSOP20-EP	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP3385GR–Z)

** For Tape & Reel, add suffix –Z (e.g. MP3385GF–Z)

TOP MARKING (QFN-20 (4mm x 4mm))

MPSYWW
MP3385
LLLLLL

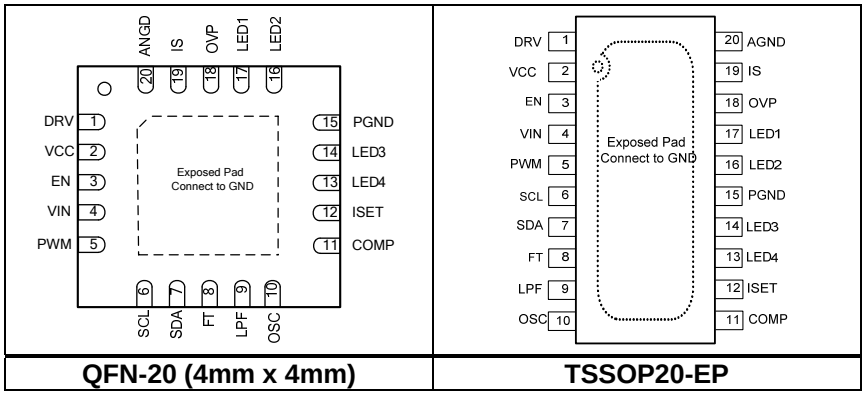
MPS: MPS prefix
Y: Year code
WW: Week code
MP3385: Part number
LLLLLL: Lot number

TOP MARKING (TSSOP20-EP)

MPSYYWW
MP3385
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP3385: Part number
LLLLLLLLL: Lot number

PACKAGE REFERENCE



QFN-20 (4mm x 4mm)	TSSOP20-EP

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ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} .....-0.3V to +40V
V_{OVP}, V_{LED1} to V_{LED4} .....-0.3V to +80V
All other pins .....-0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2)
QFN-20 4mm x 4mm 2.97W
TSSOP20-EP……...3.12W
Junction temperature .....150°C
Lead temperature .....260°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....4.5V to 33V
Operating junction temp..... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-20 (4mm x 4mm)……....42.....9…..°C/W
TSSOP20-EP…… ……..40……..8….°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will produce an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 5V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Unit
Operating input voltage	V_{IN}		4.5		33	V
Supply current (quiescent)	I_Q	V_{IN} = 12V, no switching		3		mA
Supply current (shutdown)	I_{ST}	V_{EN} = 0V, V_{IN} = 12V,			1	μA
LDO output voltage	V_{CC}	7V < V_{IN} < 28V, 0 < I_{VCC} < 10mA	5.4	6	6.3	V
VCC UVLO threshold	V_{IN_UVLO}	Rising edge	3.7	4	4.3	V
VCC UVLO hysteresis				340		mV
EN high voltage	V_{EN_HIGH}	V_{EN} rising	1.5			V
EN low voltage	V_{EN_LOW}	V_{EN} falling			0.6	V
Step-Up Converter						
Gate driver sourcing impedance		V_{CC} = 6V, V_{GATE} = 6V		4		Ω
Gate driver sinking impedance		V_{CC} = 6V, I_{GATE} = 10mA		2		Ω
Switching frequency	f_{SW}	Fsw = 0010b, R_{OSC} = 100kΩ	156	195	234	kHz
		Fsw = 1001b, R_{OSC} = 100kΩ	672	820	967	kHz
OSC voltage	V_{OSC}	R_{OSC} = 100kΩ, f_{SW} = 900kHz	1.75	1.79	1.83	V
Maximum duty cycle	D_{MAX}		90			%
Cycle-by-cycle ISENSE current limit		OCP = 000b	130	150	170	mV
		OCP = 111b	465	500	535	mV
COMP source current limit	$I_{COMP\ SOLI}$	1V < COMP < 2.9V		75		μA
COMP sink current limit	$I_{COMP\ SILI}$	1V < COMP < 2.9V		15		μA
COMP trans-conductance	G_{COMP}	ΔI_{COMP} = ±10μA		100		μA/V
Current Dimming						
PWM input low threshold	V_{PWM_LO}	V_{PWM} falling			0.4	V
PWM input high threshold	V_{PWM_HI}	V_{PWM} rising	1.5			V
Dimming transfer point		MODE = 10b		25		%
		MODE = 11b		50		%
Internal dimming frequency			20	23		kHz
Dimming ratio		Dimming resolution		0.098		%
		DIM = 1111111111b		100		%
Current Regulation						
ISET voltage	V_{ISET}		1.93	1.98	2.03	V
LEDX average current	I_{LED}	R_{ISET} = 100.8kΩ, ILED=FFh	192	201	212	mA
Full scale current		ILED = 00h		2		%
		ILED = FFh[5]		100		%

NOTE:

5) Guaranteed by design.

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Unit
Current matching (6)		I_{LED} = 200mA			1.8	%
LEDX regulation voltage	V_{LEDX}	I_{LED} = 330mA		820		mV
		I_{LED} = 200mA		700		mV
		I_{LED} = 60mA		500		mV
Protection						
OVP protection threshold	V_{OVP_OV}	OVP = 00000b	16.8	18	18.9	V
		OVP = 11100b	71.5	74	75.5	V
OVP UVLO threshold	V_{OVP_UV}	Step-up converter fails		2.5		V
LEDX UVLO threshold	V_{LEDX_UV}		147	206	265	mV
LEDX over-voltage threshold	V_{LEDX_OV}	LEDS = 000b		4		V
		LEDS = 111b		11		V
Thermal protection threshold	T_{ST}			150		°C
Thermal protection hysteresis				25		°C
I²C Interface Specifications						
Input logic low	V_{IL}				0.4	V
Input logic high	V_{IH}		1.3			V
Output logic low	V_{OL}	I_{LOAD} = 3mA			0.4	V
SCL clock frequency	f_{SCL}				400	kHz
SCL high time	t_{HIGH}		0.6			µs
SCL low time	t_{LOW}		1.3			µs
Data setup time	$t_{SU,DAT}$		100			ns
Data hold time	$t_{HD,DAT}$		0		0.9	µs
Setup time for repeated start	$t_{SU,STA}$		0.6			µs
Hold time for start	$t_{HD,STA}$		0.6			µs
Bus-free time between a start and stop condition	t_{BUF}		1.3			µs
Setup time for stop condition	$t_{SU,STO}$		0.6			µs
Rise time of SCL and SDA	t_R		20+0.1×C_B		300	ns
Fall time of SCL and SDA	t_F		20+0.1 ×C_B		300	ns
Pulse width of suppressed spike	t_{SP}		0		50	ns
Capacitance bus for each bus line	C_B				400	pF

NOTE:

6) Matching is defined as the difference between the maximum to minimum current divided by 2x the average currents.

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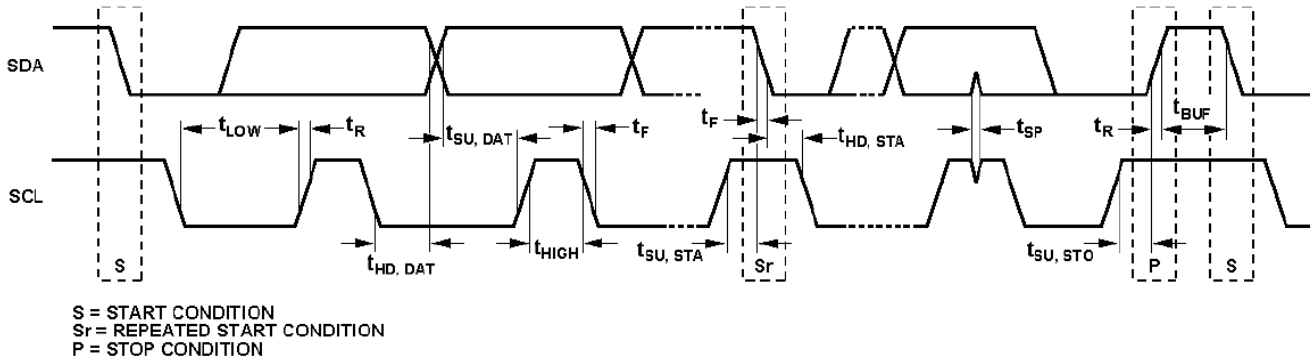

Figure 1: I²C Compatible Interface Timing Diagram

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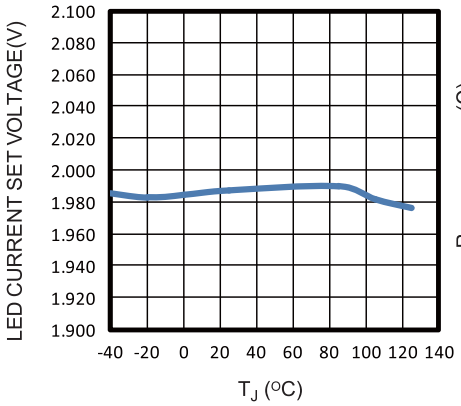
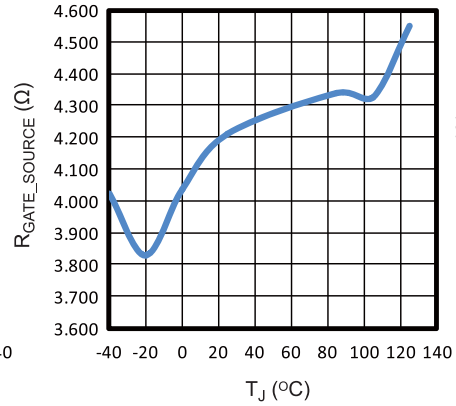
TYPICAL PERFORMANCE CHARACTREISTICS

V_{IN} = 12V, V_{EN} = 3.3V, unless otherwise noted.

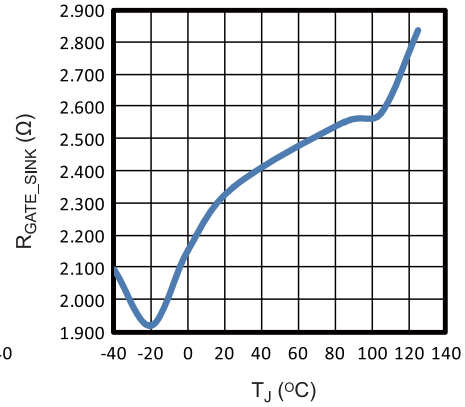
V_{ISET} vs. T_J



R_{GATE_SOURCE} vs. T_J

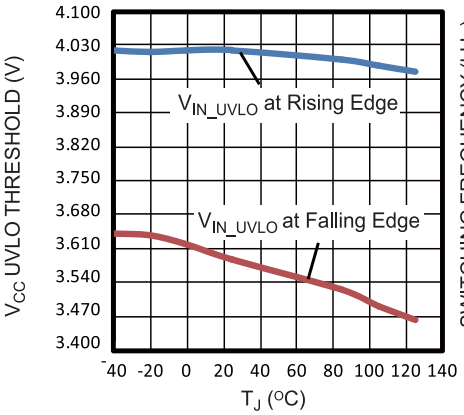


R_{GATE_SINK} vs. T_J

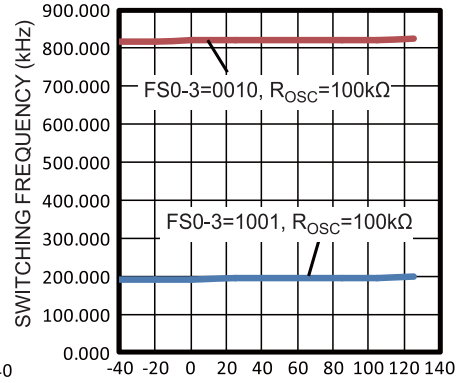


V_{IN_UVLO} vs. T_J

Sweep V_{IN}



F_{SW} vs. T_J



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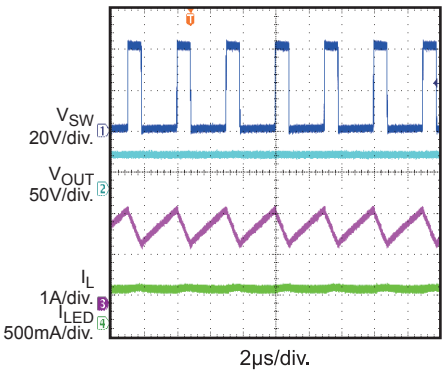
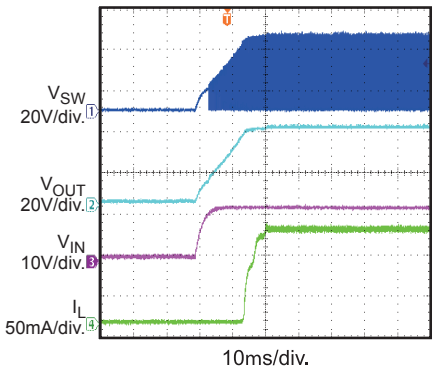
TYPICAL PERFORMANCE CHARACTREISTICS

V_{IN} = 12V, V_{EN} = 3.3V, L = 33µH, 120mA/string, 4-string, 14 LEDs, T_A = 25°C, unless otherwise noted.

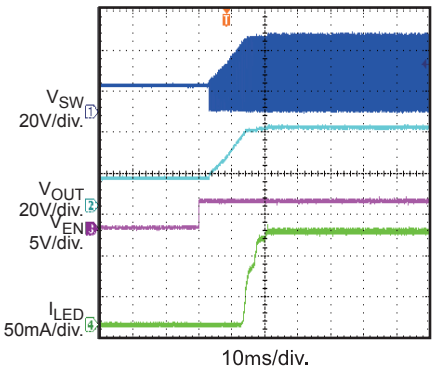
Steady State



V_{IN} Power On 30mA/String

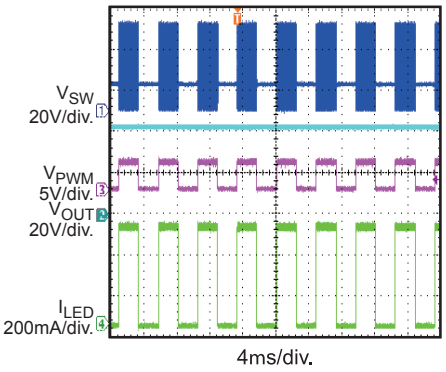


EN Power On 30mA/String



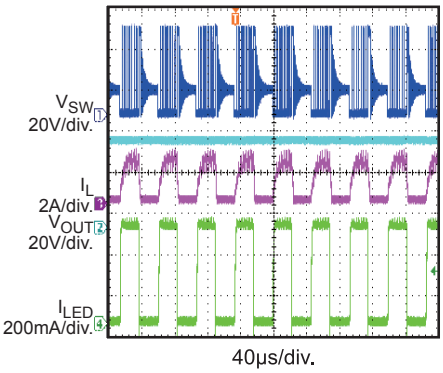
PWM Dimming by PWM Input

f_{PWM} = 200Hz, D_{PWM} = 50%



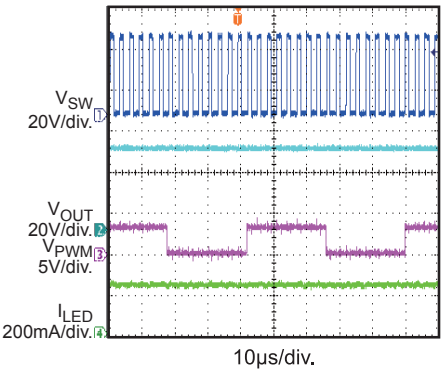
PWM Dimming by I²C Interface

D_{DIM} = 50%



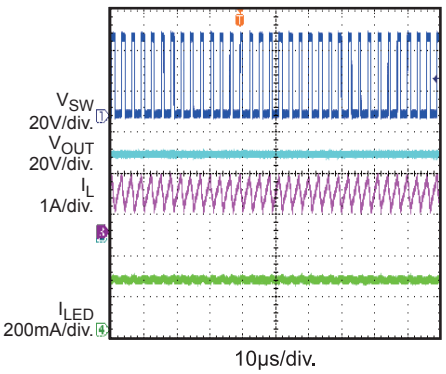
Analog Dimming by PWM Input

f_{PWM} = 20kHz, D_{PWM} = 50%



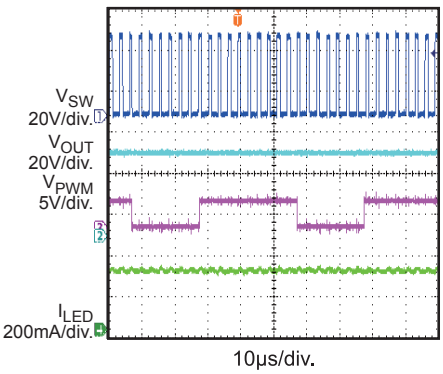
Analog Dimming by I²C Interface

D_{DIM} = 50%



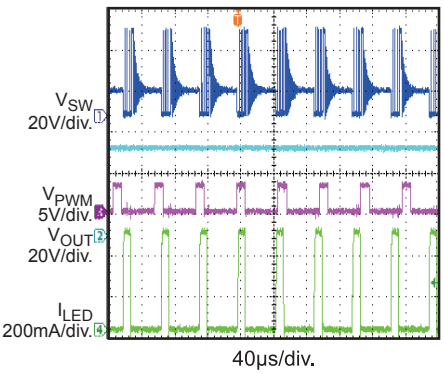
Mix Dimming by PWM Input

f_{PWM} = 20kHz, D_{PWM} = 60%



Mix Dimming by PWM Input

f_{PWM} = 20kHz, D_{PWM} = 20%



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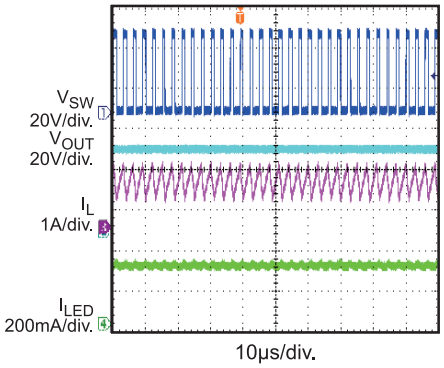
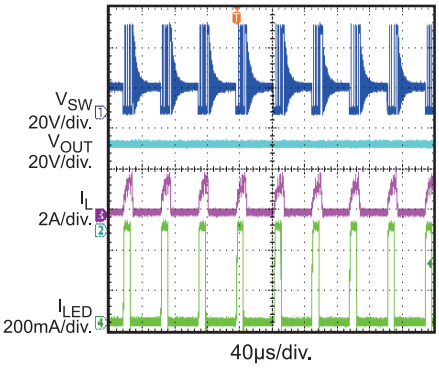
TYPICAL PERFORMANCE CHARACTREISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 3.3V, 120mA/string, 4-string, 14 LEDs, T_A = 25°C, unless otherwise noted.

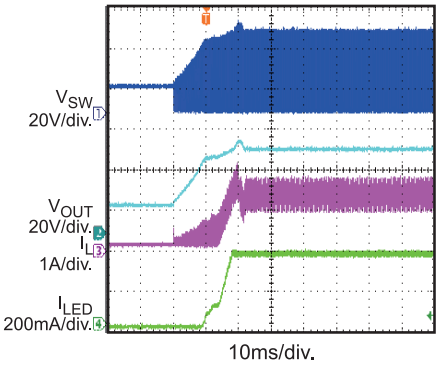
Mix Dimming by I²C Interface
D_{DIM} = 60%



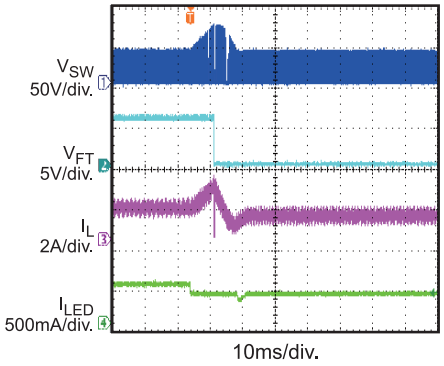
Mix Dimming by I²C Interface
D_{DIM} = 20%



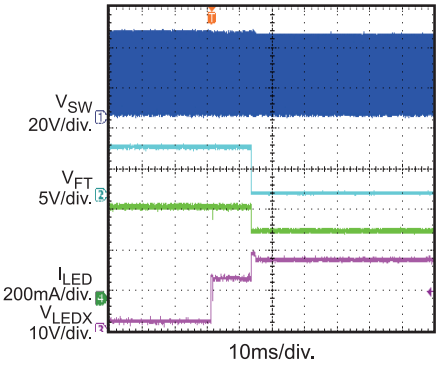
Unused String Protection when V_{IN} Power On



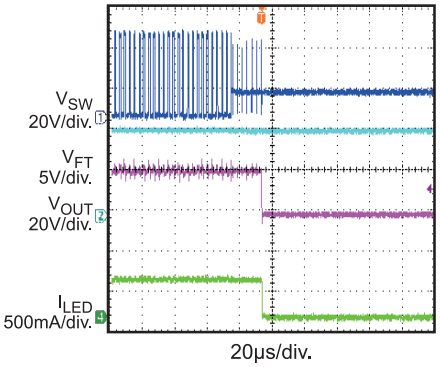
Open One String



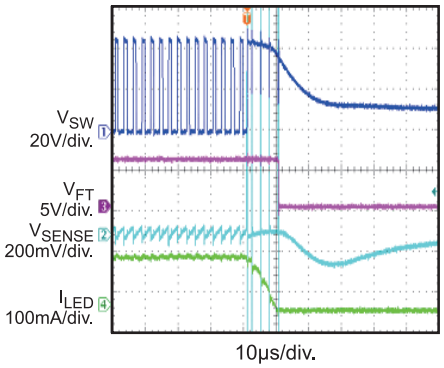
Short One String



Short Inductor Protection



Short Diode Protection
30mA/String



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PIN FUNCTIONS

Package Pin #	Name	Description
1	DRV	**Step-up converter power switch gate output.** DRV drives the external power N-MOSFET device. It is recommended to connect a resistor (e.g.,10Ω) to DRV
2	VCC	**Internal 6V linear regulator output.** VCC provides the power supply for the external MOSFET switch gate driver and the internal control circuitry. Bypass VCC to GND with a ceramic capacitor.
3	EN	**Enable control input.** A voltage greater than 1.5V turns the part on. A voltage less than 0.6V turns the part off. Do NOT float EN.
4	VIN	**Supply input.** VIN must be bypassed locally.
5	PWM	**PWM input signal for brightness control.** Make sure the PWM amplitude voltage level > VPWM_HI, and the low-level voltage < VPWM_LO. Mainly, the input PWM signal frequency determines the LED current dimming ratio when the part works in direct PWM dimming mode. For analog and mixed dimming, the PWM pulse is filtered to a DC by an LPF capacitor, and the LED current is proportional to the input PWM duty. If PWM is floated, internally pull PWM to GND weakly.
6	SCL	**I²C clock input.**
7	SDA	**I²C data input.**
8	FT	**Fault indication output**. FT is an open drain during normal operation. It is pulled low during a fault condition.
9	LPF	**Low pass filter output for analog dimming with PWM input.** A capacitor is connected between LPF and GND when the part operates in external PWM input analog dimming or mixed dimming. Remove the LPF capacitor when the part operates in direct PWM dimming mode.
10	OSC	**Switching frequency set.** Connect a resistor (R_{osc}) between OSC and GND to set the step-up converter switching frequency. The clock frequency is proportional to the current sourced from OSC. There is a 100~900kHz switching frequency selected by the I²C interface when connected to a 100kΩ resistor at OSC.
11	COMP	**Step-up converter compensation.** COMP compensates the regulation control loop. Connect a ceramic capacitor and resistor from COMP to GND.
12	ISET	**LED current set.** Tie a current-setting resistor from ISET to ground to program the current in each LED string.
13	LED4	**LED string 4 current input.** LED4 is the open-drain output of an internal dimming control switch. Connect the LED string 4 cathode to LED4.
14	LED3	**LED string 3 current input.** LED3 is the open-drain output of an internal dimming control switch. Connect the LED string 3 cathode to LED3.
15	PGND	**Power ground.**
16	LED2	**LED string 2 current input.** LED2 is the open-drain output of an internal dimming control switch. Connect the LED string 2 cathode to LED2.
17	LED1	**LED string 1 current input.** LED1 is the open-drain output of an internal dimming control switch. Connect the LED string 1 cathode to LED1.
18	OVP	**Output over-voltage protection.**
19	IS	**Current sense input.** During normal operation, IS senses the voltage across the external inductor current-sensing resistor (R_{SENSE}) for peak-current–mode control. Also, it limits the inductor current during every switching cycle. If the MP3385 is used for cascading applications, IS of the slave chip should be tied to GND. Do NOT float IS.
20	AGND	**Signal ground.**

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FUNCTIONAL BLOCK DIAGRAM

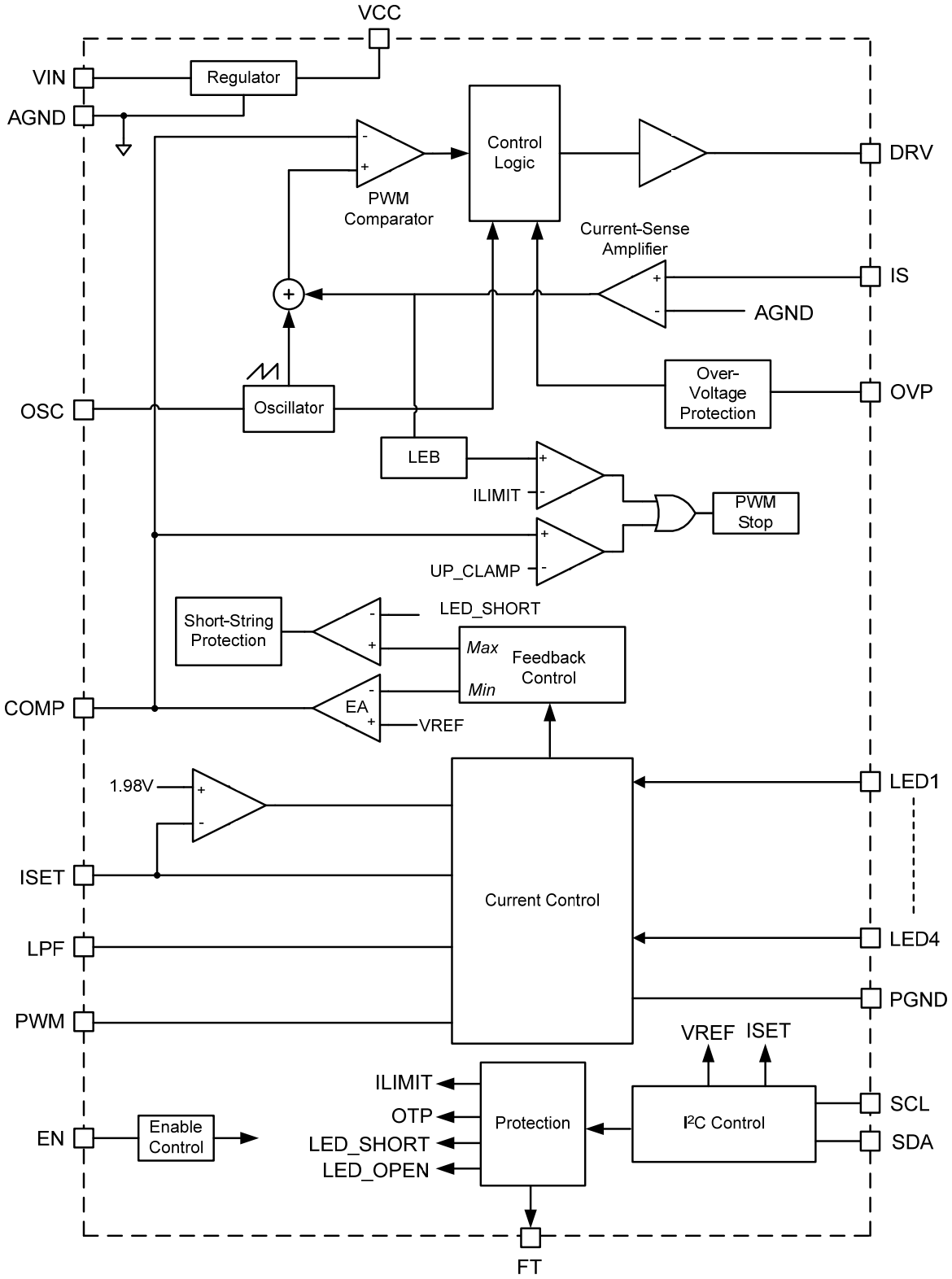

Figure 2: MP3385 Block Diagram

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OPERATION

The MP3385 employs a programmable constant frequency, peak current mode step-up converter with 4 regulated current channels to drive an array of 4 strings of white LEDs. It has an I²C interface for easy communication that flexibly sets the operation modes.

Internal 6V Regulator

The MP3385 includes an internal linear regulator (VCC). When VIN is greater than 6.5V, the regulator outputs a 6V power supply to the external MOSFET switch gate driver and the internal control circuitry. The VCC voltage drops to 0V when the chip shuts down. The MP3385 features under-voltage lockout (UVLO). The chip is disabled until VCC exceeds the UVLO threshold. The UVLO hysteresis is approximately 340mV.

System Start-Up

When enabled, the MP3385 checks the topology connection first. The chip monitors the over-voltage protection (OVP) pin to see if the Schottky diode is connected or if the boost output is shorted to GND. An OVP voltage higher than 2.5V allows the chip to switch normally. Otherwise, the switching is disabled. The MP3385 checks additional safety limits including LED open/short protection, UVLO, over-temperature protection (OTP), and over-current protection (OCP) after passing the OVP test. If all the protection tests pass, the chip starts boosting the step-up converter with an internal soft start.

Step-Up Converter

At the beginning of each switching cycle, the internal clock turns on the external MOSFET. (In normal operation, the minimum turn-on time is around 150ns.) A stabilizing ramp is added to the output of the current sense amplifier to prevent sub-harmonic oscillations for duty cycles greater than 50%. This result is fed into the PWM comparator. When the summed voltage reaches the output voltage of the error amplifier (V_{COMP}), the external MOSFET turns off.

The output voltage of the internal error amplifier is an amplified signal of the difference between the reference voltage and the feedback voltage. Automatically, the converter chooses the lowest active LEDX voltage to provide a high enough bus voltage to power all the LED arrays.

If the feedback voltage drops below the reference, the output of the error amplifier increases. This results in more current flowing through the MOSFET, thus increasing the power delivered to the output. This forms a closed loop that regulates the output voltage.

Under light-load operation, especially in the case of $V_{OUT} \approx V_{IN}$, the converter runs in pulse-skipping mode where the MOSFET turns on for a minimum on time, and then the converter discharges the power to the output for the remaining period. The external MOSFET remains off until the output voltage needs to be boosted again.

Dimming Control

The MP3385 provides flexible dimming methods according to the dimming mode settings below.

1) PWM Dimming Mode:

MODE bits = 00. The LED current duty cycle directly follows the PWM input signal duty cycle when INTERFACE = 0. The IC works in internal PWM dimming mode, and the LED current duty cycle is set by the internal registers 03H and 04H when INTERFACE = 1. The internal dimming frequency is fixed at 23kHz.

2) Analog Dimming Mode:

MODE bits = 01. The LED current amplitude follows the duty cycle of the input PWM signal when INTERFACE = 0. The IC works in internal analog dimming mode (the LED current amplitude follows the internal register value of 03H and 04H) if INTERFACE = 1.

3) Mixed Dimming Mode:

There are two transfer points from analog to PWM dimming (25% or 50%) set by the I²C interface.

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If MODE bits are set to 10 (when the dimming duty cycle is larger than the 25% threshold), the IC works in analog dimming mode. Otherwise, the IC works in PWM dimming mode, and the LED current follows the PWM ratio. If MODE bits are set to 11 (when the dimming duty cycle is larger than the 50% threshold), the IC works in analog dimming mode. Otherwise, the IC works in PWM dimming mode.

In mixed dimming mode (when INTERFACE is set to 0), the LED current amplitude is proportional to the ratio of the external PWM signal if the duty cycle of PWM is larger than the transfer point (25% or 50%). The LED current amplitude is fixed to 100% brightness while the LED current duty is equal to the input PWM ratio (if the duty cycle of PWM is lower than the transfer point). When INTERFACE is set to 1, the LED current amplitude and the duty cycle is set by registers 03H and 04H.

Regardless of the INTERFACE setting (1 or 0), the LED current frequency is fixed to 23kHz in mixed dimming mode when the duty cycle < the transfer point (25% or 50%).

In analog and mixed dimming mode, to avoid noise at the small dimming ratio, the IC turns off the current sources if the current is less than 1.2% times the full scale current.

For external analog and mixed dimming mode, the smallest pulse width of the PWM signal is limited to 2μs to avoid noise interruption.

Operation Switching Frequency

The operation frequency of the converter can be changed by the OSC resistor and the FS0-3 bit in register 01H. The switching frequency covers 100kHz to 900kHz through the I²C register bits when a 100kΩ resistor is connected to OSC. This optimizes the size of the external components and system efficiency.

Open-String Protection

Open-string protection is achieved through the OVP pin and the LED(1 to 4) pins. If one or more strings are open, the respective LEDX pins are pulled to ground; the IC keeps charging the output voltage until it reaches the over-voltage protection (OVP) threshold. If the OVP point has been triggered, the chip stops switching and marks the strings which have an LEDX pin voltage lower than 206mV. Once marked, the remaining LED strings force the output voltage back into tight regulation. The string with the largest voltage drop determines the output regulation.

The MP3385 always attempts to light at least one string. If all strings are open, the MP3385 shuts down the step-up converter. The strings remain in this marked state until the chip resets.

Unused LED String Auto-Detection

For the MP3385, if an LED string is open or unused before start-up, automatically the IC detects and marks off the open channel to avoid the output charging to the OVP value. This function avoids start-up failure, which is caused by the LED short string mis-protection due to OVP triggering. This is helpful for application use and test board debugging. The unused LED string auto-detection function is disabled if the OVP point is changed by the I²C after EN and VIN power on, and I²C is active.

In addition, the MP3385 disables the unused LED string by disabling the corresponding register control bit for each 4-channel current source. In some applications, if less than 4 LED strings are needed, the unused LED current sources can be disabled by setting the LED1/2/3/4 bit to 0 in register 00H.

Short-String Protection

The MP3385 monitors the LEDX pin voltages to determine if a short-string fault has occurred. If one or more strings are shorted, the respective LEDX pins tolerate high-voltage stress. If an LEDX pin voltage is higher than the protection threshold, which can be programmable by LEDS0/1/2 bits in 01H, this condition triggers the detection of a short-string fault. When a short-string fault remains for longer than 10ms, the fault string is marked off and disabled. Once a string is marked off, it disconnects from the output voltage loop until VIN or EN re-starts.

Cycle-by-Cycle Current Limit

To prevent the external components exceeding the current stress rating, the IC has cycle-by-cycle current limit protection. The limit value is programmable from 150mV to 500mV by OCP0/1/2 bits in register 05H. When the current exceeds the current limit value, the IC latches

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off until the power is reset or ENABLE is toggled when operating in latch-off mode (if OCPM = 0). The device re-starts when the current drops below the current limit again (if OCPM = 1).

Short Inductor/Diode Protection

When the external inductor or diode is shorted, the IC provides protection by detecting the current flowing through the power MOSFET. When the current sense voltage across the sense resistor (connected between IS and GND) hits the current protection threshold and lasts for 4 switching cycles, the IC stops switching and latches.

Thermal Shutdown Protection

To prevent the IC from operating at exceedingly high temperatures, thermal shutdown is implemented to detect the silicon die temperature. When the die temperature exceeds the upper threshold (T_{ST}), the IC shuts down. The IC resumes normal operation when the die temperature drops below the lower threshold. Typically, the hysteresis value is 25°C.

Fault Flag Output and Fault Register Indicator

FT remains in an open-drain condition when the LED driver is operating in a normal condition. It is connected to VCC by an external 100kΩ resistor and pulled to logic high when there is no fault. FT goes to logic low if a fault occurs. Meanwhile, set the corresponding fault bit in register 03H to 1.

I²C Interface Register Description

I²C Chip Address:

After the start condition, the I²C compatible master sends a 7-bit address followed by an eighth read (Read: 1) or write (Write: 0) bit. The following bit indicates the register address to/from which the data will be written/read (see Figure 3).

0	1	1	0	0	0	1	R/W

Figure 3: The I²C Compatible Device Address

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Register Mapping:

Add	D7	D6	D5	D4	D3	D2	D1	D0
00H	LED4	LED3	LED2	LED1	NA	INTERFACE	MODE1	MODE0
01H	OCPM	LEDS2	LEDS1	LEDS0	FS3	FS2	FS1	FS0
02H	ILED7	ILED6	ILED5	ILED4	ILED3	ILED2	ILED1	ILED0
03H	DIODEO_F	OVP_F	OCP_F	LEDS_F	LEDO_F	OTP_F	DIM1	DIM0
04H	DIM9	DIM8	DIM7	DIM6	DIM5	DIM4	DIM3	DIM2
05H	OVP4	OVP3	OVP2	OVP1	OVP0	OCP2	OCP1	OCP0
06H	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

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Table 1: Dimming Mode Register

Addr: 0x00				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:4	LED1/2/3/4	RW	1111	LED current source enable bits. LED1/2/3/4 controls the internal LED current sources, respectively. LED1: LED current source 1; 1 = enabled. 0 = Disabled. LED2: LED current source 2; 1 = enabled. 0 = Disabled. LED3: LED current source 3; 1 = enabled. 0 = Disabled. LED4: LED current source 4; 1= enabled. 0 = Disabled
3	NA	RW	NA	NA
2	INTERFACE	RW	0	Dimming input interface set bit. 0 = Dimming control by PWM input signal. 1 = Dimming control by I²C interface.
1:0	MODE	RW	00	Dimming mode setting bits. 00 = PWM mode. The LED current duty cycle directly follows the PWM input signal duty cycle when INTERFACE = 0. The IC works in internal PWM dimming mode, and the LED current duty cycle is set by the internal registers 03H and 04H when INTERFACE = 1. The internal dimming frequency is fixed at 23kHz. 01 = Analog dimming mode. The LED current amplitude follows the duty cycle of the input PWM signal when INTERFACE = 0 and follows the internal register value of 03H and 04H if INTERFACE = 1. 10 = Mixed dimming mode. When the dimming duty cycle is larger than the 25% threshold, the IC works in analog dimming mode. Otherwise, the IC works in PWM dimming mode. 11 = Mixed dimming mode. When the dimming duty cycle is larger than the 50% threshold, the IC works in analog dimming mode. Otherwise, the IC works in PWM dimming mode.

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Table 2: Operation Frequency Register

Addr: 0x01				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7	OCPM	RW	0	Mode selection bit for cycle-by-cycle current limit. 0 = Latch-off mode current limit. 1 = Recoverable mode current limit.
4:6	LEDS0-2	RW	100	LED short protection threshold. 000 = 4V, 001 = 5V, 111 = 11V, 1V/step. Default value is 8V.
3:0	FS0-3	RW	0100	Boost converter operation frequency set bits. 0000b = Boost converter off. 0001b-1001b is corresponding to 100kHz-900kHz, respectively. Default frequency is 400kHz.

Table 3: LED Current Full Scale Register

Addr: 0x02				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:0	ILED0-7	RW	00111011	LED current full scale set bits. The set value corresponds to the 2%-100% external setting current value by a resistor. 00000000b = 2%. 11111111b = 100%. 0.39% per step. The default value is 25%.

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Table 4: Fault Indication Register

Addr: 0x03				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7	DIODEO_F	R	0	Diode open fault indication bit. 1 = Fault, 0 = Normal.
6	OVP_F	R	0	Output over-voltage fault indication bit. 1 = Fault, 0 = Normal.
5	OCP_F	R	0	Converter over-current fault indication bit. 1 = Fault, 0 = Normal.
4	LEDS_F	R	0	LED string short fault indication bit. 1 = Fault, 0 = Normal.
3	LEDO_F	R	0	LED string open fault indication bit. 1 = Fault, 0 = Normal.
2	OTP_F	R	0	IC over-temperature fault indication bit. 1 = Fault, 0 = Normal.
1:0	DIM0-1	R/W	11	2 LSB bits of LED dimming brightness set bits.

Table 5: Internal LED Dimming Brightness Register

Addr: 0x04				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:0	DIM2-9	RW	7FH	8 MSB bits of LED dimming brightness set bits. 0.098% per step. Default value is 50% dimming brightness.

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Table 6: OVP and OCP Protection Threshold Register

Addr: 0x05				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:3	OVP0-4	RW	11100	Output over-voltage protection threshold setting based on the OVP pin connected to the LED anode. 00000 = 18V, 00001 = 20V, 11100 = 74V, 11111 = 80V. 2V/step. Default value is 74V.
2:0	OCP0-2	RW	111	Converter over-current protection threshold. 000 = 0.15V, 111 = 0.5V. 50mV/step. Default value is 0.5V.

Table 7: Vendor ID Register

Addr: 0x06				
Bit	**Bit Name**	**Access**	**Default**	**Description**
7:0	ID0-7	R	01H	Vendor ID information. Returns 01H when read.

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APPLICATION INFORMATION

Selecting the Switching Frequency

The operation frequency of the converter depends on both the resistor at OSC and the FS0-3 bit in register 01H. If a 100kΩ resistor is selected for Rosc (connected to OSC), the switching frequency is set from 100kHz-900kHz by the I²C interface. 0001b-1001b corresponds to 100kHz-900kHz respectively. Table 8 shows the list of switching frequencies.

Table 8: Switching Frequencies

FS0-3	Switching Frequency	Unit
0000b	Converter off	
0001b	100	kHz
0010b	200	
0011b	300	
0100b	400	
0101b	500	
0110b	600	
0111b	700	
1000b	800	
1001b	900	

Without the I²C interface, an oscillator resistor on OSC sets the internal oscillator frequency for the step-up converter according to Equation (1):

$$F_{SW}(kHz) = \frac{40000}{R_{OSC}(k\Omega)} \quad (1)$$

For R_{OSC} = 100kΩ, the switching frequency is set to 400kHz.

Setting the LED Current

The current of each LED string is set through the current setting resistor on ISET and the full scale LED current setting bits ILED0-7 in the 02H table.

When the INTERFACE bit in 00H is 0, the LED current is dependent on the input PWM dimming duty cycle. The setting formula is calculated using Equation (2) and Equation (3):

$$ILED(mA) = \frac{1.98V}{R_{ISET}(k\Omega)} * K_{FullScale} * 10200 \quad (2)$$

When INTERFACE bit in 00H is 1,

$$ILED(mA) = \frac{1.98V * K_{DIM}}{R_{ISET}(k\Omega)} * K_{FullScale} * 10200 \quad (3)$$

$K_{FullScale}$ is the ratio, which is set by the full scale LED current setting bits ILED0-7 in the 02H table.

K_{DIM} is the ratio, which is set by the dimming current setting bits DIM0-9 in 03H and 04H.

Without the I²C interface, the current of each LED string is set through the resistor on ISET according to Equation (4):

$$ILED(mA) = \frac{1.98V}{R_{ISET}(k\Omega)} * 0.2294 * 10200 \quad (4)$$

For R_{ISET} = 46.4kΩ, the LED current is set to 100mA. Please do NOT leave ISET open.

Selecting the Input Capacitor

The input capacitor reduces the surge current drawn from the input supply and the switching noise from the device. The input capacitor impedance at the switching frequency should be less than the input source impedance to prevent the high-frequency switching current from passing through to the input. Use ceramic capacitors with X5R or X7R dielectrics for their low ESR and small temperature coefficients. For most applications, use a 4.7μF ceramic capacitor in parallel with a 220μF electrolytic capacitor.

Selecting the Inductor and Current Sensing Resistor

A larger value inductor results in less ripple current, resulting in lower peak inductor current, which reduces stress on the N-channel MOSFET. However, the larger value inductor has a larger physical size, a higher series resistance, and a lower saturation current. Choose an inductor that does not saturate under the worst-case load conditions. Select the minimum inductor value to ensure that the boost converter works in continuous conduction mode (CCM) with high efficiency and good EMI performance.

Calculate the required inductance value using Equation (5) and Equation (6):

$$L \geq \frac{\eta \times V_{OUT} \times D \times (1-D)^2}{2 \times f_{SW} \times I_{LOAD}} \quad (5)$$

$$D = 1 - \frac{V_{IN}}{V_{OUT}} \quad (6)$$

Where V_{IN} and V_{OUT} are the input and output voltages, f_{SW} is the switching frequency; I_{LOAD} is the LED load current, and η is the efficiency.

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Usually, the switching current is used for peak-current-mode control. In order to avoid hitting the current limit, the voltage across the sensing resistor (R_{SENSE}) must be less than 70% of the current-limit voltage (V_{SENSE}), in worst cases. See Equation (7) and Equation (8):

$$R_{SENSE} = \frac{0.7 \times V_{SENSE}}{I_{L(PEAK)}} \quad (7)$$

$$I_{L(PEAK)} = \frac{V_{OUT} \times I_{LOAD}}{\eta V_{IN}} + \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times L \times F_{SW} \times V_{OUT}} \quad (8)$$

The current limit setting voltage (V_{SENSE}) is set by the OCP0-2 bits in register 05H.

Selecting the Power MOSFET

The MP3385 is capable of driving a wide variety of N-channel power MOSFETS. The critical parameters of selection for a MOSFET are:

1. maximum drain-to-source voltage, $V_{DS(MAX)}$
2. maximum current, $I_{D(MAX)}$
3. on resistance, $R_{DS(ON)}$
4. gate-source charge (Q_{GS}) and gate-drain charge (Q_{GD}), and
5. total gate charge (Q_G).

Ideally, the off-state voltage across the MOSFET is equal to the output voltage. Considering the voltage spike when it turns off, $V_{DS(MAX)}$ should be greater than 1.5x the output voltage.

The maximum current through the power MOSFET occurs at the minimum input voltage and the maximum output power. The maximum RMS current through the MOSFET is given by Equation (9) and Equation (10):

$$I_{RMS(MAX)} = I_{IN(MAX)} \times \sqrt{D_{MAX}} \quad (9)$$

$$D_{MAX} \approx \frac{V_{OUT} - V_{IN(MIN)}}{V_{OUT}} \quad (10)$$

The current rating of the MOSFET should be greater than 1.5 x I_{RMS}

The on resistance of the MOSFET determines the conduction loss. See Equation (11):

$$P_{cond} = I_{RMS}^{2} \times R_{DS(on)} \times k \quad (11)$$

Where k is the temperature coefficient of the MOSFET.

The switching loss is related to Q_{GD} and Q_{GS}, which determine the commutation time. Q_{GS1} is the charge between the threshold voltage and the plateau voltage when a driver charges the gate, which can be read in the chart of V_{GS} vs. Q_G of the MOSFET datasheet. Q_{GD} is the charge during the plateau voltage. These two parameters are needed to estimate turn-on and turn-off losses. See Equation (12):

$$P_{SW} = \frac{Q_{GS1} \times R_G}{V_{DR} - V_{TH}} \times V_{DS} \times I_{IN} \times f_{SW} + \frac{Q_{GD} \times R_G}{V_{DR} - V_{PLT}} \times V_{DS} \times I_{IN} \times f_{SW} \quad (12)$$

Where V_{TH} is the threshold voltage, V_{PLT} is the plateau voltage; R_G is the gate resistance, and V_{DS} is the drain-source voltage. Please note that calculating the switching loss is the most difficult part in the loss estimation. The formula above provides a simplified equation. For more accurate estimates, the equation becomes much more complex. The total gate charge (Q_G) is used to calculate the gate-drive loss. See Equation (13):

$$P_{DR} = Q_G \times V_{DR} \times f_{SW} \quad (13)$$

Where V_{DR} is the drive voltage.

Selecting the Output Capacitor

The output capacitor keeps the output voltage ripple small and ensures feedback loop stability. The output capacitor impedance must be low at the switching frequency. Ceramic capacitors with X7R dielectrics are recommended for their low ESR characteristics. For most applications, a 4.7μF ceramic capacitor in parallel with a 22μF electrolytic capacitor will suffice.

Setting the Over-Voltage Protection

Open-string protection is achieved through the detection of the voltage on the OVP pin. In some cases, an LED string failure results in the feedback voltage always at zero. The part then keeps boosting the output voltage higher and higher. If the output voltage reaches the programmed OVP threshold, the protection will be triggered.

To ensure the chip functions properly, an appropriate OVP voltage is needed. The recommended OVP point is about 1.1 to 1.2x higher than the output voltage for normal operation. If the OVP pin is connected to the anode of the LED load, the OVP protection

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voltage is set by the OVP0-4 bits in register 05H. It is not recommended to set the OVP value higher than 80V, considering the LED return pin voltage rating.

If the MP3385 is applied for >80V output voltage application through an external extension, connect a proper resistor (R_{OVP}) between the anode of the LED and OVP pin to change the over-voltage point of the output (V_{OVP}). V_{OVP} calculation with R_{OVP} is given with Equation (14):

$$V_{OVP}(V)=\frac{R_{OVP}(k\Omega)+1600}{40}*1.9 \quad (14)$$

Where OVP0-4 bit in register 05H is the set default.

Expanding LED Channels

The MP3385 expands the number of LED channels by using two or three ICs in parallel. To connect two ICs for a total of 8 LED strings, tie the VCC pins of the master IC and the slave IC together to power the slave IC internal logic circuitry. Tie the COMP pins of the slave IC and the master IC together to regulate the voltage of all 8 strings LEDs. The slave IC MOSFET driving signals are not used; the boost converter can be driven only by the master IC. Do NOT leave ISENSE of the slave IC floating; tie it to ground. Apply the EN and DIM signals to both ICs. The master IC's OVP should be higher than the slave IC's OVP.

PCB Layout Guidelines

Efficient PCB layout is critical to reduce EMI noise. For best results, refer to the guidelines below:

1. Make the loop from the external MOSFET, through the output diode and the output capacitor as small and short as possible as they carry a high-frequency pulse current.
2. Separate the power ground (PGND) and signal ground (GND), then connect PGND and GND together. All logic signals refer to the signal ground in order to reduce the noise affection.
3. Place ceramic capacitors for VIN and VCC pins as close as possible.

TYPICAL APPLICATION CIRCUITS

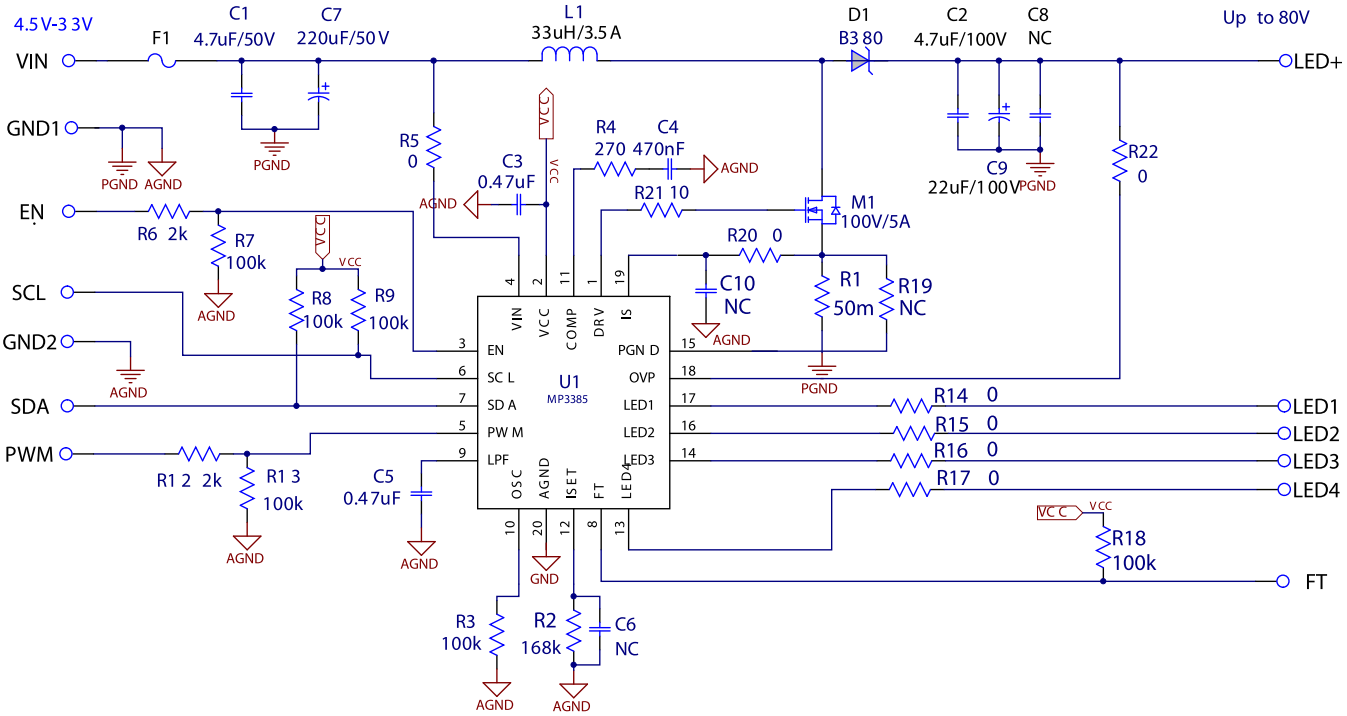

Figure 4: Driving 4 LED Strings and output voltage<80V

Note: Remove the LPF capacitor (C5) when the MP3385 works in direct PWM dimming. Some components value may need to be adjusted for different application condition

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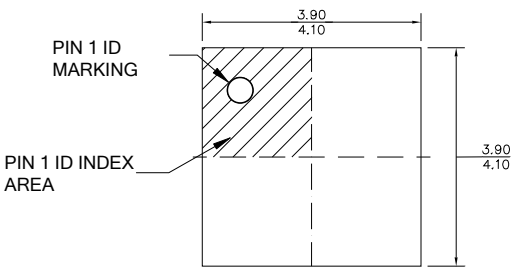
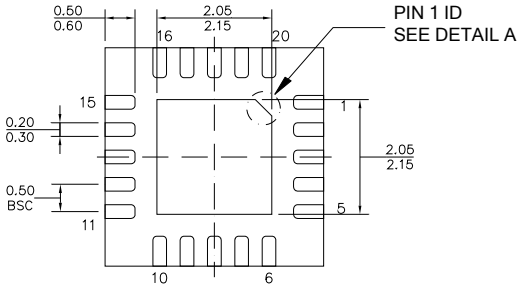
PACKAGE INFORMATION

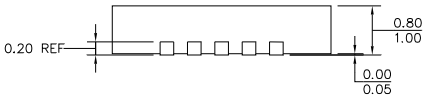
QFN-20 (4mm x 4mm)



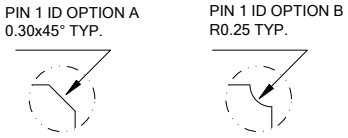
TOP VIEW



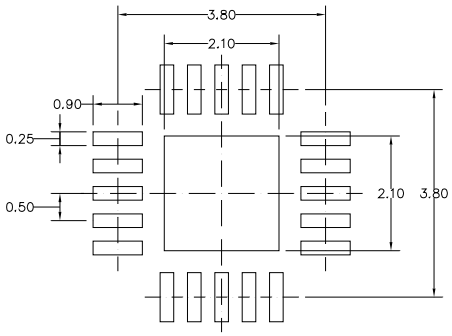
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220
5) DRAWING IS NOT TO SCALE.

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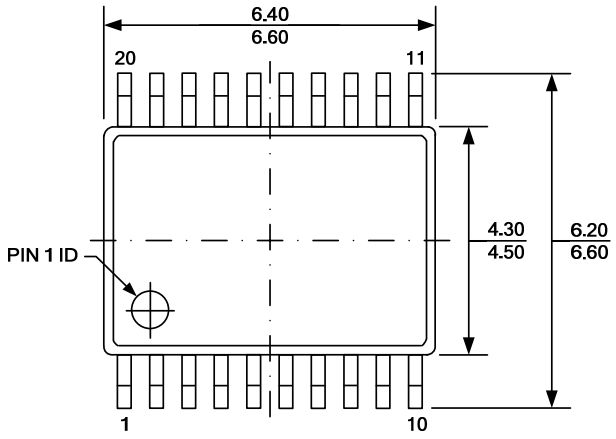
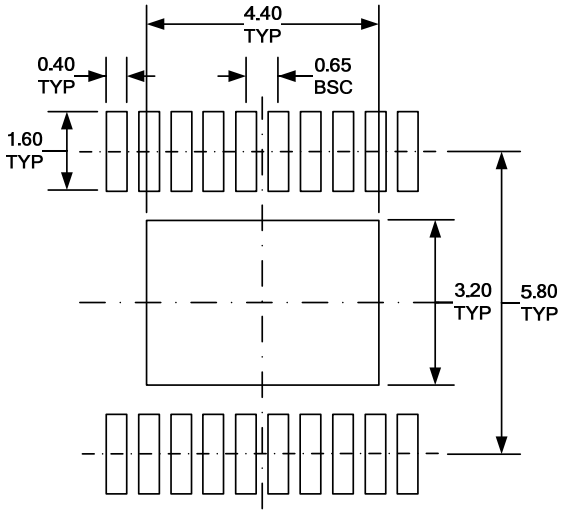
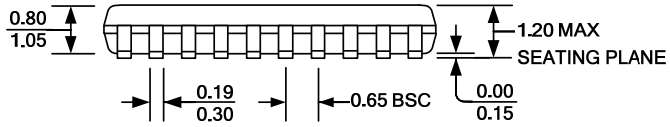
TSSOP20-EP



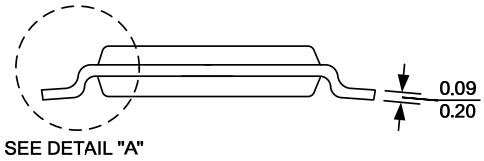
TOP VIEW



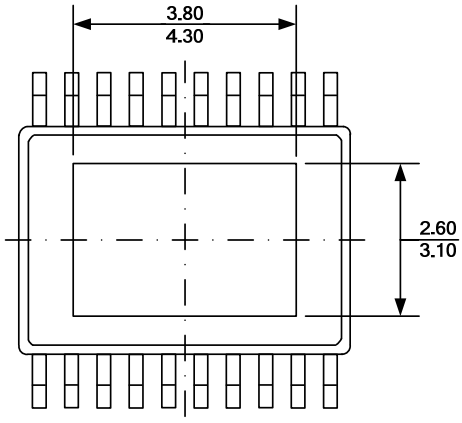
RECOMMENDED LAND PATTERN



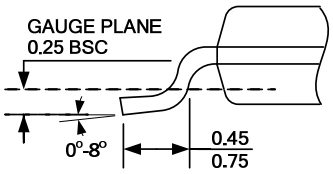
FRONT VIEW



SIDE VIEW



BOTTOM VIEW



DETAIL “A”

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION ACT.
6) DRAWING IS NOT TO SCALE.

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