MP2772

I²C-Controlled, 2A Battery Charger with ADC, Power Path, Load Switch, and Boost Operation

DESCRIPTION

The MP2772 is a highly integrated, switching battery charger that provides a complete solution for wearable and portable devices. The device provides an 8-bit successive approximation register (SAR) analog-to-digital converter (ADC) for battery and system monitoring, smart power path management, narrow-voltage DC (NVDC) charging, push-button control, integrated load switches with an individual enable function, and an autonomous battery charging profile.

The MP2772 integrates a battery charger, boost converter, and two embedded load switches into a single device. Only one inductor is required to charge a battery or boost the battery voltage to charge the device through load switches. The device achieves a low quiescent current (I_Q) down to 5μA in shipping mode and provides a low I_Q for battery self-life extension in light-load boost operation. The integrated ADC monitors battery charging parameters and load parameters during boost operation.

The MP2772 provides various safety features for battery charging and system operations, including the charge safety timer, battery and junction temperature (T_J) monitoring, over-voltage protection (OVP), and over-current protection (OCP). If a fault condition occurs, the device asserts an interrupt signal to the microcontroller unit (MCU) host.

The MP2772 also provides battery MOSFET disable control to enter shipping mode and reset the system via the /DISC pin.

The MP2772 is available in a WLCSP-30 (2.5mmx2.85mm) package.

FEATURES

- High-Performance Buck Charger:
  - Up to 6.5V Operating Input Voltage (V_{IN})
  - 26V Sustainable V_{IN}
  - Charge Efficiency is >95% at 0.5A and >94% at 1A (V_{IN} = 5V)
  - ±0.5% Charge Voltage Regulation Accuracy

FEATURES *(continued)*

  - 100mA to 3.2A I²C-Configurable Input Current Limit Compatible with BC1.2
  - 20mA to 2A I²C-Configurable Charge Current with 20mA/Step Resolution
  - Down to 10mA Termination Current
- Boost Operation:
  - Low-I_Q, Light-Load Boost Operation
  - Automatic Transition from Buck to Boost
  - Up to 6V I²C-Configurable Boost Output with 0.1V/Step Resolution
  - Up to 1.5A of I_{OUT} in OTG Mode
- Safety:
  - Safety Timers for Fast Charge, Pre-Charge, and Watchdog
  - I²C-Configurable JEITA Profile for Safety Operation
  - Adjustable Thermal Regulation Loop and Thermal Shutdown Protection
  - Input, Battery, and System OVP
- Dual, Integrated Load Switches with OCP and Short-Circuit Protection (SCP)
- Integrated ADC for Charge and Discharge Parameters
- NVDC Power Path Enabling System Instant Start-Up with Deeply Discharged Battery
- Battery Supplement Mode Provides Battery Current to Support Heavy System Loads
- Below 5μA Battery Discharge Current in Shipping Mode
- Integrated, 30mΩ, Low-$R_{DS(ON)}$ Battery MOSFET (BATFET) with Shipping Mode and System Power Reset Function
- Available in a Small WLCSP-30 (2.5mmx2.85mm) Package

APPLICATIONS

- Wearable Devices
- Earbud Charging Cases
- Headsets and Headphones
- Internet of Things (IoT) Devices

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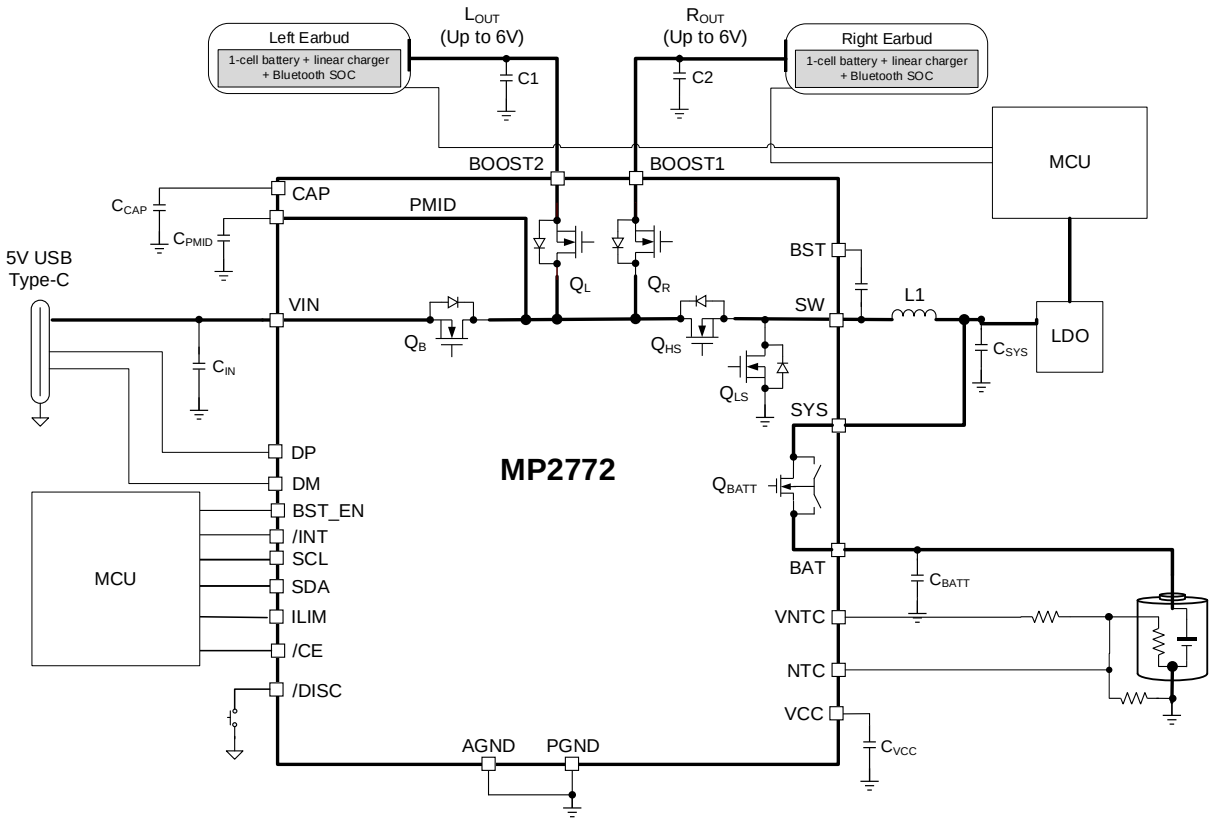
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP2772GC-xxxx**	WLCSP-30 (2.5mmx2.85mm)	*See Below*	1
EVKT-MP2772	Evaluation kit		

* For Tape & Reel, add suffix -Z (e.g. MP2772GC-xxxx-Z).

** “xxxx” is the register setting option. The factory default is “0000”. The content can be viewed in the register map. Contact an MPS FAE to obtain an “xxxx” value.

TOP MARKING

MPYYWW
MP2772
LLLLLL
AABBID

MP: MPS prefix
YY: Year code
WW: Week code
MP2772: Part Number
LLLLLL: Lot number
AABB: Die ID in X axis and Y axis
ID: Wafer

EVALUATION KIT EVKT-MP2772

EVKT-MP2772 kit contents (items below can be ordered separately):

#	Part Number	Item	Quantity
1	EVL2772-C-00A	MP2772 evaluation board	1
2	EVKT-USBI2C-02-BAG	Includes one USB-to-I²C communication interface, one USB cable, and one ribbon cable	1
3	Online resources	Include datasheet, user guide, product brief, and GUI	1

Order directly from MonolithicPower.com or our distributors.

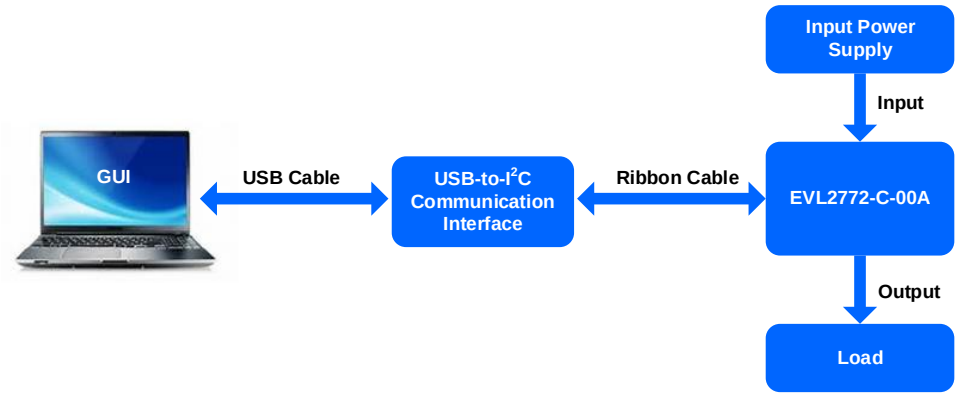

Figure 1: EVKT-MP2772 Evaluation Kit Set-Up

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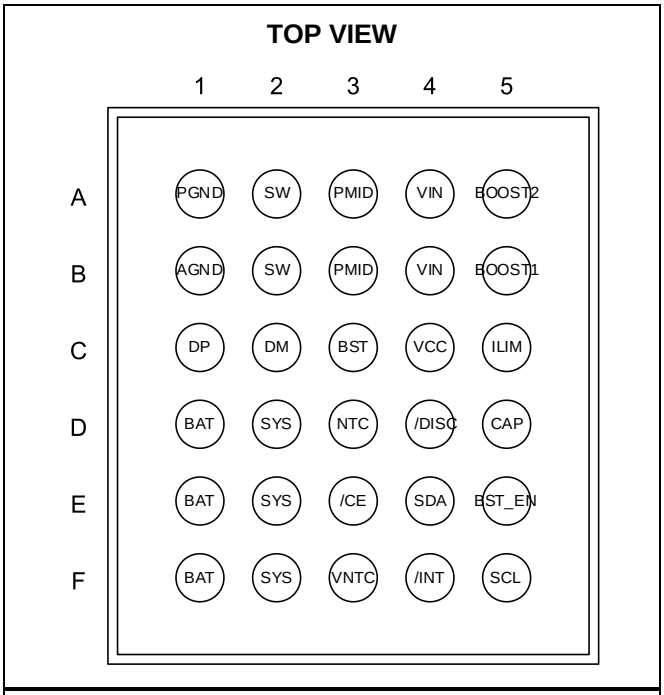
PACKAGE REFERENCE



WLCSP-30 (2.5mmx2.85mm)

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PIN FUNCTIONS

Pin #	Name	Description
A1	PGND	**Power ground.**
B1	AGND	**Analog ground.**
A2, B2	SW	**Switching node.** Connect the SW pin to the inductor.
A3, B3	PMID	**Internal power.** Bypass the PMID pin by connecting a 10µF capacitor between the PMID and PGND pins, placed as close as possible to the IC.
A4, B4	VIN	**Power input.** Bypass the VIN pin by connecting a minimum 1µF capacitor between the VIN and PGND pins.
A5	BOOST2	**Boost load switch mode output 2.** Place a 2.2µF to 4.7µF capacitor between the BOOST2 and PGND pins.
B5	BOOST1	**Boost load switch mode output 1.** Place a 2.2µF to 4.7µF capacitor between the BOOST1 and PGND pins.
C1	DP	**Positive pin of the USB data line pair.**
C2	DM	**Negative pin of the USB data line pair.**
C3	BST	**Bootstrap power for driving the high-side MOSFET (HS-FET).** Connect a 47nF bootstrap capacitor (C_{BST}) between the BST and SW pins to form a floating supply for the HS-FET driver.
C4	VCC	**Internal LDO output.** Connect the VCC pin to a 2.2µF capacitor.
C5	ILIM	**Input current limit configuration.** Pull the ILIM pin logic high to set the input current limit (I_{IN_LIMIT}) to 2.5A; pull ILIM logic low to set I_{IN_LIMIT} to 0.5A.
D1, E1, F1	BAT	**Battery positive terminal.** The internal NVDC battery MOSFET is connected between the BAT and SYS pins. Place a minimum 10µF ceramic capacitor between BAT and PGND.
D2, E2, F2	SYS	**System power supply.** Place a 10µF ceramic capacitor between the SYS and PGND pins.
D3	NTC	**Temperature sense input.** Connect the NTC pin to a negative temperature coefficient (NTC) thermistor.
D4	/DISC	**Shipping mode entry and system power reset control.** Toggle the /DISC pin low to perform battery MOSFET reset or enter shipping mode.
D5	CAP	**External capacitor for charge pump power storage.** Place a 100nF capacitor between the CAP and AGND pins.
E3	/CE	**Enable for battery charging.** Pull the /CE pin low to enable charging. /CE is low by default, and the pin can be disabled via the PIN_CTRL_EN bit (01h, bit[4]).
E4	SDA	**I²C interface data.** Connect the SDA pin to the logic rail via a 10kΩ resistor.
E5	BST_EN	**Enable for boost switching.** Pull the BST_EN pin high to enable the boost function. BST_EN is low by default, and the pin can be disabled via the PIN_CTRL_EN bit.
F3	VNTC	**Reference voltage output.** The VNTC pin powers up the NTC resistor dividers.
F4	/INT	**Open-drain interrupt output.** The /INT pin is high by default. A 256µs low pulse is generated on /INT when the IC has a status or fault report. Pull up /INT via a 10kΩ resistor.
F5	SCL	**I²C interface clock.** Connect the SCL pin to the logic rail via a 10kΩ resistor.

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ABSOLUTE MAXIMUM RATINGS (1)

VIN to PGND .....-0.3V to +26V (2)
PMID to PGND .....-0.3V to +26V (2)
SW to PGND.....-0.3V to +26V (2)
SYS to PGND .....-0.3V to +6V
BATT to PGND…….....-0.3V to +5.5V
BOOST1, BOOST2 to PGND .....-0.3V to +7.5V
CAP to AGND……...-0.3V to +9V
BST to SW…….....-0.3V to +4V
VCC to AGND……. .....-0.3V to +4V
All other pins to AGND.....-0.3V to VCC + 0.3V
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Continuous power dissipation (T_A = 25°C) (3)
..... 2.5W

ESD Ratings

Human body model (HBM) 2000V
Charged-device model (CDM).....500V

Recommended Operating Conditions (4)

Supply voltage (V_{IN}) .....4V to 6.5V
System current (I_{SYS}).....Up to 2.5A
Fast charge current (I_{CC}).....Up to 2A
Battery discharge current (I_{DISCHG}) .....Up to 4.5A
Battery voltage (V_{BATT}) .....Up to 4.6V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (5) θ_{JA} θ_{JC}

WLCSP-30 (2.5mmx2.85mm).....
.....68.5.....0.4...°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) These absolute maximum ratings are rated under room temperature.
3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on a JESD51-7, a 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, T_A = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Quiescent Current						
Battery discharge current in shipping mode	I_{BAT_SHIP}	V_{BATT} = 4V, V_{IN} = 0V, battery MOSFET (BATFET) disabled, T_A = 25°C		3	5	µA
		V_{BATT} = 4V, V_{IN} = 0V, BATFET disabled		3	10	µA
Input quiescent current during buck switching	I_{IN_BUCK}	V_{IN} = 5V, converter switching, V_{BATT} = 3.8V, charge disabled, I_{SYS} = 0A, I_{BATT} = 0A		5		mA
Input leakage current in buck high-impedance (Hi-Z) mode	I_{IN_SUSP}	V_{IN} = 5V, switching disabled, BATFET enabled, no load at SYS node		0.15	1	mA
Battery discharge current in boost discharging mode	I_{Q_BOOST}	V_{BATT} = 4V, boost switching, load switches enabled, on-the-go (OTG) mode disabled, no loading at BOOST1/BOOST2, watchdog timer disabled, BATFET over-current protection (OCP) disabled		300		µA
Battery discharge current in idle mode	I_{Q_IDLE}	V_{BATT} = 4V, V_{IN} = 0V, watchdog timer disabled, BATFET enabled, BATFET OCP disabled, analog-to-digital converter (ADC) disabled		10	22	µA
Input Power Characteristics						
Input voltage operating range	V_{IN_OP}		4		6.5	V
Input under-voltage lockout (UVLO) threshold	V_{IN_UVLO}	V_{IN} falling, V_{BATT} = 0V	2.95	3.2	3.45	V
Input UVLO threshold hysteresis	$V_{IN_UVLO_HYS}$	V_{IN} rising, V_{BATT} = 0V		250		mV
Input vs. battery voltage headroom threshold	V_{HDRM}	V_{IN} rising, V_{BATT} = 3.8V	80	200	320	mV
		V_{IN} falling, V_{BATT} = 3.8V	30	100	170	mV
Input over-voltage lockout (OVLO) threshold	V_{IN_OVLO}	V_{IN} rising	6.25	6.5	6.75	V
Input OVLO threshold hysteresis	$V_{IN_OVLO_HYS}$	V_{IN} falling		600		mV
Low-Dropout (LDO) Regulator						
VCC voltage (V_{CC}) LDO output voltage	V_{CC}	V_{IN} = 5V, V_{BATT} = 3.8V, I_{VCC} = 10mA		3.6		V
V_{CC} LDO output current upper limit	I_{VCC}	V_{IN} = 5V, V_{BATT} = 3.8V, T_A = 0°C to 70°C			10	mA
V_{CC} LDO UVLO threshold	V_{CC_UVLO}	V_{IN} falling, V_{BATT} = 0V		2		V
V_{CC} LDO UVLO hysteresis	$V_{CC_UV_HYS}$	V_{IN} rising, V_{BATT} = 0V		250		mV

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
DC/DC Buck Switching						
Minimum system regulation voltage range	V_{SYS_MIN}		3.2		4.25	V
Minimum system regulation voltage accuracy	$V_{SYS_MIN_REG_ACC}$	SYS_MIN_REG (07h, bits[3:1]) = b'010 (3.5V), V_{BATT} < V_{SYS_MIN}, V_{TRACK1} = 150mV	3.5	3.65	3.8	V
Battery tracking voltage	V_{TRACK1}	V_{BATT} = 3.3V, V_{BATT} < V_{SYS_MIN}, SYS_MIN_REG = b'010 (3.5V)	85	150	215	mV
	V_{TRACK2}	V_{BATT} = 3.6V, V_{BATT} > V_{SYS_MIN}, SYS_MIN_REG = b'010 (3.5V)	45	100	155	mV
Blocking MOSFET on resistance	$R_{DS(ON)_QB}$			30		mΩ
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)_QHS}$			30		mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)_QLS}$			60		mΩ
Buck switching frequency	f_{SW}	FRE_SEL (00h, bit[2]) = b'1 (2MHz)	1820	2000	2150	kHz
		FRE_SEL = b'0 (1.5MHz)	1320	1500	1690	kHz
System over-voltage protection (OVP) trip threshold	$V_{SYS_OVP_TRIP}$	V_{BATT} = 4.2V, SYS_OVP_RI_TH (09h, bits[7:4]) = b'1010 (4800mV), SYS pin voltage (V_{SYS}) rising	4.65	4.8	4.95	V
System OVP recovery threshold	$V_{SYS_OVP_RCVY}$	V_{BATT} = 4.2V, SYS_OVP_FL_TH (09h, bits[3:0]) = b'1000 (4600mV), V_{SYS} falling	4.45	4.6	4.75	V
System over-voltage (OV) discharge load	I_{SYS_LOAD}	SYS_OVP_RI_TH = b'1010, V_{SYS} = 5V		20		mA
Load Switches						
Load switch on resistance	$R_{DS(ON)_LDSW_QL}$			300		mΩ
	$R_{DS(ON)_LDSW_QR}$			300		mΩ
Load switch over-current (OC) threshold for each rail	I_{LDSW_OC}	Buck mode, V_{PMID} = 5V, load switch current rising, LDSW_OCP (0Eh, bits[1:0]) = b'01	310	550	820	mA
		Buck mode, V_{PMID} = 5V, load switch current rising, LDSW_OCP = b'11	580	870	1150	mA
		Boost mode, V_{PMID} = 5V, load switch current rising, LDSW_OCP = b'11	350	550		mA
Load switch short current limit	I_{LDSC}	V_{PMID} = 5V, load switch output (BOOST1/BOOST2) short to PGND		15		mA

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Battery Charging (T_A = 0°C to 70°C)						
Battery charge voltage regulation range	$V_{BATT_REG_RANGE}$		3.6		4.6	V
Battery charge voltage step	$V_{BATT_REG_STEP}$			10		mV
Battery charge voltage regulation accuracy	$V_{BATT_REG_ACC}$	V_{BATT_REG} = 3.6V, T_A = 0°C to 70°C	-0.5		+0.5	% of V_{BATT_REG}
		V_{BATT_REG} = 4.2V, T_A = 0°C to 70°C				
		V_{BATT_REG} = 4.35V, T_A = 0°C to 70°C				
Fast charge current range	I_{CC}		20		2000	mA
Fast charge current step	I_{CC_STEP}			20		mA
Fast charge current accuracy	I_{CC_ACC}	I_{CC} = 0.1A, ICC (04h, bits[7:1]) = b'0000100 (100mA), V_{BATT} = 3.8V, T_A = 0°C to 70°C	-25		+25	% of I_{CC}
		I_{CC} = 0.5A. ICC = b'0011000 (500mA), V_{BATT} = 3.8V, T_A = 0°C to 70°C	-10		+10	% of I_{CC}
		I_{CC} = 2.0A. ICC = b'1100011 (2A), V_{BATT} = 3.8V, T_A = 0°C to 70°C	-5		+5	% of I_{CC}
Pre-charge to fast charge threshold range	$V_{BATT_PRE_RANGE}$		2.4		3	V
Pre-charge to fast charge threshold step	$V_{BATT_PRE_STEP}$			200		mV
Pre-charge to fast charge threshold accuracy	$V_{BATT_PRE_ACC}$	V_{BATT} rising, VPRE (03h, bits[2:1] = b'10 (2.8V)	2.65	2.8	2.95	V
Fast charge back to pre-charge threshold hysteresis	$V_{BATT_PRE2CC_HYS}$	V_{BATT} falling		200		mV
Trickle charge to pre-charge threshold	V_{BATT_TC2PRE}	V_{BATT} rising	2.05	2.2	2.35	V
Trickle charge to pre-charge threshold hysteresis	$V_{BATT_TC_HYS}$	V_{BATT} falling		200		mV
Pre-charge current range	I_{PRE_RANGE}		10		160	mA
Pre-charge current step	$I_{PRE_RANGE_STEP}$			10		mA
Pre-charge current accuracy	I_{PRE_ACC}	V_{BATT} = 2.5V, IPRE (05h, bits[7:4]) = b'1000 (50mA), T_A = 0°C to 70°C	40	50	60	mA
		V_{BATT} = 2.5V, IPRE = b'1111 (160mA), T_A = 0°C to 70°C	140	160	180	mA
Trickle charge current range	I_{TC_RANGE}		10		70	mA
Trickle charge current accuracy	I_{TC_ACC}	V_{BATT} = 1.8V, ITRICKLE (02h, bits[2:0]) = b'100 (50mA), T_A = 0°C to 70°C	40	50	60	mA

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Charge termination current threshold range	I_{TERM_RANGE}		10		160	mA
Charge termination current threshold accuracy	I_{TERM_ACC}	ITERM (05h, bits[3:0]) = b'000 (10mA), V_{BATT_REG} = 4.2V, TERM_EN (00h, bit[1]) = b'1, T_A = 0°C to 70°C	5	10	15	mA
Charge termination current threshold accuracy	I_{TERM_ACC}	ITERM = b'100 (50mA), V_{BATT_REG} = 4.2V, TERM_EN = b'1, T_A = 0°C to 70°C	35	50	65	mA
		ITERM = b'1111 (160mA), V_{BATT_REG} = 4.2V, TERM_EN = b'1, T_A = 0°C to 70°C	130	160	190	mA
Automatic recharge battery voltage threshold	V_{RECH}	V_{BATT} falling, VRECHG (03h, bit[0]) = b'0, T_A = 0°C to 70°C	70	100	130	mV
		V_{BATT} falling, VRECHG = b'1, T_A = 0°C to 70°C	150	200	250	mV
Battery OVP threshold	V_{BATT_OVP}	V_{BATT} rising, V_{BATT_REG} = 4V, T_A = 0°C to 70°C	102	104	105.5	% of V_{BATT_REG}
Battery OVP hysteresis	$V_{BATT_OVP_HYS}$	V_{BATT} falling		2		%
Battery OCP in discharge mode	I_{DSCHG_OCP}	V_{BATT} = 4V, BATT_FET_OCP_EN (08h, bit[2]) = b'1, T_A = 0°C to 70°C	3.95	4.5	5.05	A
Battery MOSFET (BATFET) on resistance	$R_{DS(ON)_QBATT}$			30		mΩ
Thermal Regulation and Protection						
Junction temperature regulation	T_{J_REG}	TREG (0Ch, bits[7:5]) = 80°C		80		°C
		TREG = 120°C		120		°C
Thermal shutdown rising junction temperature	T_{J_SHDN}	Rising temperature		150		°C
Thermal shutdown hysteresis	T_{SHDN_HYS}	Falling temperature		30		°C
Battery Temperature Monitoring (JEITA)						
NTC cold temperature rising threshold	V_{COLD}	VCOLD (0Bh, bits[1:0]) = 74.2% (0°C), T_A = 0°C to 70°C	73.7	74.2	74.7	% of V_{NTC}
NTC cold temperature rising threshold hysteresis	V_{COLD_HYS}			1.4		% of V_{NTC}
NTC cool temperature rising threshold	V_{COOL}	VCOOL (0Bh, bits[3:2]) = 64.8% (10°C),T_A = 0°C to 70°C	64.3	64.8	65.3	% of V_{NTC}
NTC cool temperature hysteresis	V_{COOL_HYS}			1.4		% of V_{NTC}
NTC warm temperature falling threshold	V_{WARM}	VWARM (0Bh, bits[5:4]) = 29.1% (50°C), T_A = 0°C to 70°C	28.6	29.1	29.6	% of V_{NTC}
NTC warm temperature hysteresis	V_{WARM_HYS}			1.4		% of V_{NTC}

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
NTC hot temperature falling threshold	V_{HOT}	VHOT (0Bh, bits[7:6]) = 23% (60°C), T_A = 0°C to 70°C	22	23	24	% of V_{NTC}
NTC hot temperature hysteresis	V_{HOT_HYS}			1.4		% of V_{NTC}
NTC float threshold	V_{NTC_FLT}			90		% of V_{NTC}
NTC float hysteresis	$V_{NTC_FLT_HYS}$			1.4		% of V_{NTC}
NTC reference voltage	V_{NTC}			1		V
Input Voltage and Current Regulation						
Input minimum voltage regulation	V_{IN_LIM}		3.9		5.4	V
Input minimum voltage limit accuracy	$V_{IN_LIM_ACC}$	V_{IN_LIM} = 3.9V, T_A = 0°C to 70°C	3.75	3.9	4.05	V
		V_{IN_LIM} = 4.5V, T_A = 0°C to 70°C	4.35	4.5	4.65	V
Input current limit range	$I_{IN_LIM_RANGE}$	I_{IN_LIM} adjustable via the I²C, 100mA/step, default 500mA	100		3200	mA
Input current limit accuracy	$I_{IN_LIM_ACC}$	I_{IN_LIM} = 500mA, T_A = 0°C to 70°C	420	465	500	mA
		I_{IN_LIM} = 900mA, T_A = 0°C to 70°C	790	845	900	mA
		I_{IN_LIM} = 1.5A, T_A = 0°C to 70°C	1320	1410	1500	mA
		I_{IN_LIM} = 3A, T_A = 0°C to 70°C	2680	2840	3000	mA
Boost Mode and Discharge Mode						
Boost regulation voltage range	V_{BOOST_RANGE}		4		6	V
Low battery voltage threshold in boost mode	V_{BATT_LOW}	BATT_LOW_TH (08h, bits[5:4]) = b'10 (2.9V), T_A = 0°C to 70°C	2.75	2.9	3.05	V
		BATT_LOW_TH = b'01 (2.7V), T_A = 0°C to 70°C	2.55	2.7	2.85	V
Low battery voltage threshold hysteresis in boost mode	$V_{BATT_LOW_HYS}$			200		mV
OTG over-current limit range	$I_{OTG_OCL_RANGE}$		0.5		1.5	A
OTG over-current limit accuracy	$I_{OTG_OCL_ACC}$	OTG_ILIM (0Eh, bits[5:4]) = b'00, V_{BATT} = 4V, T_A = 0°C to 70°C	500			mA
		OTG_ILIM = b'11, V_{BATT} = 4V, T_A = 0°C to 70°C	1500			mA
Boost OVP threshold	V_{BOOST_OVP}	Boost mode, V_{OUT} rising, T_A = 0°C to 70°C	6.1	6.5	6.99	V
Boost OVP threshold hysteresis	$V_{BOOST_OVP_HYS}$	Boost mode, V_{OUT} falling		300		mV
Battery UVLO threshold	V_{BATT_UVLO}	T_A = 0°C to 70°C	2.39	2.5	2.61	V

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Battery UVLO hysteresis	$V_{BATT_UVLO_HYS}$			400		mV
Automatic boost threshold range	$V_{IN_AUTO-BOOST_TH}$	V_{IN} falling from 5V, V_{BATT} = 4V	3.9		4.8	V
Automatic boost threshold accuracy	$V_{IN_AUTO-BOOST_TH_ACC}$	V_{IN} falling from 5V, V_{BATT} = 4V, VIN_RM_TH (0Dh, bits[2:1]) = b'00 (3.9V), T_A = 0°C to 70°C	-1.3		+1.7	% of set value
Logic I/O for the SCL, SDA, /INT, and /DISC Pins						
Logic-low input voltage	V_{IL}				0.4	V
Logic-high input Voltage	V_{IH}		1.3			V
Open-drain low output voltage	V_{OUT_L}	I_{SINK} = 10mA			0.2	V
D+/D- Detection						
DCD D+ pull-up current	I_{DP_SRC}		6	10	14	µA
DCD D- pull-down resistance	R_{DM_DWN}		15.5	20	24.5	kΩ
D+/D- low source voltage	V_{SRC_LOW}		540	600	660	mV
D+/D- sink current	I_{SNK}		48	100	152	µA
Data detect voltage	V_{DAT_REF}		290	350	410	mV
Fault Deglitch Timers						
Boosting deglitch time during low battery	$t_{D_BATT_LOW}$	V_{BATT} falling	9.5	10	10.5	ms
Battery UVLO deglitch time	$t_{BATT_UVLO_DGL}$	V_{BATT} falling	9.5	10	10.5	µs
Battery OV deglitch time	$t_{BATT_OV_DGL}$	V_{BATT} rising		100		ms
Transition Timers						
Charge termination deglitch time	t_{TERM_DGL}		225	250	275	ms
Automatic recharge deglitch time	t_{RECHG_DGL}		225	250	275	ms
Top-off timer	t_{TOPOFF_TMR}	TOPOFF_TMR (19h, bits[3:2]) = b'01	13.5	15	16.5	min
		TOPOFF_TMR = b'10	27	30	33	min
		TOPOFF_TMR = b'11	40	45	50	min
BATFET Control Timer						
Wake-up time in shipping mode	t_{WAKE}	T_WAKE (18h, bits[1:0]) = b'00	0.45	0.5	0.55	s
		T_WAKE = b'01	0.9	1	1.1	s
		T_WAKE = b'10	1.8	2	2.2	s
		T_WAKE = b'11	3.6	4	4.4	s
BATFET turn-off time	t_{DISC}	T_DISC (18h, bits[5:4]) = b'00	0.9	1	1.1	s
		T_DISC = b'01	1.8	2	2.2	s
		T_DISC = b'10	3.6	4	4.4	s
		T_DISC = b'11	7.2	8	8.8	s

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Safety Timer						
Watchdog timer	t_{WD}	WD_CFG (07h, bits[6:5]) = b'01 (40s)	36	40	44	s
		WD_CFG = b'10 (80s)	72	80	88	s
		WD_CFG = b'11 (160s)	144	160	176	s
Pre-charge timer	t_{PRECHG_TMR}		1.8	2	2.2	hrs
Fast-charge timer	t_{FAST_TMR}	FULL_CHG_TMR (19h, bits[6:5]) = b'01 (5hrs)	4.5	5	5.5	hrs
		FULL_CHG_TMR= b'10 (10hrs)	9	10	11	hrs
		FULL_CHG_TMR= b'11 (15hrs)	13.5	15	16.5	hrs

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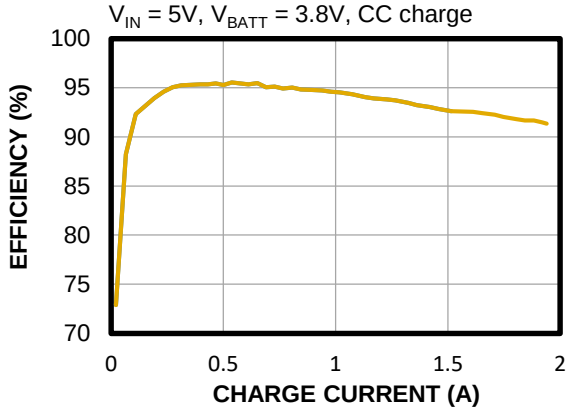
TYPICAL CHARACTERISTICS

V_{IN} = 5V, V_{BATT} = full range, I²C-controlled, I_{CC} = 0.5A to 2A, I_{IN_LIM} = 0.5A, V_{IN_MIN} = 4.5V, L = 1.5µH (DCR = 35mΩ), T_A = 25°C, unless otherwise noted.

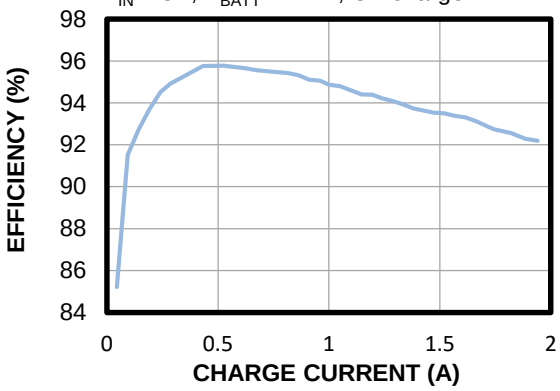
Efficiency vs. Charge Current

V_{IN} = 5V, V_{BATT} = 3.8V, CC charge

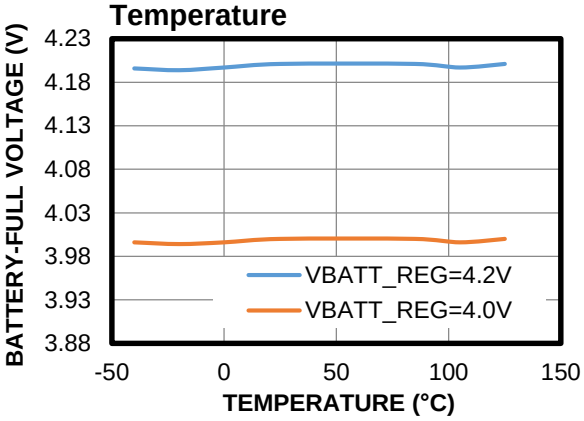


Efficiency vs. Charge Current

V_{IN} = 5V, V_{BATT} = 4.2V, CV charge

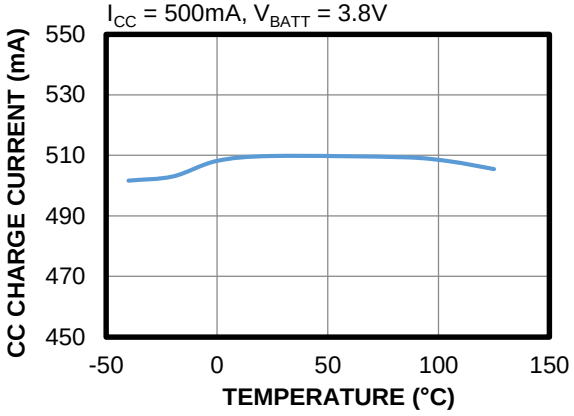


Battery-Full Voltage vs. Temperature



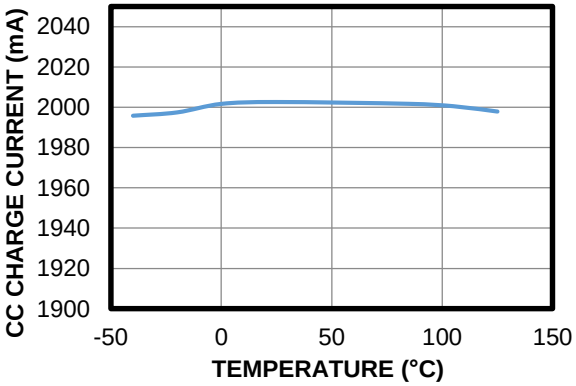
CC Charger Current vs. Temperature

I_{CC} = 500mA, V_{BATT} = 3.8V



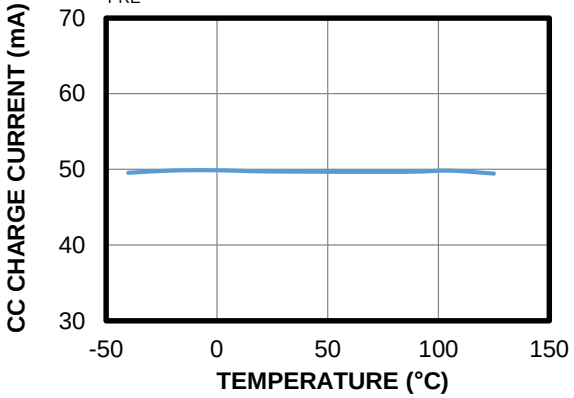
CC Charge Current vs. Temperature

I_{CC} = 2000mA, V_{BATT} = 3.8V



Pre-Charger Current vs. Temperature

I_{PRE} = 50mA



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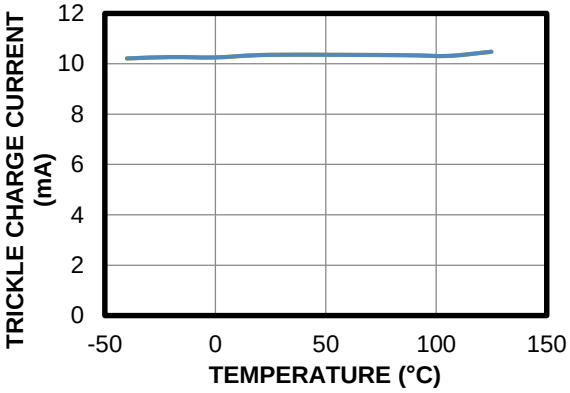
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = full range, I²C-controlled, I_{CC} = 0.5A to 2A, I_{IN_LIM} = 0.5A, V_{IN_MIN} = 4.5V, L = 1.5µH (DCR = 35mΩ), T_A = 25°C, unless otherwise noted.

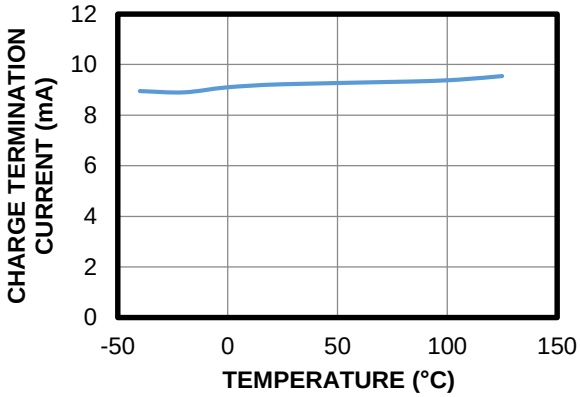
Trickle Charge Current vs. Temperature

I_{TC} = 10mA



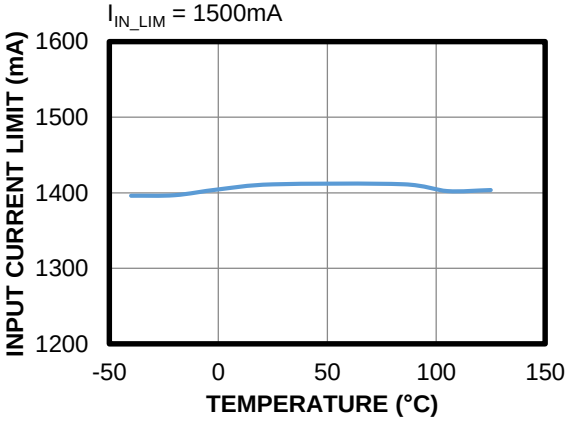
Charge Termination Current vs. Temperature

I_{TERM} = 10mA



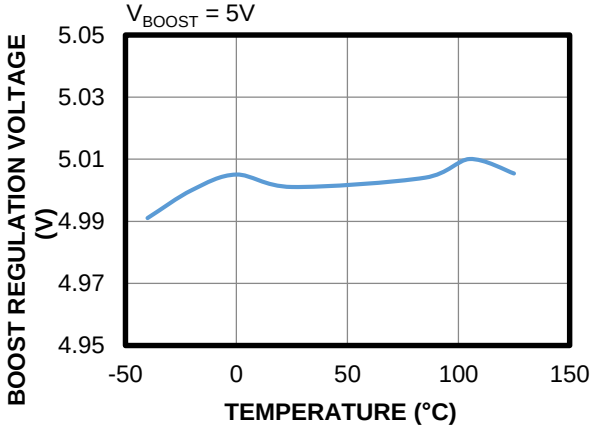
Input Current Limit vs. Temperature

I_{IN_LIM} = 1500mA



Boost Regulation Voltage vs. Temperature

V_{BOOST} = 5V



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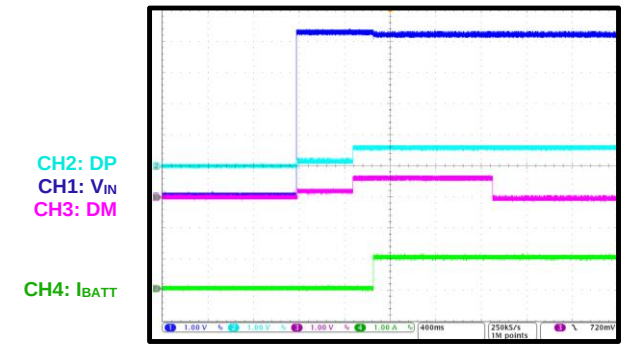
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{BATT} = full range, I²C-controlled, I_{CC} = 0.5A to 2A, I_{IN_LIM} = 0.5A, V_{IN_MIN} = 4.5V, L = 1.5µH (DCR = 35mΩ), T_A = 25°C, unless otherwise noted.

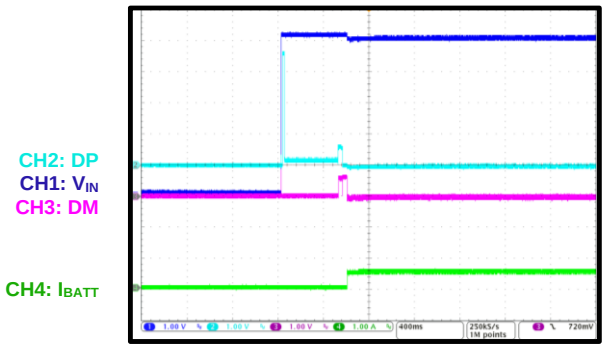
Adapter Plugged In

I_{CC} = 1A, V_{BATT} = 3.8V, dedicated charging port (DCP) adapter inserted



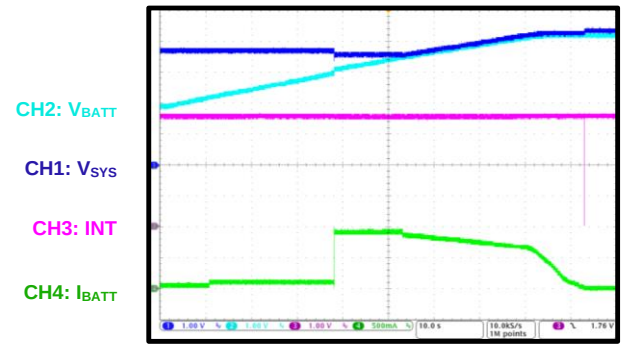
Adapter Plugged In

I_{CC} = 1A, V_{BATT} = 3.8V, USB standard downstream port (SDP) inserted



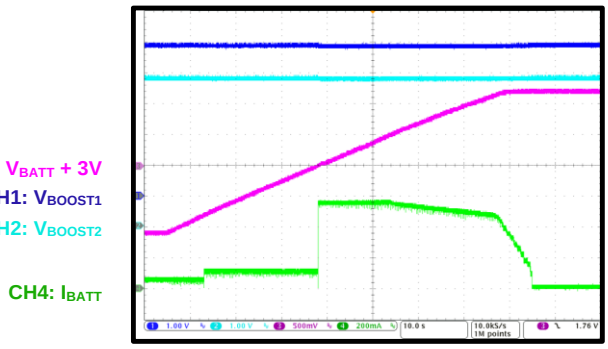
Battery Charge Profile

I_{IN_LIM} = 1.5A, I_{CC} = 1A, Q_R and Q_L are off



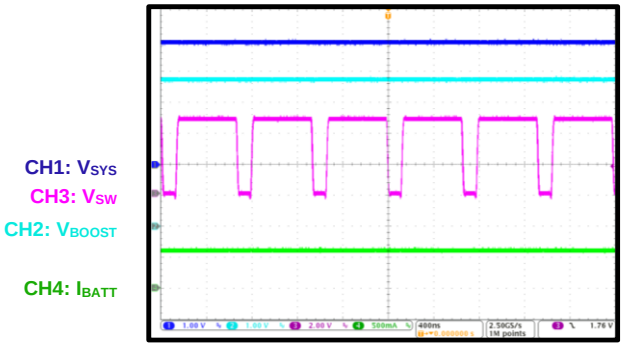
Battery Charge Profile

I_{IN_LIM} = 1.5A, I_{CC} = 1A, I_{BOOST1} = I_{BOOST2} = 0.5A



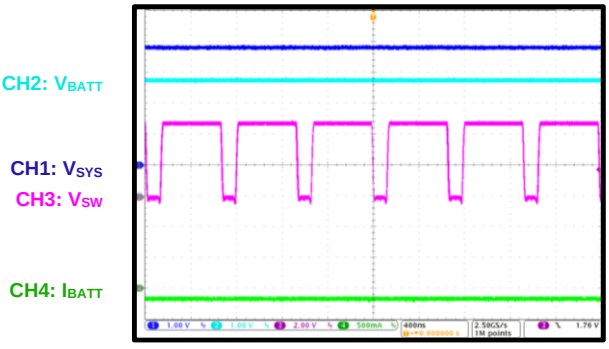
Charge Steady State

V_{BATT} = 3.8V, I_{IN_LIM} = 1.5A, I_{CC} = 1A, I_{BOOST1} + I_{BOOST2} = 1A



Charge Steady State

V_{BATT} = 3.8V, I_{IN_LIM} = 1.5A, I_{CC} = 1A, I_{SYS} = 2A



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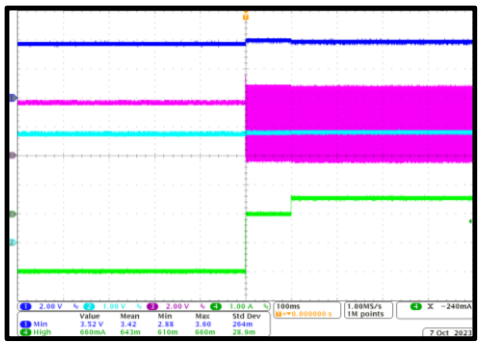
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = full range, I²C-controlled, I_{CC} = 0.5A to 2A, I_{IN_LIM} = 0.5A, V_{IN_MIN} = 4.5V, L = 1.5µH (DCR = 35mΩ), T_A = 25°C, unless otherwise noted.

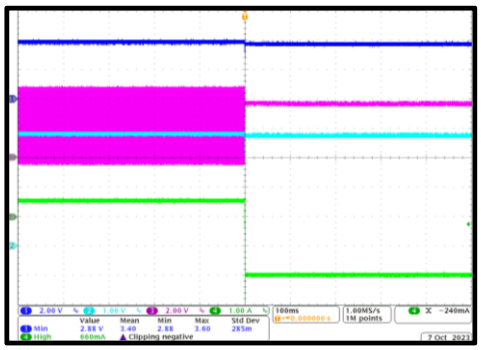
Buck Enabled

V_{BATT} = 3.8V, I_{IN_LIM} = 3.2A, I_{CC} = 0.5A, I_{SYS} = 2A



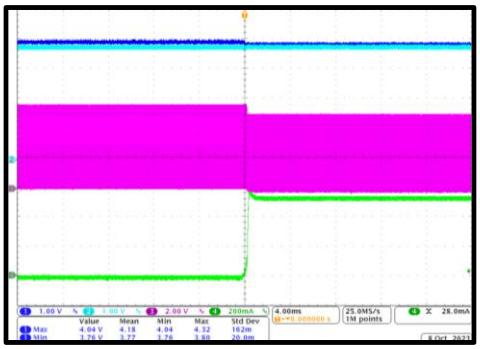
Buck Disabled

V_{BATT} = 3.8V, I_{IN_LIM} = 3.2A, I_{CC} = 0.5A, I_{SYS} = 2A



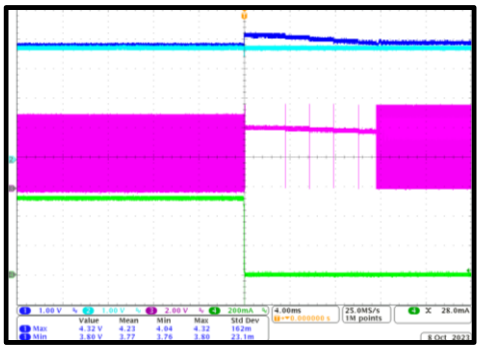
Charge Enabled

V_{BATT} = 3.8V, I_{IN_LIM} = 3.2A, I_{CC} = 0.5A, I_{SYS} = 0A



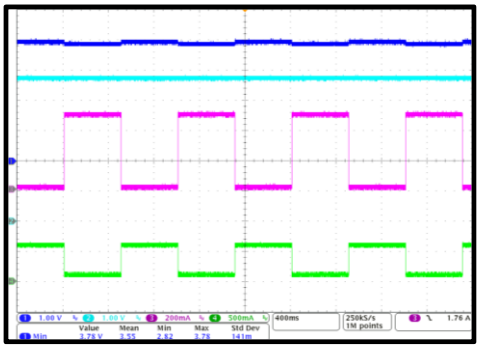
Charge Disabled

V_{BATT} = 3.8V, I_{IN_LIM} = 3.2A, I_{CC} = 0.5A, I_{SYS} = 0A



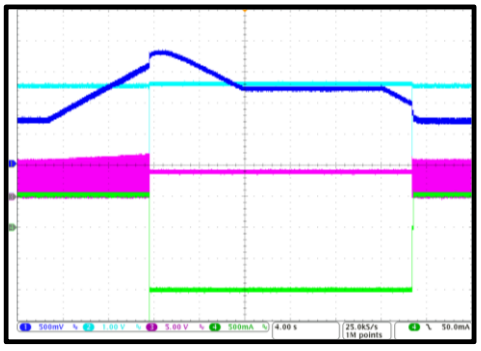
SYS Load Transient

V_{BATT} = 3.8V, I_{IN_LIM} = 1.5A, I_{CC} = 1A, I_{SYS} = 0A to 0.5A, I_{BOOST1} + I_{BOOST2} = 1A



V_{IN} OVP

V_{BATT} = 3.8V, I_{IN_LIM} = 3.2A, I_{CC} = 0.5A, I_{SYS} = 1A



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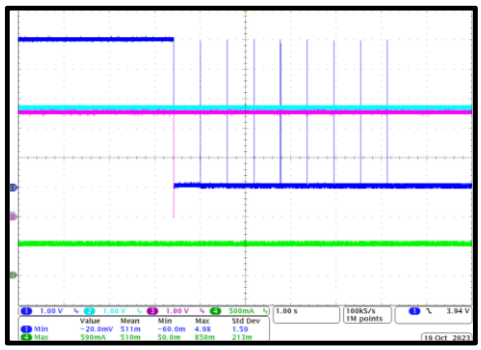
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = full range, I²C-controlled, I_{CC} = 0.5A to 2A, I_{IN_LIM} = 0.5A, V_{IN_MIN} = 4.5V, L = 1.5µH (DCR = 35mΩ), T_A = 25°C, unless otherwise noted.

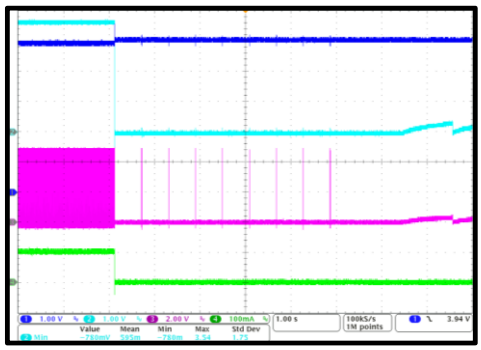
Load Switch OCP

V_{BATT} = 3.3V, I_{IN_LIM} = 1.5A, I_{CC} = 1A, I_{SYS} = 0A, I_{BOOST1} = 0.9A



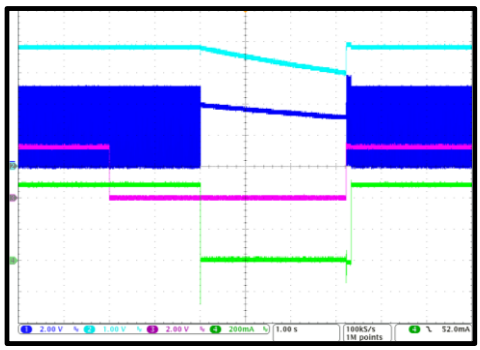
SYS SCP

V_{BATT} = 2.5V, I_{IN_LIM} = 3.2A, I_{PRE} = 100mA, I_{SYS} = 2A



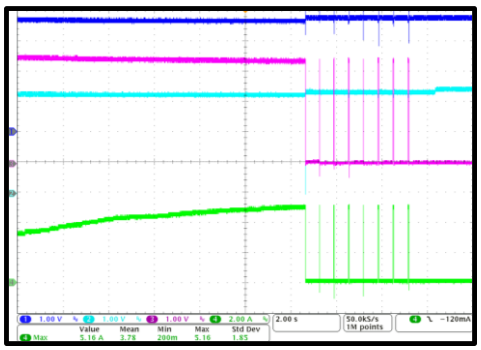
SYS Automatic Reset Mode

V_{BATT} = 3.8V, I_{IN_LIM} = 1.5A, I_{CC} = 0.5A, I_{SYS} = 0A, T_SYS_LOW (18h, bits[3:2]) = 0.5s



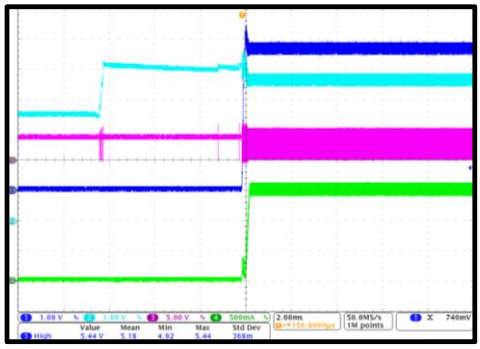
Battery Discharging OCP in Idle State

V_{BATT} = 3.7V



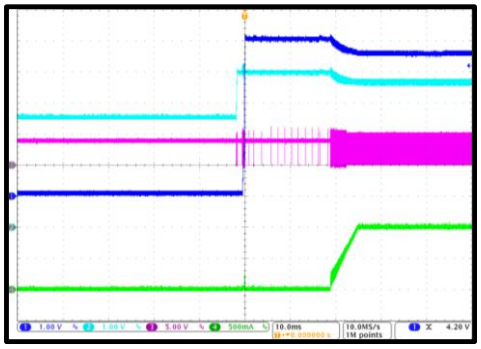
Boost Mode and OTG Mode Enabled

V_{BATT} = 3.8V, V_{BOOST} = 5V, I_{OTG_LIM} = 1.5A, I_{OTG} = 1.5A



Boost Mode and Load Switch Enabled

V_{BATT} = 3.8V, V_{BOOST} = 5V, I_{BOOST1} + I_{BOOST2} = 1A



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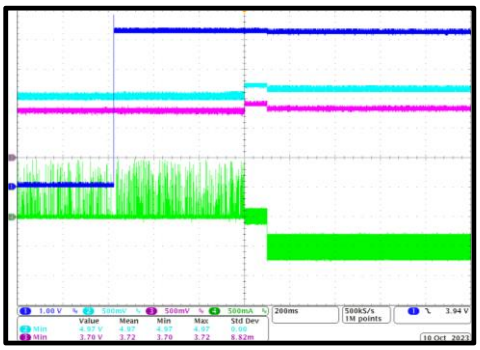
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = full range, I²C-controlled, I_{CC} = 0.5A to 2A, I_{IN_LIM} = 0.5A, V_{IN_MIN} = 4.5V, L = 1.5µH (DCR = 35mΩ), T_A = 25°C, unless otherwise noted.

Boost to Buck Transient

V_{BATT} = 3.8V, V_{BOOST} = 5V, V_{IN} = 5V, insert VIN during boost operation

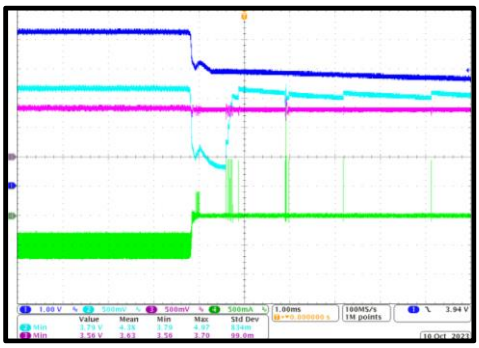
CH2: V_{PMID} + 3V
CH3: V_{SYS} + 3V
CH1: V_{IN}
CH4: I_L



Boost to Buck Transient

V_{BATT} = 3.8V, V_{BOOST} = 5V, V_{IN} = 5V, enable the boost function before removing VIN

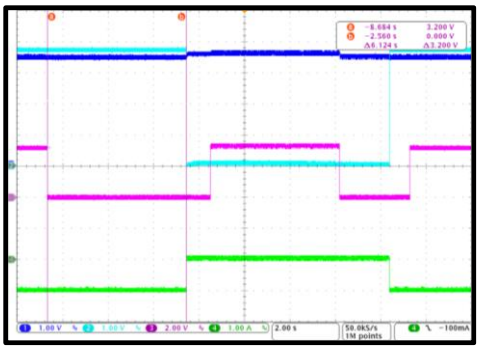
CH2: V_{PMID} + 3V
CH3: V_{SYS} + 3V
CH1: V_{IN}
CH4: I_L



Shipping Mode Entry/Exit through /DISC

V_{BATT} = 3.8V, T_DISC (18h, bits[5:4]) = 2s, BATTFET_DLY (18h, bits[7:6]) = 4s, T_WAKE (18h, bits[1:0]) = 2s

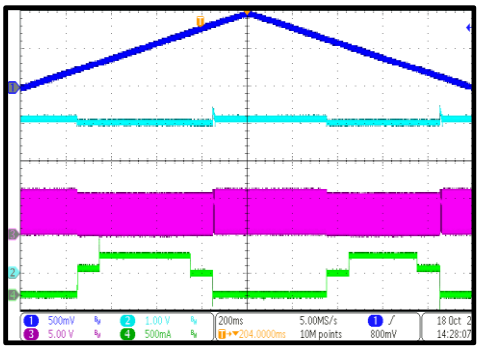
CH1: VCC
CH2: V_{SYS}
CH3: /DISC
CH4: I_{BATT}



NTC JEITA Protection

V_{BATT} = 3.95V, I_{CC} = 0.5A, JEITA_ISET = 50%, JEITA_VSET = -250mV

CH1: VNTC
CH3: V_{SW}
CH2: V_{SYS}
CH4: I_{BATT}



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FUNCTIONAL BLOCK DIAGRAM

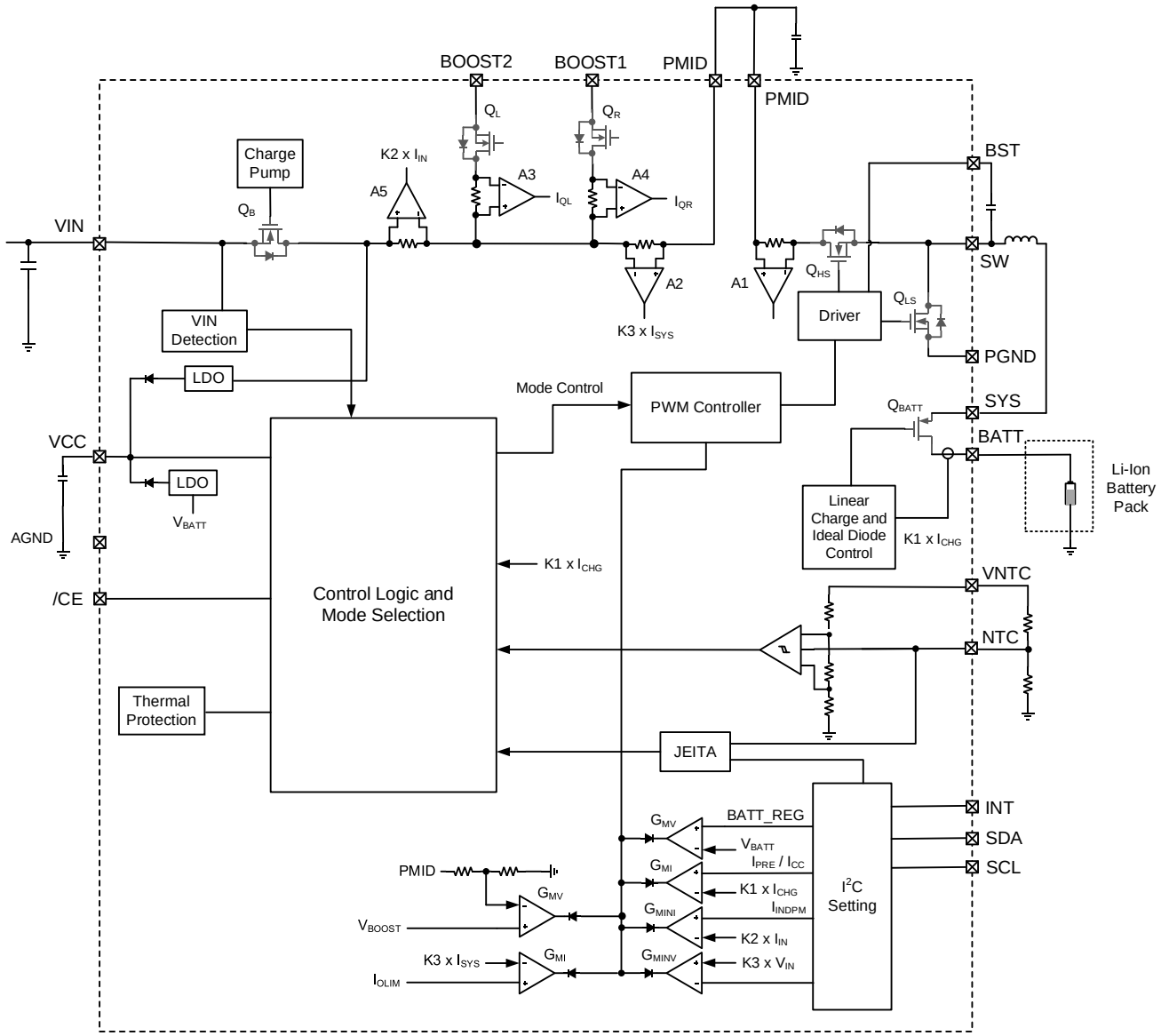

Figure 2: Functional Block Diagram

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OPERATION

The MP2772 is a highly integrated, bidirectional, switch-mode battery charger for 1-cell Li-ion battery applications. The device integrates an input reverse blocking MOSFET (Q_B), high-side MOSFET (HS-FET, also called Q_{HS}), low-side MOSFET (LS-FET, also called Q_{LS}), battery MOSFET (BATFET, also called Q_{BATT}), and load switches (Q_R and Q_L) (see Figure 2 on page 20).

Main States

The MP2772 operates in 5 main states, described below:

- Idle state: The MP2772 provides power to the system load only through the battery. The input USB power is not present, and buck or boost switching is not active.
- Buck idle state (Hi-Z mode): The input power (P_{IN}) is present, and buck switching is not active. The MP2772 remains in buck idle state, also known as high-impedance (Hi-Z) state. The load switches are also off.
- Buck switching state: Buck switching is active with a valid input source. Battery charging and load switch powering are allowed in this state.
- Boost switching state: Boost switching is active, and the battery discharges. On-the-go (OTG) mode or the load switches can be selected to power the load.
- Shipping mode state: The MP2772's BATFET turns off, and the IC consumes the minimum amount of power from the battery.

Power Supply

The VCC pin supplies internal biasing circuitry as well as the Q_{HS} and Q_{LS} gate driver. VCC can also be used as the pull-up rail for the /INT pin or /CE pin. The higher value between the input voltage (V_{IN}), battery voltage (V_{BATT}), and PMID voltage (V_{PMID}) is selected internally to power up the low-dropout (LDO) regulator, which has V_{CC} as its output.

Device Power from the Input Source

When the input source is plugged in, the MP2772 detects the input source before buck mode switching is enabled. The input source must meet the following requirements:

1. $V_{IN} > V_{BATT} + V_{HDRM}$
2. $V_{IN_UVLO} < V_{IN} < V_{IN_OVLO}$

Once the input power source meets the above conditions, input power good (PG) is detected, and the VIN_PG_STAT bit (15h, bit[7]) is set to 1 to indicate a PG condition. As the VIN state changes, the VIN_PG_FLAG bit (10h, bit[7]) is set to 1. If the flag is not cleared, the VIN_PG_FLAG bit remains at 1, even when the VIN state changes. Write 1 to the flag bit to clear it.

Idle State

When the input power source is not present and the battery is connected where V_{BATT} exceeds the under-voltage (UV) battery voltage (V_{BATT_UV}), Q_{BATT} turns on and starts up the system. The MP2772 features a low on resistance ($R_{DS(ON)}$) BATFET with a low quiescent current (I_Q) gate driver, which maintains low power consumption while extending battery life. The discharge over-current protection can be optionally enabled or disabled by setting the BATT_FET_OCP_EN bit (08h, bit[2]). The over-current protection (OCP) threshold can be determined via the one-time programmable (OTP) memory.

Buck Idle State (Hi-Z Mode)

There are two ways to enter buck idle state, describe below:

1. If the BUCK_EN bit (00h, bit[3]) is set to 0, the MP2772 enters buck idle (Hi-Z) mode with an adapter present. The device enters low input I_Q state with the internal biasing circuitry, Q_B, and load switches turned off.
2. If the BUCK_EN bit is set to 1, V_{IN} is below the sum of V_{BATT} and the input headroom. Under this condition, V_{IN} is too low to support normal buck switching, and the IC enters buck idle state.

Input Power Path Automatic Control

When a valid input power source is present, Q_B automatically turns on; when the input power is removed, Q_B automatically turns off.

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Q_B is also controlled to turn off automatically under certain abnormal events, such as entering buck idle mode or V_{IN} over-voltage protection (OVP) state.

Input Current Limit Setting

To prevent the input adapter from being overloaded, the MP2772 supports several methods for setting the input current limit (I_{IN_LIM}). If the input current (I_{IN}) increases and reaches I_{IN_LIM}, then the charge current is reduced to prioritize the system power, and the load switches power.

Method 1: Pin-Controlled

If the ILIM_PIN_EN bit (01h, bit[2]) is set to 1, I_{IN_LIM} is set by the logic on the ILIM pin. A logic high on the ILIM pin sets I_{IN_LIM} to 2.5A, and a logic low on the ILIM pin sets I_{IN_LIM} to 0.5A.

Method 2: Register-Controlled

If the ILIM_PIN_EN bit is set to 0, I_{IN_LIM} is set by either the Battery Charging 1.2 (BC1.2) detection results or via the IIN_LIM (02h, bits[7:3]) bits. If BC1.2 is disabled by setting the USB_DET_EN bit (0Fh, bit[6]) to 0 and the ILIM_RECONFIG bit (04h, bit[0]) to 1, then I_{IN_LIM} is set by the IIN_LIM bits. If BC1.2 is enabled by setting the USB_DET_EN bit to 1 and the ILIM_RECONFIG bit to 0, then I_{IN_LIM} is set by the BC1.2 detection results.

The ILIM_PIN_EN bit is set to 1. It is necessary to set the ILIM_PIN_EN bit to 0 first to use the USB BC1.2 detection results to set I_{IN_LIM}. In addition, the ILIM_RECONFIG bit must be set to 1 to set I_{IN_LIM} via the I²C.

USB Battery Charging 1.2 (BC1.2) Detection

The MP2772 initiates BC1.2 detection if the following conditions are met:

- V_{IN} power is present
- The USB_DET_EN bit is set to 1

BC1.2 detection can differentiate between the standard downstream port (SDP, with a 500mA I_{IN_LIM}), dedicated charging port (DCP, with a 1.8A I_{IN_LIM}), and charging downstream port (CDP, with a 1.5A I_{IN_LIM}) to set I_{IN_LIM} accordingly. If plugging in the adapters that are not compliant with BC1.2, the MP2772 detects the input source as an unknown type, and I_{IN_LIM} is set to 500mA for safety considerations.

After detection is finished, the input source type is reported via the VIN_STAT bits (15h, bits[1:0]).

Input Voltage Limit Setting

The MP2772 supports the configurable input voltage limit (V_{IN_LIM}) set via the VIN_LIM bits (03h, bits[6:3]). When V_{IN} drops to the configured limit due to the input source's limited power capability, the V_{IN} loop closes, and the charge current is reduced to prioritize the system power.

Buck Converter and Charger Operation

Once BC1.2 detection is complete, if the BUCK_EN bit is set to 1, the buck converter initiates soft start (SS). The buck converter's switching frequency (f_{SW}) can be selected between 1.5MHz and 2MHz, based on the FRE_SEL bit (00h, bit[2]) setting. Peak current mode control is adopted to regulate the system voltage (V_{SYS}), battery charge current, battery regulation voltage, I_{IN_LIM}, V_{IN_LIM}, and the device's die temperature loops.

The MP2772 automatically starts charging if the CHG_EN bit (00h, bit[5]) is set to 1.

Narrow-Voltage DC (NVDC) Power Path Management

Figure 3 shows the narrow-voltage DC (NVDC) power path management structure.

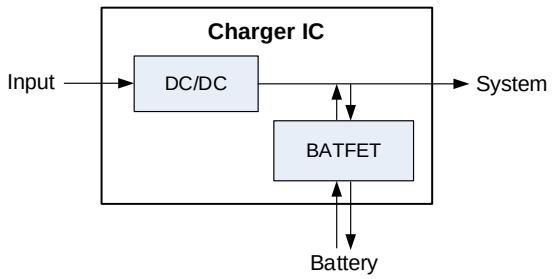

Figure 3: NVDC Power Path Management Structure

With this structure, Q_{BATT} decouples the system from the battery and controls battery charging and discharging separately. The MP2772 prioritizes the system (SYS) output using the power path function, which selects between the input source and battery, or uses both.

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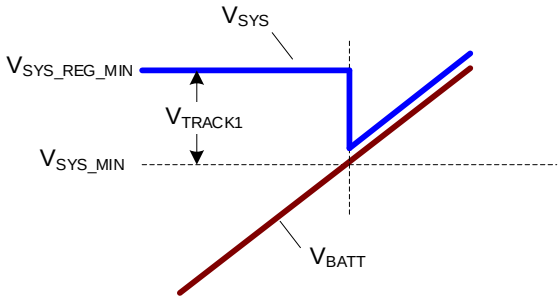
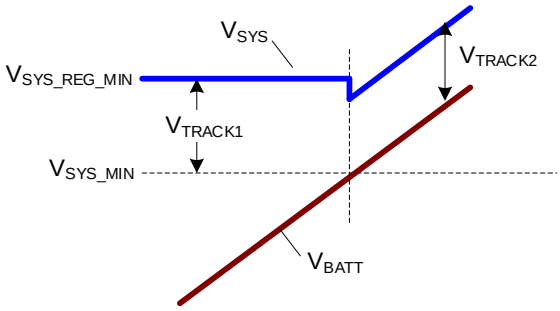
When input source is removed, Q_{BATT} turns on fully to pass the battery power to the system with a low-impedance path.

When the input source is present and the buck converter starts up, the system output is related to V_{BATT}. Figure 4 shows the V_{SYS} variation with V_{BATT} when charging is enabled and disabled.



a) Charging is enabled



b) Charging is disabled

Figure 4: V_{SYS} Variation with V_{BATT}

The steps of the charging process according to V_{BATT} are described below:

1. When the battery is below the minimum system voltage (V_{SYS_MIN}) set by the SYS_MIN_REG bits (07h, bits[3:1]), V_{SYS} is regulated at the sum of V_{SYS_MIN} and battery tracking voltage 1 (V_{TRACK1}) (150mV). Q_{BATT} works in linear mode to charge the battery with trickle-charge, pre-charge, or fast-charge current, depending on V_{BATT}.
2. As V_{BATT} starts to exceed V_{SYS_MIN}, Q_{BATT} turns on fully.
3. When the charge is suspended or completed (Q_{BATT} is turned off), the system voltage is regulated at the sum of V_{SYS_MIN} and V_{TRACK1} (150mV) if V_{BATT} is below V_{SYS_MIN}; the system voltage is regulated at the sum of V_{BATT} and battery tracking voltage 2 (V_{TRACK2}) when V_{BATT} exceeds V_{SYS_MIN}.

Dynamic Power Management

To avoid overloading the input power source, the MP2772 features dynamic power management (DPM) by continuously monitoring I_{IN} and V_{IN}. When the I_{IN_LIM} threshold or V_{IN_LIM} threshold is reached, the battery charge current is reduced to prevent the input source from overloading and to prioritize the system power, load switches' power, or both.

When the IC is operating in the I_{IN_LIM} loop or the V_{IN_LIM} loop, the INLIM_STAT bit (15h, bit[6]) or the VINLIM_STAT bit (15h, bit[5]) is set accordingly. The INPUT_LMT_FLAG bit (10h, bit[3]) is set to 1, and the interrupt alert is generated if the INPUT_LMT_MASK bit (13h, bit[3]) is set to 0 (not masked). If the interrupt is masked, the INPUT_LMT_FLAG bit remains at 1 while there is no interrupt generated.

If the charge current drops to 0A and the system voltage continues dropping while the system load increases, once the system voltage drops below V_{BATT}, the MP2772 automatically enters supplement mode.

Battery Supplement Mode

When the system voltage drops below V_{BATT}, Q_{BATT} turns on to prevent the system voltage from further dropping, and the MP2772 enters battery supplement mode. In this mode, the buck converter and the battery provide power to the system together. If the battery supplies power to the system, then an ideal diode is implemented by forcing the voltage across the BATFET to be 20mV. This facilitates the transition between the BATFET and DC/DC converter.

For load switches powering loads that exceed the input source capacity, the battery cannot enter supplement mode to discharge and power the load switches' loading with the input. Battery supplement mode is only provided for system overload conditions.

If V_{BATT} is below the battery UVLO threshold (V_{BATT_UVLO}), then supplement mode is not available. Under this condition, V_{SYS} can only be powered by the DC/DC converter.

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Therefore, the DC/DC converter is not allowed to be disabled, as the microcontroller unit (MCU) powered by V_{SYS} loses I²C control. The system may enter a locked state until the user removes the input source and inserts it again to exit the locked state.

Battery Charging Profile

The MP2772 can autonomously run a battery charge cycle without requiring the MCU host. Alternatively, the host can control the charging parameters via the registers.

A new charge cycle is initiated if the following conditions are met:

- The buck converter starts up.
- The NTC pin voltage (V_{NTC}) is within the valid temperature range.
- There is no safety timer fault.
- Charging is enabled by pulling the /CE pin low or setting the CHG_EN bit to 1.

The MP2772 checks V_{BATT} to provide four charging phases: trickle charge, pre-charge, constant-current charge, constant-voltage charge, and optional top-off charge. By default, top-off charge is disabled.

Figure 5 shows the full battery charging profile.

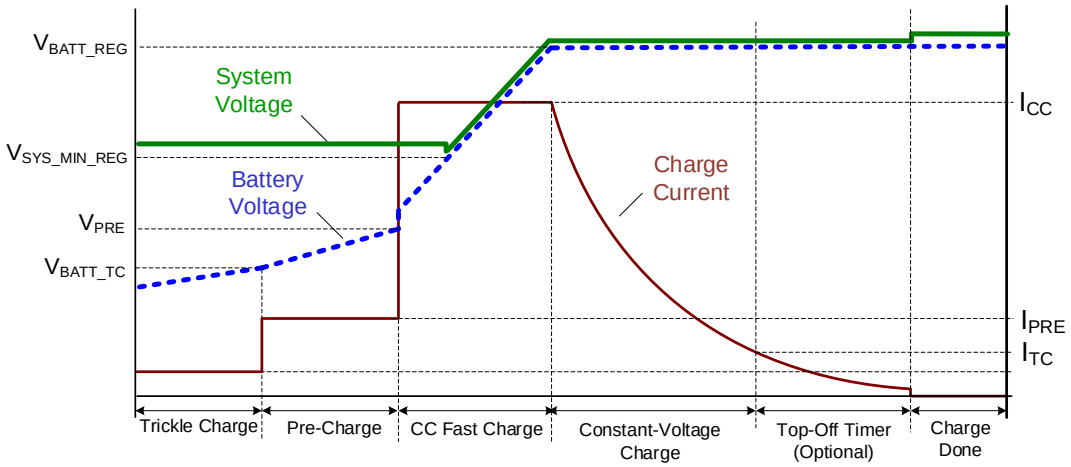

Figure 5: Battery Charging Profile

Charging Phases

Phase 1: Trickle Charge

When P_{IN} is qualified as a good power supply, the MP2772 checks V_{BATT} to determine whether trickle charge is required. If V_{BATT} is below its trickle-charge voltage (V_{BATT_TC}) (2.2V), then the trickle-charge current (I_{TC}) is applied on the battery, which helps reset the protection circuit in the battery pack. I_{TC} can be set via the ITRICKLE bits (02h, bits[2:0]).

Phase 2: Pre-Charge

When V_{BATT} exceeds V_{BATT_TC}, the MP2772 starts to safely pre-charge the deeply depleted battery until V_{BATT} reaches the pre-charge to fast charge threshold (V_{BATT_PRE}). If V_{BATT_PRE} is not reached before pre-charge timer (2hrs) expires, then the charge cycle ends, and a corresponding timeout fault signal is asserted.

The pre-charge current (I_{PRE}) can be configured via the IPRE bits (05h, bits[7:4]), which ranges between 10mA and 160mA.

Phase 3: Constant-Current (CC) Fast Charge

When V_{BATT} exceeds V_{BATT_PRE}, which is set via the VPRE bits (03h, bits[2:1]), the MP2772 enters into constant-current (CC) fast charge phase. The fast charge current (I_{CC}) can be configured via the ICC bits (04h, bits[7:1]). There are two stages during fast charge. Firstly, the BATFET works linearly to charge the battery with I_{CC}. When V_{BATT} exceeds V_{SYS_MIN}, the BATFET turns on fully. The charge current loop is implemented by the buck converter's pulse-width modulation (PWM) control.

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Phase 4: Constant-Voltage Charge

When V_{BATT} rises to the configurable float voltage (V_{BATT_REG}), which is set via the VBATT_REG bits (06h, bits[6:0]), the charge current begins to taper off.

Charge Termination

The charge cycle is considered complete when the charge current reaches the battery termination threshold (I_{TERM}), which is set via the ITERM bits (05h, bits[3:0]).

Termination occurs if the following conditions are met:

- The termination function is enabled by setting the TERM_EN bit (CTRL_CFG_0, bit[1]) to 1.
- The charge current is below the termination threshold for the charge termination deglitch time (t_{TERM_DGL}) (250ms).
- Charging is in constant-voltage phase.
- The device is not in any power limiting state, including I_{IN_LIM}, V_{IN_LIM}, and thermal regulation.

Since top-off timer operation is disabled by default, the MP2772 enters the charge done state immediately after termination occurs. The charge status bits, CHG_STAT (15h, bits[4:2]), are set to charge done state, and the interrupt signal bit, CHG_DONE_FLAG (10h, bit[6]), is set to 1 to send a signal interrupt to indicate charging is complete.

If the top-off timer is enabled, the MP2772 enters the top-off state first, then enters the charge done state after the top-off timer expires.

Top-Off Timer Operation

To further charge the battery after the termination current threshold is crossed and t_{TERM_DGL} expires, a configurable top-off timer can be used to automatically extend the charging time. The TOPOFF_TMR bits (19h, bits[3:2]) configure the top-off timer, including the top-off timer disable.

When the TOPOFF_TMR bits setting exceeds 0, charging continues until the timer expires. Then charging is terminated, and an interrupt is sent.

The top-off timer is reset when any of the following conditions occur:

- Charging is enabled from the disabled state.
- The recharge condition is triggered.
- Register reset is triggered.

Charging Enable Methods

To allow a flexible control scheme for the charging enable, the BATFET can be turned on via either bit or pin control.

Pin control is enabled when the PIN_CTRL_EN bit (01h, bit[4]) is set to 1. Pull the /CE pin low to enable the BATFET and initiate battery charging.

If the PIN_CTRL_EN bit is set to 0, the CHG_EN bit is written to 1 to generate the charge enable signal.

Recharge Operation

When the battery is fully charged and charging is terminated, the battery may be discharged through the leakage current. After V_{BATT} discharges and falls to the automatic recharge battery voltage threshold (V_{BATT_REG} - V_{RECH}), the MP2772 can automatically start another charging cycle if P_{IN} is present and the RCHG_EN bit (06h, bit[7]) is set to 1. A 250ms deglitch timer is applied for detecting V_{BATT} dropping below the recharge threshold.

After charging is terminated, input source re-plugin or re-enabling charging also starts a new charging cycle.

Shipping Mode

In applications where the battery is not removable, it is essential to disconnect the battery from the system to enter shipping mode. Shipping mode is valid without the input present. When the input is present, entering shipping mode via the register and pin control are invalid but entering shipping mode is recorded. Shipping mode entry is active after the input is removed.

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Entering Shipping Mode via the Register

Write 1 to the BATTFET_DIS bit (0Fh, bit[1]).

If the BATTFET_DLY bits (18h, bits[7:6]) are set to b'0, the IC immediately enters shipping mode. If the BATTFET_DLY bits are not set to 0, the device waits for the time specified in the bits before entering shipping mode.

Entering Shipping Mode via Pin Control

The /DISC pin can be used to enter shipping mode. To enter shipping mode through the hardware, the SYS_RST_MODE bit (0Fh, bit[2]) must be set to 0. If there is no P_{IN} present, pull down the /DISC pin for a longer period than the duration set by the T_DISC bits (18h, bits[5:4]) to enter shipping mode.

Exiting Shipping Mode

There are two ways to exit shipping mode, described below:

- Method 1: Plug in the input power source to make the part exit shipping mode automatically and initiate input detection operation.
- Method 2: If the device is in shipping mode, pull down the /DISC pin for a longer period than the duration set by the T_WAKE bits (BAT_FET_CRTL, bits[1:0]) to wake up the device from shipping mode.

Figure 6 shows how to enter and exit shipping mode by pulling the /DISC pin down in the hardware mode.

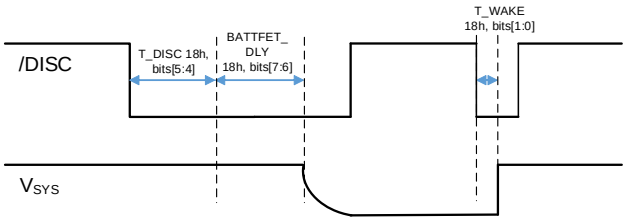

Figure 6: Shipping Mode Entry and Exit via the /DISC Pin

System Pin Power Reset

When the SYS_RST_MODE bit is set to 1, pull the /DISC pin down to trigger automatic reset. This resets the power on the MCU connected to the SYS pin by turning off the BATFET for the time period set via the T_SYS_LOW bits (18h, bits[3:2]), then turns the BATFET back on. Figure 7 shows the timing diagram of the SYS pin power reset.

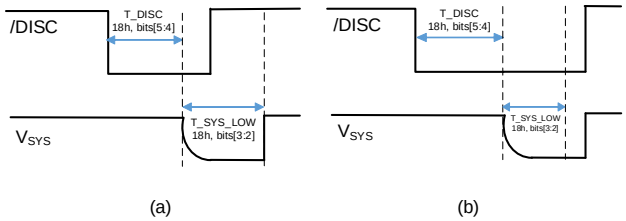

Figure 7: Timing Diagram of the SYS Pin Power Reset

If VIN is inserted, in automatic reset mode, the DC/DC converter also turns off to shut down the SYS pin voltage (V_{SYS}) to trigger the power reset function. To recover V_{SYS} to normal operation, two conditions must be met:

1. The /DISC pin is released.
2. The system's off time exceeds the period set by T_SYS_LOW bits.

Register Reset

Write 1 to the REG_RST bit (00h, bit[7]) resets all registers to the OTP values (OTP-backed) or default values (non-OTP backed).

Watchdog

After start-up, the MP2772 operates with the default set-up. The watchdog timer is disabled by default. Once the watchdog is enabled, write 1 to the WD_RST bit (07h, bit[7]) to restart the watchdog timer counter. The watchdog timer period is 40s, 80s, or 160s, which are configurable via the WD_CFG bits (07h, bits[6:5]).

The WD_ACT bit (07h, bit[4]) defines the behavior of a watchdog timer fault. If the WD_ACT bit is set to 0, the watchdog only resets the register when it times out. If the WD_ACT bit is set to 1, the watchdog not only resets the register but also turns off the BATFET and the DC/DC converter for the time period set via the T_SYS_LOW bits, then re-enables the BATFET to reset the system power at the SYS pin.

Load Switch Operation

The MP2772 integrates two load switches (Q_R and Q_L) that can supply power to the load during either buck operation or boost operation. The load switches are powered through the PMID pin and can be turned on/off separately via the LDSW_EN bits (0Eh, bits[7:6]).

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The load switches are only allowed to turn on during boost mode or buck mode. The LDSW_EN bits do not turn on the load switches during idle or Hi-Z (buck idle) mode.

Boost Start-Up Conditions

The MP2772 enables boost switching if the following conditions are met:

- V_{BATT} > BATT_LOW_TH (08h, bits[5:4])
- Boost is enabled either by setting the PIN_CTRL_EN bit (01h, bit[4]) to 0 and the BOOST_EN bit (00h, bit[4]) to 1, or by setting the PIN_CTRL_EN bit to 1 and setting the BST_EN pin to logic high.

Boost Operation

The boost voltage (V_{BOOST}) loop regulates V_{PMID} based on the setting of the VBOOST bits (0Dh, bits[7:3]). The voltage regulation step size is 100mV/step. The highest V_{BOOST} is 6V, and the lowest V_{BOOST} is selected as the higher value between V_{BATT} + 200mV and lowest VBOOST bits setting (4V). For example, if V_{BATT} is 4.2V, the lowest V_{BOOST} is 4.4V. If V_{BATT} is 3V, the lowest V_{BOOST} is 4V. Boost operation can either provide power to Q_R and Q_L, or it can provide power back to the USB input referred to as the OTG function.

Boost On-The-Go (OTG Function

Once the boost converter starts up and V_{PMID} is stable, the blocking MOSFET (Q_B) can be turned on to supply power through the USB port if the OTG_EN bit (00h, bit[6]) is set to 1 and boost switching is enabled by either bit or pin control.

Boost Load Switch Function

Once the boost converter starts up and V_{PMID} is stable, Q_R and Q_L can be turned on by writing 1 to the LDSW_EN bits.

Due to the boost converter's power constraints, the boost load switch function and OTG function cannot be turned on at the same time. If both functions are enabled, the operation chooses to provide power through Q_R and Q_L as the higher priority.

Boost Light-Load Condition Detection

To minimize power consumption and extend battery life, the MP2772 implements a boost light-load detection function by using the analog-to-digital converter (ADC) to monitor the current through Q_R and Q_L. If the current flowing through Q_R and Q_L is below the preset light-load threshold set via the BST_LIGHT_LD_TH bits (1Ah, bits[6:5]), a light-load condition is detected. An interrupt flag via the BOOST_LD_FLAG bit (11h, bit[0]) is asserted upon detection. The boost light-load condition detection is enabled by setting the LD_DET bit (1Ah, bit[7]) to 1.

Automatic Buck-Boost Transition

Buck to Boost Transition

If both buck and boost switching are enabled, the input removal detection function is activated, and the device can automatically transition from buck operation to boost operation.

When P_{IN} is removed, as V_{IN} drops below the threshold set via the VIN_RM_TH bits (0Dh, bits[2:1]), the input blocking MOSFET turns off, and the boost converter starts to switch. The boost converter is on for a minimum of 0.5s before the IC checks the V_{IN} conditions again. If V_{IN} exceeds the threshold set via the VIN_TH_RM bits again, operation resumes to charge. In most conditions, V_{IN} remains below the threshold set via the VIN_RM_TH bits. The boost lasts for the operation. This function blocks the VIN_RM_TH bits to work for a minimum of 0.5s. This avoids buck and boost transition oscillation.

Boost to Buck Transition

During boost operation, if V_{IN} is plugged in, the input detection circuit starts to validate the input power source and perform BC1.2 detection. After detection is done, the input blocking MOSFET turns on, the boost converter stops switching, and the device enters buck operation.

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Analog-to-Digital Converter (ADC) Operation

There are two types of data used for ADC operation: status data and decision data.

The MP2772 integrates an 8-bit ADC to report status information on V_{IN}, I_{IN}, the system voltage, V_{BATT}, battery charge current, and load switch voltage. The ADC also senses the decision data on the NTC pin and current through the individual load switches (below 100mA).

Write b'1 to the ADC_START bit (0Fh, bit[4]) to enable the ADC to sample all the ADC channels and update the associated registers.

The ADC_RDY_FLAG bit (10h, bit[5]) is generated to signal to the MCU that the ADC data is ready.

The ADC automatically senses the decision data at a rate determined by the ADC_RATE bit (0Fh, bit[3]) (0.5s/100ms). To enable decision data automatic sampling on the NTC pin or the current (below 100mA) through load switch detection, the following actions must be performed by the host MCU:

- NTC protection or PCB hot protection must be enabled by setting the CHG_NTC_EN bits (0Ch, bits[2:1]) to 1, or by setting the PCB_OTP_EN bit (01h, bit[1]) to 1.
- The load switch must be enabled by setting the LDSW_EN bits (0Eh, bits[7:6) to 01, 10, or 11. These bits should not be set to 00. The load switch current-sense circuitry is enabled by setting the LDSW_CS_L_EN bit (0Eh, bit[3]) to 1, or by setting the LDSW_CS_R_EN bit (0Eh, bit[2]) to 1.

Analog-to-Digital Converter (ADC) Data

Table 1 shows the data measured by the ADC.

Table 1: ADC Measurement Data

Data	Full Scale	Recommended Range	LSB
Battery voltage (V_{BATT})	6.375V	2.55V to 5V	25mV
SYS pin voltage (V_{SYS})	6.375V	2.55V to 5V	25mV
NTC pin voltage (V_{NTC})	1.275V	0V to 1.2V	5mV
Input voltage (V_{IN})	10.2V	4.55V to 5.5V	40mV
Trickle charge and pre-charge current	255mA	10mA to 160mA	1mA
Constant-current (CC) charge current (20mA to 320mA)	510mA	20mA to 320mA	2mA
CC charge current (340mA to 2000mA)	2550mA	340mA to 2000mA	10mA
Input current (I_{IN})	3.391A	20mA to 3.2A	13.3mA
LDSW load current ($I_{BOOST1/2}$)	107mA	0mA to 100mA	0.42mA
LDSW voltage ($V_{BOOST1/2}$)	6.375V	4.5V to 5.5V	25mV

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Protections

Input Over-Voltage Protection (OVP)

The input over-voltage lockout (OVLO) threshold is 6.5V. If V_{IN} exceeds increases this threshold, a 10ms deglitch timer is triggered. After the deglitch timer expires and V_{IN} remains above the OVLO threshold, the device disables switching and the load switches turn off as well.

The MP2772 also provides a 14V OVP threshold, which is always active. If V_{IN} exceeds 14V, switching is immediately disabled. After the OVP event is removed, switching is disabled for an additional 5s to prevent repetitive OVP event damage.

System Over-Voltage Protection (OVP)

System OVP ensures that V_{SYS} does not rise high enough to damage the downstream devices. If the system voltage exceeds the SYS_OVP_RI_TH bits (09h, bits[7:4]), switching is immediately disabled. A 10mA current sink is activated after 500µs of an SYS OVP event to help discharge the SYS pin capacitor (C_{SYS}), which discharges the SYS pin.

Boost Mode Over-Voltage Protection (OVP)

During boost operation, when V_{PMID} exceeds the boost OVP threshold (V_{BOOST_OVP}), the device stops switching until V_{PMID} drops below the difference between V_{BOOST_OVP} and the boost OVP hysteresis ($V_{BOOST_OVP_HYS}$).

Boost Battery Low Protection

To protect the battery from being overdrained in boost mode, boost switching automatically turns off when V_{BATT} is below the BATT_LOW_TH setting (2.7V or 2.9V). Battery low protection can also be disabled via the BATT_LOW_TH bit.

Boost On-The-Go (OTG) Short Protection

During boost OTG operation, if V_{IN} drops below the difference between V_{PMID} and 0.75V due to short or heavy loading, the device turns off the blocking MOSFET immediately and enters hiccup mode. After 600ms passes, boost starts up again and softly turns on the input blocking MOSFET again.

Battery Under-Voltage Lockout (UVLO)

To avoid V_{BATT} from being deeply discharged, once V_{BATT} drops below V_{BATT_UVLO}, Q_{BATT} latches off. To recover from this fault, the input power must be plugged in.

Battery Over-Voltage Protection (OVP)

The battery OV threshold is 4% above the battery float voltage. The deglitch time is 100ms. If a battery OV condition is detected, then charging is disabled.

Battery Over-Current Protection (OCP)

There is an over-current limit (OCL) designed in the MP2772 to avoid system over-current conditions during battery discharging. Once the discharge current exceeds the discharge current limit (I_{DSCHG_LIMIT}), the discharge BATFET turns off and enters hiccup mode. After the 600ms recovery time, the discharge BATFET turns on again. If the fault is persistent and hiccup mode continues occurring 8 consecutive times, the BATFET latches off. The BATFET is re-enabled by replugging the input source or pulling down the /DISC pin longer than the wake-up time in shipping mode (t_{WAKE}).

Load Switch Over-Current Protection (OCP)

The load switches (Q_R and Q_L) have configurable OCP thresholds set via the LDSW_OCP bits (0Eh, bits[1:0]), which are in buck mode. The value is typically at about 850mA in buck mode and 550mA in boost mode for each rail when the LDSW_OCP bits are set to the maximum 600mA. Once the current through the load switch trips the over-current (OC) threshold, the load switch enters hiccup mode and restarts every 600ms. If the OC condition remains after eight tries, the load switches are latched off. Toggling the enable register bit for the load switch clears the fault and re-enables the load switch.

Negative Temperature Coefficient (NTC) Protections

The MP2772 provides the NTC pin to connect the device to an external thermistor and the VNTC pin as the reference for standard charging NTC protection and JEITA charging NTC protection.

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Standard Charging NTC Protection

If the CHG_NTC_EN bits are set to b'01, the device performs standard NTC protection. If the detected NTC temperature is outside of the hot/cold threshold range, charging is disabled, and the charging timers are suspended.

JEITA Charging NTC Protection

If the CHG_NTC_EN bits are set to b'10 or b'11, the configurable JEITA profile is used. There are four temperature thresholds defined by JEITA, which are used in the device: cold, cool, warm, and hot. See the Electrical Characteristics section on page 7 for more details regarding the definitions for the MP2772's JEITA temperature thresholds. JEITA is only active in buck charging mode.

Charging is suspended if the NTC is outside of the hot or cold range. At cool temperatures between the NTC cold temperature rising threshold (V_{COLD}) and the NTC cool temperature rising threshold (V_{COOL}), the charge current and/or charge voltage are reduced according to the setting of the COOL_ACT bits (0Ah, bits[5:4]), JEITA_ISET bits (0Ah, bits[1:0]), and JEITA_VSET bits (0Ah, bits[3:2]). At warm temperatures between the NTC warm temperature falling threshold (V_{WARM}) and the NTC hot temperature falling threshold (V_{HOT}), the charge voltage and/or charge current are reduced according to the setting of the WARM_ACT bits (0Ah, bits[7:6]), JEITA_ISET bits, and the JEITA_VSET bits.

PCB Hot Protection

By setting the PCB_OTP_EN bit to 1, the MP2772 activates PCB over-temperature protection for battery charging. During charging, when the NTC hot threshold is reached, charging and the MOSBATFET turn off. Charging resumes once the temperature recovers from the hot condition.

Thermal Regulation and Thermal Shutdown

The thermal regulation limit is set by the TREG bits (0Ch, bits[7:5]). During battery charging, when the MP2772 reaches its internal junction temperature (T_J), the charge current is reduced. During this period, the charging safety timer runs at half-rate and charge termination is blocked.

Thermal shutdown protection is active during all operating states. If the device's internal T_J rises to the shutdown threshold (T_{J_SHDN}) (150°C), then switching is disabled and the BATFET turns off. The device resumes back to normal operation after T_J drops to the thermal shutdown hysteresis (T_{SHDN_HYS}) (30°C), which is below T_{J_SHDN}.

Interrupt Flag

The MP2772 has an open-drain output that signals an interrupt alert to the MCU host. The /INT pin is typically pulled low for 256µs to signal that an interrupt condition has occurred. If the INT_CFG bit (0Fh, bit[7]) is set to 1, when an interrupt is triggered, a 256µs pull-down pulse is generated every 1s until the interrupt is cleared.

There are three interrupt alert commands: INT_FLAG_0 (10h), INT_FLAG_1 (11h), and INT_FLAG_2 (12h). These commands report various operating conditions and the two associated mask commands: INT_FLAG_MASK_0 (13h) and INT_FLAG_MASK_1 (14h). The device sends out an interrupt alert signal only when all the interrupt alert commands are cleared, and the state interrupt mask command is set to 0, which means the interrupt is not masked. To acknowledge and clear the interrupt, write 1 to the asserted interrupt bit in the INT_FLAG_0, INT_FLAG_1, and INT_FLAG_2 commands.

Missing Battery Detection

The MP2772 detects a missing battery when missing battery detection is enabled by setting the BMA_DET_EN bit (01h, bit[0]) to 1. After a missing battery is detected, the interrupt flag of the BATTERY_MISSING_STAT bit (16h, bit[6]) and the BATTERY_MISSING_FLAG bit (10h, bit[1]) are set to 1. An interrupt signal is generated if it is not masked.

After missing battery detection is enabled, the MP2772 sinks the BAT pin to about 10mA for 10ms between 10s intervals when V_{IN} is present and the part is waiting for recharge state. If the battery node gets pulled below the recharge threshold, the algorithm continues loading the battery node for an additional 90ms to determine whether it can be discharged below the trickle charge threshold.

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If the battery node is discharged below the trickle charge threshold, the algorithm triggers charging. If charging completes within 10s, the battery is determined to be missing.

I²C Interface

The MP2772 uses an I²C slave interface for flexible charging parameter configuration and status reporting. The I²C interface supports a communication frequency up to 400kps.

The device operates as a slave device with a 72h address, receiving control inputs from the master device such as the microcontroller or digital signal processor.

SDA and SCL are open-drain lines that are connected to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are high. The data on the SDA line must be stable during the clock's high period. The data line's high or low state can only change when the clock signal on the SCL line is low. A clock pulse is generated for each data bit transferred (see Figure 8 on page 32).

All the transactions begin with a start (S) command and stop (P) command via a stop command. A high to low transition on the SDA line while SCL is high defines a start command. A low to high transition on the SDA line when SCL is high defines a stop command (see Figure 9 on page 32).

Start and stop commands are always generated by the master. The bus is considered busy after the start command, then considered free after the stop command. Each byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte must be followed by an acknowledge (ACK) bit. Data is transferred first with the most significant bit (MSB) (see Figure 9 on page 32).

If a slave cannot receive or transmit another complete data byte until it has performed some other function, then the slave can hold the SCL clock line low to force the master into a wait state (clock stretching). Data transfer resumes when the slave is ready for another data byte and release the SCL clock line.

Acknowledge occurs after each byte. The acknowledge bit allows the receiver to signal to the transmitter that the byte is successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the master.

The transmitter releases the SDA line during the acknowledge clock pulse, allowing the receiver to pull the SDA line low. The SDA line remains high during the 9th clock pulse, which is referred to as the not acknowledge (NACK) signal. The master can then generate either a stop command to halt the transfer or a repeated start command to start a new transfer. After the start command, a slave address is sent, and this address is 7 bits long, followed by the 8th data direction bit (R/W bit), A 0 indicates a transmission (write), and a 1 indicates a request for data (read). Figure 11 on page 32 shows the complete data transfer. Figure 12 on page 33 shows a single write, Figure 13 on page 33 shows a single read, Figure 14 on page 33 shows a multi-byte write, and Figure 15 on page 33 shows a multi-byte read. If the register address is not defined, the charger IC sends back the not acknowledge signal and returns to idle state. The charger device supports multi-read and multi-write via the I²C registers.

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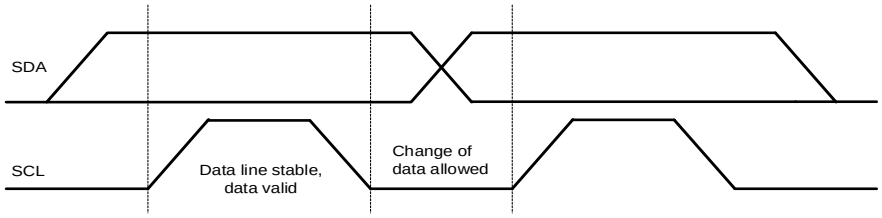

Figure 8: Bit Transfer on I²C Bus

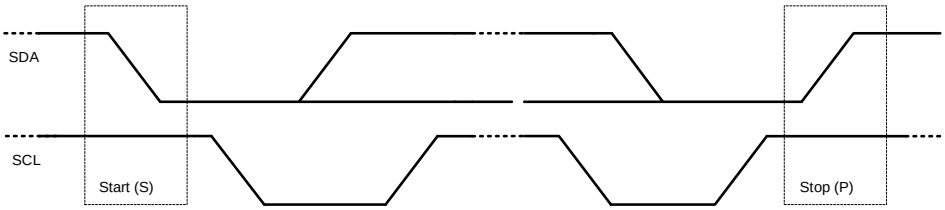

Figure 9: Start and Stop Commands

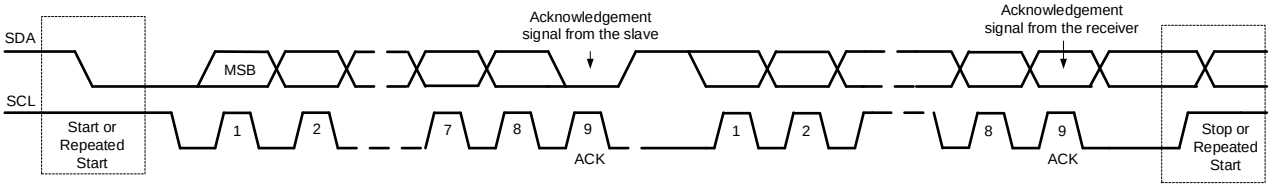

Figure 10: Data Transfer on the I²C Bus

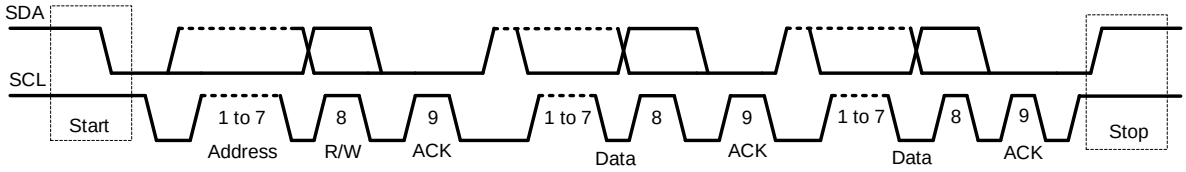

Figure 11: Compete Data Transfer

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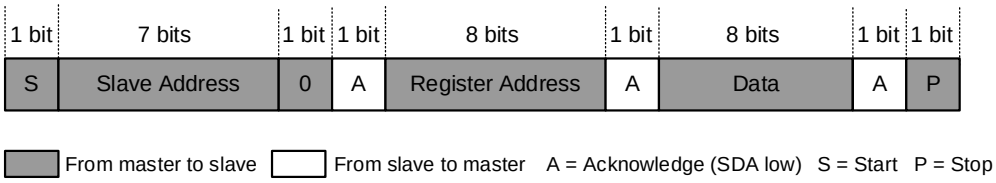

Figure 12: Single Write

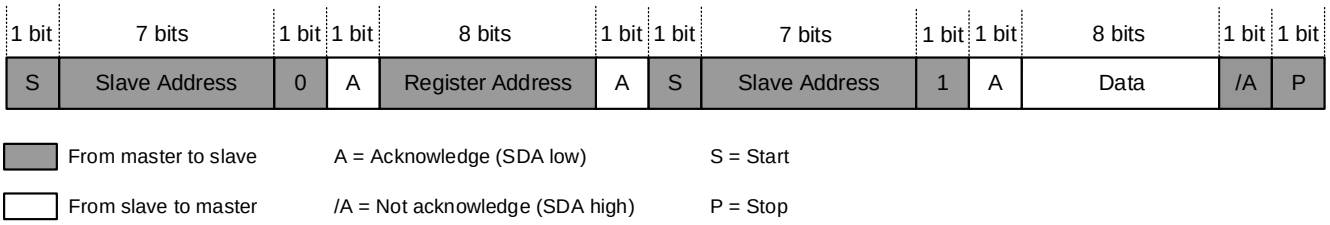

Figure 13: Single Read

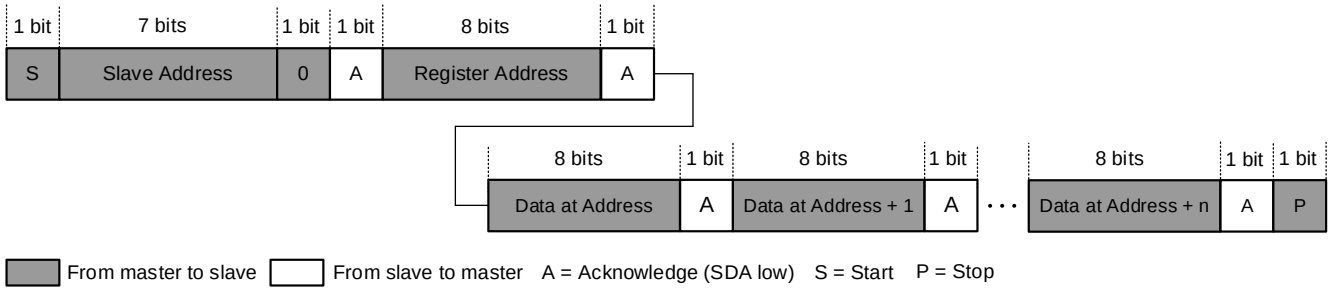

Figure 14: Multi-Byte Write

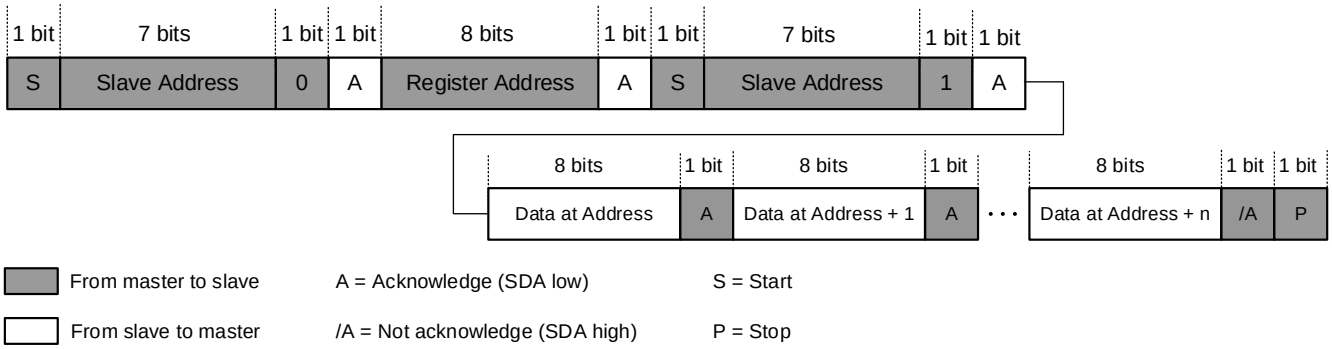

Figure 15: Multi-Byte Read

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SUPPORTED I²C COMMANDS

I²C Slave Address: 72h

Legend: WTD = watchdog, R/W = read/write, R = read-only, OTP-configurable = register's default value can be configured via the one-time programmable (OTP) memory

Command Address	Command Name	Type	Bytes	Description
00h	CTRL_CFG_0	R/W	1	Control configuration 0
01h	CTRL_CFG_1	R/W	1	Control configuration 1
02h	IIN_LIM_CFG	R/W	1	Input current limit configuration
03h	CHG_V_CFG	R/W	1	Charge voltage configuration
04h	CHG_CFG_0	R/W	1	Charging configuration 0
05h	CHG_CFG_1	R/W	1	Charging configuration 1
06h	CHG_CFG_2	R/W	1	Charging configuration 2
07h	SYS_WD_CFG	R/W	1	System watchdog configuration
08h	PROT_CFG_0	R/W	1	Protection configuration
09h	SYS_OVP_CFG	R/W	1	System over-voltage protection (OVP) configuration
0Ah	THRM_PROT_CFG_0	R/W	1	Thermal protection configuration 0
0Bh	THRM_PROT_CFG_1	R/W	1	Thermal protection configuration 1
0Ch	THRM_PROT_CFG_2	R/W	1	Thermal protection configuration 2
0Dh	BOOST_CFG	R/W	1	Boost configuration
0Eh	LDSW_CFG	R/W	1	Load switching configuration
0Fh	OP_CFG	R/W	1	Operation configuration
10h	INT_FLAG_0	R	1	Interrupt flag 0
11h	INT_FLAG_1	R	1	Interrupt flag 1
12h	INT_FLAG_2	R	1	Interrupt flag 2
13h	INT_FLAG_MASK_0	R/W	1	Interrupt flag mask 0
14h	INT_FLAG_MASK_1	R/W	1	Interrupt flag mask 1
15h	STAT_0	R	1	Status register 0
16h	STAT_1	R	1	Status register 1
17h	STAT_2	R	1	Status register 2
18h	BAT_FET_CTRL	R/W	1	Battery MOSFET control
19h	TMR_CFG	R/W	1	Timer configuration
1Ah	BSTOFF_CFG	R/W	1	Boost automatic turn-off configuration
1Bh	VBATT_ADC	R	1	ADC-sensed battery voltage
1Ch	VSYS_ADC	R	1	ADC-sensed system voltage
1Dh	NTC_ADC	R	1	ADC-sensed NTC temperature
1Eh	VIN_ADC	R	1	ADC-sensed input voltage
1Fh	ICHG_ADC	R	1	ADC-sensed charge current
20h	IIN_ADC	R	1	ADC-sensed input current
21h	I_BOOST2_ADC	R	1	ADC-sensed boost 2 current
22h	I_BOOST1_ADC	R	1	ADC-sensed boost 1 current
23h	V_BOOST2_ADC	R	1	ADC-sensed boost 2 output voltage
24h	V_BOOST1_ADC	R	1	ADC-sensed boost 1 output voltage

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REGISTER MAP

CTRL_CFG_0 (00h)

Format: Direct

The CTRL_CFG_0 command controls on-the-go (OTG) mode as well as the charge function, boost function, and buck enable control. In addition, this command controls register reset, termination enable, and frequency selection.

Bits	Access	Bit Name	Default	Description
7	R	REG_RST	1'b0	Resets any read/write (R/W) registers that are configurable by the user. 1'b0: Maintains the current setting 1'b1: Resets any R/W registers configurable by the user to the default setting This bit returns to 0 after it is written to 1.
6	R/W	OTG_EN	1'b0	1b'0: OTG mode is disabled 1b'1: OTG mode is enabled This bit enables the input blocking MOSFET in boost switching mode an can be set via the one-time programmable (OTP) memory.
5	R/W	CHG_EN	1'b1	1b'0: Battery charging is disabled 1b1: Battery charging is enabled This bit can be set via the OTP.
4	R/W	BOOST_EN	1'b0	1b'0: The boost converter is disabled 1b'1: The boost converter is enabled This bit can be set via the OTP.
3	R/W	BUCK_EN	1'b1	1b'0: Buck switching is disabled 1b'1: Buck switching is enabled
2	R/W	FRE_SEL	1'b0	1b'0: The buck charger switches at 1.5MHz 1b'1: The buck charger switches at 2MHz This bit can be set via the OTP.
1	R/W	TERM_EN	1'b1	Enables termination. 1b'0: Termination is disabled 1b'1: Termination is enabled This bit can be set via the OTP.
0	R/W	VIN_TRK_EN	1'b1	0: The input voltage limit (V_{IN_LIM}) loop is fixed 1: V_{IN_LIM} tracks the maximum between 200mV above the battery voltage (V_{BATT}) and the VIN_LIM bit (03h, bits[6:3]) setting

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CTRL_CFG_1 (01h)

Format: Direct

The CTRL_CFG_1 command sets the MP2772's address, pin control enable/disable, PCB over-temperature protection, and the missing battery detection function.

Bits	Access	Bit Name	Default	Description
7:5	R	I2C_ADDR	3'b010	3'b000: 70h 3'b001: 71h 3'b010: 72H 3'b011: 73h 3'b100: 74h 3'b101: 75h 3'b110: 76h 3'b111: 77h Default: 72h The address can only be changed in test mode. The address setting can be selected and fixed in the OTP.
4	R/W	PIN_CTRL_EN	1'b1	1'b0: Pin control is disabled for buck or boost operation 1'b1: Pin control is enabled for buck or boost operation The /CE and BST_EN pins are enabled when this bit is set to 1. If this bit is set to 0, only the CHG_EN bit (00h, bit[5]) and BOOST_EN (00h, bit[4]) can enable boost switching or battery charging. This bit can be set via the OTP.
3	R/W	BAT_OVP_SNK_EN	1'b0	1'b0: Sink discharge on the BAT pin is not enabled 1'b1: Sink discharge on the BAT pin is enabled
2	R/W	ILIM_PIN_EN	1'b1	1'b0: The input current limit (I_{IN_LIM}) is not set via the ILIM pin 1'b1: I_{IN_LIM} is set via the ILIM pin This bit can be set via the OTP.
1	R/W	PCB_OTP_EN	1'b0	1'b0: PCB over-temperature protection is not enabled 1'b1: PCB over-temperature protection is enabled This bit can be set via the OTP.
0	R/W	BMA_DET_EN	1'b1	1'b0: Missing battery detection is not enabled 1'b1: Missing battery detection is enabled

IIN_LIM_CFG (02h)

Format: Direct

The IIN_LIM_CFG command sets the IC's input current limit (I_{IN_LIM}) and the trickle charge current (I_{TC}).

Bits	Access	Bit Name	Default	Description
7:3	R/W	IIN_LIM	5'b00100	Sets I_{IN_LIM}. Range: 100mA (00000) to 3200mA (11111) Offset: 100mA Step: 100mA Default: 500mA (00100) The default I_{IN_LIM} setting can be set via the OTP.
2:0	R/W	ITRICKLE	3'b100	Sets I_{TC}. Range: 10mA (000) to 70mA (110) Offset: 10mA Default: 50mA (100) The I_{TC} > 70mA setting is clamped to 70mA. The default I_{TC} can be set via the OTP.

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CHG_V_CFG (03h)

Format: Direct

The CHG_V_CFG command sets the IC's input voltage limit (V_{IN_LIM}), pre-charge threshold, and the automatic recharge threshold.

Bits	Access	Bit Name	Default	Description
7	R	RESERVED	N/A	Reserved.
6:3	R/W	VIN_LIM	4'b0110	Sets the V_{IN_LIM} range. Range: 3.9V (0000) to 5.4V (1111) Offset: 3.9V Default: 4.5V (0110) The default value can be set via the OTP.
2:1	R/W	VPRE	2'b11	Sets the pre-charge to constant-current charge battery voltage threshold, where the default is 3V (11). 2'b00: 2.4V 2'b01: 2.6V 2'b10: 2.8V 2'b11: 3V The default value can be set via the OTP.
0	R/W	VRECHG	1'b0	Sets the automatic recharge threshold below the battery-full voltage, where the default is 100mV. 1'b0: 100mV threshold 1'b1: 200mV threshold The default value can be set via the OTP.

CHG_CFG_0 (04h)

Format: Direct

The CHG_CFG_0 command sets the constant-charge current (I_{CC}) and the method to select I_{IN_LIM}.

Bits	Access	Bit Name	Default	Description
7:1	R/W	ICC	7'b0011 000	Sets I_{CC}. Range: 20mA (0000000) to 2000mA (1100011) Offset: 20mA Step: 20mA Default: 500mA (0011000) When I_{CC} is set above 2A, it is latched to 2A. The default value can be set via the OTP.
0	R/W	ILIM_RECONFIG	1'b0	When I_{IN_LIM} is not set via ILIM pin control, this bit determines whether to use the USB Battery Charging 1.2 (BC1.2) detection results or the IIN_LIM bit value (set via 02h, bits[7:3]) to set I_{IN_LIM}. If BC1.2 is disabled and ILIM pin control is disabled, this bit is set to 0 and has no effect, and I_{IN_LIM} is determined by the IIN_LIM bits (02h, bits[7:3]) setting. 1'b0: Use I_{IN_LIM} configured as the BC1.2 detection value 1'b1: Use the IIN_LIM bit setting for the I_{IN_LIM} reference This bit can be set via the OTP.

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CHG_CFG_1 (05h)

Format: Direct

The CHG_CFG_1 command sets the pre-charge current (I_{PRE}) and the charge termination current (I_{TERM}).

Bits	Access	Bit Name	Default	Description
7:4	R/W	IPRE	4'b1001	Sets I_{PRE}. Range: 10mA (0000) to 160mA (1111) Offset: 10mA Step: 10mA Default: 100mA (1001) The default value can be set via the OTP.
3:0	R/W	ITERM	4'b1001	Sets I_{TERM}. Range: 10mA (0000) to 160mA (1111) Offset: 10mA Step: 10mA Default: 100mA (1001) The default value can be set via the OTP.

CHG_CFG_2 (06h)

Format: Direct

The CHG_CFG_2 command sets the regulation battery voltage (V_{BATT_REG}).

Bits	Access	Bit Name	Default	Description
7	R/W	RCHG_EN	1'b1	1'b0: Automatic recharge function is disabled 1'b1: Automatic recharge function is enabled This bit can be set via the OTP.
6:0	R/W	VBATT_REG	7'b0111 100	Sets V_{BATT_REG}. Range: 3.6V (0000000) to 4.6V (1100100) Offset: 3.6V Step: 10mV Default: 4.2V (0111100) When V_{BATT_REG} is set over 4.6V, it is latched to 4.6V. The default value can be set via the OTP.

SYS_WD_CFG (07h)

Format: Direct

The SYS_WD_CFG command sets the watchdog timer and the minimum system regulation voltage ($V_{SYS_MIN_REG}$).

Bits	Access	Bit Name	Default	Description
7	R/W	WD_RST	1'b0	Write 1 to this bit to reset the watchdog timer.
6:5	R/W	WD_CFG	2'b00	2'b00: Disables the timer 2'b01: 40s 2'b10: 80s 2'b11: 160s Default: Watchdog is disabled (00) The default setting can be set by OTP.

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4	R/W	WD_ACT	1'b0	1'b0: The R/W register that can be reset by watchdog timeout reloads to the default setting 1'b1: The R/W register that can be reset by watchdog timeout reloads to the default setting and power is cycled on the SYS pin Default: The R/W register that can be reset by watchdog timeout reloads to the default setting The default setting can be via the OTP.
3:1	R/W	SYS_MIN_REG	3'b010	Sets $V_{SYS_MIN_REG}$. Range: 3.2V (000) to 4.25V (111) Offset: 3.2V Step: 150mV Default: 3.5V (010) The default value can be set via the OTP.
0	R	RESERVED	N/A	Reserved.

PROT_CFG_0 (08h)

Format: Direct

The PROT_CFG_0 command sets the input over-voltage protection (OVP) threshold and the low V_{BATT} threshold for OTG mode. This command also enables protection control.

Bits	Access	Bit Name	Default	Description
7:6	R/W	RESERVED	N/A	Reserved.
5:4	R/W	BATT_LOW_TH	2'b10	Disables boost discharge when V_{BATT} is below the low voltage threshold. 2'b00: Disabled. No low voltage threshold to disable the boost converter 2'b01: 2.7V 2'b10: 2.9V 2'b11: 2.9V Default: 2.9V (10) The default value can be set via the OTP.
3	R/W	SYS_OVP_EN	1'b1	1'b0: System OVP is disabled 1'b1: System OVP is enabled Default: System OVP is enabled (1) The default value can be set via the OTP.
2	R/W	BATT_FET_OCP_EN	1'b1	1'b0: Battery MOSFET (BATFET) discharge over-current protection (OCP) is disabled 1'b1: BATFET discharge OCP is enabled Default: Enabled (1) The default value can be set via the OTP.
1	R/W	BATT_OVP_EN	1'b1	1'b0: Battery OVP is disabled 1'b1: Battery OVP is enabled Default: Battery OVP is enabled (1) The default value can be set via the OTP.
0	R	RESERVED	N/A	Reserved.

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SYS_OVP_CFG (09h)

Format: Direct

The SYS_OVP_CFG command sets the system OVP rising and falling thresholds.

Bits	Access	Bit Name	Default	Description
7:4	R/W	SYS_OVP_RI_TH	4'b1010	Sets the system OVP rising threshold. Range: 3.8V (0000) to 5.3V (1111) Offset: 3.8V Step: 100mV Default: 4.8V(1010) The default value can be set via the OTP.
3:0	R/W	SYS_OVP_FL_TH	4'b1010	Sets the system OVP recovery falling threshold. Range: 3.6V (0000) to 5.1V (1111) Offset: 3.6V Step: 100mV Default: 4.6V(1010) The default value can be set via the OTP.

THRM_PROT_CFG_0 (0Ah)

Format: Direct

The THRM_PROT_CFG_0 command sets the JIETA protection actions.

Bits	Access	Bit Name	Default	Description
7:6	R/W	WARM_ACT	2'b01	Sets the protection action at the negative temperature coefficient (NTC) warm temperature. 2'b00: No action 2'b01: Reduces V_{BATT_REG} 2'b10: Reduces I_{CC} 2'b11: Reduces both V_{BATT_REG} and I_{CC} Default: Reduces V_{BATT_REG} (01)
5:4	R/W	COOL_ACT	2'b10	Sets the protection action at the NTC cool temperature. 2'b00: No action . Charging stops 2'b01: Reduces V_{BATT_REG} 2'b10: Reduces I_{CC} 2'b11: Reduces both V_{BATT_REG} and I_{CC} Default: Reduces I_{CC} (10)
3:2	R/W	JEITA_VSET	2'b00	2'b00: V_{BATT_REG} - 100mV 2'b01: V_{BATT_REG} - 150mV 2'b10: V_{BATT_REG} - 200mV 2'b11: V_{BATT_REG} - 250mV Default: V_{BATT_REG} - 100mV (00)
1:0	R/W	JEITA_ISET	2'b00	2'b00: 50% of I_{CC} 2'b01: 33% of I_{CC} 2'b10: 25% of I_{CC} 2'b11: 16.7% of I_{CC} Default: 50% of I_{CC} (00)

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THRM_PROT_CFG_1 (0Bh)

Format: Direct

The THRM_PROT_CFG_1 command sets the JIETA protection thresholds.

Bits	Access	Bit Name	Default	Description
7:6	R/W	VHOT	2'b10	Sets the NTC hot falling threshold. 2'b00: 29.1% (50°C) 2'b01: 25.9% (55°C) 2'b10: 23.0% (60°C) 2'b11: 20.4% (65°C) Default: 23% (10)
5:4	R/W	VWARM	2'b10	Sets the NTC warm falling threshold. 2'b00: 36.5% (40°C) 2'b01: 32.6% (45°C) 2'b10: 29.1% (50°C) 2'b11: 25.9% (55°C) Default: 29.1% (10)
3:2	R/W	VCOOL	2'b10	Sets the NTC cool rising threshold. 2'b00: 74.2% (0°C) 2'b01: 69.6% (5°C) 2'b10: 64.8% (10°C) 2'b11: 59.9% (15°C) Default: 64.8% (10)
1:0	R/W	VCOLD	2'b01	Sets the NTC cold rising threshold. 2'b00: 78.4% (-5°C) 2'b01: 74.2% (0°C) 2'b10: 69.6% (5°C) 2'b11: 64.8% (10°C) Default: 74.2% (01)

THRM_PROT_CFG_2 (0Ch)

Format: Direct

The THRM_PROT_CFG_2 command sets the thermal regulation thresholds and the NTC protection options.

Bits	Access	Bit Name	Default	Description
7:5	R/W	TREG	3'b100	Sets the thermal regulation threshold for charging. 3'b000: 60°C 3'b001: 70°C 3'b010: 8°C 3'b011: 9°C 3'b100: 100°C 3'b101: 11°C 3'b110: 120°C Default: 100°C (100)
4:3	R	RESERVED	N/A	Reserved.
2:1	R/W	CHG_NTC_EN	2'b01	2'b00: Charger NTC monitoring is disabled 2'b01: Charger standard NTC monitoring (only the hot/cold threshold) 2'b10: Charger JEITA NTC monitoring is enabled 2'b11: Charger JEITA NTC monitoring is enabled Default: Standard NTC monitor (01)

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0	R	RESERVED	N/A	Reserved.

BOOST_CFG (0Dh)

Format: Direct

The BOOST_CFG command controls the boost output (V_{OUT_BOOST}) voltage as well as the OTG output.

Bits	Access	Bit Name	Default	Description
7:3	R/W	VBOOST	5'b01010	Sets V_{OUT_BOOST}. Range:4V to 6V (maximum clamped to 6V) Step: 100mV Offset: 4V Default: 5V (01010) This bit can be set via the OTP
2:1	R/W	VIN_RM_TH	2'b00	Sets the input threshold to initiate automatic boost. 2'b00: 3.9V 2'b01: 4.2V 2'b10: 4.5V 2'b11: 4.8V When input voltage (V_{IN}) drops below this threshold, the boost converter automatically turns on, where the default is 3.9V (00). The default value can be set via the OTP.
0	R	RESERVED	N/A	Reserved.

LDSW_CFG (0Eh)

Format: Direct

The LDSW_CFG command controls the output of the load switches (Q_R and Q_L) as well as the OTG output.

Bits	Access	Bit Name	Default	Description
7:6	R/W	LDSW_EN	2'b00	2'b00: Q_R and Q_L are both disabled 2'b01: Q_R is enabled 2'b10: Q_L is enabled 2'b11: Q_R and Q_L are both enabled Default: Q_R and Q_L are both disabled (00) This bit can be set via the OTP.
5:4	R/W	OTG_ILIM	2'b11	Sets the boost OTG output current limit (I_{OTG_LIM}). 2'b00: 500mA 2'b01: 900mA 2'b10: 1.2A 2'b11: 1.5A Default: 1.5A (11) The default value can be set via the OTP.
3	R/W	LDSW_CS_L_EN	1'b0	1'b0: The current sensing circuitry is disabled for Q_L 1'b1: The current sensing circuitry is enabled for Q_L
2	R/W	LDSW_CS_R_EN	1'b0	1'b0: The current sensing circuitry is disabled for Q_R 1'b1: The current sensing circuitry is enabled for Q_R

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1:0	R/W	LDSW_OCP	2'b11	Sets the over-current limit thresholds for the load switches' output in buck mode. 00: 150mA 01: 300mA 10: 450mA 11: 600mA

OP_CFG (0Fh)

Format: Direct

The OP_CFG command provides several controls for the device as well as the ADC setting.

Bits	Access	Bit Name	Default	Description
7	R/W	INT_CFG	1'b0	1'b0: One-shot interrupt pulse 1'b1: Continuous interrupt pulse (1s period) This bit can be set via the OTP.
6	R/W	USB_DET_EN	1'b1	1'b0: Automatic BC1.2 detection is disabled 1'b1: Automatic BC 1.2 detection is enabled Toggling this bit can force BC1.2 detection to restart. This bit can be set via the OTP.
5	R/W	VIN_DISCHG_EN	1'b1	Enables the VIN pin automatic discharge when the input is removed. 1'b0: Disabled 1'b1: Enabled
4	R/W	ADC_START	1'b0	1'b0: Disables the ADC 1'b1: Enables the ADC This bit is written to 1 to trigger a conversion on all ADC channels.
3	R/W	ADC_RATE	1'b0	1'b0: 0.1s ADC sampling rate 1'b1: 0.5s ADC sampling rate
2	R/W	SYS_RST_MODE	1'b1	1'b0: Manual reset. Pull down the /DISC pin to disable the BATFET; the BATFET is not automatically re-enabled 1'b1: Automatic reset. Pull down the /DISC pin to disable the VSYS output, then enable the VSYS output again
1	R/W	BATTFET_DIS	1'b0	1'b0: Enables the BATFET 1'b1: Disables the BATFET Write 1 to this bit to disable the BATFET after the time specified by the BATTFET_DLY bits (08h, bits[7:6]), then enter shipping mode. This bit control is only valid without V_{IN}.
0	R/W	BOX_TIME_EN	1'b0	1'b0: The 10s box time before entering shipping mode is not enabled 1'b1: The 10s box time before entering shipping mode is enabled

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INT_FLAG_0 (10h)

Format: Direct

The INT_FLAG_0 command shows the interrupt flag of some operation statuses or faults. Write 1 to clear these interrupt flags.

Bits	Access	Bit Name	Default	Description
7	R	VIN_PG_FLAG	1'b0	1'b0: There is no change in the V_{IN} power good (PG) status 1'b1: The V_{IN} PG status changes
6	R	CHG_DONE_FLAG	1'b0	1'b0: Charging is not finished 1'b1: Charging finished
5	R	ADC_RDY_FLAG	1'b0	1'b0: ADC conversion is not complete 1'b1:ADC conversion is complete
4	R	VIN_DET_FLGA	1'b0	1'b0: V_{IN} detection is not complete 1'b1: V_{IN} detection is complete
3	R	INPUT_LMT_FLAG	1'b0	1'b0: The device is not in an input limiting state 1'b1: The device enters an input limiting state
2	R	NTC_FAULT_FLAG	1'b0	1'b0:There is no NTC fault 1'b1: There is an NTC fault
1	R	BATTERY_MISSING_FLAG	1'b0	1'b0: A missing battery is not detected 1'b1: A missing battery is detected
0	R	CHG_TMR_FLAG	1'b0	1'b0: There is no charger timer fault 1'b1: A charger timer fault has occured (either pre-charge or full cycle timer fault)

INT_FLAG_1 (11h)

Format: Direct

The INT_FLAG_1 command shows the interrupt flag of some operation status or faults. Write 1 to clear these interrupt flags.

Bits	Access	Bit Name	Default	Description
7	R	WD_FAULT_FLAG	1'b0	1'b0: There is no watchdog timer fault 1'b1: A watchdog timer fault occurred
6	R	BOOST_LOW_FLAG	1'b0	1'b0: There is no boost low battery fault 1'b1: A boost low battery fault occurred
5	R	BOOST_OV_FLAG	1'b0	1'b0: There is no over-voltage (OV) condition for the boost output 1'b1: There is an OV condition for the boost output
4	R	BOOST_PMIDUV_FLAG	1'b0	1'b0: There is no under-voltage (UV) condition for the boost output 1'b1: There is an UV condition for the boost output
3	R	OTG_SC_FLAG	1'b0	1'b0: There is no OTG short fault 1'b1: An OTG short fault occurred
2	R	LDSW_OC_FLAG	1'b0	1'b0: There is no over-current (OC) fault for the load switch 1'b1: There is an OC fault for the load switch
1	R	LDSW_OV_FLAG	1'b0	1'b0: There is no OV fault for the load switch 1'b1: There is an OV fault for the load switch
0	R	BOOST_LD_FLAG	1'b0	1'b0: The boost converter is not under a light-load condition 1'b1: The boost converter is under a light-load condition

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INT_FLAG_2 (12h)

Format: Direct

The INT_CFG_2 command shows the interrupt flag of some operation statuses or faults. Write 1 to clear these interrupt flags.

Bits	Access	Bit Name	Default	Description
7	R	INPUT_OV_FLAG	1'b0	1'b0: There is no OV condition for the input 1'b1: There is an OV condition for the input
6	R	BATTERY_OV_FLAG	1'b0	1'b0: There is no OV battery fault 1'b1: There is an OV battery fault
5	R	SYS_OV_FLAG	1'b0	1'b0: There is no OV condition for the system output 1'b1: There is an OV condition for the system output
4	R	SYS_SC_FLAG	1'b0	1'b0: There is no short-circuit condition for the system output 1'b1: There is a short-circuit condition for the system output
3	R	BATTERY_OCP_ FLAG	1'b0	1'b0: There is no OC fault at the BATFET 1'b1: There is an OC fault at the BATFET
2	R	THRM_REG_FLAG	1'b0	1'b0: There is no thermal regulation condition 1'b1: The device operates under a thermal regulation condition
1	R	THRM_SHDN_FLAG	1'b0	1'b0: There is no thermal shutdown condition 1'b1: The device operates under a thermal shutdown condition
0	R	RESERVED	N/A	Reserved.

INT_FLAG_MASK_0 (13h)

Format: Direct

The INT_FLAG_MASK_0 command determines whether an interrupt is generated when the IC status changes.

Bits	Access	Bit Name	Default	Description
7	R/W	VIN_PG_MASK	1'b1	Masks the V_{IN} PG flag. 1'b0: Unmasked 1'b1: Masked
6	R/W	CHG_DONE_MASK	1'b1	Masks the charge done flag. 1'b0: Unmasked 1'b1: Masked
5	R/W	ADC_RDY_MASK	1'b1	Masks the ADC ready flag. 1'b0: Unmasked 1'b1: Masked
4	R/W	VIN_DET_MASK	1'b1	Masks the V_{IN} detection flag. 1'b0: Unmasked 1'b1: Masked
3	R/W	INPUT_LMT_MASK	1'b1	Masks the input limit flag. 1'b0: Unmasked 1'b1: Masked
2	R/W	CHG_FAULT_MASK	1'b1	Masks the input OV flag, battery OV flag, system OV flag, system short-circuit flag, and charger timer flag. 1'b0: Unmasked 1'b1: Masked

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1	R/W	NTC_FAULT_MASK	1’b1	Masks the NTC fault flag. 1’b0: Unmasked 1’b1: Masked
0	R	RESERVED	N/A	Reserved.

INT_FLAG_MASK_1 (14h)

Format: Direct

The INT_FLAG_MASK_1 command determines whether an interrupt is generated when the IC status changes.

Bits	Access	Bit Name	Default	Description
7	R/W	TIMER_FAULT_ MASK	1’b1	Masks the watchdog fault flag. 1’b0: Unmasked 1’b1: Masked
6	R/W	BOOST_FAULT_ MASK	1’b1	Masks the boost low flag, boost OV flag, boost PMID UV flag, and OTG short-circuit flag. 1’b0: Unmasked 1’b1: Masked
5	R/W	BOOST_LD_MASK	1’b1	Masks the boost light-load flag. 1’b0: Unmasked 1’b1: Masked
4	R/W	THRM_FAULT_MASK	1’b1	Masks the thermal shutdown flag and thermal regulation flag. 1’b0: Unmasked 1’b1: masked
3	R/W	LDSW_FAULT_MASK	1’b1	Masks the load switch OC flag and load switch OV flag. 1’b0: Unmasked 1: Masked
2	R/W	BATTERY_OCP_ MASK	1’b0	Masks the battery OCP flag. 1’b0: Unmasked 1’b1: Masked
1	R/W	BATTERY_MISSING_ MASK	1’b1	Masks the missing battery flag. 1’b0: Unmasked 1’b1: Masked
0	R	RESERVED	N/A	Reserved.

STAT_0 (15h)

Format: Direct

The STAT_0 command shows the operation status.

Bits	Access	Bit Name	Default	Description
7	R	VIN_PG_STAT	1’b0	1’b0: A PG condition is not detected 1’b1: A PG condition is detected
6	R	INLIM_STAT	1’b0	1’b0: The charger is not in an input current limiting state 1’b1: The charger in an input current limiting state
5	R	VINLIM_STAT	1’b0	1’b0: The device is not in a V_{IN} limiting state 1’b1: The device is in a V_{IN} limiting state

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4:2	R	CHG_STAT	3’b000	3’b000: The device is not charging 3’b001: The device is in a trickle charge or pre-charge state 3’b010: Constant-charge (CC) or constant-voltage (CV) state 3’b011: CV loop and I_{CHG} < I_{TERM} (between CV and charge done/top-off active) deglitch stage before termination 3’b100: Top-off active 3’b101: Charge done 3’b110: Battery OV
1:0	R	VIN_STAT	2’b00	2’b00: V_{IN} type unknown 2’b01: Standard downstream port (SDP) detected 2’b10: Charging downstream port (CDP) detected 2’b11: Dedicated charging port (DCP) detected

STAT_1 (16h)

Format: Direct

The STAT_1 command shows the operation status.

Bits	Access	Bit Name	Default	Description
7	R	BST_LD_STAT	1’b0	1’b0: The boost converter is not under a light-load condition 1’b1: The boost converter is in a light-load condition If the load switches’ current sense is not enabled, then this bit remains set to 0.
6	R	BATTERY_ MISSING_STAT	1’b0	1’b0: The battery is present 1’b1: The battery is missing If missing battery detection is not enabled, then this bit remains set to 0.
5	R	BOOST_OV_STAT	1’b0	1’b0: No OV condition is present at the boost output 1’b1: An OV condition is present at the boost output
4	R	LDSW_OV_STAT	1’b0	1’b0: No OV condition is present at the load switch output 1’b1: An OV condition is present at the load switch output
3	R	INPUT_OV_STAT	1’b0	1’b0: No OV condition is present at the input 1’b1: An OV condition is present at the input
2	R	SYS_OV_STAT	1’b0	1’b0: No OV condition is present at the system output 1’b1: An OV condition is present at the system output
1:0	R	RESERVED	N/A	Reserved.

STAT_2 (17h)

Format: Direct

The STAT_2 command shows the operation status.

Bits	Access	Bit Name	Default	Description
7	R	NTC_MISSING	1’b0	1’b0: There is no fault 1’b1: The NTC is missing
6	R	NTC_COLD	1’b0	1’b0: There is no fault 1’b1: There is an NTC cold fault
5	R	NTC_COOL	1’b0	1’b0: There is no fault 1’b1: There is an NTC cool fault
4	R	NTC_WARM	1’b0	1’b0: There is no fault 1’b1: There is an NTC warm fault
3	R	NTC_HOT	1’b0	1’b0: There is no fault 1’b1: There is an NTC hot fault

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2	R	THRM_SHDN_STAT	1’b0	1’b0: There is no fault 1’b1: Thermal shutdown occurs
1	R	THRM_REG_STAT	1’b0	1’b0: Thermal regulation is not active 1’b1: Thermal regulation is active
0	R	RESERVED	N/A	Reserved.

BAT_FET_CRTL (18h)

Format: Direct

The BAT_FET_CTRL command sets the BATFET on/off control.

Bits	Access	Bit Name	Default	Description
7:6	R/W	BATTFET_DLY	2’b11	2’b00: Turn off the BATFET immediately 2’b01: Turn off the BATFET after a 2s delay 2’b10: Turn off the BATFET after a 4s delay 2’b11: Turn off the BATFET after an 8s delay Default: Turn off the BATFET after an 8s delay (11) The default value can be set via the OTP.
5:4	R/W	T_DISC	2’b01	Sets the glitch filter timeout for the /DISC pin pulled low. Glitch filter expiration triggers turning off the BATFET or cycling power on the SYS pin. 2’b00: 1s 2’b01: 2s 2’b10: 4s 2’b11: 8s Default: 2s (01) The default value can be set via the OTP.
3:2	R/W	T_SYS_LOW	2’b00	Sets the system low time before re-enabling the BATFET during reset mode. 2’b00: 0.5s 2’b01: 1s 2’b10: 2s 2’b11: 4s Default: 0.5s (00) The default value can be set via the OTP.
1:0	R/W	T_WAKE	2’b01	Sets the /DISC pin low time to re-enable the BATFET and exit shipping mode. 2’b00: 500ms 2’b01: 1s 2’b10: 2s 2’b11: 4s Default: 1s (01) The default value can be set via the OTP.

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TMR_CFG (19h)

Format: Direct

The TMR_CFG command sets the timer options.

Bits	Access	Name	Default	Description
7	R/W	TMR2x_EN	1’b1	The timer doubles under input limiting states and the thermal regulation state. 1’b0: Disabled 1’b1: Enabled
6:5	R/W	FULL_CHG_TMR	2’b01	2’b00: Disables the timer 2’b01: 5hrs 2’b10: 10hrs 2’b11: 15hrs Default: 5hrs (01) The default value can be set via the OTP.
4	R/W	PRE_CHG_TMR_EN	1’b1	1’b0: The pre-charge timer is disabled 1’b1: The pre-charge timer is enabled (2hr) The bit can be set via the OTP.
3:2	R/W	TOPOFF_TMR	2’b00	2’b00: Disabled 2’b01: 15 minutes 2’b10: 30 minutes 2’b11: 45 minutes Default: Disabled (00) The default value can be set via the OTP.
1:0	R	RESERVED	N/A	Reserved.

BSTOFF_CFG (1Ah)

Format: Direct

The BSTOFF_CFG register sets the boost light load status.

Bits	Access	Bit Name	Default	Description
7	R/W	LD_DET	1’b0	1’b0: The automatic light-load detection function is disabled 1’b1: The automatic light load detection function is enabled
6:5	R/W	BST_LIGHT_LD_TH	2’b00	Sets the boost light-load detection thresholds. The current is measured passing through the load switch during boost switching and once the current drops below the pre-set threshold, a light-load condition is detected. 2’b00: 5mA 2’b01:10mA 2’b10: 20mA 2’b11: 40mA Default: 5mA (00) The default value can be set via the OTP.
4:0	R	RESERVED	N/A	Reserved.

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READ-ONLY REGISTERS FOR ADC (8-BIT)

Address	Name	Description
1Bh	VBATT_ADC	Sensed battery voltage
1Ch	VSYS_ADC	Sensed system voltage
1Dh	NTC_ADC	Sensed NTC voltage
1Eh	VIN_ADC	Sensed input voltage
1Fh	ICHG_ADC	Sensed charge current
20h	IIN_ADC	Sensed input current
21h	I_BOOST2_ADC	Sensed boost 2 (Q_L) current
22h	I_BOOST1_ADC	Sensed boost 1 (Q_R) current
23h	V_BOOST2_ADC	Sensed boost 2 (Q_L) voltage
24h	V_BOOST1_ADC	Sensed boost 1 (Q_R) voltage

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APPLICATION INFORMATION

Selecting the Charge Termination Current

The MP2772 provides a wide range of charge termination current options between 10mA and 160mA for different applications. In addition to the charge current, the MP2772 can supply the system load through its buck converter's output and its load switches' outputs. In applications where the input adapter power may be low and the total system output power may be high, the MP2772 activates its input current loop or input voltage loop to prevent overloading the adapter. This action reduces the charge current, which then reduces the battery voltage (V_{BATT}) due to the battery pack's internal resistance (R_{BATT}). The battery voltage drop (ΔV_{BATT}) can be calculated with Equation (1):

$$\Delta V_{BATT} = I_{TERM} \times R_{BATT} \quad (1)$$

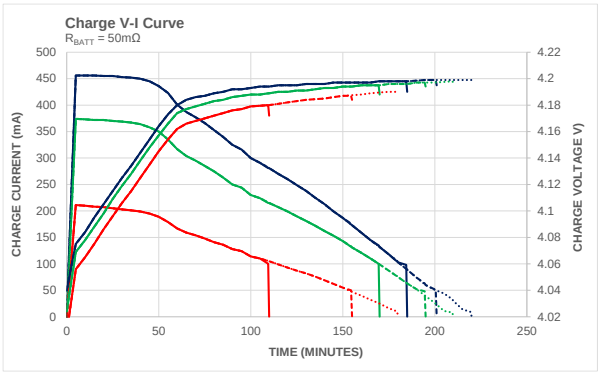
The combination of the heavy system load and battery internal resistance can result in the MP2772 terminating charging early, and becomes especially evident if R_{BATT} and the system load are high with a low-capacity input adapter.

Figure 16 shows the charge V-I curve under different system loads, where the input current limit (I_{IN_LIM}) is set to 500mA. With the same charge termination current, a heavier system load may cause charge termination to occur earlier. Setting the charge termination current lower charges the battery as high as possible.

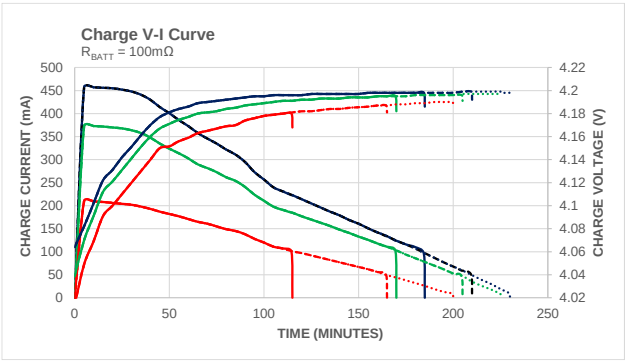
When R_{BATT} is high, it is recommended to decrease the battery termination threshold (I_{TERM}) to minimize ΔV_{BATT} as much as possible.

Figure 16 is tested under different battery specifications with varying battery internal resistances (R_{BATT} = 50mΩ, 100mΩ, or 150mΩ). For higher battery internal resistance conditions, setting the charge termination lower is recommended.

In summary, to significantly reduce the impact of heavy system loads and high battery resistance on charge termination, it is recommended to set the charge termination current below 50mA.



(a)



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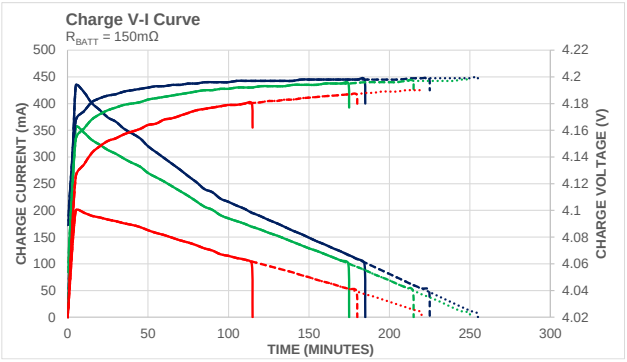

(c)

Figure 16: Charge V-I Curve under Different Specifications

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Selecting the Inductor

Inductor selection is a tradeoff between cost, size, and efficiency. A lower-value inductor corresponds to a smaller size, but also results in a higher current ripple, higher magnetic hysteretic losses, and higher output capacitances. A higher-value inductor results in lower ripple current and smaller output filter capacitors, but also results in higher inductor DC resistance (DCR) loss.

The required inductance (L) can be estimated with Equation (2):

$$L = \frac{V_{IN} - V_{SYS}}{\Delta I_{L_MAX}} \times \frac{V_{SYS}}{V_{IN} \times f_{SW}} \quad (2)$$

Where V_{IN} is the input voltage, V_{SYS} is the converter output voltage, f_{SW} is the switching frequency, and ΔI_{L_MAX} is the maximum peak-to-peak inductor current, which is typically designed to be between 20% and 40% of the maximum load current.

Choose an inductor that does not saturate under the worst-case load condition. The inductor's saturation current (I_{SAT}) can be calculated with Equation (3):

$$I_{SAT} > I_{LOAD} + \frac{\Delta I_{L_MAX}}{2} \quad (3)$$

Where I_{LOAD} is the buck converter's maximum load.

Selecting the PMID Capacitor

The PMID capacitor (C_{PMID}) decouples the switching buck converter and absorbs the switching ripple current. Select C_{PMID} based on the demand for the PMID current ripple. The input current ripple (I_{RMS_MAX}) can be calculated with Equation (4):

$$I_{RMS_MAX} = I_{LOAD} \times \frac{\sqrt{V_{SYS} \times (V_{IN} - V_{SYS})}}{V_{IN}} \quad (4)$$

Use low-ESR ceramic capacitors with an X7R or X5R rating for C_{PMID}. This capacitor should be placed as close to the PMID and PGND pins as possible. The capacitor's voltage rating must exceed V_{IN}, and it is recommended to consider the plug-in overshoot voltage. A capacitor rated for a minimum of 10V is recommended for applications with a 5V V_{IN}. Generally, a starting capacitance of 10µF is considered sufficient.

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PCB Layout Guidelines

Efficient PCB layout is critical for stable operation and to meet the specified noise, efficiency, and stability requirements. For the best results, refer to Figure 18 and follow the guidelines below:

1. Place the PMID capacitor (C_{PMID}) as close to the PMID and PGND pins as possible using a short copper plane connection. Place C_{PMID} on the same layer as the IC.
2. Minimize the high-frequency current path loop (from the PMID pin to the capacitor to ground; see Figure 17) between C_{PMID} and the buck converter's power MOSFETs.
3. Place the inductor's input terminal as close to the SW pin as possible.
4. Minimize the copper area of the inductor's input terminal trace to reduce electrical and magnetic field radiation. Ensure that the trace is wide enough to carry the charge current.
5. Minimize parasitic capacitance from the inductor input terminal to any other trace or plane.
6. Place decoupling capacitors (e.g. the VCC pin capacitor) as close to the IC pins as possible, and ensure the connection is as short as possible.
7. Connect the IC's power pins to as many copper planes as possible to conduct heat away from the IC.
8. Ensure that the number and physical size of the vias are sufficient for a current path.

Figure 17 shows a high-frequency current path, which includes the high-side MOSFET, low-side MOSFET, and C_{PMID}. The high-frequency path must be minimized.

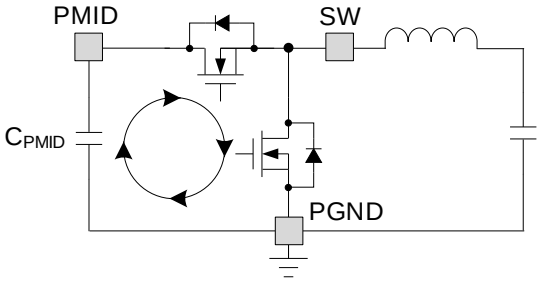

Figure 17: High-Frequency Current Path

Figure 18 shows the recommended PCB layout.

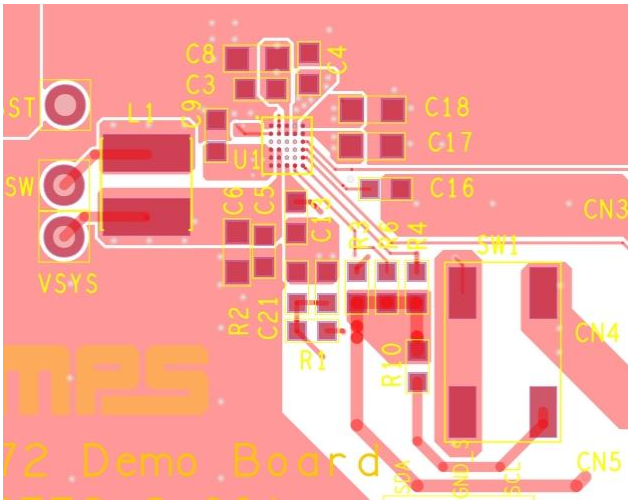

Figure 18: Recommend PCB Layout

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TYPICAL APPLICATION CIRCUIT

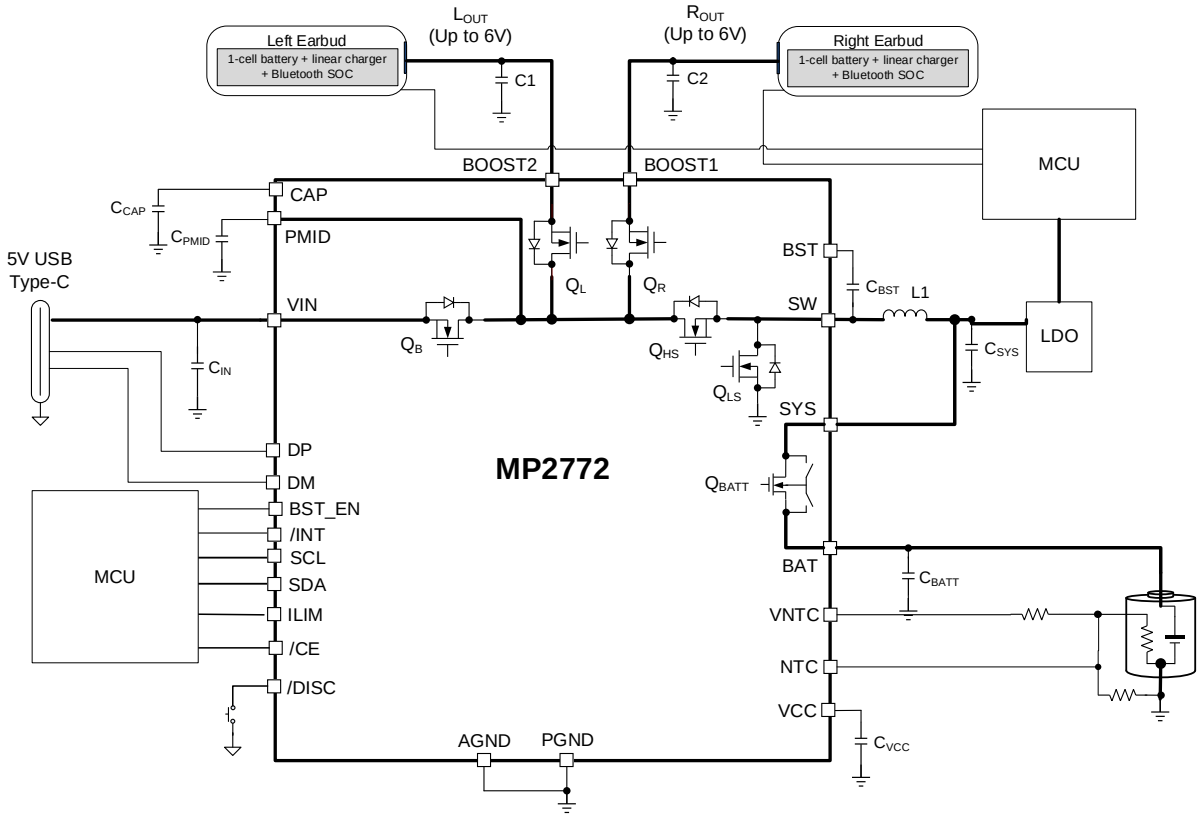

Figure 17: Typical Application Circuit

Table 2: BOM for Typical Application Circuit

Qty	Ref	Value	Description	Package	Manufacturer
1	C_{IN}	1µF	Ceramic capacitor, 10V, X5R or X7R	0603	Any
2	C_{PMID}	10µF	Ceramic capacitor, 10V, X5R or X7R	0805	Any
1	C_{SYS}	22µF	Ceramic capacitor, 10V, X5R or X7R	0805	Any
1	C_{BATT}	22µF	Ceramic capacitor, 10V, X5R or X7R	0805	Any
1	C_{VCC}	1µF	Ceramic capacitor, 10V, X5R or X7R	0603	Any
1	C_{BST}	47nF	Ceramic capacitor, 16V, X5R or X7R	0603	Any
1	C_{CAP}	100nF	Ceramic capacitor, 16V, X5R or X7R	0603	Any
2	C1, C2	2.2µF	Ceramic capacitor, 10V, X5R or X7R	0603	Any
1	L1	1.5µH	Inductor, 1µH, low DCR	SMD	Any

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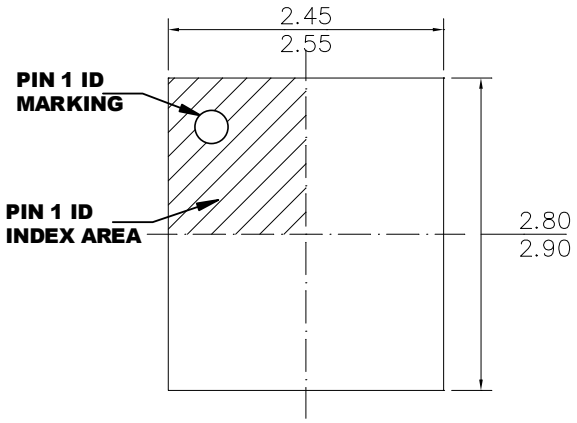
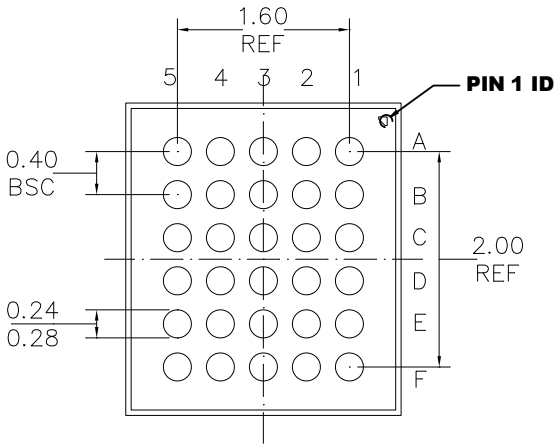
PACKAGE INFORMATION

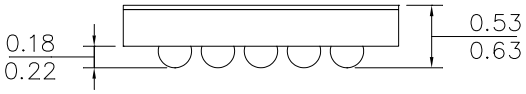
WLCSP-30 (2.5mmx2.85mm)



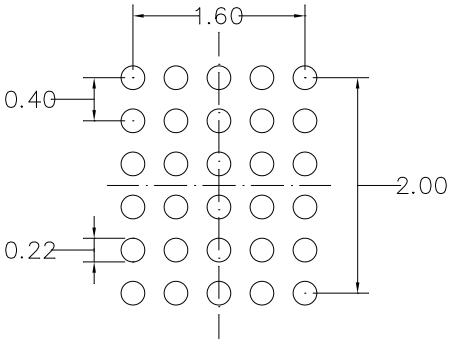
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) BALL COPLANARITY SHALL BE 0.05 MILLIMETER MAX.
3) JEDEC REFERENCE IS MO-211.
4) DRAWING IS NOT TO SCALE.

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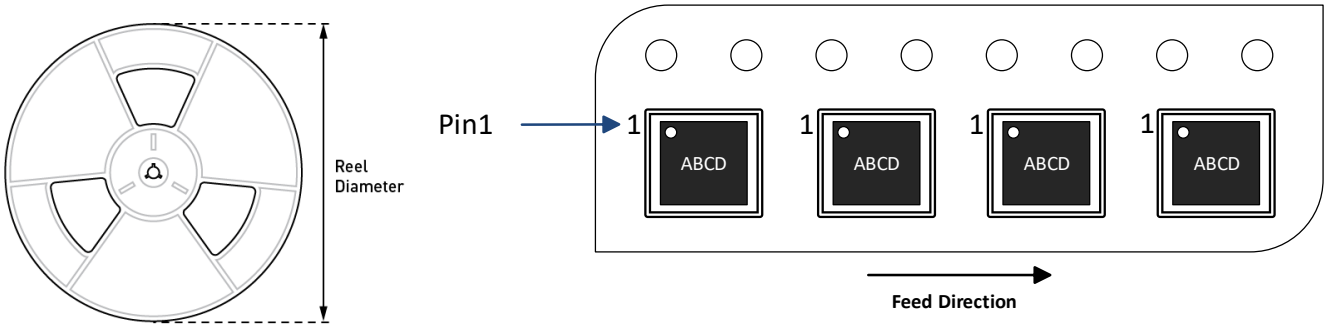
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2772GC-xxxx-Z	WLCSP-30 (2.5mmx 2.85mm)	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	11/11/2024	Initial Release	-

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