MP2764

I²C/SMBus-Controlled, Integrated Buck-Boost NVDC Charger with System Power Monitor and Processor Hot Monitor for Multi-Cell Battery Packs

DESCRIPTION

The MP2764 is a highly integrated buck-boost charger IC with narrow-voltage DC (NVDC) power path management control and USB power delivery (PD) source mode for 2-cell to 4-cell battery pack applications. All switching FETs are integrated for a compact system solution size and easy to use. The external battery MOSFET (BATFET) is flexible for IC placement and discharge current capability design.

The IC can accept a wide range of input voltages (V_{IN}, up to 22V) for charging, and it has three operating modes during the charging process: boost mode when V_{IN} is below the system voltage (V_{SYS}), buck-boost mode when V_{IN} is close to V_{SYS}, and buck mode when V_{IN} exceeds V_{SYS}. In buck mode, the MP2764 can operate in dual-phase interleaving mode to facilitate inductor selection because a lower inductor saturation current typically corresponds to a smaller inductor profile.

When the input power is present, the IC measures the battery voltage (V_{BATT}) automatically and charges the battery with four phases: constant current trickle charge, constant current pre-charge, constant current fast charge, and constant voltage charge. Other features include charge termination and automatic recharge.

The MP2764 provides a BGATE driver output to control the external N-channel MOSFET and achieve NVDC power path management. When V_{BATT} is low and the input is present, the MP2764 can regulate V_{SYS} at a minimum level to ensure that the system can start up. Meanwhile, the battery is charged through the BATFET, which is linearly regulated.

When the input source current or voltage limit is reached, power path management automatically reduces the charge current to meet the priority of the system power requirement. If the system current continues to increase (even when the charge current is reduced to zero), supplement mode allows the battery and input power supply to simultaneously power the system.

When the input is absent, the system is powered by the battery through the BATFET. The IC can also provide a wide output voltage (V_{IN_OUT}) from 4V to 21V, with 20mV/step at the input in USB PD source mode. The MP2764 also provides output current limit regulation in USB PD source mode.

With the I²C/SMBus interface, the MP2764 can be flexibly configured to set the charging parameters, such as the input current (I_{IN}) limit, V_{IN} limit, charge current, battery-full voltage, minimum V_{SYS}, and the output voltage and current in USB PD source mode. The IC can also provide the operation status through the status and fault registers with an interrupt. The interrupt can also be masked by configuring the corresponding register.

To guarantee safe operation, the IC limits the die temperature to a preset value (120°C). Other safety features include input over-voltage protection (OVP), battery OVP, system OVP, thermal shutdown, battery temperature protection, and a configurable timer to prevent prolonged charging of a dead battery.

To comply with IMVP9 specifications, the IC provides an analog output pin for the system power (PSYS), input current (IAM), and battery current (IBM). The MP2764 also has a processor hot indication pin (/PROCHOT) for system power control.

The MP2764 also integrates a Vmin Active Protection (VAP) function, which can supplement the system power from the input capacitor when the system is only powered by the battery.

The MP2764 is available in a QFN-32 (4mmx5mm) package.

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FEATURES

- All FETs Integration Buck-Boost Converter
- Seamless Mode Transition Between Buck/Boost and Buck-Boost Mode
- Configurable 500kHz to 1MHz Switching Frequency (f_{SW})
- Charge 2 to 4 Cells in Series Battery Pack:
  - Up to 28V Input Sustainable Voltage
  - 4V to 22V Operation Voltage with Input Over-Voltage Protection (OVP)
  - Input Power Source Status Indication
  - Up to 8A Configurable Charge Current
  - Configurable Battery-Full Regulation Voltage up to 4.8V/Cell with 0.5% Accuracy Across 0°C to 85°C Temperature Range
  - Configurable Input Maximum Current Limit and Input Minimum Voltage Limit
  - Thermal Regulation
- Narrow-Voltage DC (NVDC) Power Path Management via External N-Channel Battery MOSFET (BATFET)
- Configurable Minimum and Maximum System Voltage Regulation
- System OVP and System Short-Circuit Protection (SCP)
- On-the-Go (OTG) Pin Control to Enable the USB Power Delivery (PD) Source Mode:
  - 4V to 21V Output Voltage (V_{IN_OUT}) with 20mV/Step to be Compliant to USB PD Programmable Power Supply (PPS)
  - Configurable Output Current Limit with 50mV/Step in USB PD Source Mode
  - Output OVP and SCP in Source Mode
- Dual-Phase Interleaving Operation for Buck Charging Mode with Current Balancing
- IMVP9-Compliant Features for Intel CPU:
  - V_{MIN} Active Protection (VAP) Supplements the Battery from Input Capacitors during the System Peak Power Spike
  - Comprehensive $\overline{\text{PROCHOT}}$ Profile
  - Fast System Power Indication with PSYS Pin
  - Input Current and Battery Discharge Current Sensing with the IAM/IBM Pin
  - Two-Level Input Current Limit
- Ultrasonic Mode (USM) to Avoid Audible Noise
- Integrated 10-Bit Analog-to-Digital Converter (ADC) to Monitor the Voltage, Current, and Power
- Safety:
  - Thermal Shutdown
  - Battery Missing Detection
  - Battery Removal Detection
  - Battery Temperature Protection Compliant to JEITA Standard
  - Configurable Charge Safety Timer
- Available in a QFN-32 (4mmx5mm) Package

APPLICATIONS

- Tablets
- Ultrabooks
- 2-in-1 Notebooks

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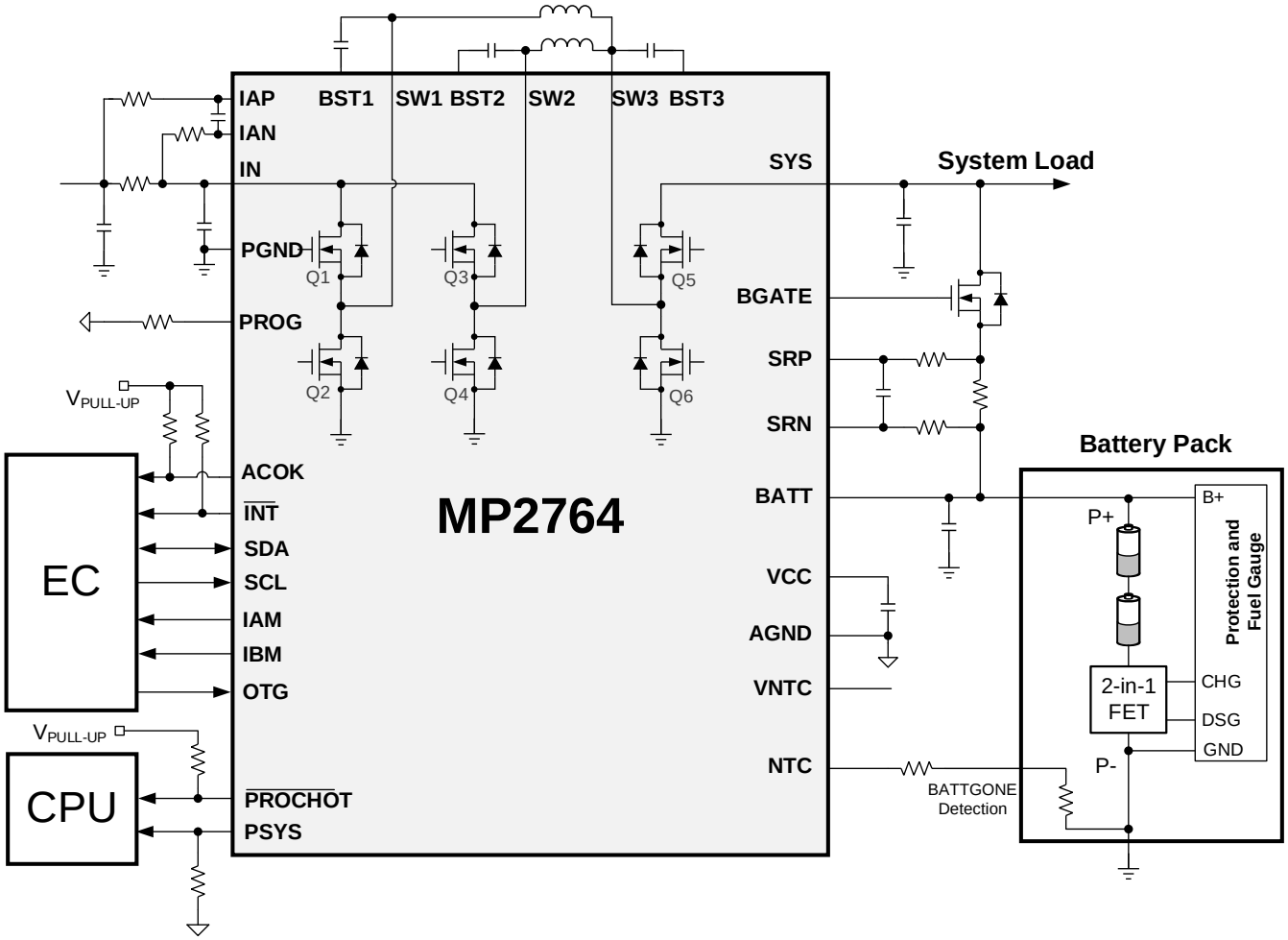
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP2764GV-xxxx**	QFN-32(4mmx5mm)	*See Below*	1
MP2764GV-0000***			
MP2764GV-0001****			

* For Tape & Reel, add suffix -Z (e.g.MP2764GV-xxxx-Z).

** “xxxx” is the register setting option. Contact an MPS FAE to obtain an “xxxx” value.

*** “0000” is the factory default for two-phase, interleaved applications.

**** “0001” is the factory default for two-phase, paralleled, single-inductor applications.

TOP MARKING

MPSYWW
MP2764
LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
MP2764: Part number
LLLLLL: Lot number

EVALUATION KIT EVKT-MP2764

EVKT-MP2764 kit contents (items below can be ordered separately):

#	Part Number	Item	Quantity
1	EV2764-V-00A or EV2764-V-00B	MP2764-0000 or MP2764-0001 evaluation board	1
2	EVKT-USBI2C-02 bag	Includes one USB-to-I²C communication interface, one USB cable, and one ribbon cable	1
3	Online resources	Include GUI and supplemental documents	1

Order direct from MonolithicPower.com or our distributors.

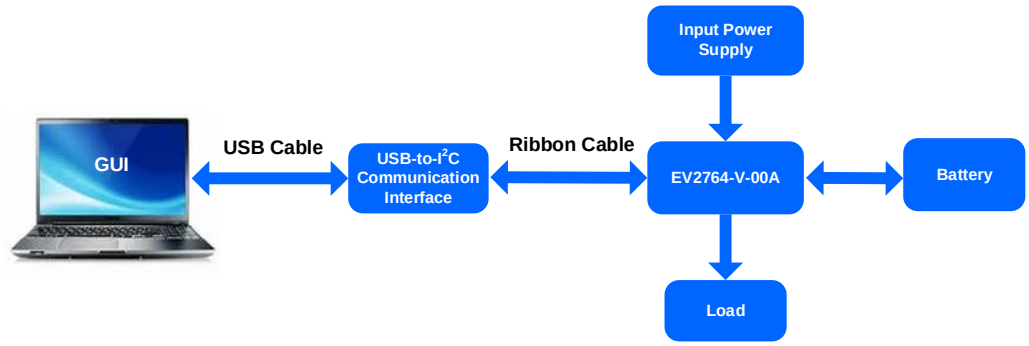

Figure 1: EVKT-MP2764 Evaluation Kit Set-Up

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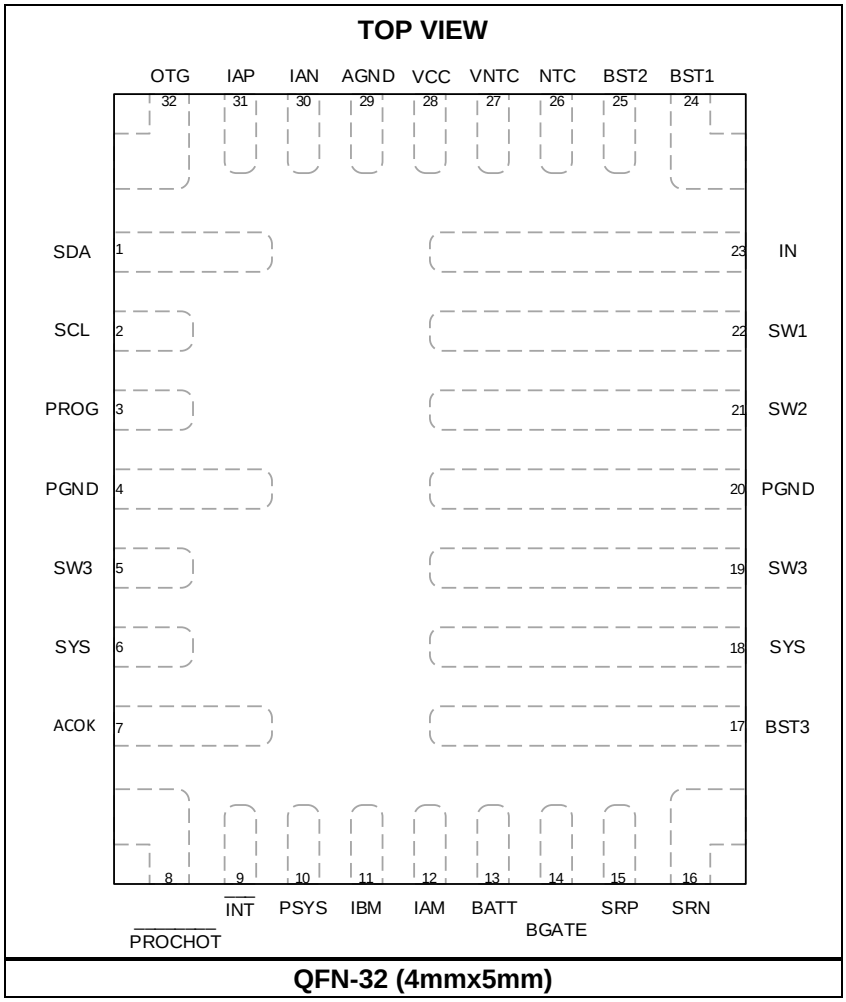
PACKAGE REFERENCE



QFN-32 (4mmx5mm)

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PIN FUNCTIONS

Pin #	Name	Description
23	IN	**Power input of the IC from the adapter or USB.** It is recommended to connect at least 5 x 22μF capacitors in front of the input sense resistor and connect 1 x 0.1μF ceramic capacitors to IN, and as close as possible to the IC.
27	VNTC	**Pull-up voltage for NTC block.** The VNTC pin is used as the voltage bias for the negative temperature coefficient (NTC) comparator resistor divider for both the feedback and the reference. If the NTC pin is configured for the BATDET function, then leave the VNTC pin floating.
26	NTC/BATDET	**Battery temperature-sense input or BATDET.** Connect an NTC thermistor to ground plane for battery temperature sensing. Configure the JEITA temperature windows with a resistor divider connected from VNTC to NTC to ground plane. For the BATDET function, this pin is configured as a current source. When the battery ID is connected to ground plane with a resistor (e.g. 10kΩ), the resistor pulls down this pin to indicate that a battery is present; otherwise, this pin is floating, and it is pulled to high (exceeding 1.6V) by the current source to indicate that the battery is absent.
4, 20	PGND	**Power ground.**
32	OTG/VAP	**USB On-the-Go (OTG) and Vmin Active Protection (VAP) enable control**. When REG13h, bit[5] = 1, the high level is used to enable OTG mode; when REG13h, bit[5] = 0, the high level is used to enable VAP.
6, 18	SYS	**System output.** It is recommended to connect 5 x 22μF and 1 x 0.1μF ceramic capacitors from SYS to PGND and placed as close as possible to the IC.
13	BATT	**Battery positive terminal for battery voltage sense**. It is recommended to connect 2 x 22μF ceramic capacitors from BATT to PGND and placed as close as possible to the IC.
8	$\overline{\text{PROCHOT}}$	**Processor hot indicator terminal**. This pin is an open-drain structure. It is pulled to AGND when the $\overline{\text{PROCHOT}}$ signal asserts, and it floats when no $\overline{\text{PROCHOT}}$ events occur. This pin must be pulled up externally. This pin can be left floating if it is not used.
9	$\overline{\text{INT}}$	**Open-drain interrupt output.** The $\overline{\text{INT}}$ pin can send charging status and fault interrupts to the host. It must be pulled up externally. This pin can be left floating if it is not used.
1	SDA	**I²C interface data.** Connect SDA to the logic rail through a 10kΩ resistor.
2	SCL	**I²C interface clock**. Connect SCL to the logic rail through a 10kΩ resistor.
3	PROG	**Battery cell or target address setting.** This pin can be configured to set different target addresses or battery cell numbers with different resistor values connected to ground plane. The function is configured by the one-time programmable (OTP) memory, and the default is the battery cell setting.
10	PSYS	**System power indication pin**. The PSYS pin outputs a current source that is proportional to the total system power. The gain is configurable via REG1A, bits[4:3]. Place a resistor from this pin to ground plane to generate the output voltage. This pin can be left floating if it is not used.
11	IBM	**Battery current-sense output pin.** Place a maximum 100pF ceramic decoupling capacitor from this pin to ground plane. This pin can be left floating if it is not used.
12	IAM	**Input current-sense output pin.** Place a maximum 100pF ceramic decoupling capacitor from this pin to ground plane. This pin can be left floating if it is not used.
24	BST1	**Bootstrap pin**. It is recommended to connect a 470nF bootstrap capacitor between the BSTx and SWx pins to form a floating supply across the power switch driver.
25	BST2	
17	BST3	
22	SW1	**Buck phase switching node.**
21	SW2	
5, 19	SW3	**Boost phase switching node**. Pin 19 must be connected to the inductor, while pin 5 is not necessary.

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PIN FUNCTIONS *(continued)*

Pin #	Name	Description
28	VCC	**VCC LDO output.** The VCC pin is used for internal power. Connect a 10μF ceramic capacitor from VCC to AGND, and place it as close as possible to the IC.
29	AGND	**Analog ground.**
7	ACOK	**Input power indicator terminal**. The ACOK pin is an open-drain pin, and it is active open. This pin can be left floating if it is not used.
31	IAP	**Input current-sense positive terminal.**
30	IAN	**Input current-sense negative terminal.**
15	SRP	**Sense resistor positive terminal.** The SRP pin is the battery current-sense amplifier's positive input terminal.
16	SRN	**Sense resistor negative terminal.** The SRN pin is the battery current-sense amplifier's negative input terminal.
14	BGATE	**Battery FET gate driver.** The BGATE pin is the driver output to drive the external N-channel MOSFET between the system and the battery.

ABSOLUTE MAXIMUM RATINGS (1)

IN, IAN, IAP to PGND .....-0.3V to +28V
BATT, SYS to PGND .....-0.3V to +28V
SRP, SRN to PGND .....-0.3V to +28V
SW1/SW2 to PGND .....-0.3V to +26V
SW1/SW2 to PGND (20ns).....-2V to +28V
SW1/SW2 to PGND (10ns).....-5V to +28.5V
SW3 to PGND.....-0.3V to +26V
SW3 to PGND (20ns).....-2V to +28V
SW3 to PGND (10ns).....-5V to +28.5V
BGATE to PGND ..... 0 to 28V
BST1 to PGND .....SW1 to SW1 + 4V
BST2 to PGND .....SW2 to SW2 + 4V
BST3 to PGND .....SW3 to SW3 + 4V
SRP to SRN.....-1V to +1V
IAP to IAN .....-1V to +1V
VCC to AGND.....-0.3V to +4V
All other pins to AGND.....-0.3V to +0.3V + V_{CC}
Continuous power dissipation (T_A = 25°C) (2)
..... 3.29W
Junction temperature (T_J) .....150°C
Lead temperature (solder) .....260°C
Storage temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM) 2kV
Charged-device model (CDM) 500V

Recommended Operating Conditions (3)

V_{IN} .....4V to 22V
I_{IN}.....Up to 5A
I_{SYS} .....Up to 8A
I_{CHG}.....Up to 8A
V_{BATT}.....Up to 19.2V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-32 (4mmx5mm)..... 31.3 ..... 1.3 ... °C/W

Notes:

1) The absolute maximum ratings are related under room temperature, unless otherwise noted. Exceeding these ratings may damage the device. The SW1, SW2, and SW3 voltage ratings within 10ns of SW1, SW2, and SW3 are measured on the EVB.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on a JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

R_{S_IN} = 10mΩ, R_{S_BAT} = 10mΩ, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Voltage (V_{IN}) Range						
Input under-voltage lockout (UVLO) threshold	V_{IN_UVLO}	V_{IN} falling	3.3	3.65	4	V
		V_{IN} rising	3.6	3.98	4.36	V
Input UVLO hysteresis		V_{IN} rising		0.33		V
Input UVLO deglitch time		V_{IN} rising		30		ms
Input over-voltage lockout (OVLO) threshold	V_{IN_OVLO}	V_{IN} rising	24	24.6	25.1	V
		V_{IN} falling	23.3	23.8	24.3	
Input OVLO hysteresis		V_{IN} falling		0.77		V
Input OVLO response time		V_{IN} rising, REG12h, bit[0] = 1		1		µs
Input OVLO recovery deglitch time		V_{IN} falling		30		ms
DC/DC Characteristics						
Input shutdown current (-40°C to +125°C)	I_{SHDN}	V_{IN} = 5V/20V, DC/DC converter is disabled, BGATE driver is disabled			0.1	mA
Input quiescent current (-40°C to +125°C)	I_Q	V_{IN} = 5V, DC/DC converter is enabled, charge disabled, I_{SYS} = 0A			12	mA
		V_{IN} = 20V, DC/DC converter is enabled, charge disabled, I_{SYS} = 0A			15	mA
VCC low-dropout (LDO) regulator output voltage	V_{CC}	V_{IN} = 5V, V_{BATT} = 0V, I_{VCC} = 10mA	3.3	3.5	3.7	V
		V_{IN} = 0V, V_{BATT} = 5V, I_{VCC} = 10mA	3.3	3.5	3.7	V
VCC LDO output current limit	I_{VCC}	V_{IN} = 9V, V_{BATT} = 0V, V_{CC} = 3.3V	75	85	95	mA
IN to SW1 N-channel MOSFET (Q1) on resistance	R_{ON_Q1}			16		mΩ
SW1 to PGND N-channel MOSFET (Q2) on resistance	R_{ON_Q2}			10		mΩ
IN to SW2 N-channel MOSFET (Q3) on resistance	R_{ON_Q3}			16		mΩ
SW2 to PGND N-channel MOSFET (Q4) on resistance	R_{ON_Q4}			10		mΩ
SW3 to SYS N-channel MOSFET (Q5) on resistance	R_{ON_Q5}			5		mΩ
SW3 to PGND N-channel MOSFET (Q6) on resistance	R_{ON_Q6}			20		mΩ
Operation frequency	f_{SW}	REG17h, bits[6:4] = 011	440	540	660	kHz
		REG17h, bits[6:4] = 101	680	860	1100	kHz
Battery track regulation voltage	V_{TRACK}	2-cell, charge terminated, V_{SYS} - V_{BATT}, REG09h, bits[8:6] = 100		200		mV
		3cell, charge terminated, V_{SYS} - V_{BATT}, REG09h, bits[8:6] = 100		300		mV

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ELECTRICAL CHARACTERISTICS *(continued)*

R_{S_IN} = 10mΩ, R_{S_BAT} = 10mΩ, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Minimum system regulation voltage	$V_{SYS_REG_MIN}$	2 cells, REG17h, bits[1:0] = 00, REG09h = 0x00E0h, V_{SYS_MIN} = 3.2V/cell, V_{TRACK} = 75mV/cell		6.55		V
		3 cells, REG17h, bits[1:0] = 01, REG09h = 0x00A0h, V_{SYS_MIN} = 3.2V/cell, V_{TRACK} = 50mV/cell		9.8		V
		4 cells, REG17h, bits[1:0] = 10, REG09h = 0x00A0h, V_{SYS_MIN} = 3.2V/cell, V_{TRACK} = 50mV/cell		13		V
Minimum system regulation voltage accuracy			-2%		+2%	
Minimum system regulation voltage accuracy (-40°C to +85°C)			-2.5%		+2.5%	
Current foldback voltage threshold		2-cell, lower by $V_{SYS_REG_MIN}$	100	200	300	mV
System over-voltage protection (OVP) threshold	V_{SYS_OVP}	As a percentage of V_{SYS_REG}, REG12h, bit[2] = 0	107.5%	110%	112%	
		As a percentage of V_{SYS_REG}, REG12h, bit[2] = 1	103.5%	106%	108%	
System OVP hysteresis		As a percentage of V_{SYS_REG}, REG12h, bit[2] = 0		4%		
		As a percentage of V_{SYS_REG}, REG12h, bit[2] = 1		2%		
System OVP response time				1		µs
System short-circuit protection (SCP) threshold		V_{SYS} falling	1.5	2	2.5	V
System SCP hysteresis		V_{SYS} rising		0.56		V
System SCP deglitch time				10		ms
System SCP hiccup recovery time				375		ms
Charging Characteristics						
Trickle charge current range			62.5		937.5	mA
Trickle charge current accuracy (0°C to 85°C)	I_{TC}	V_{BATT} = 1V, I_{TC} = 250mA	100	250	400	mA
		V_{BATT} = 3.8V, I_{TC} = 250mA	200	250	300	mA
Trickle charge to pre-charge threshold	V_{BATT_TC}	V_{BATT} rising	1.9	2	2.1	V/cell
Trickle charge to pre-charge hysteresis		V_{BATT} falling		200		mV/cell
Trickle charge/ pre-charge transition deglitch time				30		ms

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ELECTRICAL CHARACTERISTICS *(continued)*

R_{S_IN} = 10mΩ, R_{S_BAT} = 10mΩ, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Pre-charge current range			125		1875	mA
Pre-charge current accuracy (0°C to 85°C)	I_{PRE}	250mA	-20%		+20%	
		500mA	-20%		+20%	
		1.5A	-10%		+10%	
Pre-charge to constant current (CC) fast charge threshold	V_{BATT_PRE}	REG0Eh, bits[4:2] = 000	2.1	2.2	2.3	V/cell
		REG0Eh, bits[4:2] = 010	2.4	2.5	2.6	V/cell
		REG0Eh, bits[4:2] = 101	2.9	3.0	3.1	V/cell
		REG0Eh, bits[4:2] = 111	3.3	3.4	3.5	V/cell
Pre-charge to linear CC fast charge hysteresis				100		mV/cell
Pre-charge/CC fast charge hysteresis				30		ms
Linear CC fast charge range			125		3875	mA
Linear CC fast charge accuracy (0°C to 85°C)	I_{CC_LNR}	250mA	-20%		+20%	
		500mA	-15%		+15%	
		1A	-5%		+7%	
		3A	-4%		+5.5%	
Linear CC to switching CC threshold		V_{SYS_MIN} = 6.4V, V_{TRACK} = 0.15V, 2 cells		6.55		V
Linear CC to switching CC hysteresis				100		mV/cell
Switching CC charge current accuracy (0°C to 85°C)	I_{CC_SW}	I_{CC_SW} = 500mA	-20%		+20%	
		I_{CC_SW} = 1A	-10%		+10%	
		I_{CC_SW} = 2A	-5%		+5%	
		I_{CC_SW} = 3A	-3%		+3%	
		I_{CC_SW} ≥ 4A	-2%		+2.5%	
Battery-full voltage regulation (0°C to 85°C)	V_{BATT_REG}	V_{BATT_REG} = 8.4V, OTP default REG17h, bits[1:0] = 00	-0.5%		+0.5%	
		V_{BATT_REG} = 12.6V, OTP default REG17h, bits[1:0] = 01	-0.5%		+0.5%	
		V_{BATT_REG} = 16.8V, OTP default REG17h, bits[1:0] = 10	-0.5%		+0.5%	
Termination current range			31		468	mA
Termination current accuracy (0°C to 85°C)	I_{TERM}	125mA	80	130	190	mA
		250mA	190	255	315	mA
		468mA	410	475	550	mA
Termination deglitch time				1		sec
Auto-recharge threshold	V_{RECH}	100mV	25	100	175	mV/cell
		200mV	130	200	270	mV/cell
Recharge deglitch time				30		ms
Battery OVP rising threshold		Exceeding V_{BATT_REG}	100	160	220	mV/cell
Battery OVP hysteresis				80		mV/cell

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ELECTRICAL CHARACTERISTICS *(continued)*

R_{S_IN} = 10mΩ, R_{S_BAT} = 10mΩ, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Battery OVP deglitch time				1.5		ms
Input current limit range			100		6350	mA
Input current limit accuracy (-40°C to +85°C)	I_{IN_LIM1}	I_{IN_LIM1} = 100mA	30	65	100	mA
		I_{IN_LIM1} = 500mA	400	450	500	mA
		I_{IN_LIM1} = 1A	880	940	1000	mA
		I_{IN_LIM1} = 2A	1800	1900	2000	mA
		I_{IN_LIM1} = 3A	2700	2895	3000	mA
		I_{IN_LIM1} = 4A	3750	3900	4000	mA
		I_{IN_LIM1} = 5A	4750	4900	5000	mA
Input voltage limit accuracy (-40°C to +85°C)	V_{IN_MIN}	V_{IN_MIN} = 4.5V	-2%		+2%	
		V_{IN_MIN} = 8.5V	-2%		+2%	
		V_{IN_MIN} = 11.5V	-2%		+2%	
		V_{IN_MIN} = 14.5V	-2%		+2%	
		V_{IN_MIN} = 18.5V	-2%		+2%	
NTC Protection						
VNTC voltage		I_{VNTC} = 0.3mA		1.6		V
VNTC voltage accuracy (0°C to 85°C)			-0.5%		+0.5%	
NTC hot temp falling voltage threshold (0°C to 85°C)	V_{HOT}	NTC pin voltage falling as a percentage of V_{NTC}, REG10h, bits[7:6] = 10	32.4	33.35	34.2	%
NTC hot temp threshold hysteresis		NTC pin voltage rising		1	1.5	%
NTC warm temp falling voltage threshold (0°C to 85°C)	V_{WARM}	NTC pin voltage falling as a percentage of V_{NTC}, REG10h, bits[5:4] = 01	39.8	40.8	41.8	%
NTC warm temp threshold hysteresis (0°C to 85°C)		NTC pin voltage rising		1	1.5	%
NTC cool temp rising voltage threshold (0°C to 85°C)	V_{COOL}	NTC pin voltage rising as a percentage of V_{NTC}, REG10h, bits[3:2] = 10	66.3	67.12	67.9	%
NTC cool temp threshold hysteresis		NTC pin voltage falling		1	1.5	%
NTC cold temp rising voltage threshold (0°C to 85°C)	V_{COLD}	NTC pin voltage rising as a percentage of V_{NTC}, REG10h, bits[1:0] = 01	74.6	75.43	76.2	%
NTC cold temp threshold hysteresis		NTC pin voltage falling		1	1.5	%
NTC floating threshold (0°C to 85°C)	V_{FLT}	NTC pin voltage rising	93.5	95	96.5	%
NTC floating threshold hysteresis (0°C to 85°C)			1.6	3	3.8	%

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ELECTRICAL CHARACTERISTICS *(continued)*

R_{S_IN} = 10mΩ, R_{S_BAT} = 10mΩ, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Accuracy of voltage decrease when warm/cool protection (0°C to 85°C)		REG0Fh, bits[3:2] = 01	142	150	158	mV/cell
Accuracy of current reduction when warm/cool protection		I_{CC} reduction = 50%, I_{CC} = 2A	45	50	58	%
Timer and Thermal Protection						
Linear charge timer (TC and pre-charge)	t_{TC_PRE}		1.8	2	2.2	hours
CC/CV charge timer	t_{CC_CV}		18	20	22	hours
Watchdog timer	t_{WDT}		144	160	176	sec
Thermal shutdown threshold				150		°C
Thermal shutdown hysteresis				20		°C
Thermal regulation threshold	T_J	REG0Dh, bits[1:0] = 11	110	120	130	°C
		REG0Dh, bits[1:0] = 10	90	100	110	°C
		REG0Dh, bits[1:0] = 01	70	80	90	°C
		REG0Dh, bits[1:0] = 00	50	60	70	°C
Source Output Characteristic						
Source output voltage accuracy (0°C to 85°C)	V_{IN_SRC}	V_{IN_SRC} = 5V,no load	-3%		5%	
		V_{IN_SRC} = 9V, no load	-3%		+4%	
		V_{IN_SRC} = 12V, no load	-2%		+4%	
		V_{IN_SRC} = 15V, no load	-2%		+3%	
		V_{IN_SRC} = 20V, no load	-2%		+2.5%	
Source output current range			500		5000	mA
Source output current limit accuracy (0°C to 85°C)	I_{IN_SRC}	I_{IN_SRC} = 0.5A	0%		+20%	
		I_{IN_SRC} = 1A	0%		+10%	
		I_{IN_SRC} = 1.5A	0%		+8%	
		I_{IN_SRC} = 3A	0%		+5%	
		I_{IN_SRC} = 5A	0%		+4%	
Source output OVP threshold		REG12h, bit[1] = 0	105.5%	110%	114.5%	
		REG12h, bit[1] = 1	103%	106%	110%	
Source output OVP hysteresis		REG12h, bit[1] = 0		4%		
		REG12h, bit[1] = 1		2%		
Source OVP response time				1		µs
Source SCP threshold			1.7	2	2.3	V
Source SCP deglitch time				0.5		ms
Source SCP hiccup recovery time				375		ms
Battery discharge current limit in source mode	$I_{BATT_DSCHG_LIM}$	3A	-5%		+5%	
		5A	-3%		+3%	
Battery UVLO threshold		V_{BATT} falling, OTG enabled	2.5	2.6	2.7	V/cell
Battery UVLO hysteresis				280		mV/cell

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ELECTRICAL CHARACTERISTICS *(continued)*

R_{S_IN} = 10mΩ, R_{S_BAT} = 10mΩ, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Battery UVLO deglitch time				0.7		ms
Battery low voltage threshold		Falling	2.7	2.8	2.9	V/cell
Battery low voltage hysteresis				250		mV/cell
Battery low voltage deglitch time				30		ms
Battery Quiescent Current						
Battery quiescent current	I_{BATT_Q}	BGATE is off, ADC, PROCHOT, PSYS, WDT are all off		25	35	µA
		BGATE is on, ADC, PROCHOT, PSYS, WDT are all off		60	75	µA
		BGATE and WDT are on. ADC, PROCHOT, PSYS are all off		500	600	µA
		BGATE, ADC, WDT timer, PROCHOT, PSYS are all on		1	1.5	mA
BGATE driver voltage	V_{BGATE}	Higher than V_{BATT} when enabled.	6	7	8.7	V
Analog-to-Digital Converter (ADC) Accuracy						
ADC sample rate				50		kHz
ADC resolution				10		bits
ADC accuracy		V_{BATT} = 6V	-30	4	+34	LSB
		V_{BATT} = 12V	-32	6	+38	LSB
		V_{IN} = 5V	-8	3	+10	LSB
		V_{IN} = 20V	-8	4	+14	LSB
		I_{IN} = 0.1A	-10	1	+10	LSB
		I_{IN} = 1A	-10	1	+10	LSB
		I_{IN} = 3A	-11	0	+9	LSB
		I_{CHG} = 0.1A	-11	-2	+5	LSB
		I_{CHG} = 1A	-11	-1	+6	LSB
		I_{CHG} = 3A	-11	2	+10	LSB
		V_{SYS} = 6V	-9	1	+11	LSB
		V_{SYS} = 12V	-9	1	+12	LSB
Logic Input Pins (SCL, SDA, OTG)						
Input low voltage threshold					0.4	V
Input high voltage threshold			1.3			V
Logic Output Open-Drain Pins (ACOK, $\overline{INT}$, $\overline{PROCHOT}$, SDA)						
Output saturation voltage		5mA drain current			0.4	V
Pin leakage current		V = 3.6V	-200		+200	nA
IAP, IAN leakage current			-200		+200	nA
ISP, ISN leakage current			-200		+200	nA

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ELECTRICAL CHARACTERISTICS *(continued)*

R_{S_IN} = 10mΩ, R_{S_BAT} = 10mΩ, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
IMVP Specifications						
Second input current limit	I_{IN_LIM2}	6A	5.76	5.87	6	A
Input over-current protection (OCP) threshold	I_{IN_OC}		18	20	22	A
Input OCP deglitch time				0.5		ms
Input OCP hiccup recovery time				375		ms
PROCHOT Characteristics						
First input OC threshold to trigger PROCHOT	I_{IN_PHOT1}	As a percentage of I_{IN_LIM1}, average current	105%	110%	115%	
I_{IN_PHOT1} deglitch time		REG1Ah, bit[10] = 1		50		ms
Second input OC threshold to trigger PROCHOT	I_{IN_PHOT2}	As a percentage of I_{IN_LIM2}, peak current, REG1Ah, bit[12] = 0	105%	110%	115%	
I_{IN_PHOT2} deglitch time		REG19h, bits[9:8] = 00	10	15	20	µs
Two input current limit period		REG18h, bits[14:8] = 110 0100	19	20	21	ms
Second input current limit duration		REG18h, bits[6:0] = 000 1010	1.8	2	2.2	ms
First input current limit duration to trigger PROCHOT		REG1Ah, bits[8:7] = 01		2		sec
Second input current limit duration to trigger PROCHOT		REG1Ah, bits[6:5] = 10		5		ms
Battery OC threshold to trigger PROCHOT		REG1Ah, bits[2:0] = 011	10.8	12	13.5	A
Battery OC threshold deglitch time		REG19h, bits[7:6] = 01		2		ms
System UV threshold to trigger PROCHOT		REG19h, bits[15:10] = 001111	5.85	6	6.15	V
System UV PROCHOT deglitch time		REG19h, bit[2] = 1		5	6	µs
PROCHOT pulse duration time		REG19h, bits[5:3] = 010		1		ms
PSYS output current			0		150	µA
PSYS gain		REG1Ah, bits[4:3] = 00		1		µA/W
PSYS output real-time delay				10		µs
PSYS gain accuracy (1µA/W gain)		Input only, V_{IN} = 20V with system power = 45W, 0°C to 85°C	-4%		4%	
		Battery only, V_{BATT} = 11V with system power = 45W, 0°C to 85°C	-4%		4%	

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ELECTRICAL CHARACTERISTICS *(continued)*

R_{S_IN} = 10mΩ, R_{S_BAT} = 10mΩ, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
IAM gain		REG17h, bit[3] = 0		20		V/V
		REG17h, bit[3] = 1		40		V/V
IAM offset (0°C to 85°C)			194	200	206	mV
IAM accuracy (0°C to 85°C)		5mV	-10%		+10%	
		10mV	-5%		+5%	
		20mV	-3%		+3%	
		40mV	-2%		+2%	
IBM gain		REG17h, bit[2] = 0		10		V/V
		REG17h, bit[2] = 1		20		V/V
IBM offset (0°C to 85°C)			195	200	205	mV
IBM accuracy (0°C to 85°C)		5mV	-10%		+10%	
		10mV	-5%		+5%	
		20mV	-3%		+3%	
		40mV	-2%		+2%	
V_{SYS} threshold to trigger V_{IN} discharging in V_{MIN} active protection (VAP) mode		REG19h, bits[15:10] = 001101	5.85	6	6.25	V
V_{SYS} threshold to trigger V_{IN} discharging deglitch time.		REG19h, bit[2] = 1		5	6	µs
SMBus Interface (SMBus Should Support I²C Specifications. I²C/SMBus Lines are Compatible with 1.8V/3.3V Logic)						
Input high threshold level	V_{IH}	V_{PULL_UP} = 1.8V, SDA and SCL	1.3			V
Input low threshold level	V_{IL}	V_{PULL_UP} = 1.8V, SDA and SCL			0.4	V
Output low threshold level	V_{OL}	I_{SINK} = 5mA			0.4	V
Pin leakage current	I_{LEAK}		-0.2		+0.2	µA
SMBus Timing Characteristics (5)						
SMBus clock frequency	f_{SCL}		10		400	kHz
Bus free time		Between a stop and start command	1.3			µs
Start command hold time (after which the first clock is generated)			0.6			µs
Start command set-up time			0.6			µs
Stop command set-up time			0.6			µs
Data hold time			0			ns
Data set-up time			100			ns
Clock low timeout			25		35	ms
Clock low period			1.3			µs
Clock high period			0.6			µs
Clock/data falling time					300	ns
Clock/data rising time					300	ns

Note:

5) Guaranteed by design.

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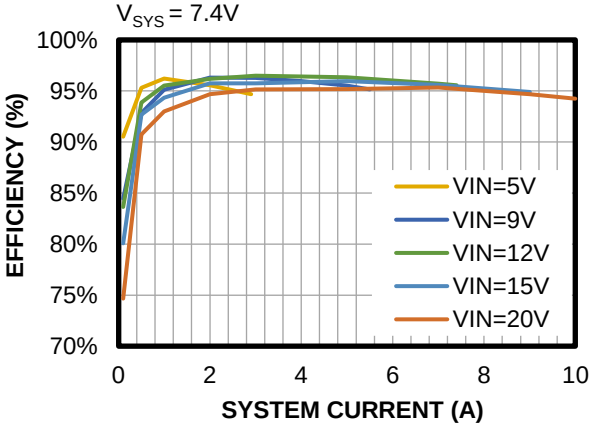
TYPICAL CHARACTERISTICS

R_{S_IN} = 10mΩ, R_{S_BAT} = 10mΩ, f_{SW} = 600kHz, L1 = L2 = 3.3μH, T_A = 25°C, unless otherwise noted.

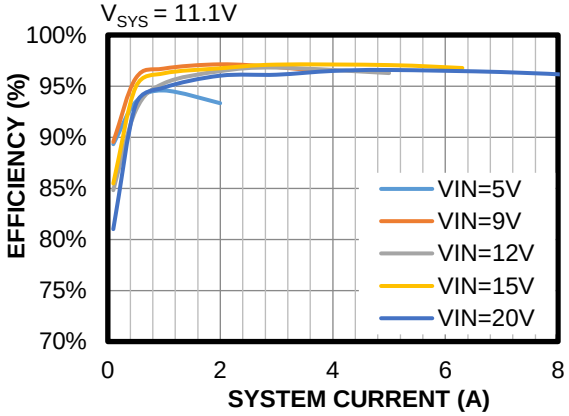
System Efficiency with 2S Battery

V_{SYS} = 7.4V



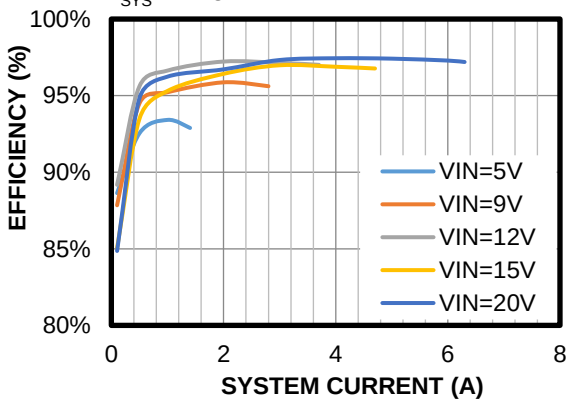
System Efficiency with 3S Battery

V_{SYS} = 11.1V



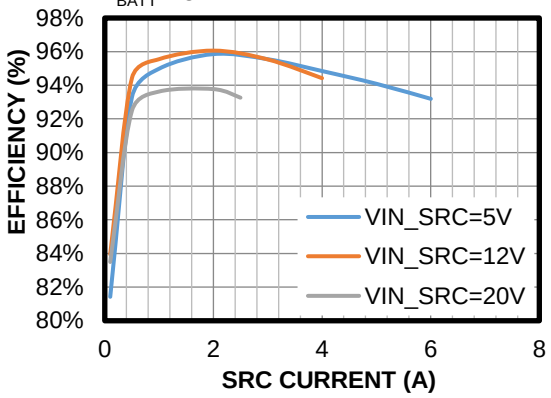
System Efficiency with 4S Battery

V_{SYS} = 14.8V



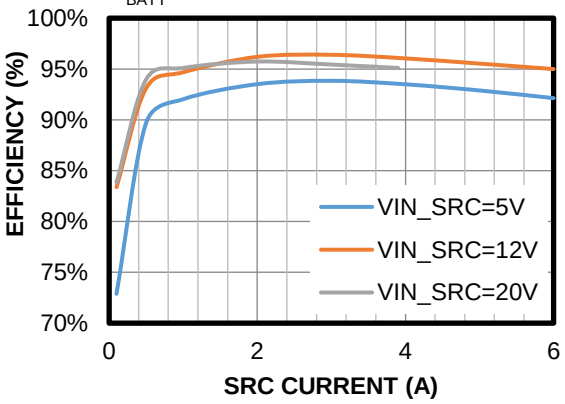
SRC Efficiency with 2S Battery

V_{BATT} = 8V



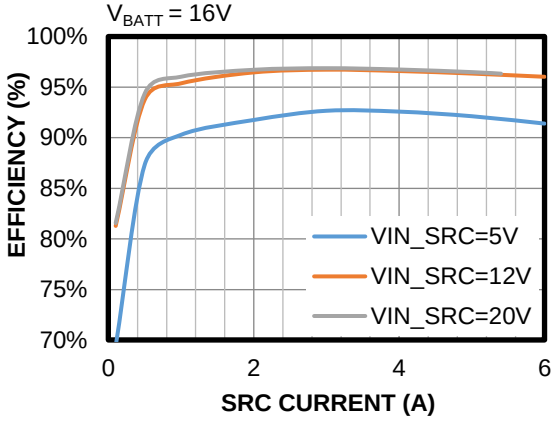
SRC Efficiency with 3S Battery

V_{BATT} = 12V



SRC Efficiency with 4S Battery

V_{BATT} = 16V



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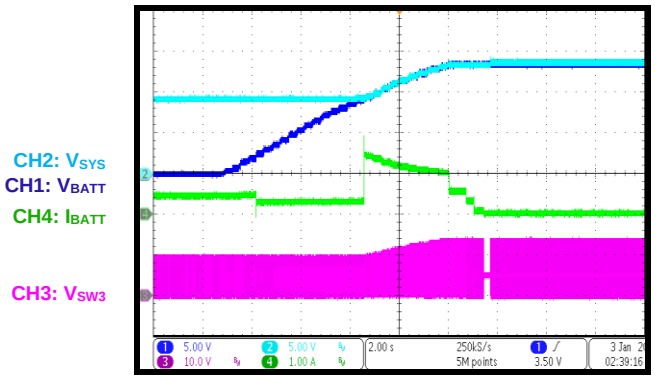
TYPICAL PERFORMANCE CHARACTERISTICS

R_{S_IN} = 10mΩ, R_{S_BAT} = 10mΩ, f_{SW} = 600kHz, L1 = L2 = 3.3μH, T_A = 25°C, unless otherwise noted.

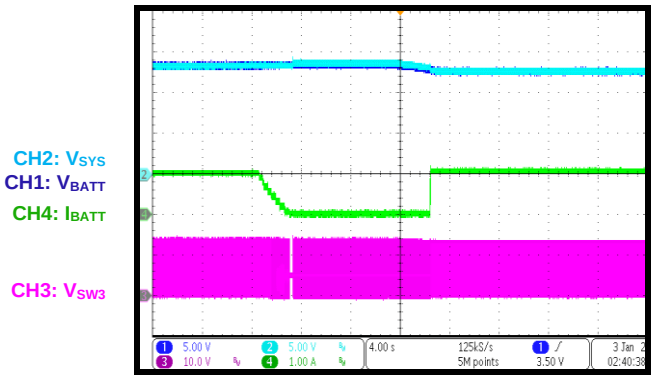
Battery Charge Curve

V_{IN} = 5V, V_{BATT} = 0V to 13.5V, I_{TERM} = 0.125A, I_{IN_LIM} = 3A, I_{CC} = 3A, auto-termination is enabled



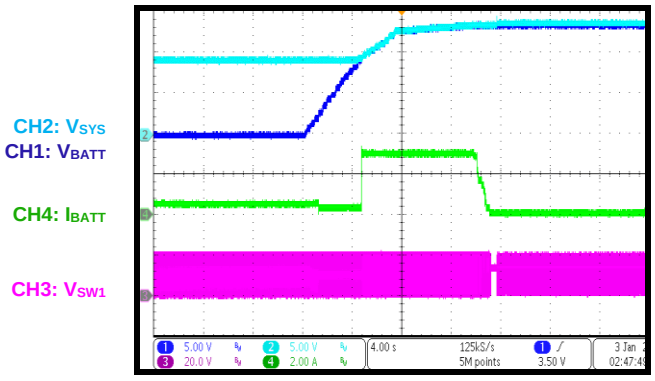
Auto-Recharge

V_{IN} = 5V, V_{BATT} = 13.5V to 12.7V, I_{CC} = 3A, auto-termination is enabled



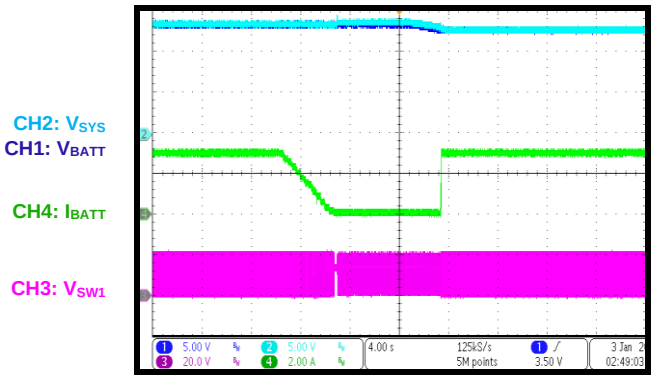
Battery Charge Curve

V_{IN} = 20V, V_{BATT} = 0V to 13.5V, I_{TERM} = 0.125A, I_{IN_LIM} = 3.25A, I_{CC} = 3A, auto-termination is enabled



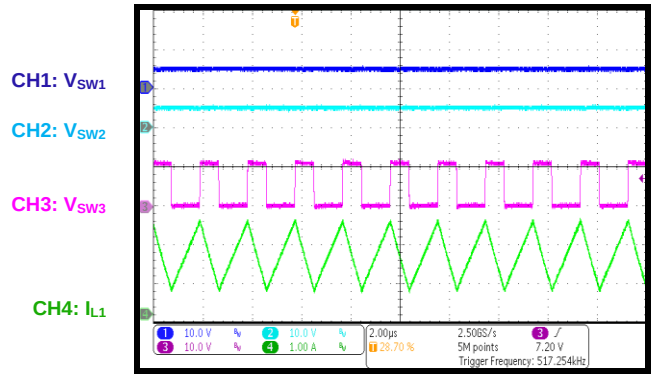
Auto-Recharge

V_{IN} = 20V, V_{BATT} = 13.5V to 13V, I_{CC} = 3A, auto-termination is enabled



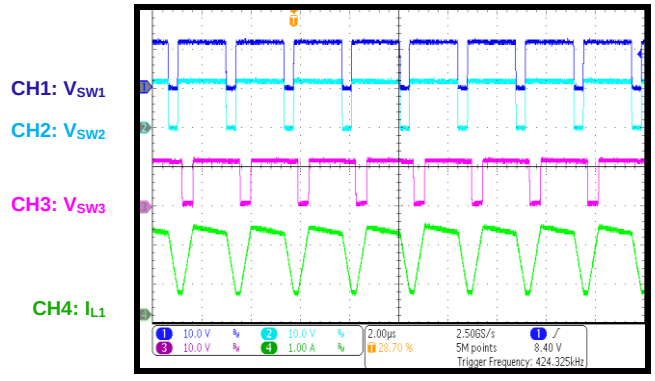
Boost Charge Steady Operation

V_{IN} = 9V, V_{BATT} = 12V, I_{CC} = 3A, I_{IN_LIM} = 3A



Buck-Boost Charge Steady Operation

V_{IN} = 12V, V_{BATT} = 12V, I_{CC} = 3A, I_{IN_LIM} = 3A



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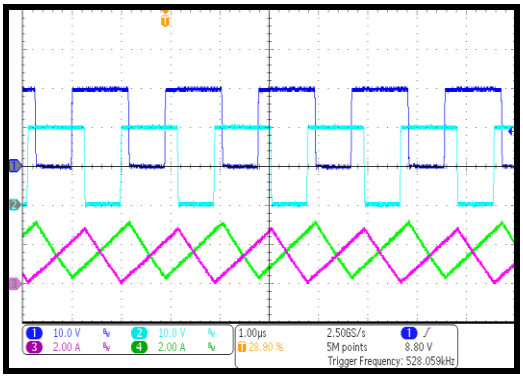
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

R_{S_IN} = 10mΩ, R_{S_BAT} = 10mΩ, f_{SW} = 600kHz, L1 = L2 = 3.3μH, T_A = 25°C, unless otherwise noted.

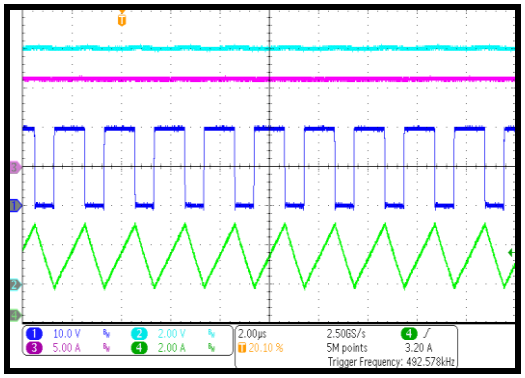
Buck Charge Steady Operation (Interleave Two Inductors)

V_{IN} = 20V, V_{BATT} = 12V, I_{CC} = 3A, I_{IN_LIM} = 3A



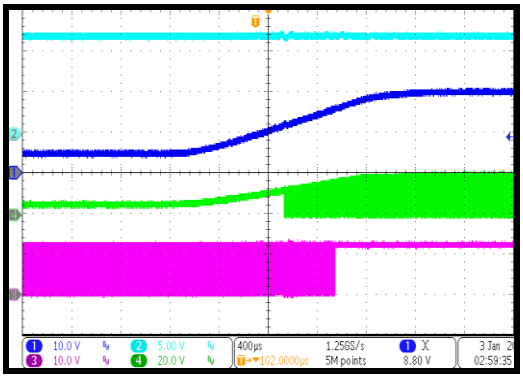
Buck Charge Steady Operation (Parallel Single Inductor)

V_{IN} = 20V, V_{BATT} = 12V, I_{CC} = 3A, I_{IN_LIM} = 3A



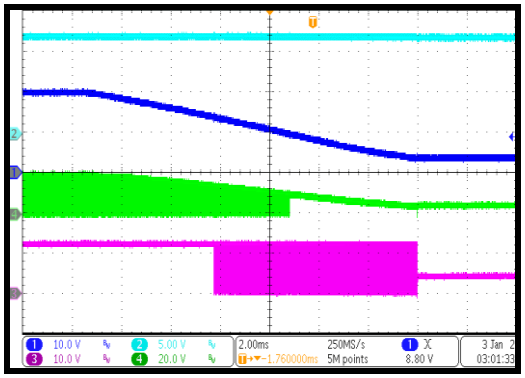
Boost to Buck-Boost to Buck Transition

V_{IN} = 5V to 20V, V_{BATT} = 12V, I_{CC} = 3A



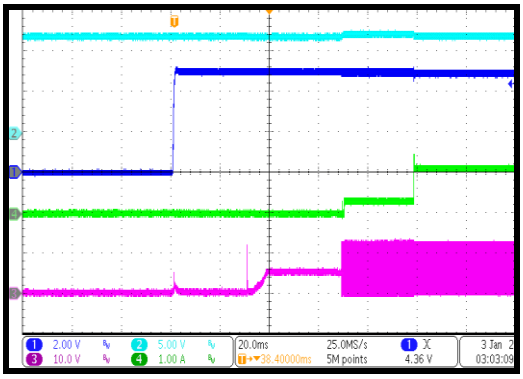
Buck to Buck-Boost to Boost Transition

V_{IN} = 20V to 5V, V_{BATT} = 12V, I_{CC} = 3A



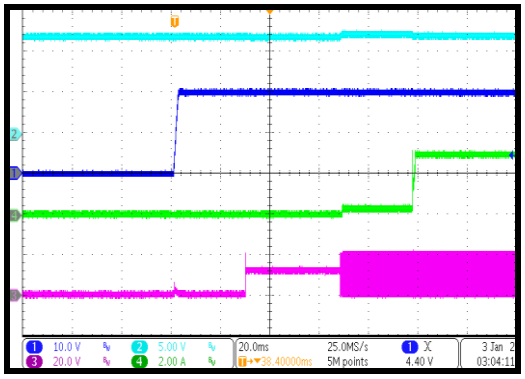
Start-Up through VIN

V_{IN} = 5V, V_{BATT} = 12V, I_{CC} = 3A



Start-Up through VIN

V_{IN} = 20V, V_{BATT} = 12V, I_{CC} = 3A



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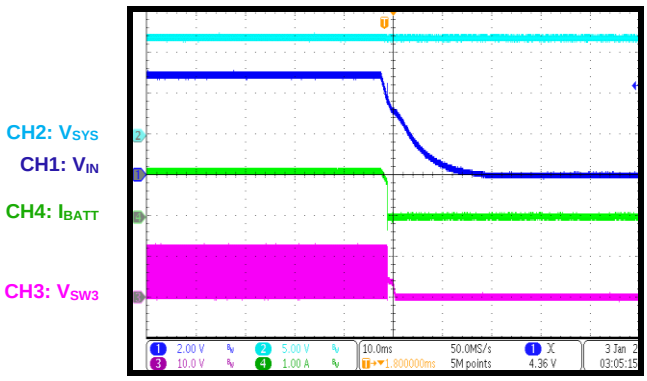
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

R_{S_IN} = 10mΩ, R_{S_BAT} = 10mΩ, f_{SW} = 600kHz, L1 = L2 = 3.3μH, T_A = 25°C, unless otherwise noted.

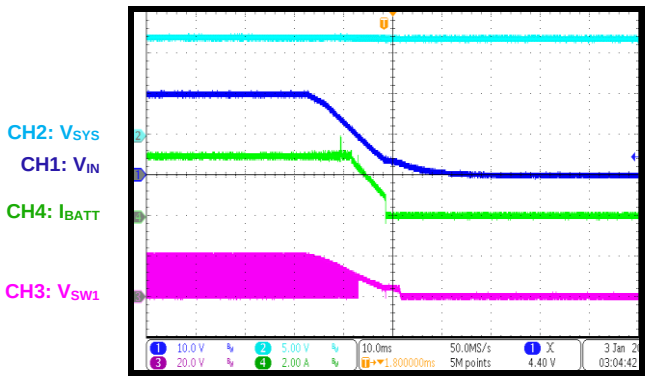
Shutdown through VIN

V_{IN} = 5V, V_{BATT} = 12V, I_{CC} = 3A



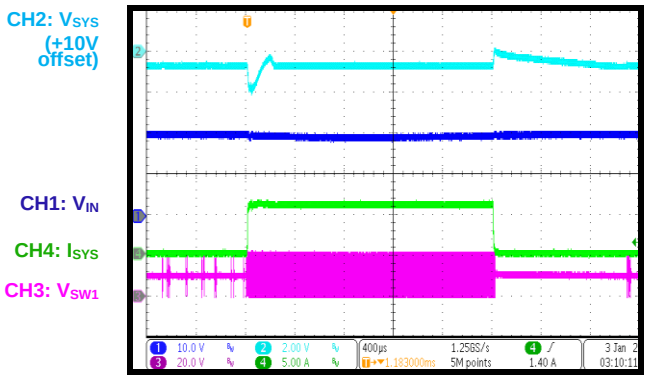
Shutdown through VIN

V_{IN} = 20V, V_{BATT} = 12V, I_{CC} = 3A



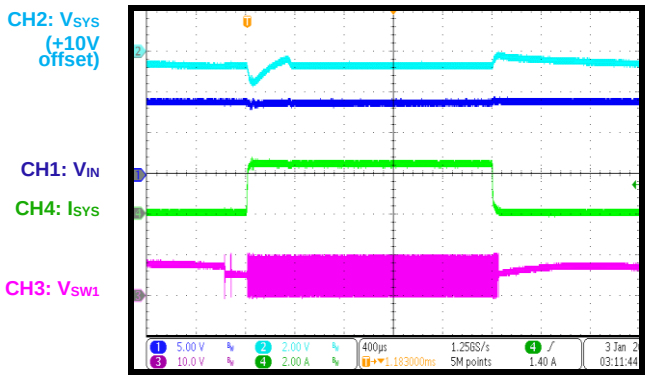
System Regulation in Buck Mode

V_{IN} = 20V, V_{SYS} = 9.3V, $I_{INLIMIT}$ = 3A, no BATT, charge disabled, I_{SYS} = 0A to 6A to 0A



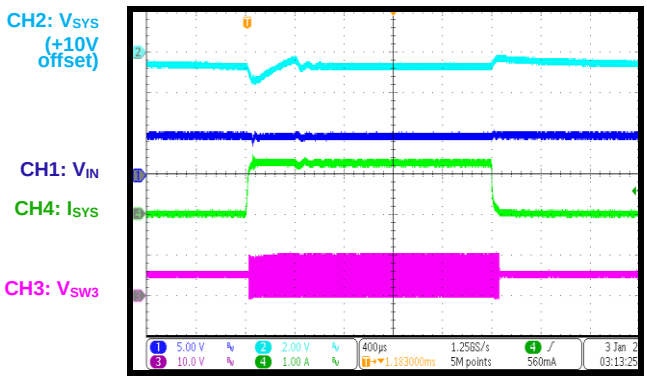
System Regulation in Buck-Boost Mode

V_{IN} = 9V, V_{SYS} = 9.3V, $I_{INLIMIT}$ = 3A, no BATT, charge disabled, I_{SYS} = 0A to 2.5A to 0A



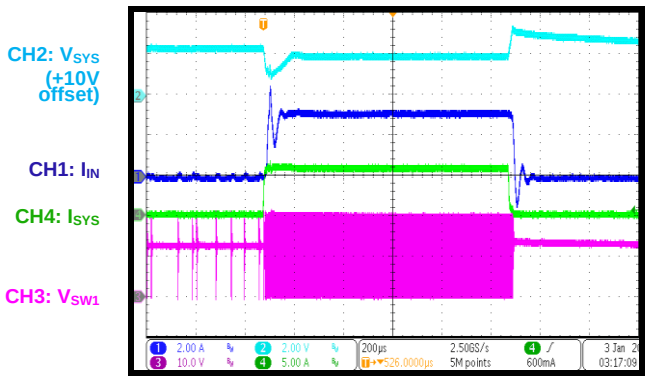
System Regulation in Boost Mode

V_{IN} = 5V, V_{SYS} = 9.3V, $I_{INLIMIT}$ = 3A, no BATT, charge disabled, I_{SYS} = 0A to 1.3A to 0A



Input Current Regulation in Buck Mode

V_{IN} = 20V, V_{BATT} = 12V, I_{INLMIT} = 3A, charge disabled, I_{SYS} = 0A to 6A to 0A



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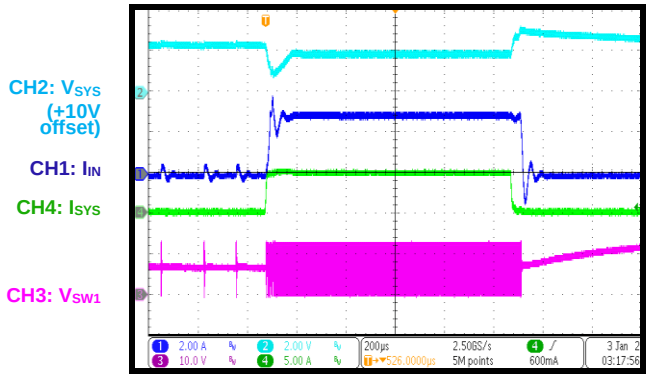
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

R_{S_IN} = 10mΩ, R_{S_BAT} = 10mΩ, f_{SW} = 600kHz, L1 = L2 = 3.3μH, T_A = 25°C, unless otherwise noted.

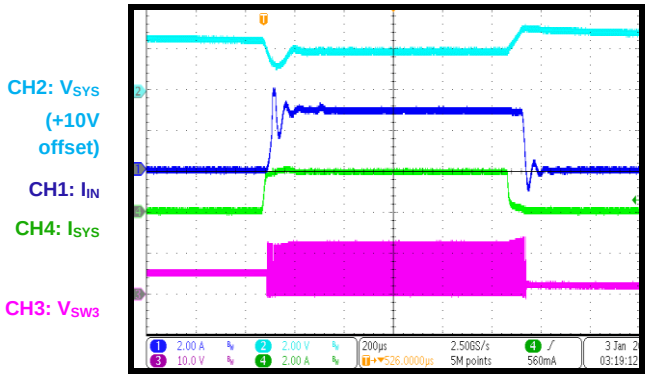
Input Current Regulation in Buck-Boost Mode

V_{IN} = 12V, V_{BATT} = 12V, $I_{INLIMIT}$ = 3A, charge disabled, I_{SYS} = 0A to 5A to 0A



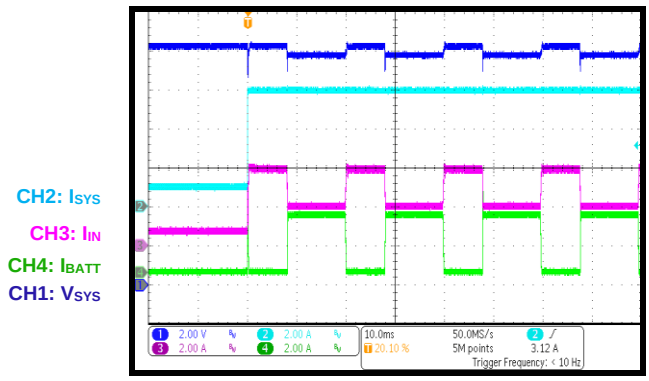
Input Current Regulation in Boost Mode

V_{IN} = 5V, V_{BATT} = 12V, $I_{INLIMIT}$ = 3A, charge disabled, I_{SYS} = 0A to 2A to 0A



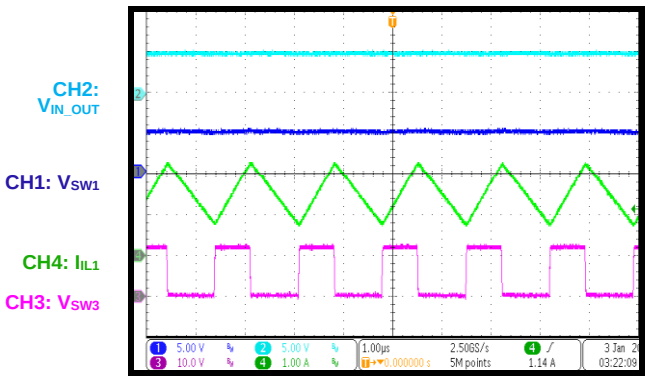
Two-Level Input Current Limit for Peak Power Mode

V_{IN} = 20V, V_{BATT} = 12V, charge disabled, $I_{INLIMT1}$ = 2A, $I_{INLIMIT2}$ = 4A, t_{PERIOD} = 20ms, t_{ILIM2} = 8ms, I_{SYS} = 1A to 6A



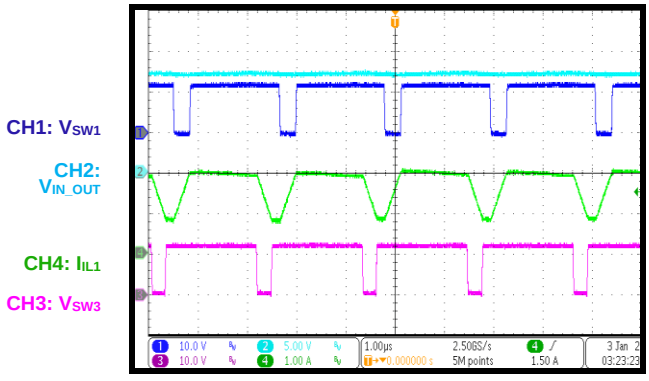
In Source Mode Buck Operation

V_{BATT} = 12V, V_{IN_OUT} = 5V, I_{IN_SRC} = 3A



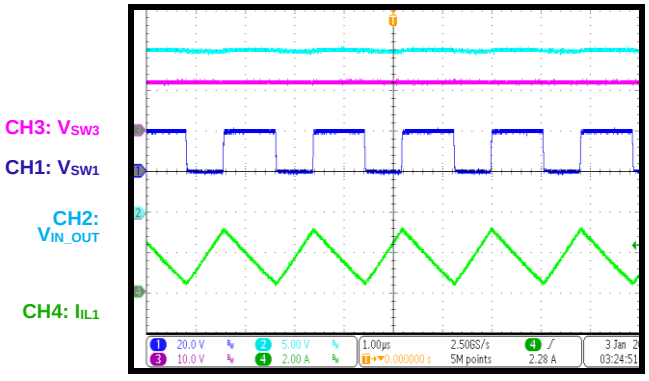
In Source Mode Buck-Boost Operation

V_{BATT} = 12V, V_{IN_OUT} = 12V, I_{IN_SRC} = 3A



In Source Mode Boost Operation

V_{BATT} = 12V, V_{IN_OUT} = 20V, I_{IN_OUT} = 2A



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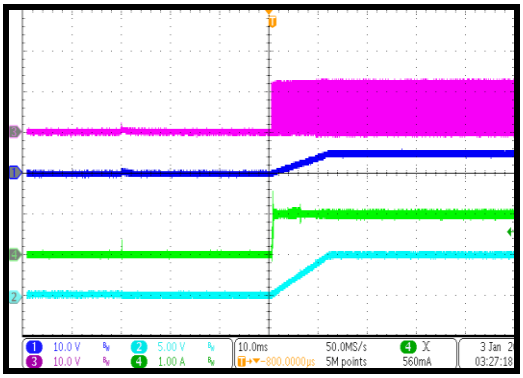
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

R_{S_IN} = 10mΩ, R_{S_BAT} = 10mΩ, f_{SW} = 600kHz, L1 = L2 = 3.3μH, T_A = 25°C, unless otherwise noted.

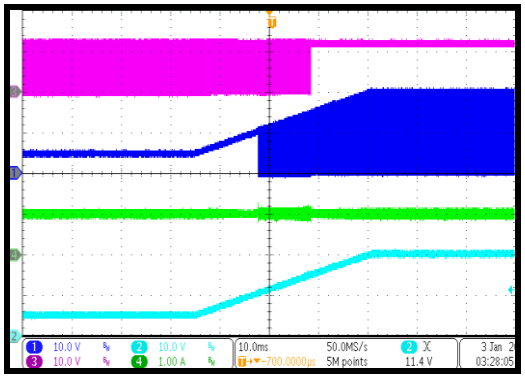
In Source Mode Start-Up

V_{BATT} = 12V, V_{IN_OUT} = 5V, I_{IN_OUT} = 1A



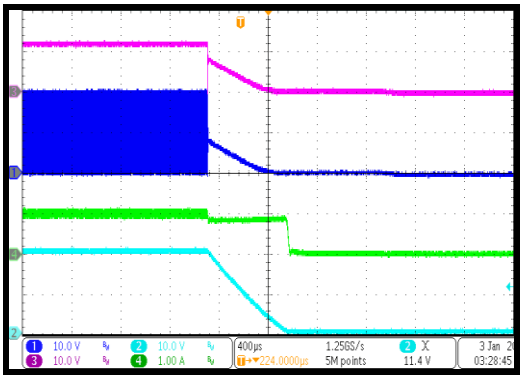
In Source Mode Voltage Ramping Up

V_{BATT} = 12V, V_{IN_OUT} = 5V to 20V, I_{IN_OUT} = 1A



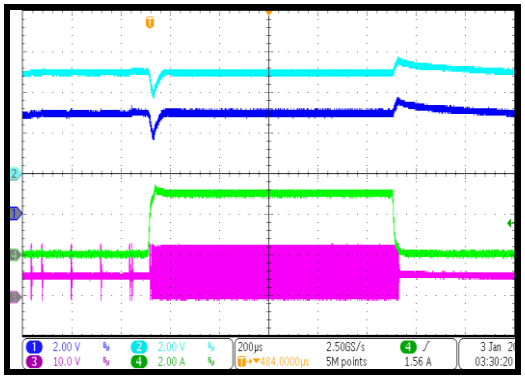
In Source Mode Shutdown

V_{BATT} = 12V, V_{IN_OUT} = 20V, I_{IN_SRC} = 3A, I_{IN_OUT} = 2A



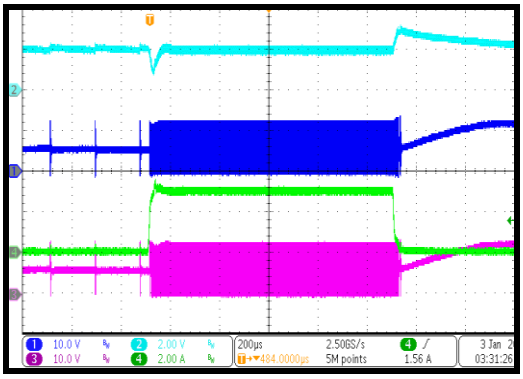
In Source Mode Load Transient

V_{BATT} = 12V, V_{IN_OUT} = 5V, I_{IN_SRC} = 5A, I_{IN_OUT} = 0A to 3A to 0A



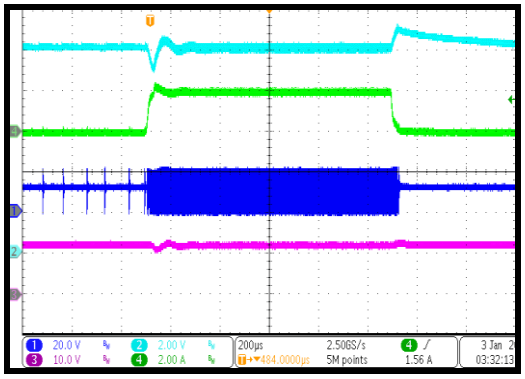
In Source Mode Load Transient

V_{BATT} = 12V, V_{IN_OUT} = 12V, I_{IN_SRC} = 5A, I_{IN_OUT} = 0A to 3A to 0A



In Source Mode Load Transient

V_{BATT} = 12V, V_{IN_OUT} = 20V, I_{IN_SRC} = 3A, I_{IN_OUT} = 0A to 2A to 0A



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FUNCTIONAL BLOCK DIAGRAM

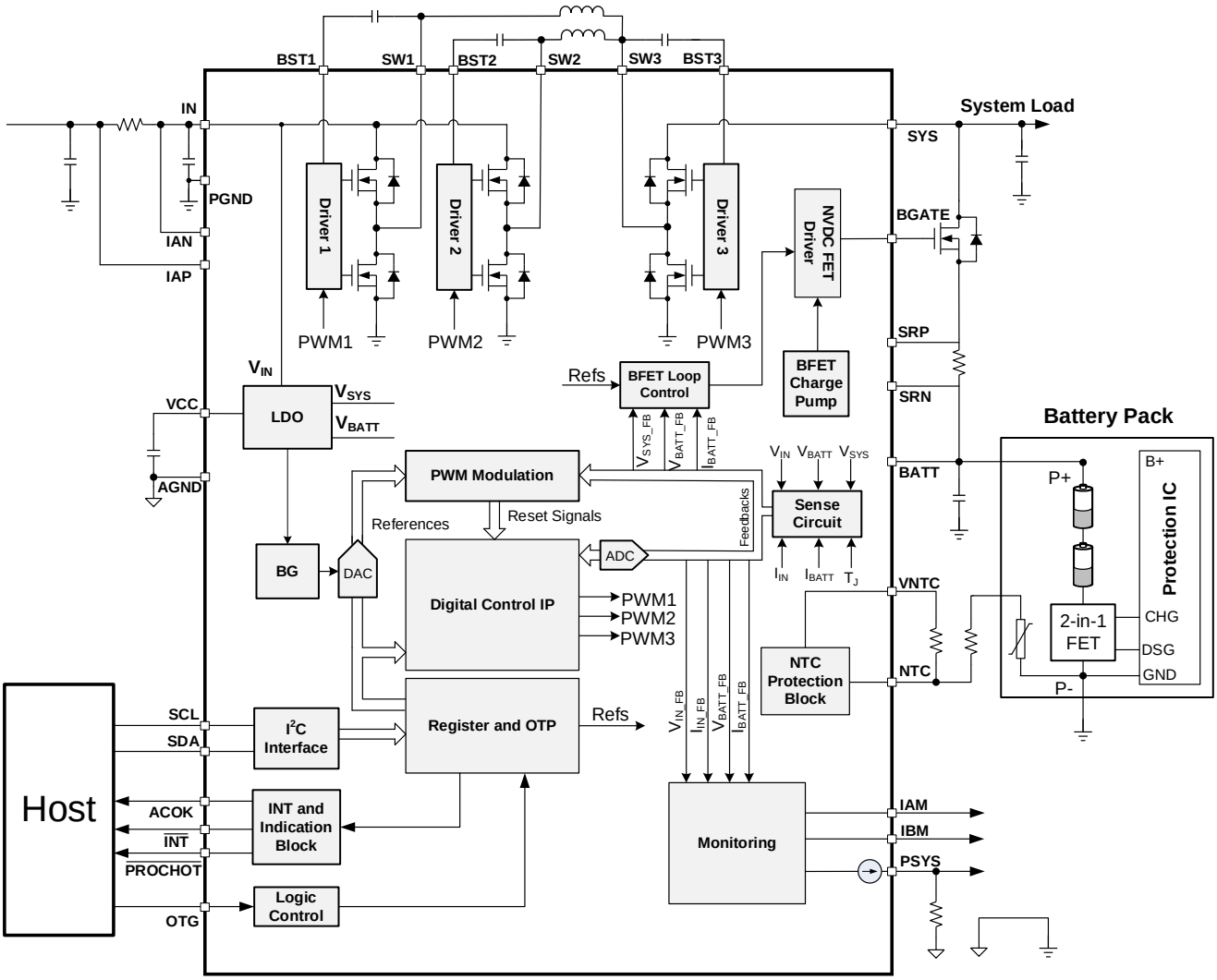

Figure 2: Functional Block Diagram

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OPERATION

The MP2764 is a highly integrated buck-boost charger IC with integrated switching FETs that can charge battery packs with 2 to 4 cells in series. The device also integrates an N-channel MOSFET driver for narrow-voltage DC (NVDC) power path management.

The MP2764 can also operate in reverse to power the input from the battery. This function is compliant with USB power delivery (PD) source mode.

The converter has three operating modes:

- Boost mode when the input voltage (V_{IN}) is below the system voltage (V_{SYS}).
- Buck mode when V_{IN} exceeds V_{SYS}.
- Buck-boost mode when V_{IN} is almost equal to V_{SYS}.

When the input power is present, the MP2764 operates in charging mode to charge 2-cell to 4-cell in series battery packs with a wide 4V to 22V V_{IN} range.

When the input is absent, the MP2764 can operate in reverse to power the input from the battery. In this scenario, the MP2764 can provide between 4V and 21V of output voltage (V_{IN_OUT}), with 6.25mV/step at the input. The device also has a 50mA/step current limit in this mode. Generally, this mode is called source mode in USB PD applications.

Buck, Buck-Boost, and Boost Mode Transitions

The MP2764 is a buck-boost charger that can receive a wide 4V to 19.2V battery voltage range for 2-cell to 4-cell battery packs. It can automatically transition between each mode according to V_{IN} and the system voltage (V_{SYS}).

Figure 3 shows the mode transitions.

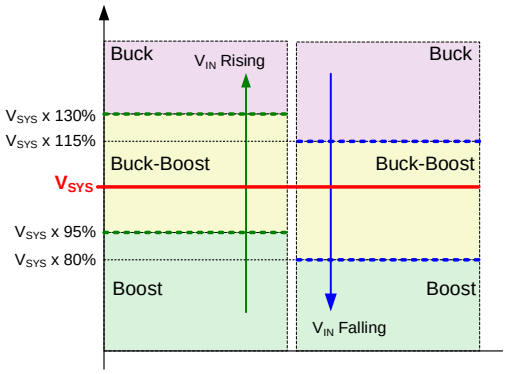

Figure 3: Mode Transition Threshold

Dual-Phase Interleaving Operation

In charge mode, the MP2764 integrates two buck phases that can support dual-phase interleaving operation with two inductors in buck charge mode. Q5 is always on, and the pulse-width modulation (PWM) of phase 2 (Q3/Q4) is always 180° behind phase 1 (Q1/Q2). Phase 2 stays off until the input current (I_{IN}) exceeds 1.2A.

In buck-boost or boost mode, the PWM of phase 2 (Q3/Q4) always follows phase 1 (Q1/Q2).

Figure 4 shows dual-phase interleaving mode.

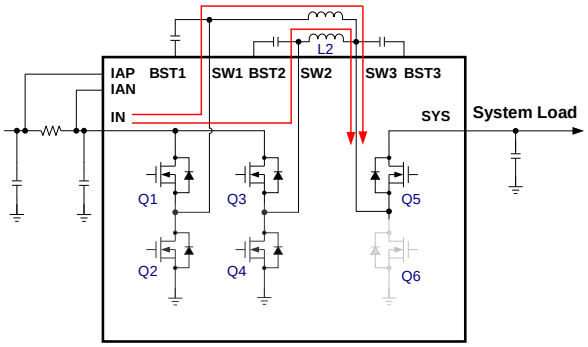

Figure 4: Dual-Phase Interleaving Mode

Figure 5 shows the dual-phase interleaving waveform in buck mode.

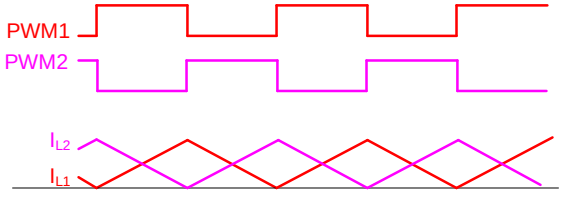

Figure 5: Dual-Phase Interleaving Waveform in Buck Mode

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Dual-Phase Parallel Operation

In addition to the dual buck phase, the MP2764 can also operate with a single inductor with two phases in parallel. In this scenario, the PWM of the two phases is the exact same.

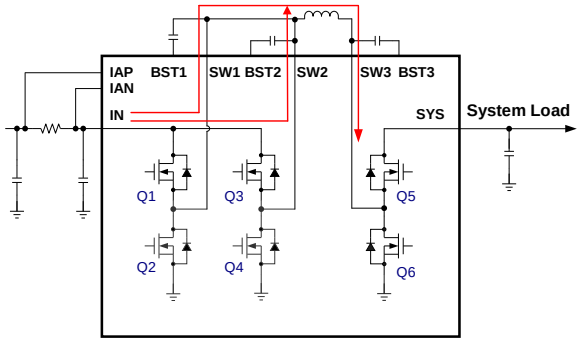

Figure 6: Dual-Phase Parallel Mode

The different dual-phase modes can be configured via the one-time programmable (OTP) memory. Customers can request the 4-digit suffix code “0000” for dual-phase interleaving operation and “0001” for dual-phase parallel mode operation.

VCC Low-Dropout (LDO) Regulator Output

The MP2764 integrates an LDO to generate the VCC voltage (V_{CC}). The VCC LDO supplies the internal bias circuits as well as the high-side and low-side MOSFETs (HS-FET and LS-FET, respectively) of the DC/DC converter. The pull-up rail of the open-drain outputs, such as ACOK, $\overline{INT}$, and $\overline{PROCHOT}$ can also be connected to VCC. VCC is powered by V_{IN} or V_{BATT}. When $V_{IN} > V_{IN_POR}$ rising threshold, VCC is powered by V_{IN} in charge mode and source mode. When the input is absent or $V_{IN} < V_{IN_POR}$ falling threshold, VCC is powered by V_{BATT}. The VCC pin has a 3.6V output and 50mA of current capability.

Input Under-Voltage Lockout (UVLO) Input Power-On Reset (POR)

The MP2764 has an input power-on reset (POR) voltage threshold (V_{IN_POR}). If V_{IN} drops below V_{IN_POR} and the battery is present, only the BGATE block (charge pump, battery under voltage lockout (UVLO), battery over-current protection (OCP)), and the I²C/SMBus continue to operate.

The MP2764 also integrates an input UVLO threshold. When $V_{IN_POR} < V_{IN} < V_{IN_UVLO}$, the internal control blocks such as the reference, digital-to-analog converter (DAC), and analog-to-digital converter (ADC) start to operate. However, the power stage is not ready until $V_{IN} > V_{IN_UVLO}$ with a 30ms deglitch time. Then the MP2764 enters buck, buck-boost, or boost charge mode.

Input Over-Voltage Lockout (OVLO)

The MP2764 also has input over-voltage lockout (OVLO) protection. When $V_{IN} > V_{IN_OVLO}$, the DC/DC converter stops operating after a 1µs or 10ms deglitch time (set via REG12h, bit[0]). During OVLO protection, the internal control blocks (such as the reference, DAC, and ADC) are still working.

Input Power Status Indicator

The MP2764 qualifies the voltage of the input source before start-up. The input source must meet the following requirement:

- $V_{IN_UVLO} < V_{IN} < V_{IN_OVLO}$

Once the input power source meets the above condition, the status register asserts that the input power is good, and then the DC/DC converter is ready to operate after 30ms.

In addition to register status reporting, the MP2764 also has an open-drain pin (ACOK) that indicates the presence of the input. The ACOK pin is pulled high as long as $V_{IN_UVLO} < V_{IN} < V_{IN_OVLO}$.

NVDC Power Path Power Management

The MP2764 is designed as a charger with narrow-voltage DC (NVDC) power-path power management, which guarantees the priority of the system power requirement under input plug-out or heavy load system conditions. An external battery FET is controlled by the BGATE pin to achieve NVDC power path control (see Figure 7).

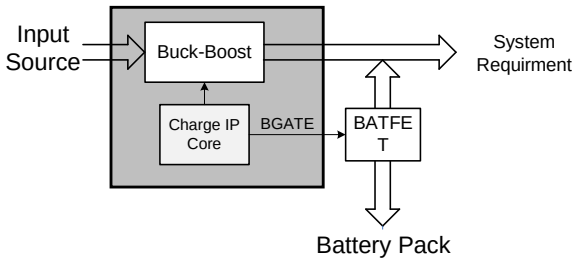

Figure 7: NVDC Power Path Management Structure

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A BGATE driver provides the following features:

- The system instantly starts up after the input power turns on when V_{BATT} is low.
- V_{SYS} stays almost equal to V_{BATT} to allow to use of a low voltage point-of-load (PoL). The battery can supplement the system power when the input power is limited or absent.
- When the input is present, the system takes power from the input after charge termination.

The MP2764 has a minimum system voltage (V_{SYS_MIN}) setting. When charging is disabled (the BATFET is off), V_{SYS} is regulated above the maximum values (V_{SYS_MIN}, V_{BATT}) by the battery track regulation voltage (V_{TRACK}). When V_{BATT} > V_{SYS_MIN}, V_{SYS} always tracks the real battery voltage. Figure 8 shows the system voltage tracking when the BATFET is off.

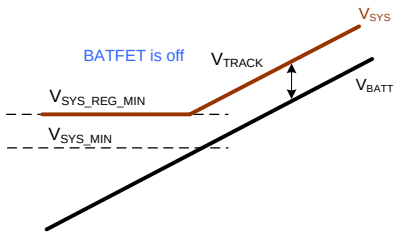

Figure 8: System Voltage Tracking When BATFET is off

When charging is enabled, the BATFET fully turns on when V_{BATT} > $V_{SYS_REG_MIN}$ (V_{SYS_MIN} + V_{TRACK}). In this scenario, the charge current loop and battery voltage loop are implemented by the buck-boost converter's PWM control. Figure 9 shows the system's voltage tracking when the BATFET is on.

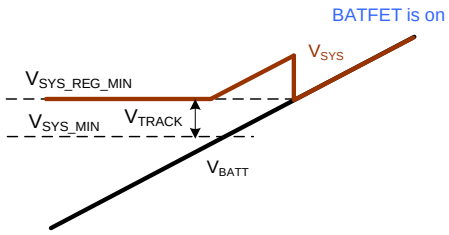

Figure 9: System Voltage Tracking When BATFET Is On

Even when charging a deeply discharged battery, the buck-boost converter regulates V_{SYS} at $V_{SYS_REG_MIN}$ to ensure that the host chip at the system starts up. In this mode, the battery FET operates in linear mode to charge the battery via the BATFET, which is usually called linear charging mode. Depending on the battery voltage, the charge current can be one of the following: trickle charge current, pre-charge current, or linear constant charge current

As described above, V_{SYS} is supposed to be regulated so that V_{TRACK} exceeds the maximum of V_{BATT} and V_{SYS_MIN}. Another maximum system voltage regulation is also defined to clamp the system voltage in the event that V_{BATT} runs away. $V_{SYS_REG_MAX}$ is defined as V_{BATT_REG} + V_{TRACK}.

Charge Profile

In charge mode, the MP2764 has 6 control loops to regulate V_{IN}, input current, charge current, battery charge voltage, V_{SYS}, and device junction temperature (T_J).

The IC provides four main charging phases: constant current (CC) trickle charge, CC pre-charge, CC fast charge, and constant voltage (CV) charge (see Figure 10).

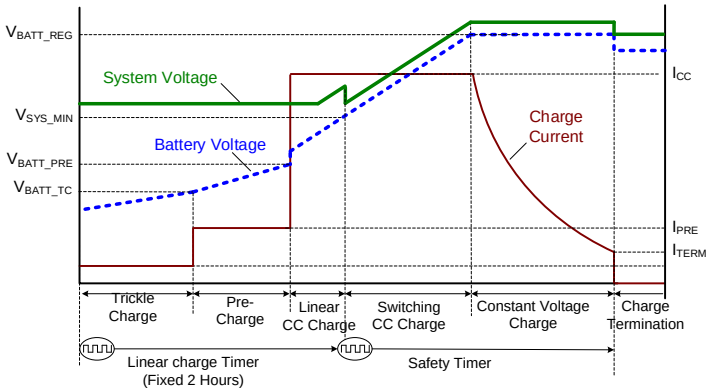

Figure 10: Charge in NVDC Mode

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Phase 1 (Constant Current Trickle Charge)

When the input power qualifies as a good power supply, the IC checks V_{BATT} to determine whether trickle charging is required. If V_{BATT} is below the trickle charge to pre-charge threshold (V_{BATT_TC}), a configurable trickle charge current is set to charge the battery.

Phase 2 (Constant Current Pre-Charge)

When V_{BATT} exceeds V_{BATT_TC}, the IC starts to safely pre-charge the deeply depleted battery until V_{BATT} reaches the pre-charge to fast charge threshold (V_{BATT_PRE}).

Phase 3 (Constant Current Fast Charge)

When V_{BATT} exceeds V_{BATT_PRE}, the IC enters the constant current charge (fast charge) phase. The constant current charge has two different charge modes:

Fast linear charge mode: The device operates in this mode when $V_{BATT_PRE} < V_{BATT} < V_{SYS_REG_MIN}$.

In this mode, V_{SYS} is regulated at $V_{SYS_REG_MIN}$, and the charge current loop is implemented by BGATE. The charge current is independently configured via REG14h, bits[12:8].

If $V_{SYS_REG_MIN}$ is not reached before the linear charge timer (2 hours) expires, the charge cycle ends and a corresponding timeout fault signal asserts.

Switching charge mode: The device operates in this mode when $V_{BATT} > V_{SYS_REG_MIN}$.

In this mode, the battery FET (BATFET) is fully on and the charge current loop is implemented by the PWM of the DC/DC converter.

Phase 4 (Constant Voltage Charge)

When V_{BATT} rises to the battery-full regulation voltage (V_{BATT_REG}), the charge current tapers off due to battery voltage loop control.

Automatic Termination and Recharge

The charge cycle is considered to be complete when the charge current reaches the termination threshold (I_{TERM}) and the constant voltage control loop is controlling the charging loop. A 1s deglitch time is designed for termination.

When each of the input current (I_{IN}) limit, V_{IN} limit, or thermal regulation limit is reached, termination is blocked.

When the battery is fully charged and charging is terminated, the battery may be discharged because of system consumption or self-discharge. When V_{BATT} is discharged below the recharge threshold, the IC automatically starts another charging cycle without requiring a manual restart as long as the input power is valid. The safety charge timer resets when the auto-recharge cycle begins.

A new charge cycle can only start when the following conditions are valid:

- The input power is re-plugged
- Battery charging is enabled via the I²C/ SMBus
- No thermistor fault has occurred
- No safety timer fault has occurred
- No battery over-voltage (OV) condition has occurred
- The BATFET is not forced to turn off

This means that re-plugging the input power or toggling the battery charging control bit can restart a charge cycle without any fault occurring. The new charge cycle can start in any charging phase, depending on V_{BATT}.

Charge termination can be disabled via REG12h, bit[12]. When charge termination is disabled, the host can terminate the charging cycle by setting the CHG_EN bit to 0 or setting I_{CC} = 0A when the battery is full or when the battery is in a not good charge condition.

Battery Supplement Mode

When the I_{IN} or V_{IN} limit loop operates, PWM control limits the power from the input. As a result, V_{SYS} and the charge current decrease.

If the system power still increases and exceeds the input power, V_{SYS} keeps falling. The charge current drops to 0A or becomes negative, which means the battery must start to discharge and supplement the system. This is called battery supplement mode. In this mode, the system load is powered by the battery and DC/DC converter simultaneously.

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Virtual Diode Loop

Virtual diode mode is designed to optimize the control transition between the battery and the buck-boost converter. In virtual diode mode, BGATE regulates the BATFET's source-to-drain voltage (V_{SD}) under light discharge current conditions from the battery to the system. The virtual diode mode block is only valid when the input is present.

A comparator compares V_{SYS} to V_{BATT} to determine when the device should enter or exit virtual diode. When $V_{SYS} < V_{BATT}$ - 30mV, virtual diode mode is enabled, and BGATE regulates V_{SD} to 37mV. As the discharge current increases, the battery's gate drive increases while the drain-to-source resistance (R_{DS}) decreases, until the BATFET is fully on. When the system load current drops, V_{SYS} rises above V_{BATT}. The device exits virtual diode mode when $V_{SYS} > V_{BATT}$ + 30mV.

Junction Temperature (T_J) Regulation

In charge mode, the thermal regulation loop always monitors the IC's internal junction temperature (T_J). When the internal T_J exceeds the temperature limit, the charge current is reduced to keep T_J at the regulation point. The multiple, configurable thermal regulation thresholds (from 80°C to 120°C) set via REG0Dh, bits[1:0] help the system design meet the thermal requirement in different applications.

Battery Impedance Compensation to Accelerate Charging

Throughout the whole charging cycle, the constant-voltage (CV) charging stage is the longest stage. To accelerate the charging cycle, it is better to have the device stay at the constant current charge stage for as long as possible.

The IC allows the user to compensate for the intrinsic battery resistance by adjusting the V_{BATT_REG} according to the charge current and internal resistance. In addition, a maximum allowed regulated voltage (V_{CLAMP}) is also set to keep the maximum battery voltage below (V_{BATT_REG} + V_{CLAMP}). The real battery regulation voltage ($V_{BATT_REG_ACT}$) can be calculated with Equation (1):

$$V_{BATT_REG_ACT} = V_{BATT_REG} + Min\ (V_{CLAMP}, I_{CHG_ACT} \times R_{BATT}) \quad (1)$$

Where V_{BATT_REG} is the battery regulation voltage, and I_{CHG_ACT} is the real-time charge current during operation.

Battery Over-Voltage Protection (OVP)

The MP2764 also has battery over-voltage protection (OVP). If V_{BATT} exceeds the battery OV threshold (160mV higher than the battery regulation voltage per cell), charging is disabled. Battery OVP has a 1.5ms deglitch time.

Under this condition, the BATFET turns off while REG11h, bit[4] = 1, and the buck-boost converter tries to regulate V_{SYS} at V_{TRACK} + V_{BATT_REG}. Once the MP2764 enters the battery OV state, the battery OV condition is continuously monitored until the OV condition is removed. When the battery OV condition is removed, the MP2764 goes to the charge termination state.

When the battery dummy load is enabled (REG11h, bit[14] = 1), and a battery OV condition is detected, the dummy load turns on to automatically discharge the battery until the OV state is removed.

Charge Enable Control

The MP2764 has a register bit (REG13h, bit[0]) to enable or disable charging. When charging is disabled, the BATFET turns off. Meanwhile, the DC/DC converter is still operating, and V_{SYS} is regulated depending on V_{BATT}.

Suspend Mode Control

The MP2764 also has a register bit (REG13h, bit[1]) to enable or disable the DC/DC converter's suspend mode. When suspend mode is enabled, the buck-boost converter turns off and forces the battery to power the system load, regardless of the input source status.

System Over-Voltage Protection (OVP)

The MP2764 provides OVP for system voltage regulation. When V_{SYS} exceeds a percentage (set via REG12h, bit[12]) of the V_{SYS} regulation voltage, the PWM of the DC/DC converter stops immediately. The device asserts an interrupt ($\overline{INT}$) and monitors the system's OV status continuously until it is removed.

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System Short-Circuit Protection (SCP)

When V_{SYS} is below its under-voltage (UV) threshold for 0.5ms, the PWM of the DC/DC converter stops and automatically tries to start after 300ms.

Current Balance Loop

An optional current balance loop is also designed to ensure that the two phases deliver the same power to the system. When the current balance loop is enabled, PWM2 can be extended or shrunk to ensure that the average current flowing through each phase is equivalent.

The current balance loop is only valid in buck interleaving mode.

Watchdog Timer

The MP2764 has a watchdog timer to monitor the actions of the I²C/SMBus interface. If the watchdog timer is enabled, the host must periodically reset the watchdog timer reset bit before the watchdog timer expires. If the watchdog timer expires, all of the registers are reset to their default values.

The watchdog timer can be disabled via REG12h, bits[11:10].

Safety Timer

The IC provides both a trickle charge and pre-charge timer and CC/CV timer to prevent extended charging cycles due to abnormal battery conditions. The safety timer for trickle charge and pre-charge is 2 hours when V_{BATT} is below $V_{SYS_REG_MIN}$

The CC/CV charge safety timer starts when the battery enters the switching CC charging phase. The user can configure this timer via REG13h, bits[9:6]. The two safety timers discussed above can be disabled via REG11h, bit[0].

The safety timer can be reset by the following events:

- A new charging cycle begins
- Writing REG13h, bit[0] from 0 to 1 (charge enabled)
- Writing REG11h, bit[0] from 0 to 1 (safety timer enabled)

The timer is suspended when any of the following conditions occurs:

- The battery supplements the system
- An NTC hot or cold fault occurs
- I_{CC} decreases in the JEITA NTC cool or warm window

Battery Detection or Battery Temperature Sensing via the NTC/BATDET Pin

The NTC/BATDET pin is a dual-purpose pin. It can be configured for battery detection (BATDET) or NTC monitoring (NTC) via the OTP. The default setting is for the BATDET function.

When configured for battery detection, the NTC/BATDET pin is a 10μA current source. A resistor combined with the battery pack should be connected to the NTC/BATDET pin. Once the NTC/BATDET pin's voltage exceeds 1.6V, a battery removal condition is detected. This is reported in the status register, and an interrupt is generated on the $\overline{PROCHOT}$ pin.

When configured for the temperature sense function, the NTC/BATDET pin should be biased from VNTC by a divider with a thermistor at the low side. The MP2764 continuously monitors the battery's temperature by measuring the voltage at the NTC/BATDET pin. To satisfy the JEITA requirement, the MP2764 also has a ratio threshold for cool and warm temperatures. The charge behavior for cool or warm protections can be configured.

Battery Missing Protection

If the battery is disconnected, the MP2764 reports that the battery is missing in the status register and initiates an $\overline{INT}$ signal once termination has been detected three times within 6.4s. Battery missing detection works while the following events are valid:

- The charge termination function is enabled
- No BATDET or NTC fault has occurred

Source Mode

The MP2764 can also work in source mode to supply an IN pin from the battery power. The output voltage in source mode (V_{IN_OUT}) can be configured via REG0Bh, bits[11:0]. The MP2764 also has an output current limit in source mode (I_{IN_OUT}); the output current limit can be configured via REG0Ch, bits[6:0].

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Source mode can be enabled via either the OTG pin or associated register bit (REG13h, bit[4]).

The OTG pin only can enabled in source mode when it is configured for OTG control via REG13h, bit[5].

Output Over-Voltage Protection (OVP) in Source Mode

The MP2764 also has OVP in source mode. If V_{IN_OUT} exceeds the percentage (110%) of the regulation voltage, the DC/DC converter turns off immediately.

Short-Circuit Protection (SCP) in Source Mode

The MP2764 provides SCP. If V_{IN_OUT} falls below its UV threshold for 0.5ms, the DC/DC converter turns off and tries to restart after 300ms.

Battery Low-Voltage Protection in Source Mode

The MP2764 has battery low-voltage protection in source mode. When V_{BATT} falls below the V_{BATT_LOW} threshold, the DC/DC converter stops and latches off, and an interrupt ($\overline{INT}$) asserts. In this scenario, the battery FET is still on to power the system from the battery power. After the DC/DC converter latches off, toggling the source enable bit or OTG pin can reset the latched condition. An OTP option is also reserved to only assert an $\overline{INT}$ signal without latching off the DC/DC converter.

Battery Discharge Current Loop

The MP2764 also integrates an optional battery discharge current limit loop in source mode. When the battery discharge current exceeds the battery discharge current limit, the output power is limited to ensure the system power priority.

Thermal Shutdown

The IC continuously monitors the chip's internal T_J in forward charge mode and source mode. When T_J reaches 150°C, the DC/DC converter shuts down. The device does not resume normal operation until T_J drops below 120°C.

PROG Pin Setting

The MP2764 has a PROG pin to set the target address (see Table 1) or battery cell number (see Table 2 on page 30). The PROG pin can be configured for three modes via the OTP:

- PROG disabled: When the PROG pin is configured as disabled, the device's target address is 0x5C, and the battery cell can be configured via REG17h, bits[1:0]. The PROG pin can be left floating or connected to GND.
- PROG for address setting: When the PROG pin is configured for address setting, then the default 0x5C address is invalid, and the lowest 3 bits of the target address is determined by the resistor value connected between PROG and GND. The highest 4 bits are configured via the OTP with a default setting of 0010. The battery cell number can be configured via register REG17h, bits[1:0]. The target address configured via the PROG pin (see Table 1).
- PROG for battery cell setting: When the PROG pin is configured to set the battery cell number, the battery number cell is configured by the resistor connected between PROG and GND. The target address is fixed to 0x5C. The battery number cell can be configured via the PROG pin (see Table 2 on page 30).

The PROG pin function is configured to set the battery cell number by default.

Table 1: Target Address Setting via the PROG Pin

PROG Pin to GND Resistor (1%)	Lowest 3 Bits of Target Address	Target Address
0 to 1kΩ	'000	0x10
6.19kΩ to 8.06kΩ	'001	0x11
15.4kΩ to 20kΩ	'010	0x12
45.3kΩ to 53.6kΩ	'100	0x14
73.2kΩ to 90.9kΩ	'101	0x15
100kΩ to 112kΩ	'110	0x16

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Table 2: Battery Cell Number Setting via the PROG Pin

PROG Pin to GND Resistor (1%)	Battery Cell Number
0 to 1kΩ	2 cells
6.19kΩ to 8.06kΩ	3 cells
15.4kΩ to 20kΩ	4 cells

Current Monitoring via the IAM and IBM Pins

The IC has an IBM pin to obtain the real-time battery current in both charge mode and discharge mode. The IBM voltage (V_{IBM}) is a fraction of the charge current. V_{IBM} indicates whether the current is following into or out of the battery. V_{IBM} has a 200mV offset and configurable battery current gain (0.1V/A or 0.05V/A). The gain can be configured via REG17h, bit[8]. V_{IBM} can be estimated with Equation (2):

$$V_{IBM} = I_{BATT} \times Gain + 0.2V \quad (2)$$

Similarly to the IBM pin, the IAM pin obtains the real-time input current in charge mode (I_{IN}) and output current in source mode (I_{IN_OUT}). The IAM pin's voltage (V_{IAM}) also has a 0.2V offset and configurable current gain (0.2V/A or 0.1V/A). The gain can be configured via REG17h, bit[7]. V_{IAM} can be calculated with Equation (3):

$$V_{IAM} = I_{IN} \times Gain + 0.2V \quad (3)$$

Two-Level Input Current Limit

The input current limit has two steps: I_{IN_LIM1} for the lower limit, and I_{IN_LIM2} for the higher limit. I_{IN_LIM2} can only last for t_{IIN_LIM2} and repeat once every t_{ADP_PERIOD}. Figure 11 shows the two current-limit levels, as well as the time durations for t_{ADP_PERIOD} and t_{IIN_LIM2}.

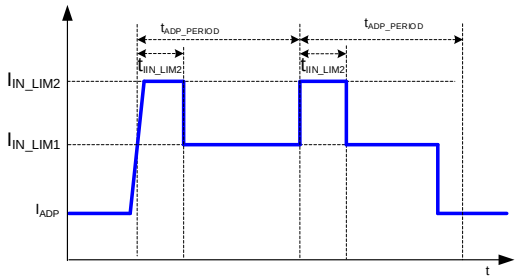

Figure 11: Two-Level Input Current Limit

The two-level current limit function has an enable control bit (REG12h, bit[3]). When it is disabled, the input current limit is determined by I_{IN_LIM1}, regardless of the I_{IN_LIM2} setting; when it is enabled, the device utilizes the input adapter surge capability to extend battery life. I_{IN_LMT1} and I_{IN_LMT2} can be configured via the I²C register REG0Ah. t_{ADP_PERIOD} and t_{IIN_LIM2} can be configured via the I²C register REG18h.

System Power Monitor Analog Output (PSYS)

The IC has a PSYS pin to monitor the real-time system power. The PSYS pin provides a current signal proportional to the total power consumed by the platform, and it can be calculated with Equation (4):

$$P_{SYS} = P_{SYS\text{-}GAIN} \times (V_{IN} \times I_{IN} + V_{BATT} \times I_{BATT}) \quad (4)$$

Where V_{IN} is the adapter voltage, I_{IN} is the adapter current, V_{BATT} is the battery voltage, and I_{BATT} is the battery current. When the battery is charged, I_{BATT} is a negative value. PSYS is an analog-controlled current source output that is proportional to the system power. The gain (P_{SYS_GAIN}) can be configured via REG1Ah, bits[4:3]. The PSYS function is enabled automatically when V_{IN} is present, and it can be disabled via REG16h, bit[1] in battery-only mode.

V_{MIN} Active Protection (VAP) in Battery-Only Mode

In battery-only mode, when there is no external load connected to the USB OTG port, the MP2764 can charge the input capacitor to store energy while the system works with normal power loads. During the system's high-power spike, the energy stored in the input capacitor supplies the system to prevent V_{SYS} from dropping below the minimum system voltage.

VAP can be enabled when REG13h, bit[15] = 1 and the OTG pin is pulled high. The input capacitor's regulated voltage is set via REG0Bh, bits[11:0].

Processor Hot Interrupt (PROCHOT)

The IC continuously monitors the input current, battery discharge current, system voltage, input source presence, and whether the battery is present. The PROCHOT pin is pulled low if any of the following conditions occur:

- $I_{IN} > I_{IN_PHOT2}$
- $V_{IN} < V_{IN_MIN}$
- $I_{BAT} > I_{BAT_OC}$

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- $V_{SYS} < V_{SYS_UV}$
- Adapter plug-out
- Battery plug-out

All of these $\overline{PROCHOT}$ events can be enabled/disabled with their respective control bit.

Host Mode and Default Mode

The IC is a host-controlled device. After POR, the IC starts in the watchdog timer expiration state, or its default mode. All registers revert to their default settings. Any write to the IC is transmitted to host mode. All the device parameters can be configured by the host.

To keep the device in host mode when the watchdog timer is enabled, the host must reset the watchdog timer regularly by writing 1 to REG1Dh, bit[0] before the watchdog timer expires. The IC goes back to its default mode once the watchdog timer expires.

The MP2764 has OTP memory to configure the default values of certain registers while they are assembled in the factory.

I²C/SMBus Interface

The IC uses an I²C-compatible interface for flexible charging parameter setting and instantaneous device status reporting. The I²C is a 2-wire serial interface with two required bus lines: a serial data line (SDA) and a serial clock line (SCL). Both the SDA and SCL lines are open-drain and must be connected to the positive supply voltage via a pull-up resistor.

The IC operates as a target device, receiving control inputs from the initiator device, such as a microcontroller. The SCL line is always driven by the initiator device. The I²C interface supports standard mode (up to 100kbps) and fast mode (up to 400kbps).

All transactions begin with a start (S) command and are terminated by a stop (P) command (see Figure 12). Start and stop commands are always generated by the initiator. A high to low transition on the SDA line while SCL is high defines a start command. A low to high transition on the SDA line when the SCL is high defines a stop command.

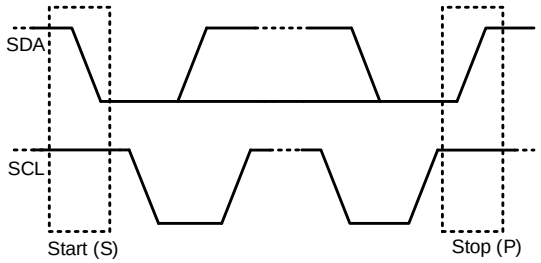

Figure 12: Start and Stop Commands

For data validity, the data on the SDA line must be stable during the high period of the clock. The high or low state of the SDA line can only change when the clock signal on the SCL line is low. Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Data is transferred with the most significant bit (MSB) first.

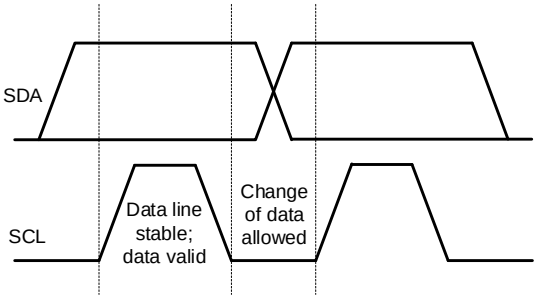

Figure 13: Bit Transfer on the I²C Bus

Each byte has to be followed by an acknowledge (ACK) bit, which is generated by the receiver to signal to the transmitter that the byte was successfully received.

The ACK signal is defined as follows: the transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line low and it remains low during the high period of the 9th clock.

If SDA line is high during the 9th clock, this is defined as the not acknowledge (NACK) signal. The initiator can then generate either a stop command to abort the transfer or a repeated start (Sr) command to start a new transfer.

After the start signal, a target address is sent. This address is 7 bits long, followed by the 8th bit as a data direction bit (R/W bit). A 0 indicates a transmission (write), and a 1 indicates a request for data (read).

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Figure 14 shows the address bit arrangement.

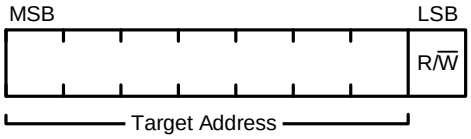


Figure 14: 7-Bit Addresses

Figure 15 shows the data transfer. Figure 16 on shows a single write transmission. Figure 17 shows a single read transaction.

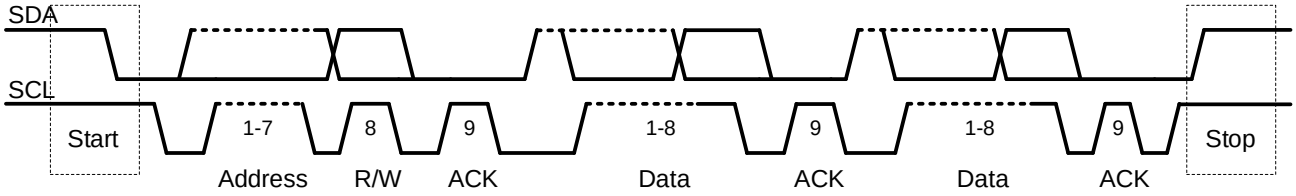
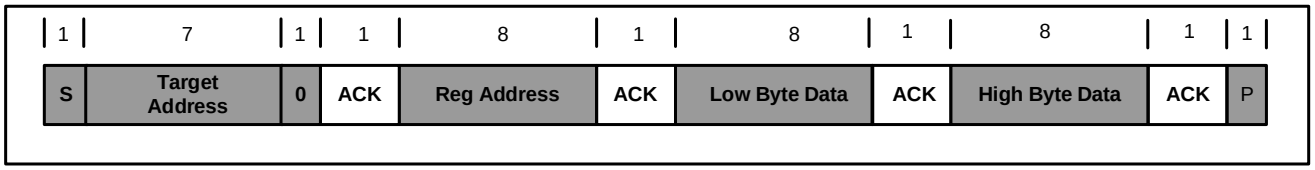


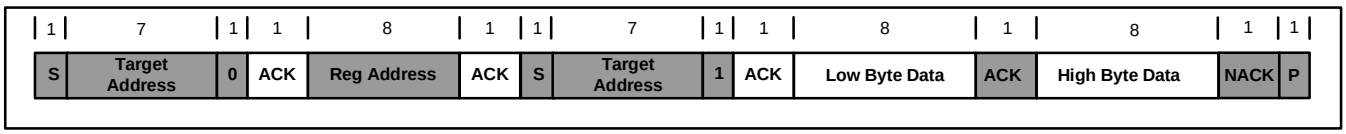
Figure 15: Data Transfer on the I²C Bus



From Initiator to Target A = Acknowledge (SDA Low) S = Start

From Target to Initiator /A = Not Acknowledge (SDA High) P = Stop

Figure 16: Single Write



From Initiator to Target A = Acknowledge (SDA Low) S = Start

From Target to Initator /A = Not Acknowledge (SDA High) P = Stop

Figure 17: Single Read

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REGISTER MAP

I²C Target Address: 5Ch

Legend: R/W = read/write; R = read-only

Register Name	Register Address	OTP	R/W	Description
REG07h	0x07	Yes	R/W	Sets the trickle, pre-charge, and termination charge current.
REG08h	0x08	Yes	R/W	Sets the input minimum voltage.
REG09h	0x09	Yes	R/W	Sets the minimum system voltage.
REG0Ah	0x0A	Yes	R/W	Sets the input current limit.
REG0Bh	0x0B	No	R/W	Sets the output voltage in source mode.
REG0Ch	0x0C	No	R/W	Sets the battery current and output current limit in source mode.
REG0Dh	0x0D	No	R/W	Sets the battery impedance compensation.
REG0Eh	0x0E	Yes	R/W	Configures the device (register 0).
REG0Fh	0x0F	No	R/W	Sets the JEITA NTC action.
REG10h	0x10	No	R/W	Sets the temperature protection parameters.
REG11h	0x11	Yes	R/W	Configures the device (register 1).
REG12h	0x12	Yes	R/W	Configures the device (register 2).
REG13h	0x13	Yes	R/W	Configures the device (register 3).
REG14h	0x14	Yes	R/W	Sets the fast charge current.
REG15h	0x15	Yes	R/W	Sets the battery regulation voltage.
REG16h	0x16	No	R/W	Configures the device (register 4).
REG17h	0x17	Yes	R/W	Configures the device (register 5).
REG18h	0x18	No	R/W	Sets the two-level input current limit.
REG19h	0x19	No	R/W	Configure PROCHOT (configuration 0).
REG1Ah	0x1A	No	R/W	Configure PROCHOT (configuration 1).
REG1Bh	0x1B	No	R/W	Configure PROCHOT (configuration 2).
REG1Ch	0x1C	No	R/W	Controls the $\overline{\text{INT}}$ mask.
REG1Dh	0x1D	No	W	Resets the WDT register.
REG1Eh	0x1E	No	W	Resets the registers.
REG1Fh	0x1F	No	R/W	Configures the battery lock register.
REG2Bh	0x2B	No	R/W	Sets the V_{IN_MIN} VAP threshold.
REG2Ch	0x2C	No	R/W	Sets the V_{SYS_REG} VAP threshold.
REG30h	0x30	No	R/W	Ultrasonic mode (USM) control.
REG43h	0x43	No	R	Returns the ADC result for the input voltage.
REG44h	0x44	No	R	Returns the ADC results for the input current.
REG45h	0x45	No	R	Returns the ADC results for the battery voltage per cell.
REG46h	0x46	No	R	Returns the ADC results for the system voltage.
REG47h	0x47	No	R	Returns the ADC results for the charge current.
REG48h	0x48	No	R	Returns the ADC results for the junction temperature.
REG49h	0x49	No	R	Returns the ADC results for the output voltage in source mode.
REG4Ah	0x4A	No	R	Returns the ADC results for the output current in source mode.
REG4Bh	0x4B	No	R	Returns the ADC results for the battery discharge current.
REG4Ch	0x4C	No	R	Returns the status and faults information (register 0).
REG4Dh	0x4D	No	R	Returns the status and faults information (register 1).
REG4Eh	0x4E	No	R	Returns the faults status of the latch register.

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REG07h

The REG07h register sets the charge current, including the trickle charge current, the pre-charge current, and the charge termination current.

Bits	Access	Bit Name	Default	Description
15:12	N/A	RESERVED	0	Reserved. Do not change these bit values.
11	R/W	I_{TC}[3]	0	Sets the trickle charge current (I_{TC}). The default can be configured via the OTP. Range: 0mA to 937.5mA Default: 250mA (0100) LSB: 62.5mA I_{TC} = DEC(Bits[11:8]) x 62.5 (mA)
10	R/W	I_{TC}[2]	1	
9	R/W	I_{TC}[1]	0	
8	R/W	I_{TC}[0]	0	
7	R/W	I_{PRE}[3]	0	Sets the pre-charge current (I_{PRE}). The default can be configured via the OTP. Range: 0mA to 1875mA Default: 250mA (0010) LSB: 125mA I_{PRE} = DEC(Bits[7:4]) x 125 (mA)
6	R/W	I_{PRE}[2]	0	
5	R/W	I_{PRE}[1]	1	
4	R/W	I_{PRE}[0]	0	
3	R/W	I_{TERM}[3]	0	Sets the termination current (I_{TERM}). Range: 62.5mA to 468.75mA Default: 125mA LSB: 31.25mA I_{TERM} = DEC(Bits[3:0]) x 31.25 (mA)
2	R/W	I_{TERM}[2]	1	
1	R/W	I_{TERM}[1]	0	
0	R/W	I_{TERM}[0]	0	

REG08h

The REG08h register sets the input minimum voltage limit.

Bits	Access	Bit Name	Default	Description
15:9	N/A	RESERVED	0	Reserved. Do not change these bit values.
8	R/W	V_{IN_MIN}[8]	0	Sets the minimum input voltage (V_{IN_MIN}). The default can be configured via the OTP. Range: 0mV to 22000mV Default: 4500mV LSB: 50mV V_{IN_MIN} = DEC(Bits[8:0]) x 50 (mV)
7	R/W	V_{IN_MIN}[7]	0	
6	R/W	V_{IN_MIN}[6]	1	
5	R/W	V_{IN_MIN}[5]	0	
4	R/W	V_{IN_MIN}[4]	1	
3	R/W	V_{IN_MIN}[3]	1	
2	R/W	V_{IN_MIN}[2]	0	
1	R/W	V_{IN_MIN}[1]	1	
0	R/W	V_{IN_MIN}[0]	0	

REG09h

The REG09h register sets V_{TRACK} and the minimum system voltage per cell in NVDC power path management control. The minimum system voltage is regulated at (V_{SYS_MIN} + V_{TRACK}) x BAT_NUM.

Bits	Access	Bit Name	Default	Description
15:9	N/A	RESERVED	0	Reserved. Do not change these bit values.
8	R/W	V_{TRACK}[2]	1	Sets the track voltage (V_{TRACK}) per cell for NVDC power path management control. Range: 0mV/cell (000) to 175mV/cell (111) Default: 100mV/cell LSB: 25mV/cell V_{TRACK}/Cell = DEC(Bits[8:6]) x 25 (mV)
7	R/W	V_{TRACK}[1]	0	
6	R/W	V_{TRACK}[0]	0	

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5	R/W	V_{SYS_MIN}[5]	0	Sets the minimum system voltage (V_{SYS_MIN}) per cell for NVDC power path management control. The default be configured via the OTP. Range: 0mV/cell to 4800mV/cell Default: 3000mV/cell LSB: 100mV/cell V_{SYS_MIN}/cell = DEC(Bits[5:0]) x 100 (mV)
4	R/W	V_{SYS_MIN}[4]	1	
3	R/W	V_{SYS_MIN}[3]	1	
2	R/W	V_{SYS_MIN}[2]	1	
1	R/W	V_{SYS_MIN}[1]	1	
0	R/W	V_{SYS_MIN}[0]	0	

REG0Ah

The REG0Ah register sets the input current limit. When two-level current limiting is enabled, the I_{IN_LIM1} and I_{IN_LIM2} settings are all valid; otherwise, only I_{IN_LIM1} is valid.

Bits	Access	Bit Name	Default	Description
15	R/W	I_{IN_LIM2}[7]	1	Sets the second level for the input current limit (I_{CCIN_LIM2}). The default can be configured via the OTP. Range: 0mA to 7000mA Default: 4500mA LSB: 31.25mA I_{IN_LIM2} = DEC(Bits[15:8]) x 31.25 (mA)
14	R/W	I_{IN_LIM2}[6]	0	
13	R/W	I_{IN_LIM2}[5]	0	
12	R/W	I_{IN_LIM2}[4]	1	
11	R/W	I_{IN_LIM2}[3]	0	
10	R/W	I_{IN_LIM2}[2]	0	
9	R/W	I_{IN_LIM2}[1]	0	
8	R/W	I_{IN_LIM2}[0]	0	
7	R/W	I_{IN_LIM1}[7]	0	Sets the first level for the input current limit (I_{CCIN_LIM1}). These bits can be configured via the OTP. Range: 0A (00000000) to 7A (11100000) Default: 3000mA (01100000) LSB: 31.25mA I_{IN_LIM1} = DEC(Bits[7:0]) x 31.25 (mA)
6	R/W	I_{IN_LIM1}[6]	1	
5	R/W	I_{IN_LIM1}[5]	1	
4	R/W	I_{IN_LIM1}[4]	0	
3	R/W	I_{IN_LIM1}[3]	0	
2	R/W	I_{IN_LIM1}[2]	0	
1	R/W	I_{IN_LIM1}[1]	0	
0	R/W	I_{IN_LIM1}[0]	0	

REG0Bh

The REG0Bh register sets the output voltage at the IN port in reverse source mode.

Bits	Access	Bit Name	Default	Description
15:12	N/A	RESERVED	0	Reserved. Do not change these bit values.
11	R/W	V_{IN_SRC}[11]	0	Sets the output voltage in source mode (V_{IN_SRC}). Range: 4000mV to 21000mV Default: 5000mV LSB: 6.25mV V_{IN_SRC} = DEC(Bits[11:0]) x 6.25 (mV)
10	R/W	V_{IN_SRC}[10]	0	
9	R/W	V_{IN_SRC}[9]	1	
8	R/W	V_{IN_SRC}[8]	1	
7	R/W	V_{IN_SRC}[7]	0	
6	R/W	V_{IN_SRC}[6]	0	
5	R/W	V_{IN_SRC}[5]	1	
4	R/W	V_{IN_SRC}[4]	0	
3	R/W	V_{IN_SRC}[3]	0	
2	R/W	V_{IN_SRC}[2]	0	
1	R/W	V_{IN_SRC}[1]	0	
0	R/W	V_{IN_SRC}[0]	0	

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REG0Ch

The REG0Ch register sets the battery current limit and output current limit in source mode.

Bits	Access	Bit Name	Default	Description
15	R/W	I_{BATT_DISCHG}[7]	1	Sets the battery discharge current limit (I_{BATT_DISCHG}) in source mode. Range: 0mA to 14000mA Default: 8000mA LSB: 62.5mA I_{BATT_DISCHG} = DEC(Bits[15:8]) x 62.5 (mA)
14	R/W	I_{BATT_DISCHG}[6]	0	
13	R/W	I_{BATT_DISCHG}[5]	0	
12	R/W	I_{BATT_DISCHG}[4]	0	
11	R/W	I_{BATT_DISCHG}[3]	0	
10	R/W	I_{BATT_DISCHG}[2]	0	
9	R/W	I_{BATT_DISCHG}[1]	0	
8	R/W	I_{BATT_DISCHG}[0]	0	
7	N/A	RESERVED	0	Reserved. Do not change this bit value.
6	R/W	I_{IN_SRC}[6]	0	Sets the output current limit in source mode. Range: 0mA to 5000mA Default: 2500mA. LSB: 62.5mA I_{IN_SRC}= DEC(Bits[6:0]) x 62.5 (mA)
5	R/W	I_{IN_SRC}[5]	1	
4	R/W	I_{IN_SRC}[4]	0	
3	R/W	I_{IN_SRC}[3]	1	
2	R/W	I_{IN_SRC}[2]	0	
1	R/W	I_{IN_SRC}[1]	0	
0	R/W	I_{IN_SRC}[0]	0	

REG0Dh

The REG0Dh register sets the battery impedance compensation parameters and thermal regulation threshold.

Bits	Access	Bit Name	Default	Description
15:9	N/A	RESERVED	0	Reserved. Do not change these bit values.
8	R/W	R_BATT[2]	0	Sets the predicted battery impedance. Range: 0mΩ/cell to 175mΩ/cell Default: 0mΩ/cell LSB: 25mΩ/cell R_{BATT}/Cell = DEC(Bits[8:6]) x 25 (mΩ)
7	R/W	R_BATT[1]	0	
6	R/W	R_BATT[0]	0	
5	R/W	V_{CLAMP}[2]	0	Sets the maximum compensation voltage for the battery-full voltage according to the battery impedance. Range: 0mV/cell to 210mV/cell Default: 0mV/cell LSB: 30mV/cell V_{CLAMP}/cell = DEC(Bits[5:3]) x 30 (mV)
4	R/W	V_{CLAMP}[1]	0	
3	R/W	V_{CLAMP}[0]	0	
2	R/W	$T_{J_REG_EN}$	1	Enables the thermal regulation loop. 0: Disabled 1: Enabled (default)
1	R/W	T_{J_REG}[1]	1	Sets the junction temperature's regulation threshold. 00: 60°C 01: 80°C 10: 100°C 11:120°C (default)
0	R/W	T_{J_REG}[0]	1	

REG0Eh

The REG0Eh register provides some control bits.

Bits	Access	Bit Name	Default	Description
15	N/A	RESERVED	0	Reserved. Do not change this bit value.

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14	R/W	BFET_OC_ACT	0	Determines the BATFET behaviors when the discharge current exceeds the over-current protection (OCP) threshold in battery-only mode. The default can be configured via the OTP. 0: Stays on (default) 1: Hiccup mode
13	R/W	V_{RECH}	1	Configures the battery recharge threshold. V_{RECH} is invalid if charge termination is disabled. 0: 100mV/cell 1: 200mV/cell (default)
12	R/W	$I_{IN_SRC_LOOP_EN}$	1	Enables the output current loop in source mode. 0: Disabled 1: Enabled (default)
11	R/W	$I_{BATT_DSCHG_EN}$	0	Enables the battery discharge current loop in source mode. 0: Disabled (default) 1: Enabled
10	R/W	$I_{IN_LIM_EN}$	1	Enables the input current loop in charge mode. 0: Disabled 1: Enabled (default)
9	R/W	$V_{BATT_LOW_EN}$	0	Enables battery low-voltage protection in source mode. 0: Disabled (default) 1: Enabled
8	R/W	$V_{BATT_LOW_ACT}$	0	Configures the action when $V_{BATT} < V_{BATT_LOW}$ in source mode. 0: Only generate an $\overline{INT}$ to inform the host (default) 1: Generate $\overline{INT}$ and latch the DC/DC converter off
7	R/W	V_{BATT_LOW}[1]	0	Sets the battery low-voltage protection falling threshold in source mode. The hysteresis is 250mV. 00: 2.8V/cell 01: 2.8V/cell (default) 10: 3V/cell 11: 3.1V/cell
6	R/W	V_{BATT_LOW}[0]	1	
5	R/W	$V_{BATT_UV_EN}$	1	Enables battery under-voltage (UV) protection in both charge and source mode. When this bit is enabled and the battery's UV threshold is reached, the BATFET turns off in charge supplement mode, and the DC/DC converter turns off in source mode. The default can be configured via the OTP. 0: Disabled 1: Enabled (default)
4	R/W	V_{BATT_PRE}[2]	1	Sets the pre-charge to linear CC charge transition threshold. The default can be configured via the OTP. 000: 2.2V/cell 001: 2.4V/cell 010: 2.5V/cell 011: 2.6V/cell 100: 2.8V/cell 101: 3V/cell (default) 110: 3.2V/cell 111: 3.4V/cell
3	R/W	V_{BATT_PRE}[1]	0	
2	R/W	V_{BATT_PRE}[0]	1	

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1	R/W	$I_{IN_OC_EN}$	0	Enables input over-current protection (OCP) in charge mode. After I_{IN} > I_{IN_OCP} (set via REG1Ah, bit[8]) for 100µs, the DC/DC converter is disabled then restarts after 300ms. The default can be configured via the OTP. 0: Disabled (default) 1: Enabled
0	R/W	$I_{BATT_OC_EN}$	1	Enables battery OCP in source mode. After I_{BATT} > I_{BATT_OC} for 100µs, the DC/DC converter is disabled and restarts after 300ms. The BATFET stays on to power the system. The default can be configured via the OTP. 0: Disabled 1: Enabled (default)

REG0Fh

The REG0Fh register sets the JEITA actions for hot, warm, cool, and cold protection.

Bits	Access	Bit Name	Default	Description
15:8	N/A	RESERVED	0	Reserved. Do not change this bit value.
7	R/W	WARM_ACT[1]	0	Configures the charging action for NTC warm protection. 00: No action 01: Only reduce V_{BATT_REG} (default) 10: Only reduce I_{CC} 11: Reduce both V_{BATT_REG} and I_{CC}
6	R/W	WARM_ACT[0]	1	
5	R/W	COOL_ACT[1]	1	Configures the charging action for NTC cool protection. 00: No action 01: Only reduce V_{BATT_REG} 10: Only reduce I_{CC} (default) 11: Reduce both V_{BATT_REG} and I_{CC}
4	R/W	COOL_ACT[0]	0	
3	R/W	JEITA_VSET[0]	0	Configures how much V_{BATT_REG} is reduced by when NTC warm or cool protection occurs. 00: -100mV/cell (default) 01: -150mV/cell 10: -200mV/cell 11: -250mV/cell
2	R/W	JEITA_VSET[1]	0	
1	R/W	JEITA_ISET[0]	0	Configures the charge current for NTC warm or cool protection. 00: 1/2 x I_{CC} (default) 01: 1/4 x I_{CC} 10: 1/8 x I_{CC} 11: Disabled charge
0	R/W	JEITA_ISET[0]	0	

REG10h

The REG10h register sets the JEITA temperature thresholds.

Bits	Access	Bit Name	Default	Description
15:10	N/A	RESERVED	0	Reserved. Do not change these bit values.
9	R/W	NTC_EN	1	Enables NTC protection. When disabled, no action is taken when NTC/VNTC is out of the warm/cool/cold/hot range. 0: Disabled 1: Enabled (default)

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8	R/W	NTC_ACT	1	Configures the IC behavior after an NTC fault occurs. 0: Only deliver $\overline{INT}$ in cold and hot windows 1: Deliver $\overline{INT}$ and take corresponding JEITA actions (default)
7	R/W	V_{HOT}[1]	1	Configures the NTC hot protection thresholds. 00: 37.89% (50°C) 01: 35.43% (55°C) 10: 33.35% (60°C) (default) 11: 31.32% (65°C)
6	R/W	V_{HOT}[0]	0	
5	R/W	V_{WARM}[1]	0	Configures the NTC warm protection thresholds. 00: 43.69% (40°C) 01: 40.8% (45°C) (default) 10: 37.89% (50°C) 11: 35.43% (55°C)
4	R/W	V_{WARM}[0]	1	
3	R/W	V_{COOL}[1]	1	Configures the NTC cool protection thresholds. 00: 75.43% (0°C) 01: 71.34% (5°C) 10: 67.12% (10°C) (default) 11: 62.85% (15°C)
2	R/W	V_{COOL}[0]	0	
1	R/W	V_{COLD}[1]	0	Configures the NTC cold protection thresholds. 00: 79.29% (-5°C) 01: 75.43% (0°C) (default) 10: 71.34% (5°C) 11: 67.12% (10°C)
0	R/W	V_{COLD} [0]	1	

REG11h

The REG11h register controls some protections.

Bits	Access	Bit Name	Default	Description
15:14	N/A	RESERVED	0	Reserved. Do not change these bit values.
13	R/W	LOW_PWR_EN	0	Enables the minimum battery quiescent current in battery-only mode by turning off battery discharge current detection. 0: Disabled (default) 1: Enabled
12	R/W	BGATE_HIZ	0	Enables BGATE_HIZ. 0: Disable Hi-Z (enable BGATE driver) (default) 1: Enable Hi-Z (disable BGATE driver)
11	R/W	FORCE_BFET_OFF	0	Turns off the battery FET (BGATE to GND). 0: Disabled (default) 1: Enabled
10	R/W	SRC_UV_SWAP_EN	0	Sets the source mode start-up condition When this bit is enabled, an output under-voltage (UV) condition is used as an essential condition to enable source mode. 0: Disabled (default) 1: Enabled
9	R/W	SRC_FAST_ON_EN	0	Sets the deglitch time between forward charge mode and reverse source mode and shortens the soft-start time to a minimum. 0: Disabled (default) 1: Enabled

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8	R/W	IBATT_DSCHG_OCP_TH	0	Sets the battery discharge over-current protection (OCP) threshold in both supplement and source mode. 0: 20A (default) 1: 12A
7	R/W	IBATT_DSCHG_OCP_DGL	0	Sets the turn-off time for BATFET hiccup mode when battery discharge OCP occurs in supplement mode. 0: 100ms (default) 1: 51µs
6	R/W	ADC_EN	0	In battery-only mode, when this bit is enabled, the ADC turns on. When the DC/DC converter is enabled, the ADC is enabled and automatically ignores this bit. 0: Disabled (default) 1: Enabled
5	R/W	SYS_OVP_EN	1	Enables system over-voltage protection (OVP). When this bit is enabled, the DC/DC converter turns off when system OVP occurs. The default can be configured via the OTP. 0: Disabled 1: Enabled (default)
4	R/W	BATT_OVP_EN	0	Determines whether to turn off BATFET when battery OVP occurs. When enabled, the BATFET turns off; when disabled, the BATFET stays on. The default can be configured via the OTP. 0: Disabled (default) 1: Enabled
3	R/W	SYS_SCP_EN	1	When V_{SYS} < 2V, the DC/DC converter enters hiccup mode with a 300ms period. The default can be configured via the OTP. 0: Disabled 1: Enabled (default)
2	R/W	SRC_SCP_EN	1	Enables output short-circuit protection (SCP) in source mode. When SCP occurs, the DC/DC converter enters hiccup mode with a 300ms period. The default can be configured via the OTP. 0: Disabled 1: Enabled (default)
1	R/W	WEAK_SOURCE_EN	1	Enables the weak source auto shutdown function. When enabled, the DC/DC converter turns off when the V_{IN_MIN} threshold is reached and the input current is below 200mA. The default can be configured via the OTP. 0: Disabled 1: Enabled (default)
0	R/W	TMR_EN	1	Enables the charge safety timer. The default can be configured via the OTP. 0: Disabled 1: Enabled (default)

REG12h

The REG12h register configures discharge protections and thresholds.

Bits	Access	Bit Name	Default	Description
15:13	N/A	RESERVED	0	Reserved. Do not change these bit values.

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12	R/W	TERM_EN	1	Enables charge termination. 0: Disabled 1: Enabled (default)
11	R/W	WDT[1]	0	Configures the watchdog timer. The default can be configured via the OTP. 00: Disabled (default) 01: 40s 10: 80s 11: 160s
10	R/W	WDT[0]	0	
9	R/W	RESERVED	0	Reserved. Do not change this bit value.
8	R/W	BATT_DSCHG_EN	0	Enables the dummy load at the BATT terminal. When it is enabled, the dummy load turns on automatically when battery over-voltage protection (OVP) occurs. 0: Disabled (default) 1: Enabled
7	R/W	IN_DSCHG_EN	0	Enables the dummy load at the IN terminal. When this bit is set to 0, the dummy load is always turned off. When this bit is set to 1, the dummy load turns on when source mode (SRC) OVP occurs or V_{IN_MIN} reaches its threshold and I_{IN} is below 200mA. 0: Disabled (default) 1: Enabled
6	R/W	RESERVED	0	Reserved. Do not change this bit value.
5	N/A	RESERVED	0	Reserved. Do not change this bit value.
4	N/A	RESERVED	0	Reserved. Do not change this bit value.
3	R/W	TWO_INLIM_EN	0	Enables the two-level input current limit. The default can be configured via the OTP. 0: Disabled (default) 1: Enabled
2	R/W	VSYS_OV	1	Configures the system OV threshold. It is defined as a percentage that refers to the system regulation voltage. The default can be configured via the OTP. 0: 110% 1: 106% (default)
1	R/W	SRC_OV	0	Configures the output OVP threshold in source mode. It is defined as a percentage that refers to the source regulation voltage. The default can be configured via the OTP. 0: 110% (default) 1: 106%
0	R/W	VIN_OVP_DGL	1	Configures the input OVP deglitch time. The default can be configured via the OTP. 0: 1μs 1: 10ms (default)

REG13h

The REG13h register configures charge control and the charge timer.

Bits	Access	Bit Name	Default	Description
15:10	N/A	RESERVED	0	Reserved. Do not change these bit values.

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9	R/W	CHG_TMR[3]	1	Configures the CC/CV charge safety timer. Range: 0 hours to 30 hours Default: 20 hours LSB: 2 hours CHG_TMR = DEC(Bits[9:6]) x 2 (hours)
8	R/W	CHG_TMR[2]	0	
7	R/W	CHG_TMR[1]	1	
6	R/W	CHG_TMR[0]	0	
5	R/W	OTG_VAP_SEL	1	Configures the OTG pin's function. When this bit is set to 0, it is used to control V_{MIN} Active protection (VAP); when this bit is set to 1, it is used to control On-the-Go (OTG) mode. 0: VAP 1: OTG (default)
4	R/W	SRC_EN	0	Enables source mode. 0: Disabled (default) 1: Enabled
3	R/W	RESERVED	0	Reserved. Do not change this bit value.
2	R/W	CLK_EN	0	Forcefully enables the system clock in battery-only mode. 0: Disabled (default) 1: Enabled
1	R/W	DCDC_EN	1	Enables the buck-boost converter. Bit[4] of this command overrides this control. The default can be configured via the OTP. 0: Disabled 1: Enabled (default)
0	R/W	CHG_EN	1	Enables charge mode. The default can be configured via the OTP. 0: Disabled 1: Enabled (default)

REG14h

The REG14h register sets the fast constant current (CC) charge current.

Bits	Access	Bit Name	Default	Description
15:13	N/A	RESERVED	0	Reserved. Do not change these bit values.
12	R/W	I_{CC_LNR}[4]	0	Sets the charge current in linear mode when V_{BATT} < $V_{SYS_REG_MIN}$. The default can be configured via the OTP. Range: Up to 3.875A Default: 250mA LSB: 125mA I_{CC_LNR} = DEC(Bits[12:8]) x 125 (mA)
11	R/W	I_{CC_LNR}[3]	0	
10	R/W	I_{CC_LNR}[2]	0	
9	R/W	I_{CC_LNR}[1]	1	
8	R/W	I_{CC_LNR}[0]	0	
7	R/W	I_{CC}[7]	0	Sets the charge current in switching mode when V_{BATT} > $V_{SYS_REG_MIN}$. The default can be configured via the OTP. Range: Up to 8A Default: 3A LSB: 62.5mA I_{CC} = DEC(Bits[7:0]) x 62.5 (mA)
6	R/W	I_{CC}[6]	0	
5	R/W	I_{CC}[5]	1	
4	R/W	I_{CC}[4]	1	
3	R/W	I_{CC}[3]	0	
2	R/W	I_{CC}[2]	0	
1	R/W	I_{CC}[1]	0	
0	R/W	I_{CC}[0]	0	

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REG15h

The REG15h register sets the battery-full regulation voltage.

Bits	Access	Bit Name	Default	Description
15:10	N/A	RESERVED	0	Reserved. Do not change these bit values.
9	R/W	V_{BATT_REG}[9]	1	Sets the battery-full regulation voltage per cell. The default can be configured via the OTP. Range: Up to 4.8V/cell Default: 4.2V/cell LSB: 5mV/cell V_{BATT_REG}/cell = DEC(Bits[9:0]) x 5 (mV)
8	R/W	V_{BATT_REG}[8]	1	
7	R/W	V_{BATT_REG}[7]	0	
6	R/W	V_{BATT_REG}[6]	1	
5	R/W	V_{BATT_REG}[5]	0	
4	R/W	V_{BATT_REG}[4]	0	
3	R/W	V_{BATT_REG}[3]	1	
2	R/W	V_{BATT_REG}[2]	0	
1	R/W	V_{BATT_REG}[1]	0	
0	R/W	V_{BATT_REG}[0]	0	

REG16h

The REG16h register sets some monitor controls.

Bits	Access	Bit Name	Default	Description
15:6	N/A	RESERVED	0	Reserved. Do not change these bit values.
5	R/W	SYS_UV_PROCHOT_CMP_EN	0	Enables the $\overline{\text{PROCHOT}}$ system's under-voltage (UV) comparator in battery-only mode. 0: Disabled (default) 1: Enabled
4	N/A	RESERVED	1	Reserved. Do not change this bit value.
3:2	N/A	RESERVED	0	Reserved. Do not change these bit values.
1	R/W	PSYS_EN	0	Enables the PSYS measurement circuit in battery-only mode. 0: Disabled (default) 1: Enabled
0	R/W	IBM_EN	0	Enables the battery current monitor buffer in battery-only mode. 0: Disabled (default) 1: Enabled

REG17h

The REG17h register sets the frequency and controls the battery cell number.

Bits	Access	Bit Name	Default	Description
15:11	N/A	RESERVED	0	Reserved. Do not change these bit values.
10	R/W	I2C_TWO_EN	0	When this bit is enabled, if the SMBus clock (CLK) stays low for longer than 25ms, the SMBus state machine resets. In battery-only mode, REG13h, bit[2] should also be enabled when this function is needed. 0: Disabled (Default) 1: Enabled
9	R/W	WD_RUN_ONLY_BATT	0	Enables the watchdog timer when only the battery is connected. This bit is only valid when the watchdog is enabled. 0: Disabled (default) 1: Enabled

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8	R/W	IBATT_GAIN	0	Provides an additional option to reduce the gain by half to support a higher battery current. 0: x1 (10V/V, 20V/V) (default) 1: x0.5 (5V/V, 10V/V)
7	R/W	IN_GAIN	0	Provides an additional option to reduce the gain by half to support a higher input current. 0: x1 (20V/V, 40V/V) (default) 1: x0.5 (10V/V, 20V/V)
6	R/W	SW_FREQ[2]	0	Configures the frequency of the DC/DC converter. The default can be configured via the OTP. 010: 450kHz 011: 540kHz (default) 100: 700kHz 101: 860kHz
5	R/W	SW_FREQ[1]	1	
4	R/W	SW_FREQ[0]	1	
3	R/W	IIN_RSENSE_SEL	0	Configures the current-sense gain of the input current. The default can be configured via the OTP. 0: 20V/V (10mΩ) (default) 1: 40V/V (5mΩ)
2	R/W	IBATT_RSENSE_SEL	0	Configures the current-sense gain of the battery current. The default can be configured via the OTP. 0: 10V/V (10mΩ) (default) 1: 20V/V (5mΩ)
1	R/W	BAT_NUM[1]	0	Configures the battery cell count in series. The default can be configured via the OTP. 00: 2-cell 01: 3-cell (default) 10: 4-cell
0	R/W	BAT_NUM[0]	1	

REG18h

The REG18h register sets two-level current limit related timings.

Bits	Access	Bit Name	Default	Description
15	N/A	RESERVED	0	Reserved. Do not change these bit values.
14	R/W	t_{ADP_PERIOD}[6]	1	Configures the total time duration of the second and first input current limit. Range: 0ms to 25.4ms Default: 20ms (Default) LSB: 0.2ms t_{ADP_PERIOD} = DEC(Bits[14:8]) x 0.2 (ms)
13	R/W	t_{ADP_PERIOD}[5]	1	
12	R/W	t_{ADP_PERIOD}[4]	0	
11	R/W	t_{ADP_PERIOD}[3]	0	
10	R/W	t_{ADP_PERIOD}[2]	1	
9	R/W	t_{ADP_PERIOD}[1]	0	
8	R/W	t_{ADP_PERIOD}[0]	0	
7	N/A	RESERVED	0	Reserved. Do not change this bit value.
6	R/W	t_{IN_LIM2}[6]	0	Configures the max duration time to allow the input current limit to change from the IINLIMIT1 to IINLIMIT2 setting within t_{ADP_PERIOD}. Rang: 0ms to 25.4ms Default: 1.2ms LSB: 0.2ms t_{IN_LIM2} = DEC(Bits[6:0]) x 0.2 (ms)
5	R/W	t_{IN_LIM2}[5]	0	
4	R/W	t_{IN_LIM2}[4]	0	
3	R/W	t_{IN_LIM2}[3]	0	
2	R/W	t_{IN_LIM2}[2]	1	
1	R/W	t_{IN_LIM2}[1]	1	
0	R/W	t_{IN_LIM2}[0]	0	

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REG19h

The REG19h register sets the PROCHOT related parameters.

Bits	Access	Bit Name	Default	Description
15	R/W	$V_{SYS_UV_PROCHOT}$[5]	0	Configures the system's under-voltage (UV) threshold for a PROCHOT interrupt. Offset: 4.5V Range: 4.5V to 9V Default: 5.4V LSB: 100mV $V_{SYS_UV_PROCHOT}$ = DEC(Bits[15:10]) x 100 (mV)
14	R/W	$V_{SYS_UV_PROCHOT}$[4]	0	
13	R/W	$V_{SYS_UV_PROCHOT}$[3]	1	
12	R/W	$V_{SYS_UV_PROCHOT}$[2]	0	
11	R/W	$V_{SYS_UV_PROCHOT}$[1]	0	
10	R/W	$V_{SYS_UV_PROCHOT}$[0]	1	
9	R/W	$t_{IIN_PHOT2_DEGL}$[1]	0	Configures the deglitch time during which the input current can exceed I_{IN_PHOT2} before outputting PROCHOT. 00: 15µs (default) 01: 100µs 10: 400µs 11: 800µs
8	R/W	$t_{IIN_PHOT2_DEGL}$[0]	0	
7	R/W	$t_{IBATT_OC_DEGL}$[1]	0	Configures the deglitch time during where a battery over-current (OC) condition can exist before outputting PROCHOT. 00: 100µs (default) 01: 2ms 10: 5ms 11: 10ms
6	R/W	$t_{IBATT_OC_DEGL}$[0]	0	
5	R/W	$t_{PROCHOT_DUR}$[2]	0	Configures the duration of the low state for the PROCHOT output. 000: 0.1ms 001: 0.5ms 010: 1ms 011: 2ms (default) 100: 5ms 101: 10ms 110: 20ms 111: 5s
4	R/W	$t_{PROCHOT_DUR}$[1]	1	
3	R/W	$t_{PROCHOT_DUR}$[0]	1	
2	R/W	$t_{DEGL_VSYS_UV}$	0	Configures the deglitch time during which a system under-voltage (UV) condition can exist before outputting PROCHOT. 0: 1µs (default) 1: 5µs
1	R/W	$t_{DEGL_VBAT_PLUG}$	0	Configures the deglitch time during which the battery can be removed before outputting PROCHOT. 0: 1µs (default) 1: 5µs
0	R/W	$t_{DEGL_VIN_PLUG}$	0	Configures the deglitch time during which input plug-out can occur before outputting PROCHOT. 0: 1µs (default) 1: 5µs

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REG1Ah

The REG1Ah register sets PROCHOT protection related parameters.

Bits	Access	Bit Name	Default	Description
15:13	N/A	RESERVED	0	Reserved. Do not change these bit values.
12	R/W	I_{IN_PHOT2}	0	Configures the threshold for IIN_PROT2; when I_{IN} exceeds this threshold, then this PROCHOT event is triggered. 0: 110% of IIN_LIM2 (default) 1: 150% of IIN_LIM2
11	N/A	RESERVED	0	Reserved. Do not change this bit value.
10	R/W	$t_{_DEGL_IIN_PHOT1}$	0	Configures the deglitch time for I_{IN} PROCHOT1. 0: 1ms (default) 1: 50ms
9	R/W	I_{IN_OC}	0	Sets the input over-current protection (OCP) threshold. When the input current exceeds this threshold for 100µs, the DC/DC converter can be shut down optionally via Reg1Ah, bit[10]. 0: 10A (default) 1: 20A
8	R/W	$t_{_IN_MAX1}$[1]	1	Configures the time limitation during which the input current can exceed the first input current limit but stay below the second input current limit. Once this limit is reached, a PROCHOT signal should assert. 00: 1s 01: 2s 10: 5s (default) 11: 10s
7	R/W	$t_{_IN_MAX1}$[0]	0	
6	R/W	$t_{_IN_MAX2}$[1]	0	Configures the time limitation during which the input current can stay at the second input current limit. Once this limit is reached, a PROCHOT signal should assert. 00: 1ms (default) 01: 2ms 10: 5ms 11: 10ms
5	R/W	$t_{_IN_MAX2}$[0]	0	
4	R/W	P_{SYS_GAIN}[1]	0	Configures the PSYS output current gain. 00/11: 1µA/W (default) 01: 0.25µA/W 10: 0.5µA/W
3	R/W	P_{SYS_GAIN}[0]	0	
2	R/W	$I_{BATT_PROCHOT}$[2]	1	Configures the battery OC threshold for a PROCHOT interrupt. 000: 6A 001: 8A 010: 10A 011: 12A 100: 14A 101: 16A 110: 18A 111: 20A (default)
1	R/W	$I_{BATT_PROCHOT}$[1]	1	
0	R/W	$I_{BATT_PROCHOT}$[0]	1	

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REG1Bh

The REG1Bh register sets the $\overline{\text{PROCHOT}}$ signal's control. When enabled, the $\overline{\text{PROCHOT}}$ signal asserts when the related event is triggered.

Bits	Access	Bit Name	Default	Description
15:9	N/A	RESERVED	0	Reserved. Do not change these bit values.
8	R/W	VAP_EXIT_PHOT_EN	1	Enables V_{MIN} active protection (VAP) to exit the $\overline{\text{PROCHOT}}$ output. 0: Disabled 1: Enabled (default)
7	R/W	I_{INLIM}_PHOT_EN	1	Enables the I_{INLIM} $\overline{\text{PROCHOT}}$ output. 0: Disabled 1: Enabled (default)
6	R/W	V_{IN_MIN}_PHOT_EN	1	Enables the V_{IN_MIN} $\overline{\text{PROCHOT}}$ output. 0: Disabled 1: Enabled (default)
5	R/W	BAT_OC_PHOT_EN	1	Enables the battery over-current (OC) $\overline{\text{PROCHOT}}$ output. 0: Disabled 1: Enabled (default)
4	R/W	IIN_PHOT2_EN	1	Enables the second input OC $\overline{\text{PROCHOT}}$ output. 0: Disabled 1: Enabled (default)
3	R/W	IIN_PHOT1_EN	1	Enables the first input OC $\overline{\text{PROCHOT}}$ output. 0: Disabled 1: Enabled (default)
2	R/W	V_{SYS_UV}_PHOT_EN	1	Enables the V_{SYS_UV} $\overline{\text{PROCHOT}}$ output. 0: Disabled 1: Enabled (default)
1	R/W	BATT_PRES_PHOT_EN	1	Enables the battery removal $\overline{\text{PROCHOT}}$ output. 0: Disabled 1: Enabled (default)
0	R/W	IN_PRES_PHOT_EN	1	Enables the input plug-out $\overline{\text{PROCHOT}}$ output. 0: Disabled 1: Enabled (default)

REG1Ch

The REG1Ch register masks the interrupt ($\overline{\text{INT}}$) signal.

Bits	Access	Bit Name	Default	Description
15	R/W	SYS_OVP/SCP_MASK	0	Masks $\overline{\text{INT}}$ for system over-voltage protection (OVP) and short-circuit protection (SCP). 0: Masked (default) 1: Not masked

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14	R/W	SRC_OVP/SCP_ MASK	0	Masks $\overline{INT}$ for the source output OVP and SCP. 0: Masked (default) 1: Not masked
13	R/W	VIN_OVP_MASK	0	Masks $\overline{INT}$ for an input voltage OVP fault. 0: Masked (default) 1: Not masked
12	R/W	PG_STAT_MASK	0	Masks $\overline{INT}$ for good input voltage (V_{IN} exceeds the UVLO threshold and is below the OVLO threshold). 0: Masked (default) 1: Not masked
11	R/W	VBAT_OVP_MASK	0	Masks $\overline{INT}$ for battery OVP. 0: Masked (default) 1: Not masked
10	R/W	WDT_FLT_MASK	1	Masks $\overline{INT}$ for a watchdog timer fault. 0: Masked 1: Not masked (default)
9	R/W	BATT_MISS_MASK	0	Masks $\overline{INT}$ for a battery missing fault. 0: Masked (default) 1: Not masked
8	R/W	TMR_FLT_MASK	0	Masks $\overline{INT}$ for a safety timer fault. 0: Masked (default) 1: Not masked
7	R/W	NTC_FLT_MASK	0	Masks $\overline{INT}$ for an NTC status change. 0: Masked (default) 1: Not masked
6	R/W	MD_STAT_MASK	0	Masks $\overline{INT}$ when the DC/DC converter mode changes. 0: Masked (default) 1: Not masked
5	R/W	CHG_STAT_MASK	0	Masks $\overline{INT}$ when the charge status changes. 0: Masked (default) 1: Not masked
4	R/W	VAP_STAT_MASK	0	Masks $\overline{INT}$ for V_{MIN} active protection (VAP) operation. 0: Masked (default) 1: Not masked
3	R/W	THERMAL_MASK	0	Masks $\overline{INT}$ for thermal shutdown or the thermal regulation loop. 0: Masked (default) 1: Not masked
2	R/W	VIN_LIM_STAT_ MASK	0	Masks $\overline{INT}$ for the V_{IN_MIN} regulation loop. 0: Masked (default) 1: Not masked

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1	R/W	IIN_LIM_STAT_MASK	0	Masks $\overline{INT}$ for I_{IN_MIN} regulation loop. 0: Masked (default) 1: Not masked
0	R/W	BAT_OCP_MASK	0	Masks the $\overline{INT}$ for battery over-current protection (OCP). 0: Masked (default) 1: Not masked

REG1Dh

The REG1Dh register resets the watchdog timer.

Bits	Access	Bit Name	Default	Description
15:1	N/A	RESERVED	0	Reserved. Do not change these bit values.
0	R/W	WDT_RST	0	Resets the watchdog timer. This bit resets to 0 after the bit is written to 1. 0: Normal (default) 1: Reset

REG1Eh

The REG1Eh register resets all the registers.

Bits	Access	Bit Name	Default	Description
15:1	N/A	RESERVED	0	Reserved. Do not change these bit values.
0	R/W	REG_RST	0	This bit is used to reset all the registers. This bit resets to 0 after the bit is written 1. 0: Keep current register setting (default) 1: Reset all registers to default

REG1Fh

The REG1Fh register unlocks battery cell number and V_{BATT_REG} control.

Bits	Access	Bit Name	Default	Description
15:2	N/A	RESERVED	0	Reserved. Do not change these bit values.
1	R/W	VBAT_REG_LOCK	0	When this bit is set to 0, the user can configure V_{BAT_REG} via the I²C/SMBus. 0: Unlocked (default) 1: Locked
0	R/W	BAT_NUM_LOCK	0	When this bit is set to 0, the user can configure the battery cell count via the I²C/SMBus. 0: Unlocked (default) 1: Locked

REG2Bh

The REG2Bh register sets Vmin active protection (VAP) threshold ($V_{IN_MIN_VAP}$).

Bits	Access	Bit Name	Default	Description
15:8	N/A	RESERVED	0	Reserved. Do not change these bit values.

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7	R/W	$V_{IN_MIN_VAP}$[7]	0	Configures the V_{IN_MIN} VAP threshold in VAP mode. If this threshold is reached, a PROCHOT should assert. Range: 0V to 25.5V Default: 4000mV LSB: 100mV $V_{IN_MIN_VAP}$ = DEC(Bits[7:0]) x 100 (mV)
6	R/W	$V_{IN_MIN_VAP}$[6]	0	
5	R/W	$V_{IN_MIN_VAP}$[5]	1	
4	R/W	$V_{IN_MIN_VAP}$[4]	0	
3	R/W	$V_{IN_MIN_VAP}$[3]	1	
2	R/W	$V_{IN_MIN_VAP}$[2]	0	
1	R/W	$V_{IN_MIN_VAP}$[1]	0	
0	R/W	$V_{IN_MIN_VAP}$[0]	0	

REG2Ch

The REG2Ch register sets the system regulation voltage in VAP mode ($V_{SYS_REG_VAP}$).

Bits	Access	Bit Name	Default	Description
15:12	N/A	RESERVED	0	Reserved. Do not change these bit values.
11	R/W	$V_{SYS_REG_VAP}$[11]	0	Sets the system regulation voltage in VAP mode. Range: 0mV/cell to 6400mV/cell Default: 3050mV/cell LSB: 1.5625mV/cell $V_{SYS_REG_VAP}$/cell = DEC(Bits[10:0]) x 1.5625 (mV)
10	R/W	$V_{SYS_REG_VAP}$[10]	1	
9	R/W	$V_{SYS_REG_VAP}$[9]	1	
8	R/W	$V_{SYS_REG_VAP}$[8]	1	
7	R/W	$V_{SYS_REG_VAP}$[7]	1	
6	R/W	$V_{SYS_REG_VAP}$[6]	0	
5	R/W	$V_{SYS_REG_VAP}$[5]	1	
4	R/W	$V_{SYS_REG_VAP}$[4]	0	
3	R/W	$V_{SYS_REG_VAP}$[3]	0	
2	R/W	$V_{SYS_REG_VAP}$[2]	0	
1	R/W	$V_{SYS_REG_VAP}$[1]	0	
0	R/W	$V_{SYS_REG_VAP}$[0]	0	

REG30h

The REG30h register enables ultrasonic mode (USM).

Bits	Access	Bit Name	Default	Description
15:8	N/A	RESERVED	0	Reserved. Do not change these bit values.
7:6	N/A	RESERVED	2’b11	Reserved. Do not change these bit values.
5	R/W	USM_EN	0	Enables USM. When USM is enabled, under extremely light-load conditions, the minimum switching frequency is limited at 30kHz to avoid audible noise. 0: Disabled (default) 1: Enabled
4:0	N/A	RESERVED	5’b11101	Reserved. Do not change these bit values.

REG40h

The REG40h register stores the device’s I²C/SMBus address.

Bits	Access	Bit Name	Default	Description
15	R	ADDR_SET[6]	1	Sets the device address. When the PROG pin is configured to set the address, the highest 4 bits are “0010” and the lowest 3 bits can be configured by an external resistor connected between the PROG and GND pins. Default address: 0x5C
14	R	ADDR_SET[5]	0	
13	R	ADDR_SET[4]	1	
12	R	ADDR_SET[3]	1	
11	R	ADDR_SET[2]	1	
10	R	ADDR_SET[1]	0	
9	R	ADDR_SET[0]	0	
8	N/A	RESERVED	0	Reserved. Do not change this bit value.

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7	R	CUSTOMER_ID[3]	0	These bits are used for customized ID tracking. These bits can be configured via the OTP.
6	R	CUSTOMER_ID[2]	0	
5	R	CUSTOMER_ID[1]	0	
4	R	CUSTOMER_ID[0]	0	
3	R	REV[3]	0	These bits are used for customized revision tracking. These bits can be configured via the OTP.
2	R	REV[2]	0	
1	R	REV[1]	0	
0	R	REV[0]	0	

REG4Ch

The REG4Ch register indicates the charge status and faults.

Bits	Access	Bit Name	Default	Description
15	R	MODE_STAT	0	Indicates the DC/DC converter's operation status. 0: Standby mode (default) 1: Active mode
14	R	DIR_STAT	0	Indicates the device's mode. 0: Forward mode (default) 1: Reverse mode
13	R	VINPG_STAT	0	Indicates whether the input power is good. The device asserts an $\overline{INT}$ signal when the state changes. 0: V_{IN} is not power good (default) 1: V_{IN} is power good
12	R	DC/DC_STAT[1]	0	Indicates the DC/DC converter's mode. 00: Suspend (default) 01: Buck mode 10: Buck-boost mode 11: Boost mode
11	R	DC/DC_STAT[0]	0	
10	R	BATT_MISS	0	Indicates whether the battery is missing. The device asserts an $\overline{INT}$ signal when the state changes. 0: Not missing (default) 1: Missing
9	R	VAP_STAT	0	Indicates whether the device works in VAP mode. The device asserts an $\overline{INT}$ signal when the state changes. 0: Not in VAP mode (default) 1: In VAP mode
8	R	VIN_MIN_STAT	1	Indicates whether the device stays in V_{IN_MIN} regulation loop. The device asserts an $\overline{INT}$ signal when the state changes. 0: In V_{IN_LIM} regulation 1: Not in V_{IN_LIM} regulation (default)
7	R	IIN_LIM_STAT	0	Indicates whether the device is in the I_{IN_LIM} regulation loop. The device asserts an $\overline{INT}$ signal when the state changes. 0: Not in I_{IN_LIM} regulation (default) 1: In I_{IN_LIM} regulation

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6	R	CHG_STAT[2]	0	Indicates the charging status. The device asserts an INT signal when the state changes. 000: Not charging (default) 001: Trickle charge 010: Pre-charge 011: Linear CC 100: Switching CC 101: CV charge 110: Charge termination 111: Supplement
5	R	CHG_STAT[1]	0	
4	R	CHG_STAT[0]	0	
3	R	THERMAL_STAT	0	Indicates whether the device stays in the thermal regulation loop. The device asserts an INT signal when the state changes. 0: Not in thermal regulation (default) 1: In thermal regulation
2	N/A	RESERVED	0	Reserved.
1	R	IBATT_OCP	0	Indicates whether the battery discharge current reaches the over-current (OC) threshold. The device asserts an interrupt (INT) when the fault occurs. 0: Normal (default) 1: In I_{BATT_DSG} OCP
0	R	VSYS_MIN_REG	0	Indicates whether the device is in the V_{SYS_MIN} regulation loop. 0: Not in V_{SYS_MIN} regulation (default) 1: In V_{SYS_MIN} regulation

REG4Dh

The REG4Dh register indicates the protection status.

Bits	Access	Bit Name	Default	Description
15	R	OTG_OVP	0	Indicates whether output over-voltage protection (OVP) has occurred in source mode. The device asserts an INT signal if the fault occurs. 0: Normal (default) 1: OTG OVP has occurred
14	R	SYS_OVP	0	Indicates whether system OVP has occurred. The device asserts an INT signal if a fault occurs. 0: Normal (default) 1: System OVP has occurred
13	R	OTG_SCP	0	Indicates whether OTG short-circuit protection (SCP) has occurred. The device asserts an INT signal if a fault occurs. 0: Normal (default) 1: OTG SCP has occurred
12	R	SYS_SCP	0	Indicates whether system SCP has occurred. The device asserts an INT signal if a fault occurs. 0: Normal (default) 1: System SCP has occurred

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11	R	IN_OVP	0	Indicates whether input OVP has occurred. The device asserts an INT signal if a fault occurs. 0: Normal (default) 1: Input OVP has occurred
10	R	BATT_OVP	0	Indicates whether battery OVP has occurred. The device asserts an INT signal if a fault occurs. 0: Normal (default) 1: Battery OVP has occurred
9	R	BATT_LOW	0	Indicates whether a low battery voltage fault has occurred in source mode. 0: Normal (default) 1: A low battery voltage fault has occurred
8	R	WDT_FLT	0	Indicates whether the watchdog timer (WDT) has expired. The device asserts an INT signal when a fault occurs. 0: Normal (default) 1: The watchdog timer has expired
7	R	TMR_FLT	0	Indicates whether the charge timer has expired. The device asserts an INT signal if a fault occurs. 0: Normal (default) 1: The safety charge timer has expired
6	R	THER_SHDN	0	Indicates whether thermal shutdown has occurred. The device asserts an INT signal if a fault occurs. 0: Normal (default) 1: Thermal shutdown has occurred
5	N/A	RESERVED	0	Reserved. Do not change this bit value.
4	R	NTC_FLT[2]	0	Indicates whether an NTC fault has occurred. The device asserts an INT signal if a fault occurs. 000: Normal (default) 001: NTC cold 010: NTC cool 011: NTC warm 100: NTC hot 111: NTC floating/BATDET
3	R	NTC_FLT[1]	0	
2	R	NTC_FLT[0]	0	
1:0	N/A	RESERVED	0	Reserved. Do not change these bit values.

REG4Eh

The REG4Eh register indicates whether certain faults have occurred. If a fault indication bit in this register is set, then it is latched, even the fault is removable. The relevant bit does not reset until it is read by the I²C/SMBus.

Bits	Access	Bit Name	Default	Description
15	R	OTG_OVP	0	0: Normal 1: OTG over-voltage protection (OVP) has occurred
14	R	SYS_OVP	0	0: Normal 1: System OVP has occurred
13	R	OTG_SCP	0	0: Normal 1: OTG short-circuit protection (SCP) has occurred

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12	R	SYS_SCP	0	0: Normal 1: System SCP has occurred
11	R	IN_OVP	0	0: Normal 1: Input OVP has occurred
10	R	BATT_OVP	0	0: Normal 1: Battery OVP has occurred
9	R	BATT_LOW	0	0: Normal 1: A low battery voltage fault has occurred
8	R	WDT_FLT	0	0: Normal 1: The watchdog timer has expired
7	R	TMR_FLT	0	0: Normal 1: The safety charge timer has expired
6	R	THER_SHDN	0	0: Normal 1: Thermal shutdown has occurred
5	N/A	RESERVED	0	Reserved.
4	R	NTC_FLT[2]	0	000: Normal 001: NTC cold 010: NTC cool 011: NTC warm 100: NTC hot 111: NTC floating/BATDET
3	R	NTC_FLT[1]	0	
2	R	NTC_FLT[0]	0	
1:0	N/A	RESERVED	0	Reserved. Do not change these bit values.

REG43h

The REG43h register returns the V_{IN} ADC result.

Bits	Access	Bit Name	Default	Description
15:10	N/A	RESERVED	0	Reserved.
9	R	V_{IN}[9]	0	Returns the ADC results of the input voltage in charging mode. Range: 0V to 25.5V LSB: 25mV V_{IN} = DEC(Bits[9:0]) x 25 (mV)
8	R	V_{IN}[8]	0	
7	R	V_{IN}[7]	0	
6	R	V_{IN}[6]	0	
5	R	V_{IN}[5]	0	
4	R	V_{IN}[4]	0	
3	R	V_{IN}[3]	0	
2	R	V_{IN}[2]	0	
1	R	V_{IN}[1]	0	
0	R	V_{IN}[0]	0	

REG44h

The REG44h register returns the ADC's I_{IN} result.

Bits	Access	Bit Name	Default	Description
15:10	N/A	RESERVED	0	Reserved.
9	R	I_{IN}[9]	0	Returns the ADC result for the input current. The I_{IN} sense gain is 0.2V/A. Range: 0A to 7A LSB: 7.8125mA I_{IN} = DEC(Bits[9:0]) x 7.8125 (mA)
8	R	I_{IN}[8]	0	
7	R	I_{IN}[7]	0	
6	R	I_{IN}[6]	0	
5	R	I_{IN}[5]	0	
4	R	I_{IN}[4]	0	
3	R	I_{IN}[3]	0	
2	R	I_{IN}[2]	0	
1	R	I_{IN}[1]	0	
0	R	I_{IN}[0]	0	

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REG45h

The REG45h register returns the ADC's V_{BATT} result per cell.

Bits	Access	Bit Name	Default	Description
15:12	N/A	RESERVED	0	Reserved.
11	R	V_{BATT}[11]	0	Returns the ADC results for V_{BATT} per cell. Range: 0mV/cell to 6400mV/cell LSB: 1.5625mV/cell V_{BATT}/cell = DEC(Bits[9:0]) x 1.5625 (mV)
10	R	V_{BATT}[10]	0	
9	R	V_{BATT}[9]	0	
8	R	V_{BATT}[8]	0	
7	R	V_{BATT}[7]	0	
6	R	V_{BATT}[6]	0	
5	R	V_{BATT}[5]	0	
4	R	V_{BATT}[4]	0	
3	R	V_{BATT}[3]	0	
2	R	V_{BATT}[2]	0	
1	R	V_{BATT}[1]	0	
0	R	V_{BATT}[0]	0	

REG46h

The REG46h register indicates the ADC's V_{SYS} result per cell.

Bits	Access	Bit Name	Default	Description
15:10	N/A	RESERVED	0	Reserved.
9	R	V_{SYS}[9]	0	Returns the ADC result for V_{SYS}. Range: 0mV/cell to 6393mV/cell LSB: 6.25mV/cell V_{SYS}/cell = DEC(Bits[9:0]) x 6.25 (mV)
8	R	V_{SYS}[8]	0	
7	R	V_{SYS}[7]	0	
6	R	V_{SYS}[6]	0	
5	R	V_{SYS}[5]	0	
4	R	V_{SYS}[4]	0	
3	R	V_{SYS}[3]	0	
2	R	V_{SYS}[2]	0	
1	R	V_{SYS}[1]	0	
0	R	V_{SYS}[0]	0	

REG47h

The REG47h register indicates the ADC's charge current (I_{CHG}) result.

Bits	Access	Bit Name	Default	Description
15:12	N/A	RESERVED	0	Reserved.
11	R	I_{CHG}[11]	0	Returns the ADC result for the charge current. The I_{BATT} sense gain is 0.1V/A. Range: 0A to 14A LSB: 3.90625mA I_{CHG} = DEC(Bits[11:0]) x 3.9025 (mA)
10	R	I_{CHG}[10]	0	
9	R	I_{CHG}[9]	0	
8	R	I_{CHG}[8]	0	
7	R	I_{CHG}[7]	0	
6	R	I_{CHG}[6]	0	
5	R	I_{CHG}[5]	0	
4	R	I_{CHG}[4]	0	
3	R	I_{CHG}[3]	0	
2	R	I_{CHG}[2]	0	
1	R	I_{CHG}[1]	0	
0	R	I_{CHG}[0]	0	

REG48h

The REG48h register indicates ADC's junction temperature (T_J) result.

Bits	Access	Bit Name	Default	Description
15:10	N/A	RESERVED	0	Reserved.

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9	R	T_J[9]	0	Returns the ADC result for T_J. Range: -33.9°C to +170.7°C LSB: 0.3989°C T_J = 374.54 - 0.3989 x DEC(Bits[9:0]) (°C)
8	R	T_J[8]	0	
7	R	T_J[7]	0	
6	R	T_J[6]	0	
5	R	T_J[5]	0	
4	R	T_J[4]	0	
3	R	T_J[3]	0	
2	R	T_J[2]	0	
1	R	T_J[1]	0	
0	R	T_J[0]	0	

REG49h

The REG49h register indicates the ADC's output voltage result in source mode.

Bits	Access	Bit Name	Default	Description
15:10	N/A	RESERVED	0	Reserved.
9	R	V_{IN_SRC}[9]	0	Indicates the ADC result for the output voltage in source mode. Range: 0V to 25.5V LSB: 25mV V_{IN_SRC} = DEC(Bits[9:0]) x 25 (mV)
8	R	V_{IN_SRC}[8]	0	
7	R	V_{IN_SRC}[7]	0	
6	R	V_{IN_SRC}[6]	0	
5	R	V_{IN_SRC}[5]	0	
4	R	V_{IN_SRC}[4]	0	
3	R	V_{IN_SRC}[3]	0	
2	R	V_{IN_SRC}[2]	0	
1	R	V_{IN_SRC}[1]	0	
0	R	V_{IN_SRC}[0]	0	

REG4Ah

The REG4Ah register indicates the ADC's output current result in source mode (I_{IN_SRC}).

Bits	Access	Bit Name	Default	Description
15:10	N/A	RESERVED	0	Reserved.
9	R	I_{IN_SRC}[9]	0	Returns the ADC result for the source output current. Range: 0A to 7A LSB: 7.8125mA I_{IN_SRC} = DEC(Bits[9:0]) x 7.8125 (mA)
8	R	I_{IN_SRC}[8]	0	
7	R	I_{IN_SRC}[7]	0	
6	R	I_{IN_SRC}[6]	0	
5	R	I_{IN_SRC}[5]	0	
4	R	I_{IN_SRC}[4]	0	
3	R	I_{IN_SRC}[3]	0	
2	R	I_{IN_SRC}[2]	0	
1	R	I_{IN_SRC}[1]	0	
0	R	I_{IN_SRC}[0]	0	

REG4Bh

The REG4Bh register returns the battery discharge current in supplement mode or source mode.

Bits	Access	Bit Name	Default	Description
15:10	N/A	RESERVED	0	Reserved.
9	R	I_{BATT_DSG}[9]	0	Returns the ADC result for the battery discharge current. Range: 0A to 25.5A LSB: 15.625mA I_{BATT_DSG} = DEC(Bits[9:0]) x 15.625 (mA)
8	R	I_{BATT_DSG}[8]	0	
7	R	I_{BATT_DSG}[7]	0	
6	R	I_{BATT_DSG}[6]	0	
5	R	I_{BATT_DSG}[5]	0	
4	R	I_{BATT_DSG}[4]	0	
3	R	I_{BATT_DSG}[3]	0	
2	R	I_{BATT_DSG}[2]	0	
1	R	I_{BATT_DSG}[1]	0	
0	R	I_{BATT_DSG}[0]	0	

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INTERNAL OTP BITS FOR FUNCTION CONFIGURATION

Function	Description
Two phases operation modes	Option 1: Two-phase interleaving with two inductors (0000 default) Option 2: Two-phase paralleled with a single inductor (0001 default)
PROG pin setting	Option 1: Battery cell setting (default) Option 2: Device address setting Option 3: Disable this pin's function
NTC/BATDET pin setting	Option 1: Battery temperature detection and JEITA NTC protection Option 2: BATDET detection (default)

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APPLICATION INFORMATION

Selecting the Input Capacitor

The input capacitor absorbs the maximum ripple current from the PWM converter. In buck mode, the input current is discontinuous. The input RMS ripple current (I_{CIN_RMS}) can be estimated with Equation (5):

$$I_{CIN_RMS} = I_{SYS} x \frac{\sqrt{V_{SYS} x (V_{IN} - V_{SYS})}}{V_{IN}} \quad (5)$$

The worst-case RMS ripple current occurs at a 50% duty cycle. V_{SYS} is about 12V while the battery is configured for 3 cells, so the worst-case condition occurs when the input voltage (V_{IN}) exceeds 20V.

Low-ESR ceramic capacitors with X7R or X5R dielectrics are recommended to be the input decoupling capacitor, and they should be placed in front of the input sense resistor (R_{S_IN}). For input current limits up to 3A, it is recommended to use at least five 22µF capacitors. Capacitance after R_{S_IN} but before power stage should be limited to 100nF + 1nF because too much capacitance after R_{S_IN} may filter out R_{S_IN}'s ripple current sensing information. The capacitors' voltage rating must exceed the normal V_{IN} level. For example, if there is a 20V V_{IN}, it is recommended to use capacitors with a voltage rating that is at least 25V. These capacitors should be placed as close as possible to the IN and PGND pins.

Consider that ceramic capacitors show a DC-bias effect. This effect reduces the effective capacitance when a DC voltage is applied to a ceramic capacitor, especially for high V_{IN} applications. Tantalum capacitors (POSCAP) can avoid the DC-bias effect and temperature effects; it is recommended to add a POSCAP in front of R_{S_IN}. Overall, the minimum effective capacitance in front of R_{S_IN} should exceed 10µF.

VCC Decoupling Capacitor

VCC is an internal LDO output. An external 10µF decoupling capacitor must be placed between VCC and AGND, and as close as possible to these pins.

Selecting the Inductor

Inductor selection is a tradeoff between cost, size, and efficiency. A lower-value inductor offers a smaller size, but results in higher ripple current, magnetic hysteresis losses, and output capacitance.

The MP2764 supports interleaving dual-phase operation, which reduces the output current ripple. This allows a smaller inductor to be used, which balances DCR and size. The recommended inductors are based on a 50% current ripple.

The MP2764 can operate in buck more or boost mode, so the inductor current is equal to either the charging current (I_{CHG}) or the input current (I_{IN}). The inductor's saturation current should exceed the larger value between I_{IN} and I_{CHG}, plus half of the ripple current. The inductor current ripple for buck mode (I_{RIPPLE_BUCK}) and boost mode (I_{RIPPLE_BOOST}) can be calculated with Equation (6) and Equation (7), respectively:

$$I_{RIPPLE_BUCK} = \frac{V_{SYS} x (V_{IN} - V_{SYS})}{V_{IN} x f_{SW} x L} \quad (6)$$

$$I_{RIPPLE_BOOST} = \frac{V_{IN} x (V_{SYS} - V_{IN})}{V_{SYS} x f_{SW} x L} \quad (7)$$

The inductor ripple current (I_{RIPPLE}) depends on the input voltage (V_{IN}), the output system voltage (V_{SYS}), the switching frequency (f_{SW}), and the inductance (L).

The inductance (L) in buck mode can be calculated with Equation (8):

$$L = \frac{V_{SYS} x (V_{IN} - V_{SYS})}{I_{RIPPLE_BUCK} x V_{IN} x f_{SW}} \quad (8)$$

Table 3 on page 59 shows how to select the inductance based on different voltages in buck mode.

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Table 3: Inductor Values in Buck Mode

Specs	Inductance Selection			
V_{IN}	Conditions	L_{MIN}	L	I_{SAT}
9V	• I_{SYS} = 6A • I_{RIPPLE_BUCK} = 50% x I_{SYS} • f_{SW} = 600kHz	1.1µH	1.5µH	>5A
12V		1.7µH	2.2µH	>5A
15V		2.1µH	2.2µH	>5A
20V		2.8µH	3.3µH	>5A

The required inductance (L) in boost mode can be estimated with Equation (9):

$$L = \frac{V_{IN} x (V_{SYS} - V_{IN})}{V_{SYS} x f_{SW} x I_{RIPPLE_BOOST}} \quad (9)$$

Table 4 shows how to select the inductance based on different voltages in boost mode.

Table 4: Inductances in Boost Mode

Specs	Inductance Selection			
V_{IN}	Conditions	L_{MIN}	L	I_{SAT}
5V	• I_{IN} = 5A • I_{RIPPLE_BOOST} = 50% x I_{IN} • f_{SW} = 600kHz	1.4µH	1.5µH	>5A

If V_{SYS} is about 12V while the battery is configured for 3 cells, a 2.2µH inductor with a >5A saturation current is recommended for most specifications.

For applications that can support a higher ripple current, a lower-value inductor can be used to reduce the PCB size.

Selecting the Output Capacitor

The output system capacitor (C_{SYS}) should have a ripple current rating that can absorb the output AC current, as well as sufficient capacitance to maintain the small output voltage ripple. In the boost mode, the output current is discontinuous and dominates the output RMS ripple current (I_{CSYS_BOOST}), which can be calculated with Equation (10):

$$I_{CSYS_BOOST} = I_{SYS} x \frac{\sqrt{V_{IN} \times (V_{SYS} - V_{IN})}}{V_{IN}} \quad (10)$$

The worst-case output RMS ripple current occurs at the lowest V_{BUS} input voltage. V_{SYS} is approximately 12V for a 3-cell battery configuration, so the worst case occurs under the 5V source mode condition. Low-ESR ceramic capacitors, such as those with X7R or X5R dielectrics, are recommended for the output decoupling capacitor, and should be placed as close as possible to the IC's SYS and PGND pins.

The voltage rating of the capacitors must exceed the normal battery voltage level. A capacitor with a minimum 16V voltage rating is recommended for 3-cell battery configurations. For a 6A charging current, it is recommended to place 5pcs 22µF capacitors at the SYS pin.

Similar to the input capacitor, it is recommended to place another POSCAP at the SYS pin to avoid the DC-bias effect and temperature effect and ensure that the effective output capacitance is not below 45µF.

Current Sense

The MP2764 has current loops to limit the current and improve the current accuracy and loop stability. An external current-sense resistor is required to sense the average current (see Figure 18).

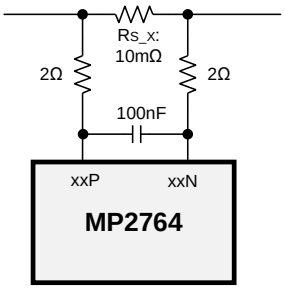

Figure 18: Current-Sensing Circuit

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The input current loop limits the current drawn from the USB port. The input current is sensed through the IAP and IAN pins.

The battery current loop limits the battery's charge current and discharge current. The battery current is sensed through the SRP and SRN pins.

NTC Sense Resistor Divider

In real applications, an external negative temperature coefficient (NTC) thermistor is placed close to the battery to sense the battery's temperature. The MP2764 measures the battery temperature by monitoring the voltage ratio between the NTC/BATDET and VNTC pins (see Figure 19). Every temperature corresponds to a voltage ratio. The MP2764 has four temperature thresholds to satisfy JEITA requirements.

For a given NTC thermistor, the NTC hot and cold temperature thresholds can be calculated with Equation (11) and Equation (12), respectively:

$$\frac{R_{T2}+R_{NTC_HOT}}{R_{T1}+R_{T2}+R_{NTC_HOT}}=\frac{V_{HOT}}{V_{VNTC}} \quad (11)$$

$$\frac{R_{T2}+R_{NTC_COLD}}{R_{T1}+R_{T2}+R_{NTC_COLD}}=\frac{V_{COLD}}{V_{VNTC}} \quad (12)$$

Where R_{NTC_HOT} is the thermistor value at the expected hot temperature protection point, and R_{NTC_COLD} is the thermistor value at the expected cold temperature protection point. V_{HOT} / V_{VNTC} and V_{COLD} / V_{VNTC} are 33.25% and 75.43%, respectively.

Assume the expected hot and cold temperature thresholds are 60°C and 0°C. For example, when using a 103AT-2 thermistor, the thermistor values are:

- R_{NTC_HOT} = 3.02kΩ
- R_{NTC_COLD} = 27.28kΩ

R_{T1} and R_{T2} can also be calculated with Equation (11) or Equation (12). In this scenario, R_{T1} = 9.43kΩ, and R_{T2} = 1.68kΩ.

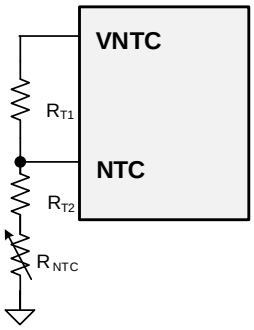

Figure 19: NTC Sensing

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PCB Layout Guidelines

Efficient PCB layout is critical for specified noise, efficiency, and stability requirements. A 6-layer layout (and at least 2 layers for PGND) is recommended. For the best performance, refer to Figure 20 and Figure 21, and follow the guidelines below:

1. Place the VCC capacitor between the VCC pin and AGND pin, and placed as close as possible to the IC.
2. Connect the AGND-to-PGND plane with the shortest possible path via a single-point connection after the VCC capacitor.
3. Connect the PGND pins to other layers' PGND copper areas with as many vias as possible under the IC. The PGND planes should be as large as possible for better thermal dissipation. Pin 5 can be left floating to extend the PGND plane (see Figure 20 and Figure 21).
4. A Kelvin connection is required for the input current-sense resistor and battery current-sense resistor. It is recommended to run the current-sense trace of each sense resistor in parallel.
5. Place the input capacitors between IN and PGND with a large copper area, and close to the IC. Several decoupling capacitors must be placed as close as possible to the IC after the input sense resistor to decouple the high-frequency loop noise.
6. Connect input PGND to the adapter's output PGND.
7. Place the output capacitors between SYS and PGND with a large copper area, and as close as possible to the IC. Place the output decoupling capacitors as close as possible to the IC.
8. Connect output PGND to the downstream system's PGND.
9. Place the BST capacitors as close as possible to the corresponding BST pin and SW pin.
10. It is recommended to lay out each SW copper in at least two layers, and connect the different layers' copper areas with enough vias

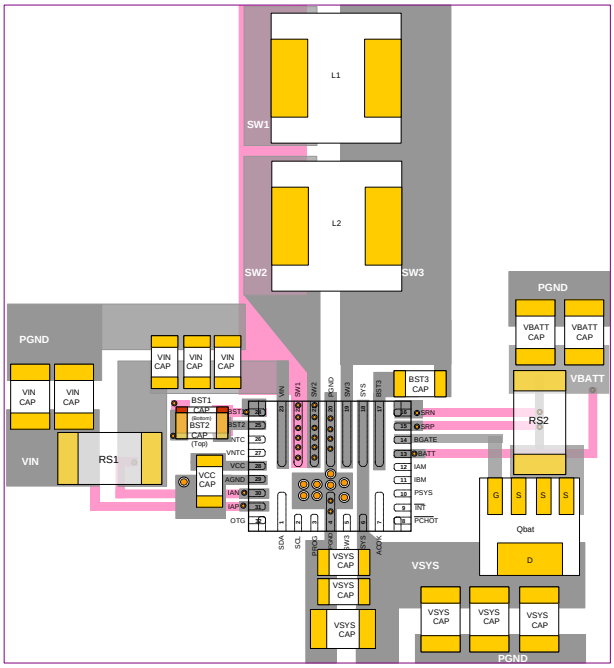

Figure 20: PCB Layout Example (Two Phases Interleaved)

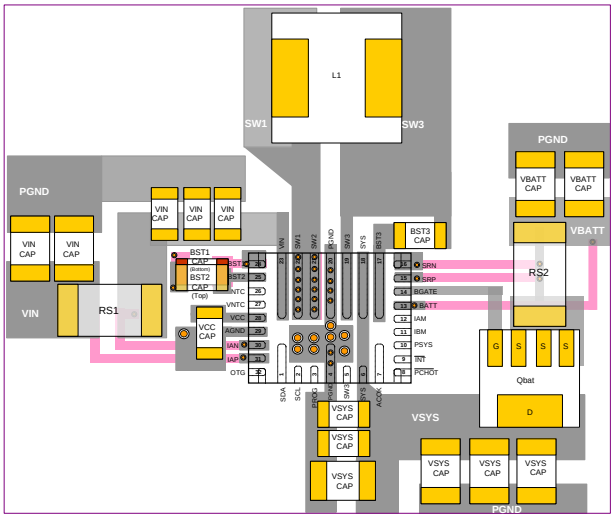

Figure 21: PCB Layout Example (Two Phases Paralleled)

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TYPICAL APPLICATION CIRCUITS

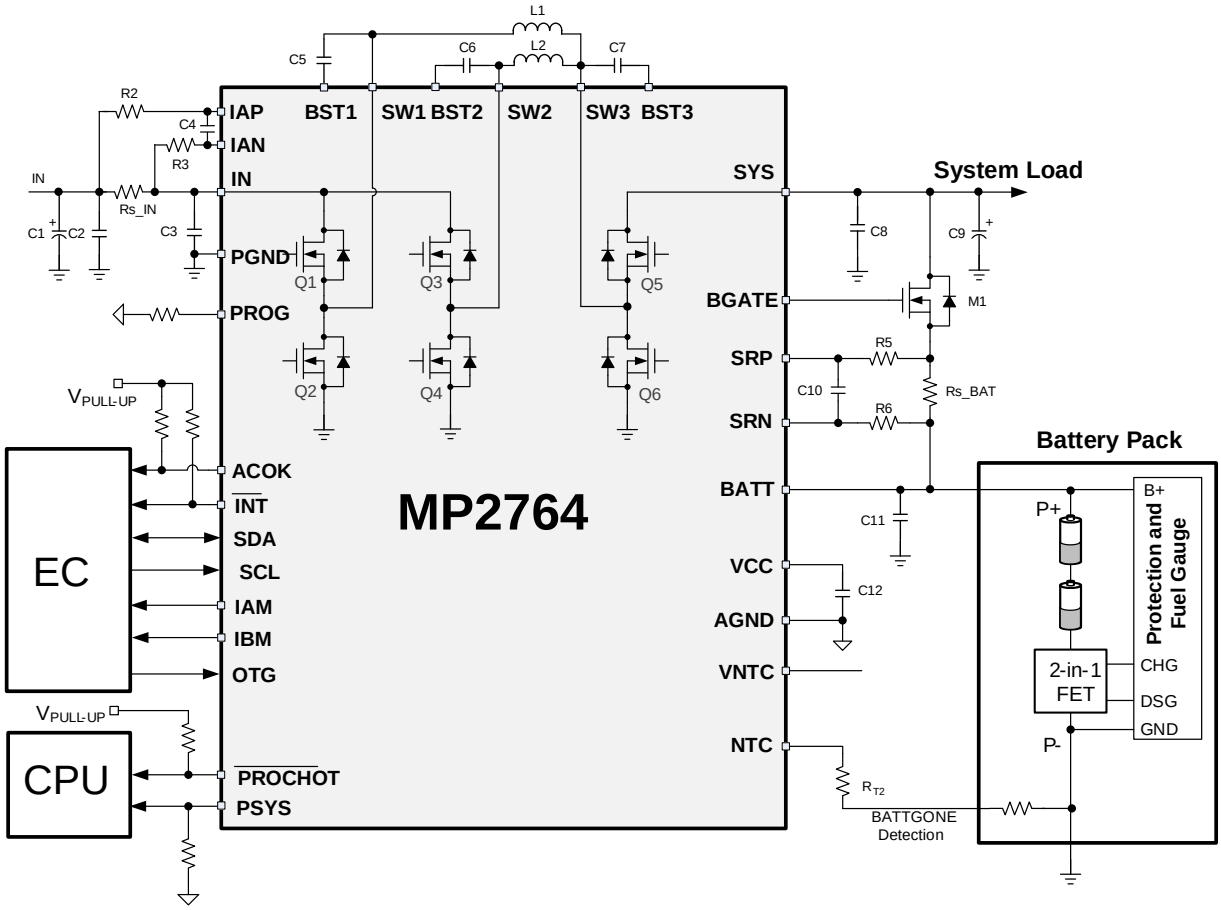

Figure 22: Typical Two-Phased Interleaved Application Circuit

Table 5: Key BOM for Figure 22

Qty	Ref	Value	Description	Package	Manufacturer
1	C1	22µF	Tantalum capacitor, 25V, 100mΩ	3528	Any
1	C2	5 x 22µF	Ceramic capacitor, 25V, X5R or X7R	0805	Any
1	C3	100nF + 1nF	Ceramic capacitor, 25V, X5R or X7R	0603	Any
2	C4, C10	100nF	Ceramic capacitor, 25V, X5R or X7R	0603	Any
3	C5, C6, C7	470nF	Ceramic capacitor, 25V, X5R or X7R	0603	Any
1	C8	5 x 22µF	Ceramic capacitor, 25V, X5R or X7R	0805	Any
1	C9	22µF	Tantalum capacitor, 25V, 100mΩ	3528	Any
1	C11	2 x 22µF	Ceramic capacitor, 25V, X5R or X7R	0805	Any
1	C12	10µF	Ceramic capacitor, 10V, X5R or X7R	0603	Any
2	Rs_IN, Rs_BAT	10mΩ	Current sense resistor, 1W, 1%	1206	Any
4	R2, R3, R5, R6	2Ω	Film resistor, 1%	0603	Any
1	RT2	1kΩ	Film resistor, 1%	0603	Any
2	L1, L2	3.3µH	Inductor, 3.3µH, low DCR, I_{SAT} > 5A	SMD	Any
1	M1	30V	N-channel MOSFET, V_{DS} > 20V, V_{GS} > 10V, I_D > 10A, low R_{DS_ON}	SMD	Any

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TYPICAL APPLICATION CIRCUITS *(continued)*

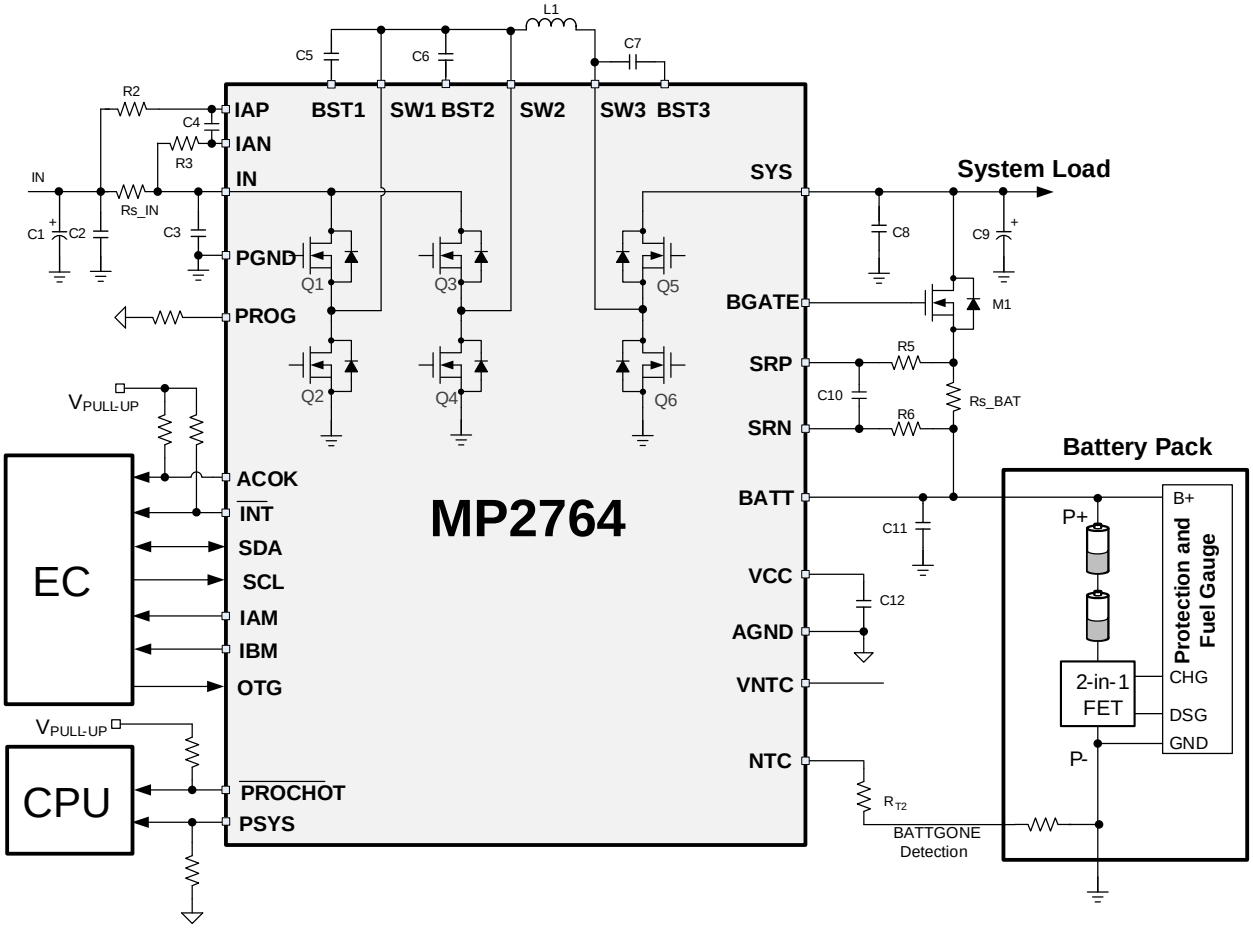

Figure 23: Typical Two-Phased Parallel with Single Inductor Application Circuit

Table 6: Key BOM for Figure 23

Qty	Ref	Value	Description	Package	Manufacturer
1	C1	22µF	Tantalum capacitor, 25V, 100mΩ	3528	Any
1	C2	5 x 22µF	Ceramic capacitor, 25V, X5R or X7R	0805	Any
1	C3	100nF + 1nF	Ceramic capacitor, 25V, X5R or X7R	0603	Any
2	C4, C10	100nF	Ceramic capacitor, 25V, X5R or X7R	0603	Any
3	C5, C6, C7	470nF	Ceramic capacitor, 25V, X5R or X7R	0603	Any
1	C8	5 x 22µF	Ceramic capacitor, 25V, X5R or X7R	0805	Any
1	C9	22µF	Tantalum capacitor, 25V, 100mΩ	3528	Any
1	C11	2 x 22µF	Ceramic capacitor, 25V, X5R or X7R	0805	Any
1	C12	10µF	Ceramic capacitor, 10V, X5R or X7R	0603	Any
2	Rs_IN, Rs_BAT	10mΩ	Current-sense resistor, 1W, 1%	1206	Any
4	R2, R3, R5, R6	2Ω	Film resistor, 1%	0603	Any
1	RT2	1kΩ	Film resistor, 1%	0603	Any
1	L1	2.2µH	Inductor, 2.2µH, low DCR, I_{SAT} > 5A	SMD	Any
1	M1	30V	N-channel MOSFET, V_{DS} > 20V, V_{GS} >7V, I_D > 10A, low R_{DS_ON}	SMD	Any

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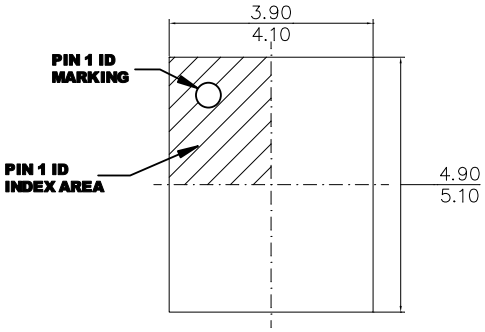
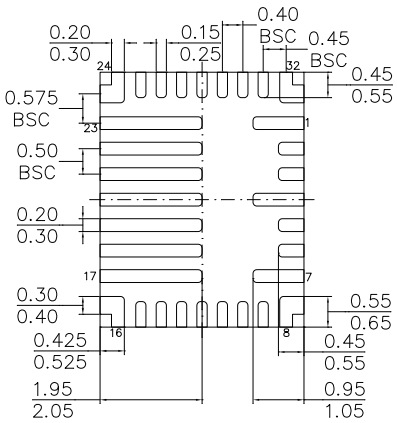
PACKAGE INFORMATION

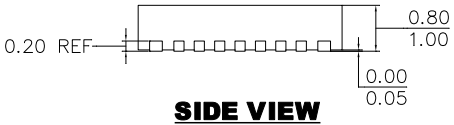
QFN-32 (4mmx5mm)



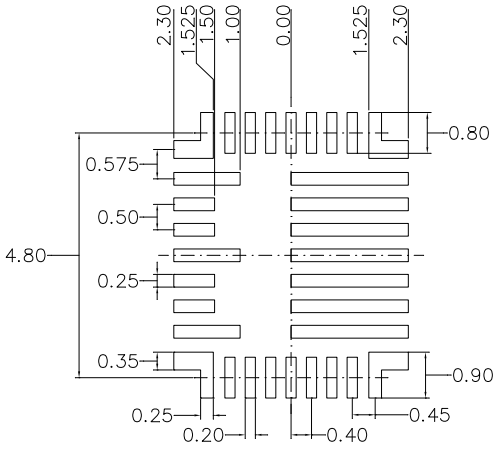
TOP VIEW



BOTTOM VIEW



SIDE VIEW



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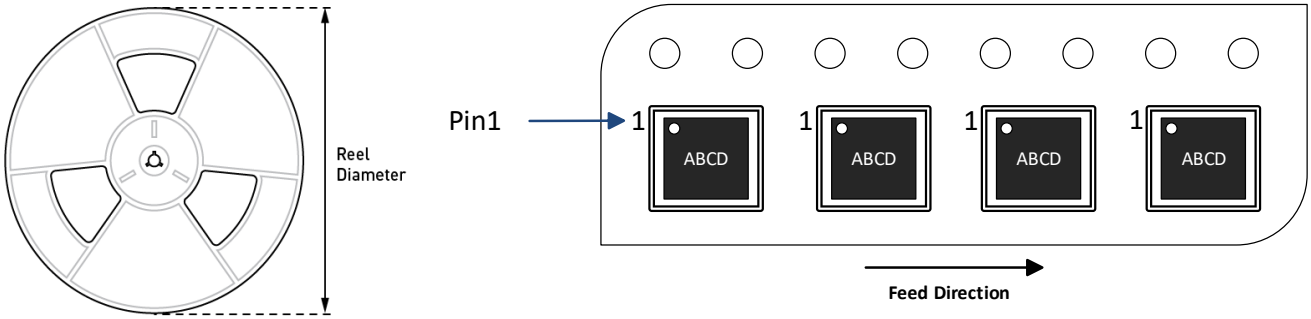

Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2764GV-xxxx-Z	QFN-32 (4mmx5mm)	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	7/17/2025	Initial Release	-

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