MP2696B

I²C-Controlled, Single-Cell Switching Charger with Power-Path Management, Boost Output, and 3.5A Input Current Limit

DESCRIPTION

The MP2696B is a highly integrated, flexible, switch-mode, battery-charging, power-path management device designed for a single-cell Li-ion and Li-polymer battery. This device can be used in a wide range of portable applications.

The MP2696B integrates three battery-charging phases: pre-charge, constant current charge, and constant voltage charge. This device also manages the input power source through input current limit regulation and minimum input voltage regulation.

The MP2696B can switch to boost mode to generate the system power output from the battery.

The MP2696B has an integrated IN to SYS pass-through path to pass the input voltage to the system.

Using an I²C interface, the host can flexibly configure the charge and boost parameters. The device operating status can also be read in the registers.

Safety features include SYS short-circuit protection (SCP), input over-voltage protection (OVP), battery under-voltage protection (UVP), thermal shutdown, and JEITA battery temperature monitoring.

The MP2696B is available in a QFN-21 (3mmx3mm) package.

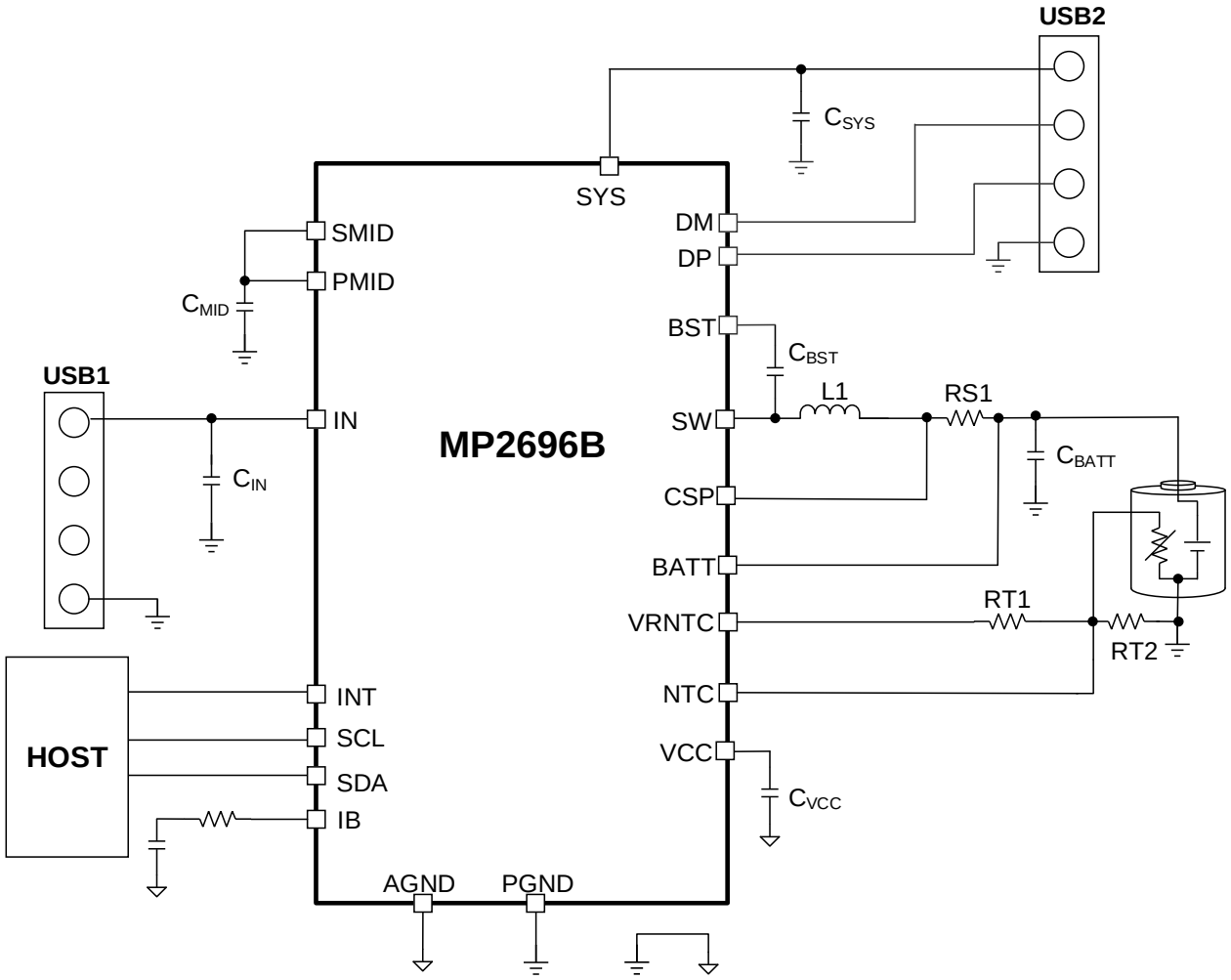
FEATURES

- 4.0V to 11V Operating Voltage Range
- Up to 16V Sustainable Input Voltage
- 500mA to 3.6A Configurable Charge Current
- 3.6V to 4.45V Configurable Charge Regulation Voltage with ±0.5% Accuracy
- 500mA to 3.5A Configurable Input Current Limit with ±10% Accuracy
- Minimum Input Voltage Loop for Maximum Adapter Power Tracking
- Ultra-Low 25μA Battery Discharge Current in Idle Mode
- Boost Converter with Up to 4.0A of Output Current:
  - Configurable Output Current Limit Loop
  - Configurable Boost Output Voltage
  - USB Output Cable Compensation
  - Configurable Inductor Peak Current Limiting
- Comprehensive Safety Features:
  - Fully Customizable JEITA Profile with Configurable Temperature Threshold
  - Charge Safety Timer
  - Input Over-Voltage Protection (OVP)
  - Thermal Shutdown
  - SYS Over-Current (OC) and Short-Circuit Protection (SCP)
- Analog Voltage Output IB Pin for Battery Current Monitoring
- SYS Plug-In Detection
- SYS No Load Detection
- SYS DP/DM Interface for BC1.2 and Non-Standard Adapters
- Status and Fault Monitoring
- Available in a QFN-21 (3mmx3mm) Package

APPLICATIONS

- Sub-Battery Applications
- Power Bank Applications for Smartphones, Tablets, and Other Portable Devices

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP2696BGQ-0000**	QFN-21 (3mmx3mm)	*See Below*	1
EVKT-MP2696B	Evaluation kit	-	

* For Tape & Reel, add suffix -Z (e.g. MP2696BGQ-xxxx-Z).

**"xxxx" is the register setting option. The factory default is "0000." This content can be viewed in the I²C register map. Contact an MPS FAE to obtain an "xxxx" value.

TOP MARKING

BPFY

LLLL

BPF: Product code of MP2696BGQ
Y: Year code
LLLL: Lot number

EVALUATION KIT EVKT-MP2696B

EVKT-MP2696B kit contents (items below can be ordered separately):

#	Part Number	Item	Quantity
1	EV2696B-Q-00A	MP2696B evaluation board	1
2	EVKT-USBI2C-02-BAG	Includes one USB to I²C communication interface, one USB cable, and one ribbon cable	1
3	Online resources	Include datasheet, user guide, product brief, and GUI	1

Order directly from MonolithicPower.com or our distributors.

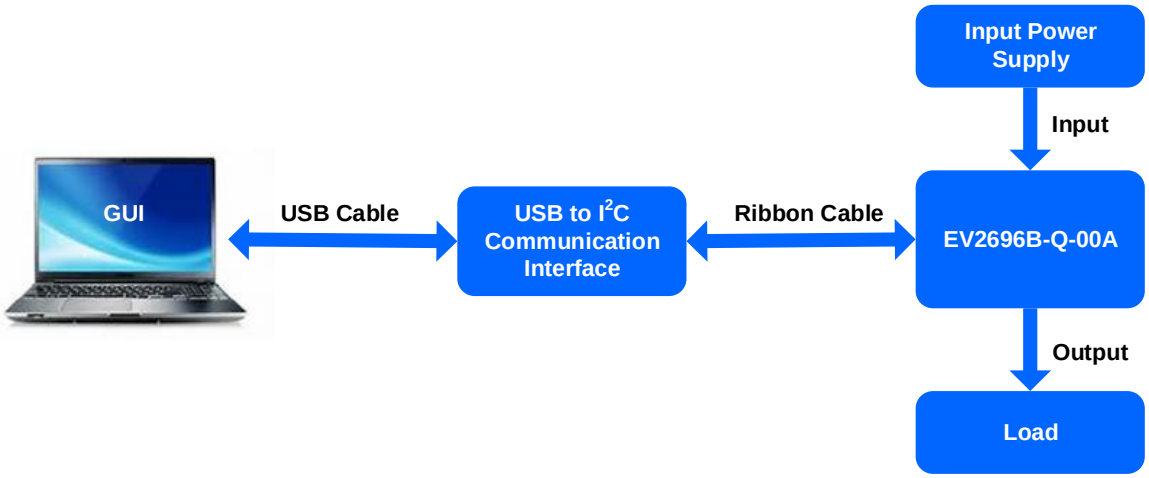
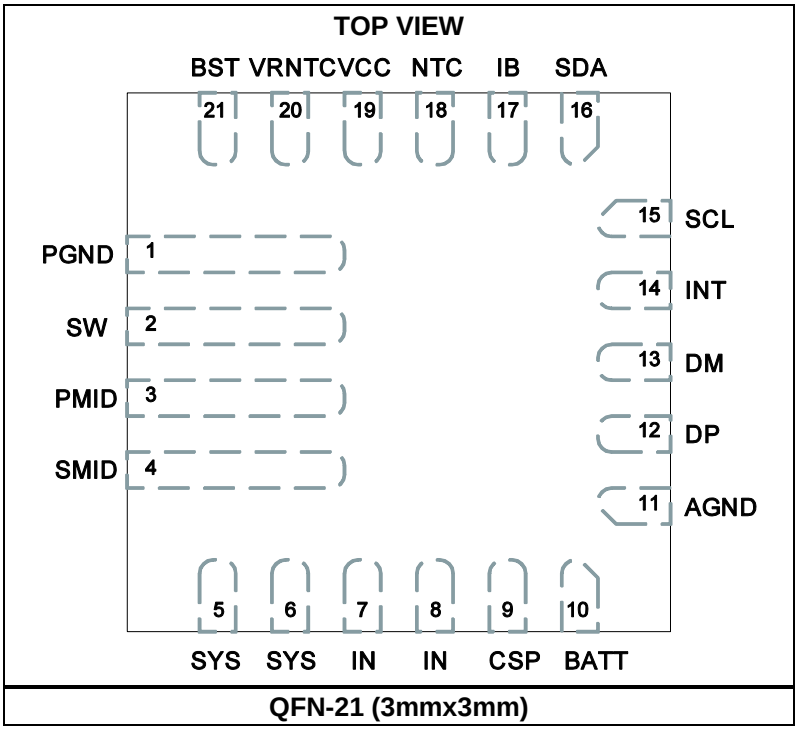


Figure 1: EVKT-MP2696B Evaluation Kit Set-Up

PACKAGE REFERENCE



QFN-21 (3mmx3mm)

PIN FUNCTIONS

Pin #	Name	I/O	Description
1	PGND	Power	**Power ground.**
2	SW	Power	**Switching output node.** Connect SW to the inductor.
3	PMID	Power	**Drain of the high-side switching MOSFET.** Bypass PMID with ceramic capacitors from PMID to PGND, placed as close to the IC as possible.
4	SMID	Power	**Connected to the drain of Q1 and Q2.** Short SMID to PMID on the PCB.
5, 6	SYS	Power	**System power output.** Place ceramic capacitors from SYS to PGND.
7, 8	IN	Power	**Power input of the IC.** Place ceramic capacitors from IN to PGND.
9	CSP	I	**Battery current-sense positive input.**
10	BATT	I	**Battery positive terminal**.
11	AGND	Power	**Analog ground.** Short to PGND on the PCB.
12	DP	I/O	**Positive port of the USB data for the output.** High ESD rating.
13	DM	I/O	**Negative port of the USB data for the output.** High ESD rating.
14	INT	O	**Open-drain interrupt output.** Connect INT to the logic rail through a 10kΩ resistor.
15	SCL	I	**I²C interface clock.** Connect SCL to the logic rail through a 10kΩ resistor.
16	SDA	I/O	**I²C interface data**. Connect SDA to the logic rail through a 10kΩ resistor.
17	IB	O	**Battery current indicator.** The voltage at IB indicates the battery's charge current in charge mode, and the battery's discharge current in boost mode.
18	NTC	I	**Temperature-sense input.** Connect NTC to a negative temperature coefficient thermistor. Configure the temperature window with a resistor divider from VRNTC to NTC to GND. Configurable JEITA thresholds are supported.
19	VCC	Power	**Internal circuit and switch driver power supply.** Bypass VCC to AGND with a ceramic capacitor, placed as close to the IC as possible. For the external load capacity, see the VCC Power Supply section on page 15.
20	VRNTC	Power	**Reference voltage output for powering up NTC.**
21	BST	Power	**Bootstrap.** Connect a 470nF bootstrap capacitor between BST and SW to form a floating supply across the high-side power switch driver.

ABSOLUTE MAXIMUM RATINGS (1)

IN, PMID, SMID, SYS to PGND....-0.3V to +16V
SW to PGND.....-0.3V (-2V for 20ns) to +14V (16V for 20ns)
BST to PGND…….....SW to SW + 5V
All other pins to AGND.....-0.3V to +5.0V
Continuous power dissipation (T_A = 25°C) (2)..... ..... 2.5W
Junction temperature .....150°C
Lead temperature (solder) .....260°C
Storage temperature…. ..... -65°C to +150°C

ESD Ratings

DP, DM pins:
Human body model (HBM) 8000V
Charged device model (CDM) 800V
All other pins:
Human body model (HBM) 2000V
Charged device model (CDM) 250V

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....4V to 11V
Input current (I_{IN}).....Up to 3.5A
System current (I_{SYS}).....Up to 4.0A
Charge current (I_{CC}) .....Up to 3.6A
Battery voltage (V_{BATT}) .....Up to 4.5V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-21 (3mmx3mm)..... 50 ..... 12....°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5.0V, V_{BATT} = 3.5V, RS1 = 10mΩ, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Quiescent Current						
Battery discharge current in idle mode	I_{BATT_IDLE}	Idle mode		25	36	μA
Input quiescent current without switching	I_{IN_Q}	V_{IN} > V_{IN_UVLO}, V_{IN} > V_{BATT} + V_{HDRM}, charge disabled, float SYS		0.6	1	mA
Input quiescent current when switching	I_{IN_QSW}	V_{IN} > V_{IN_UVLO}, V_{IN} > V_{BATT} + V_{HDRM}, charge enabled, float BATT and SYS		1		mA
Battery discharge current in boost mode	I_{BOOST_Q}	I_{SYS} = 0, VBOOST, bits[2:0] = 5.15V, boost enabled, V_{BATT} = 4.2V		2		mA
Power On/Off						
IN operating range	V_{IN_OP}	Converter switching	4		11	V
Input under-voltage lockout	V_{IN_UV}	V_{IN} falling	2.95	3.10	3.25	V
Input under-voltage lockout hysteresis		V_{IN} rising		305		mV
Input vs. battery headroom	V_{HDRM}	V_{IN} rising		200	310	mV
		V_{IN} falling	10	80		mV
Battery under-voltage lockout	V_{BATT_UV}	During boost	2.4	2.5	2.6	V
		Before boost starts	2.8	2.9	3.0	V
VCC LDO output voltage	V_{VCC}	V_{IN} = 5V, I_{VCC} = 30mA	3.3	3.55	3.8	V
VCC under-voltage lockout	V_{CC_UV}	VCC rising	1.9	2.1	2.3	V
VCC under-voltage lockout hysteresis				80		mV
Power Path						
IN to PMID MOSFET (Q1) on resistance	R_{ON_Q1}			25		mΩ
PMID to SYS MOSFET (Q2) on resistance	R_{ON_Q2}			15		mΩ
High-side MOSFET (Q3) on resistance	R_{ON_HS}			15		mΩ
Low-side MOSFET (Q4) on resistance	R_{ON_LS}			14		mΩ
Peak current limit for high-side MOSFET in buck mode	I_{HS_PK}	Constant current charge mode		6.5		A
		Pre-charge mode		1.3		A
Peak current limit for low-side MOSFET in boost mode	I_{LS_PK}	BST_IPK, bits[1:0] = 6.5A	5.9	6.6	7.3	A
		BST_IPK, bits[1:0] = 5A	4.2	4.9	5.6	A
Switching frequency	f_{SW}	SW_FREQ = 700kHz		720		kHz
		SW_FREQ = 1200kHz		1200		kHz

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT} = 3.5V, RS1 = 10mΩ, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Charge Mode						
Charge voltage regulation	V_{BATT_REG}	BATT_REG range (5)	3.6		4.45	V
		BATT_REG, bits[2:0] = 3.6V	3.582	3.6	3.618	V
		BATT_REG, bits[2:0] = 4.1V	4.080	4.1	4.120	V
		BATT_REG, bits[2:0] = 4.2V	4.179	4.2	4.221	V
		BATT_REG, bits[2:0] = 4.3V	4.279	4.3	4.321	V
		BATT_REG, bits[2:0] = 4.35V	4.328	4.35	4.372	V
		BATT_REG, bits[2:0] = 4.4V	4.378	4.40	4.422	V
		BATT_REG, bits[2:0] = 4.45V	4.428	4.45	4.472	V
Fast charge current	I_{CC}	ICC, bits[4:0] = 3A	2.7	3	3.4	A
		ICC, bits[4:0] = 1.5A	1.35	1.5	1.7	A
		ICC, bits[4:0] = 0.5A	0.41	0.5	0.62	A
Charge termination current	I_{TERM}	ITERM, bits[1:0] = 100mA	40	100	160	mA
		ITERM, bits[1:0] = 200mA	100	200	300	mA
Recharge threshold below V_{BATT_REG}	V_{RECH}	V_{BATT} falling	100	200	320	mV
Pre-charge to fast charge threshold	V_{BATT_PRE}	V_{BATT} rising	2.9	3.0	3.1	V
Pre-charge to fast charge hysteresis		V_{BATT} falling		290		mV
Pre-charge current	I_{PRE}	IPRE, bits[1:0] = 150mA, V_{BATT} = 1.8V		150		mA
		IPRE, bits[1:0] = 350mA, V_{BATT} = 1.8V		350		mA
Safety timer for charging cycle				20		hours
Input Regulation						
Input minimum voltage regulation	V_{IN_MIN}	VINMIN, bits[2:0] = 4.5V	4.41	4.51	4.61	V
		VINMIN, bits[2:0] = 4.65V	4.56	4.66	4.76	V
Input current limit	I_{IN_LIM}	IINLIM, bits[2:0] = 3A	2.62	2.75	2.9	A
		IINLIM, bits[2:0] = 1.5A	1.3	1.38	1.5	A
		IINLIM, bits[2:0] = 0.5A	0.4	0.45	0.5	A
Boost Mode						
Boost output voltage at PMID	V_{PMID_BST}	VBOOST, bits[2:0] = 5.15V, I_{SYS} = 10mA	5.05	5.13	5.21	V
		VBOOST, bits[2:0] = 5.225V, I_{SYS} = 10mA	5.13	5.21	5.29	V
Boost output current limit	I_{BST_LMT}	IOLIM, bits[3:0] = 3A	3.0	3.16	3.37	A
		IOLIM, bits[3:0] = 2A	2	2.25	2.5	A
		IOLIM, bits[3:0] = 1A	1.05	1.25	1.45	A

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT} = 3.5V, RS1 = 10mΩ, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Analog Control						
SYS no load current threshold	I_{BST_OFF}	NOLOAD_THR, bits[1:0] = 30mA		30		mA
		NOLOAD_THR, bits[1:0] = 50mA		50		mA
		NOLOAD_THR, bits[1:0] = 75mA		75		mA
		NOLOAD_THR, bits[1:0] = 100mA		100		mA
SYS plug-in detection threshold	V_{PLUG_IN}	SYS falling, percentage of V_{BATT}	70	75	80	%
Discharge dummy load at IN	R_{IN_DUM}			250		Ω
Discharge dummy load at SYS	R_{SYS_DUM}			30		Ω
Protection						
Battery over-voltage threshold	V_{BATT_OVP}		102	104	106	%
BATT over-voltage hysteresis				1.5		%
IN over-voltage protection	V_{IN_OV}	V_{IN} rising, VIN_OVP = 6V	5.8	6	6.2	V
		V_{IN} rising, VIN_OVP = 11V	10.6	11	11.4	V
IN over-voltage protection hysteresis		V_{IN} falling		300		mV
Thermal Shutdown and Temperature Control						
Thermal shutdown rising threshold (5)	T_{J_SHDN}	T_J rising		150		°C
Thermal shutdown hysteresis (5)				20		°C

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT} = 3.5V, RS1 = 10mΩ, T_A = 25°C, unless otherwise noted.

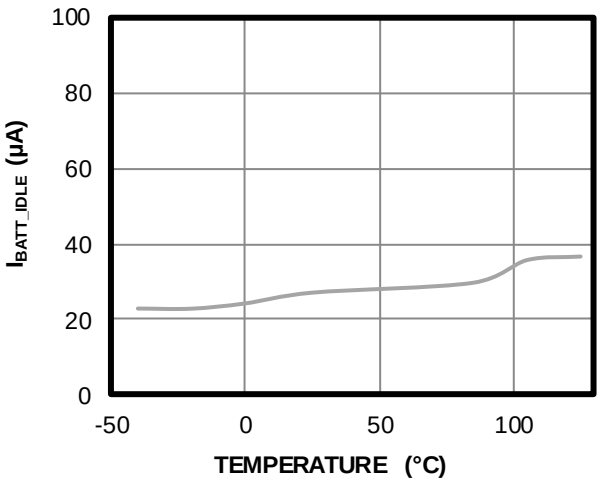
Parameters	Symbol	Condition	Min	Typ	Max	Units
VRNTC voltage	V_{VRNTC}	V_{IN} = 5V, I_{VRNTC} = 100μA		3.5		V
NTC low temp rising threshold	V_{COLD}	As a percentage of V_{VRNTC}, VCOLD, bits[1:0] = 72%	72	73.1	74.3	%
NTC low temp rising threshold hysteresis		As a percentage of V_{VRNTC}		1.6		%
NTC cool temp rising threshold	V_{COOL}	As a percentage of V_{VRNTC}, VCOOL, bits[1:0] = 60%	59.7	61	62.2	%
NTC cool temp rising threshold hysteresis		As a percentage of V_{VRNTC}		1.6		%
NTC warm temp falling threshold	V_{WARM}	As a percentage of V_{VRNTC}, VWARM, bits[1:0] = 40%	39.4	40.6	42	%
NTC warm temp falling threshold hysteresis		As a percentage of V_{VRNTC}		1.6		%
NTC hot temp falling threshold	V_{HOT}	As a percentage of V_{VRNTC}, VHOT, bits[1:0] = 36%	35.3	36.6	37.9	%
NTC hot temp falling threshold hysteresis		As percentage of V_{VRNTC}		1.6		%
SYS DP/DM Signaling						
DP/DM source voltage 2V7	V_{SRC_2V7}		2.6	2.7	2.8	V
DP/DM source resistance	R_{SRC}		23	30	37	kΩ
DP/DM comparator threshold 2.9V	V_{TH_2V9}		2.75	2.9	3.1	V
DP/DM comparator threshold 2.1V	V_{TH_2V1}		1.95	2.1	2.25	V
Deglitch time for exiting non-standard adapter			8	10	12	ms
DP/DM short resistance	R_{SHORT}			150		Ω
Pull-down resistor on DP pin	R_{PULL_DWN}			300		kΩ
Timer for DCP to enter non-standard adapter				2		s
I²C Interface						
Input high threshold level		SDA and SCL	1.3			V
Input low threshold level		SDA and SCL			0.4	V
Output low threshold level		I_{SINK} = 5mA			0.3	V
I²C clock frequency	f_{SCL}				400	kHz
Battery Current Indicator						
IB voltage output		I_{CC} = 1A in charge mode	0.28	0.34	0.4	V
		I_{DSCHG} = 1A in boost mode	0.135	0.155	0.175	V

Note:

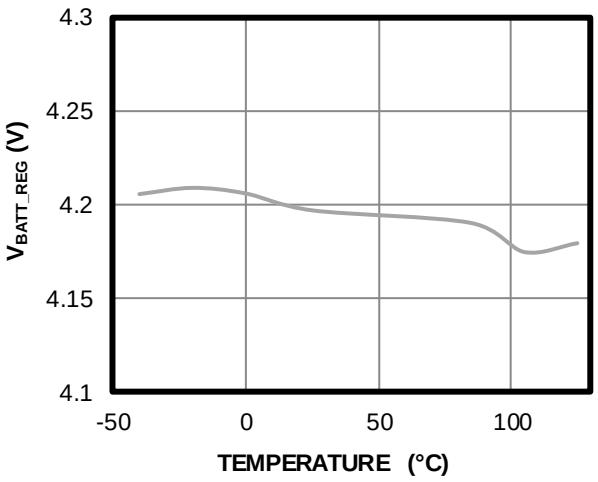
5) Guaranteed by design.

TYPICAL CHARACTERISTICS

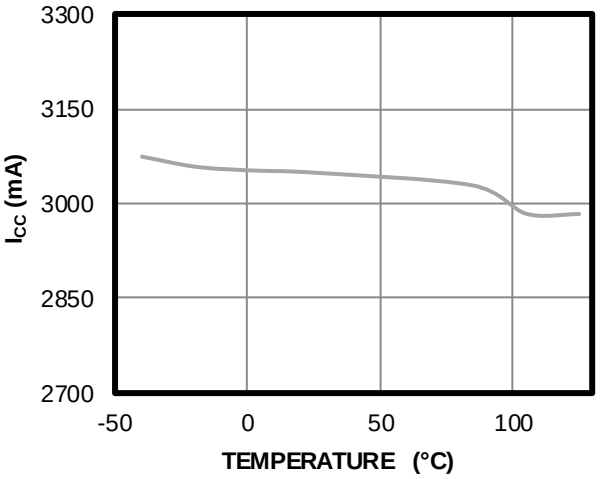
I_{BATT_IDLE} vs. Temperature
V_{BATT} = 5V



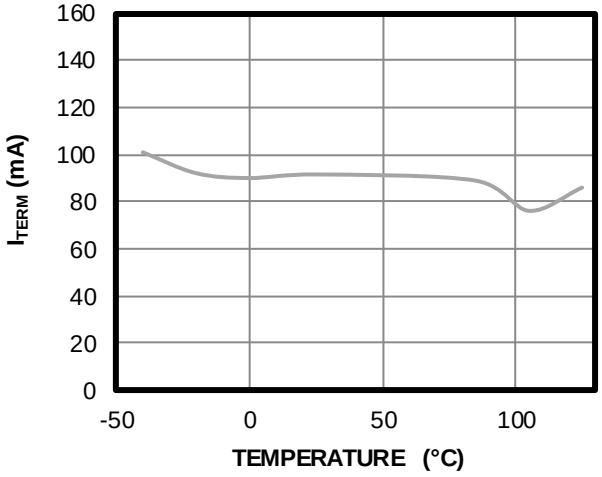
V_{BATT_REG} vs. Temperature
V_{BATT_REG} = 4.2V



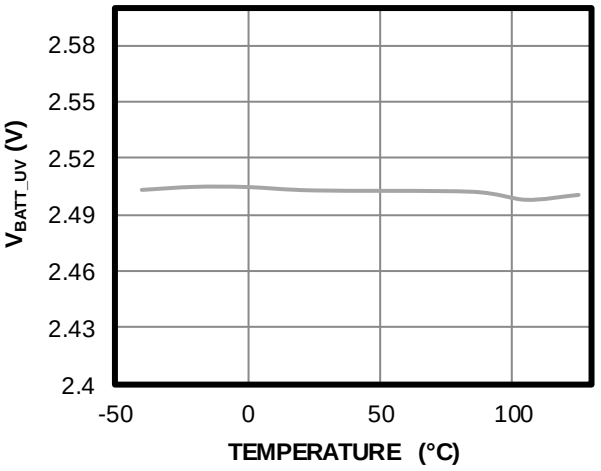
I_{CC} vs. Temperature
I_{CC} = 3A



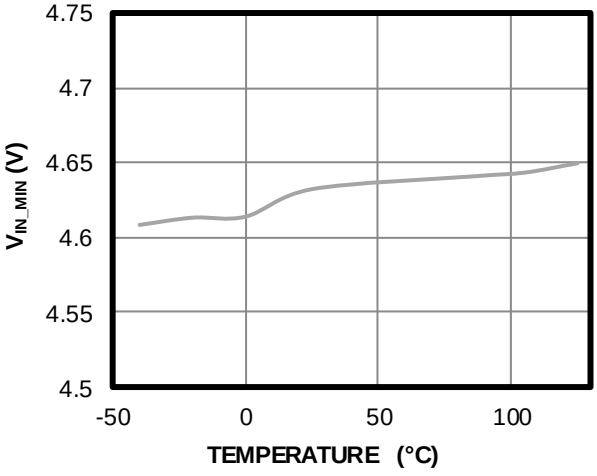
I_{TERM} vs. Temperature
I_{TERM} = 100mA



V_{BATT_UV} vs. Temperature
During boost



V_{IN_MIN} vs. Temperature
V_{IN_MIN} = 4.65V

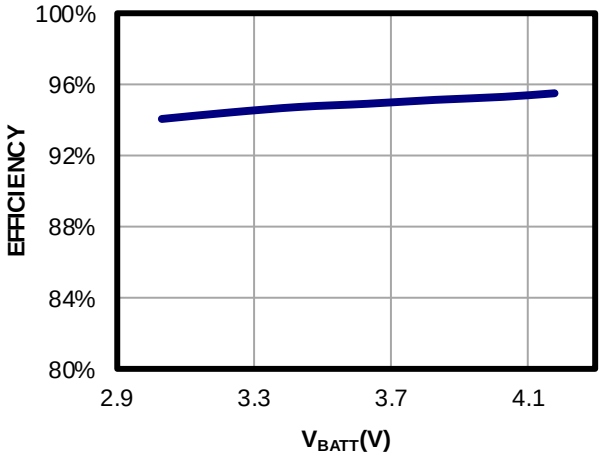


TYPICAL PERFORMANCE CHARACTERISTICS

L1 = 1µH/10mΩ, C_{BATT} = 22µF, RS1 = 10mΩ, T_A = 25°C, battery simulator load, unless otherwise noted.

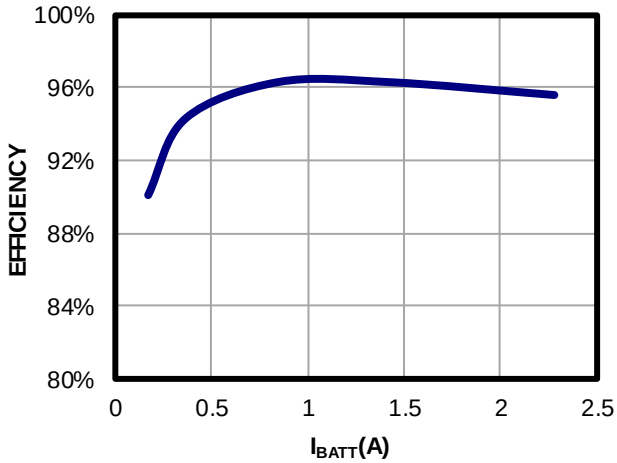
Constant Current Charge Mode Efficiency

V_{IN} = 5V, I_{CC} = 2.5A



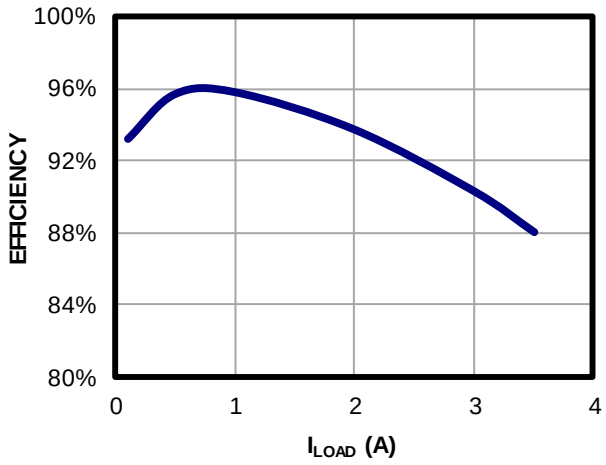
Constant Voltage Charge Mode Efficiency

V_{IN} = 5V, V_{BATT} = 4.2V



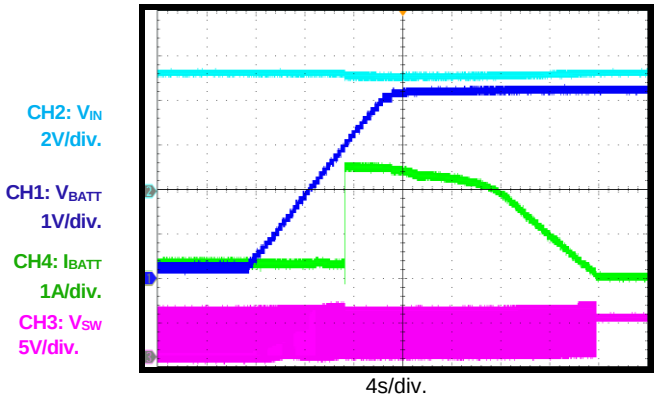
Boost Mode Efficiency

V_{BATT} = 3.5V, V_{SYS} = 5.15V



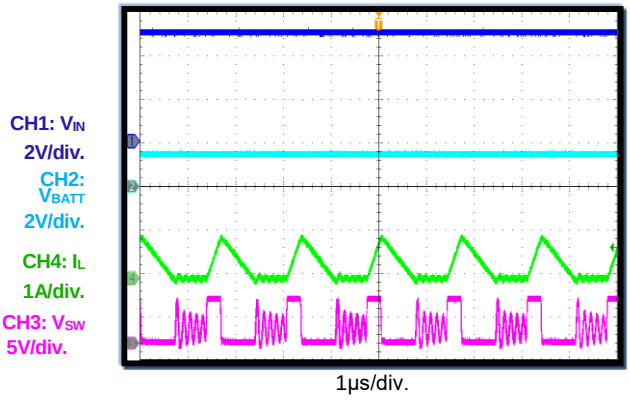
Battery Charge Curve

V_{IN} = 5V



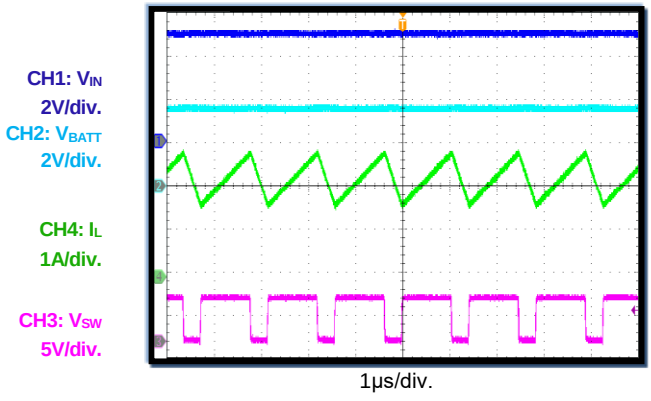
Pre-Charge Steady State

V_{IN} = 5V, V_{BATT} = 1.5V, I_{PRE} = 150mA



Constant Current Charge Steady State

V_{IN} = 5V, V_{BATT} = 3.5V, I_{CC} = 2A

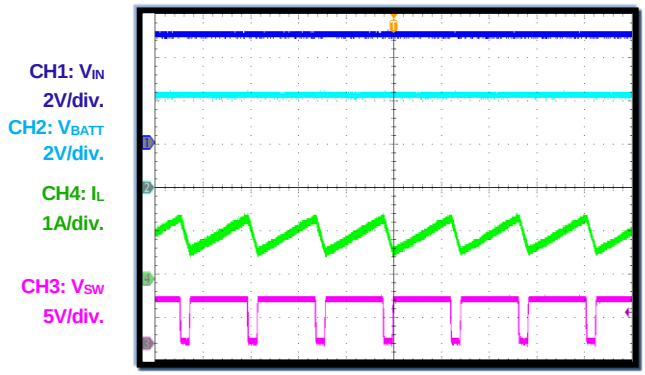


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

L1 = 1µH/10mΩ, C_{BATT} = 22µF, RS1 = 10mΩ, T_A = 25°C, battery simulator load, unless otherwise noted.

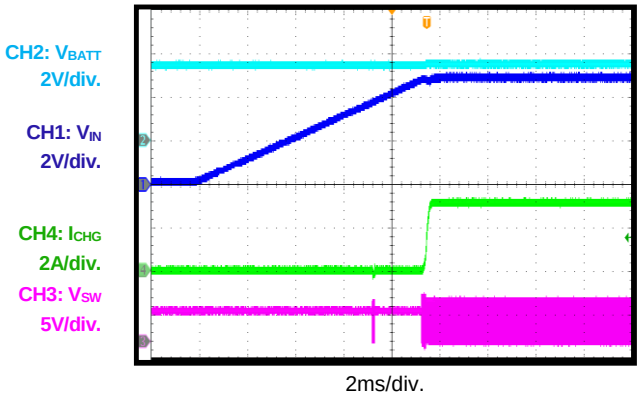
Constant Voltage Charge Steady State

V_{IN} = 5V, V_{BATT} = 4.2V



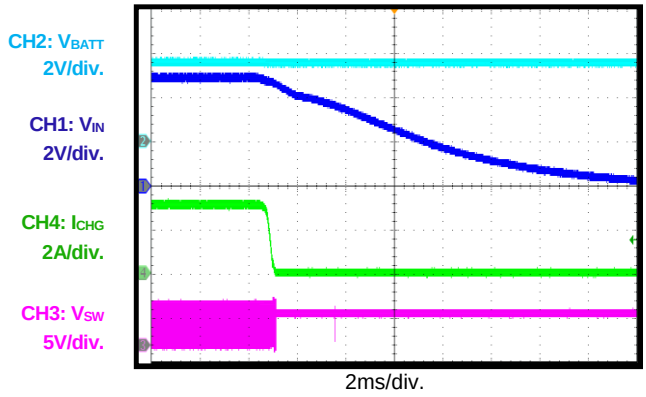
Start-Up in Constant Current Charge Mode

V_{IN} = 5V, V_{BATT} = 3.5V, I_{CC} = 3A



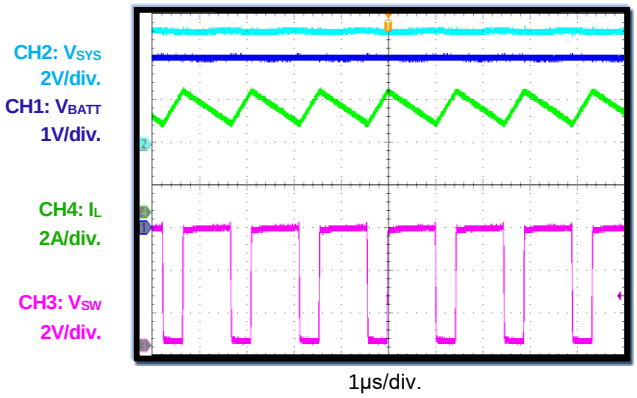
Shutdown in Constant Current Charge Mode

V_{IN} = 5V, V_{BATT} = 3.5V, I_{CC} = 3A



Boost Steady State

V_{BATT} = 4V, I_{SYS} = 3.5A



FUNCTIONAL BLOCK DIAGRAM

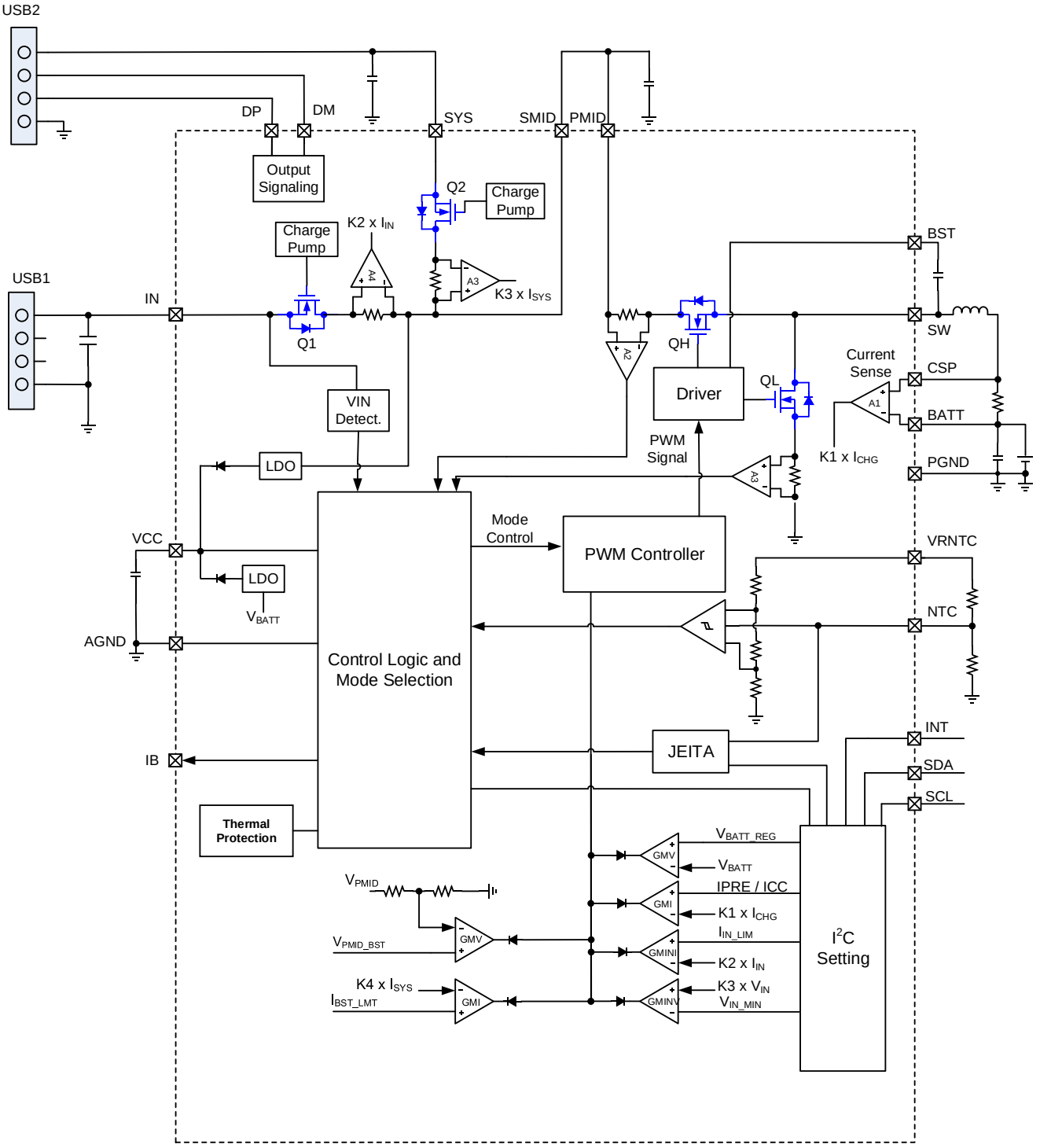


Figure 2: Functional Block Diagram

OPERATION

Introduction

The MP2696B is an I²C-controlled switching charger with bidirectional operation that can step up the battery voltage to power the system. Depending on the input and output status, the device operates in one of three modes: charge mode, boost mode, or idle mode. In charge mode, the IC supports a precision Li-ion or Li-polymer charging system for single-cell applications. In boost mode, the IC boosts the battery voltage to a regulated voltage at SYS to power the load. In idle mode, the IC stops charging or boosting, and operates at a low current from the input or the battery. This reduces power consumption when the IC is not operating.

VCC Power Supply

VCC provides power for the internal bias circuit, as well as the low-side switch driver. VCC is powered from the higher voltage between the PMID and BATT pins. When the VCC voltage rises above the under-voltage lockout threshold (V_{VCC_UV}), the I²C interface is ready for communication, and all the registers are reset to their default values. When the device is switching, VCC can provide up to 30mA for the external load.

CHARGER MODE OPERATION

Battery Charging Profile

The IC can run a charging cycle autonomously without host involvement. The host can also control the charge operations and parameters via the registers.

A new charge cycle can start when the following conditions are valid:

- V_{IN} is above V_{IN_UV}
- V_{IN} is below V_{IN_OV}
- V_{IN} is above V_{BATT} + V_{HDRM}
- The NTC voltage is in the proper range (if the NTC_STOP bit is set to 1)
- There is no charge timer fault
- Charging is enabled (CHG_EN = 1)
- There is no battery over-voltage condition

After charging is done, unplug and re-insert VIN or toggle the CHG_EN bit to start a new charge cycle.

Charge Cycle

The IC checks the battery voltage to provide three main charging phases: pre-charge, constant current (CC) charge, and constant voltage (CV) charge.

The IC regulates the voltage drop on the current-sense resistor (RS1) for the battery pre-charge and constant current charge current. Table 1 shows the default value for a 10mΩ resistor.

Table 1: Charge Current vs. Battery Voltage (RS1 = 10mΩ)

Battery Voltage	Charge Current	Default Value	CHG_STAT
BATT < 3V	IPRE, bits[1:0]	150mA	01
BATT > 3V	ICC, bits[4:0]	1A	10

The charge current can be scaled by implementing different current-sense resistor values. The charge current for constant current charge and pre-charge can be calculated with Equation (1) and Equation (2), respectively:

$$I_{CC} = \frac{ICC[4:0] \times 10m\Omega}{RS1} \quad (1)$$

$$I_{PRE} = \frac{IPRE[1:0] \times 10m\Omega}{RS1} \quad (2)$$

Note that the soldering tin for the current-sense resistor has resistance, which must be compensated.

During the entire charging process, the actual charge current may be less than the register setting due to other loop regulations, such as the input current limit or the input voltage limit.

Charge Termination

Charging terminates if all of the following conditions are met:

- The charge current is below the termination threshold for 20ms.
- The IC works in a constant voltage charge loop.
- The IC is not in the input current loop or input voltage loop.

After termination, the status register CHG_STAT is set to 11, and an INT pulse is generated (see Figure 3).

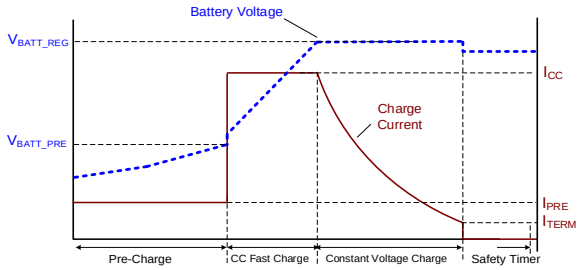


Figure 3: Battery Charge Profile

Automatic Recharge

When the battery is fully charged and charging is terminated, the battery may be discharged because of the system consumption or self-discharge. When the battery voltage is discharged below the recharge threshold (V_{BATT_REG} - 200mV), the IC starts a new charging cycle automatically if the input power is valid. The timer restarts when the auto-recharge cycle begins.

Safety Timer

The IC provides a safety timer to prevent extended charging cycles due to abnormal battery conditions. The safety timer feature can be disabled via the I²C. The safety timer does not operate in boost mode.

The safety timer restarts at the beginning of a new charging cycle. The following actions restart the safety timer:

- A new charge cycle starts
- The EN_TIMER bit is toggled

An INT pulse is generated if the safety timer expires before charging is done. Then the charge cycle stops, and CHG_FAULT is set to 11, which indicates that the safety timer has expired. Unplug and re-insert VIN can clear this fault after safety timer expires.

Input Voltage Based and Input Current Based Power Management

The IC features both input current and input voltage based power management by monitoring the input current and input voltage continuously.

When the input current reaches the limit set by IINLIM, bits[2:0], the charge current tapers off to keep the input current from increasing further.

If the preset input current limit exceeds the adapter rating, the backup input voltage based power management also works to prevent the input source from being overloaded. When the input voltage falls below the input voltage regulation threshold set by VINMIN, bits[2:0] due to the heavy load, the charge current is also reduced to keep the input voltage from dropping further.

An INT pulse is generated once the device enters a VINPPM or INPPM condition.

Thermistor Qualification

VRNTC is driven to be equal to the VCC voltage when the IC is in charge/boost mode. The IC monitors the battery's temperature continuously by measuring the voltage at the NTC pin. The NTC function can be disabled by setting EN_NTC = 0.

When NTC_STOP is set to 1, the NTC voltage should be within the V_{HOT} to V_{COLD} range for both charge and boost operation. The IC resumes switching when the NTC voltage returns to the V_{HOT} to V_{COLD} range.

When NTC_STOP is set to 0, the IC only generates an interrupt signal and reports the NTC pin status if the status changes on NTC_FAULT, bits[2:0].

The JEITA profile is supported when the JEITA_DIS bit is set to 0.

In the cool temperature range (V_{COLD} to V_{COOL}), the charge current is reduced according to the JEITA_ISET setting (see Figure 4).

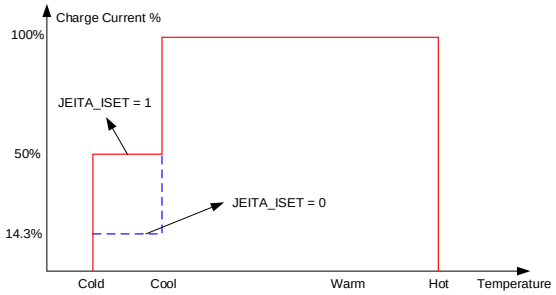


Figure 4: JEITA Profile (Charge Current)

In the warm temperature range (V_{WARM} to V_{HOT}), the charge voltage is reduced according to the JEITA_VSET setting (see Figure 5).

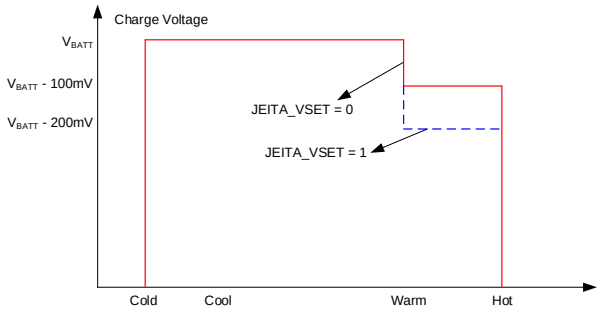


Figure 5: JEITA Profile (Charge Voltage)

The hot and cold thresholds have two options in the register. The warm and cool thresholds have four options in the register, which offers accurate and flexible JEITA control.

Interrupt to Host (INT)

A 50μs interrupt pulse is generated on the open-drain INT pin when any of the events below occur:

- A good input source is detected
- A USB2 plug-in is detected
- Status register 05h changes
- Fault register 06h changes

Battery Over-Voltage Protection (OVP)

When the battery voltage exceeds 104% of V_{BATT_REG}, the IC suspends charging immediately, and the BATT_OVP bit is set to 1. An 800μA current source discharges the battery until the battery voltage returns to the normal range.

Battery over-voltage protection (OVP) can be disabled by setting the BATT_OVP_DIS bit to 1.

Input Over-Voltage Protection (OVP)

Once IN senses a voltage greater than the V_{IN} over-voltage protection (OVP) threshold, the DC/DC converter stops immediately.

The input OVP threshold can be set to 6V or 11V by the VIN_OVP bit.

BOOST MODE OPERATION

The IC can supply a regulated 5V output at SYS to power the system. To ensure that the battery is not drained, boost mode does not start if BATT is below 2.9V. To enable boost mode, the IN voltage must be below 2.0V.

The boost output current limit can be configured to be between 1.0A and 4.0A. Boost mode has an output current limit loop when $V_{SYS} > V_{BATT}$.

Once boost mode is enabled, the IC boosts PMID to the preset voltage first, and then the block MOSFET (Q2) turns on linearly. When V_{SYS} is charged above 4.2V within 3ms, Q2 turns on fully. Otherwise, Q2 turns off and tries to turn on again after 300ms.

Boost Power Limitation

During boost operation, the inductor peak current in each switching cycle is limited by the peak current limit of the low-side switch (Q_L), set by BST_IPK, bits[1:0]. This helps limit the maximum battery discharge current.

Battery Under-Voltage Lockout (UVLO) Protection

If the battery voltage drops below 2.5V in boost mode, boost mode stops, and the BATT_UVLO bit is set to 1. Boost mode recovers when the battery voltage rises above 2.9V, but the BATT_UVLO bit is not reset until the input source plug-in and battery is charged again.

SYS Over-Current (OC) and Short-Circuit Protection (SCP)

In boost mode, the MP2696B always monitors the current flowing through Q2. When the SYS output current exceeds the preset boost output current limit, the output current loop takes control, and both the PMID and SYS voltages decrease. When V_{SYS} drops to V_{BATT} + 200mV, Q2 turns off. After 300ms, Q2 tries to restart.

The IC also features fast SYS over-current protection (OCP) in both boost mode and pass-through mode. If the Q2 current exceeds 8A, Q2 turns off immediately. After 300ms, Q2 tries to restart.

Impedance Compensation for Boost Output

The IC allows the user to compensate the intrinsic resistance of Q2 and the USB2 output wire voltage drop by adjusting the boost output voltage according to the system load current, calculated with Equation (3):

$$V_{PMID} = V_{BOOST} + (I_{SYS} \times R_{SYS\_CMP}) \quad (3)$$

Where V_{PMID} is the voltage at PMID, and V_{BOOST} is the boost regulation voltage set by VBOOST, bits[2:0]. I_{SYS} is the real-time SYS load current during normal operation, and R_{SYS_CMP} is the cable resistance compensation set by RSYS_CMP, bits[2:0]

USB2 Plug-In Detection

If the USB2_EN_PLUG bit is enabled in standby mode, the SYS voltage (V_{SYS}) is pulled up to the BATT voltage (V_{BATT}). After V_{SYS} reaches 90% of V_{BATT}, detection starts. Once V_{SYS} drops to 75% of V_{BATT}, the USB2 plug-in is detected, the USB2_PLUG_IN bit is set to 1, and an INT pulse is generated.

The host can respond to the interrupt signal and enable boost mode Q2.

The host must clear the USB2_PLUG_IN bit, and toggle the USB2_EN_PLUG bit for the next detection. Note that writing 1 to the USB2_PLUG_IN bit clears it to 0.

No-Load Detection

During boost or pass-through operation, the Q2 current is monitored. If the Q2 current is below the value set by NOLOAD_THR, bits[1:0], the NO_LOAD bit is set to 1, and an INT pulse is generated. The host can monitor the NO_LOAD bit to decide whether boost mode or Q2 must be turned off.

Thermal Shutdown

The IC continuously monitors the internal junction temperature to maximize power delivery and avoid overheating the chip. If the junction temperature reaches 150°C, the converter shuts down. If the junction temperature drops to 120°C, normal operation resumes.

Battery Current Analog Output

The device has an IB pin to obtain the real-time battery current value in both charge and boost mode. The voltage at IB is a fraction of the battery current. The IB pin indicates the current flowing in and out of the battery during charge and boost mode.

With a 10mΩ current-sense resistor. calculate the voltage at IB for charge mode and boost mode with Equation (4) and Equation (5), respectively:

$$V_{IB} = I_{CHG} \times 0.35(V) \quad (4)$$

$$V_{IB} = I_{DSCHG} \times 0.16(V) \quad (5)$$

Note that scaling the current-sense resistor also scales the gain of IB.

Idle Mode

When the input power source is not present and boost mode is disabled, the IC goes into idle mode. In idle mode, all the MOSFETs and most of the internal circuits are turned off to minimize leakage and extend the battery run time.

SYS DP/DM Signaling

Initially, the DP and DM pins are biased at 2.7V with an internal resistance of 30kΩ for non-standard adapter imitation.

If the DP or DM pin is out of the 2.1V to 2.9V range for 10ms in DCP mode, the 2.7V reference is disconnected, and DP and DM are tied together with a 100Ω resistor.

If DP stays below 0.35V for 2 seconds in DCP mode, the IC returns to non-standard adapter mode with DP/DM biased at 2.7V.

Series Interface

The IC uses an I²C-compatible interface for flexible charging parameter setting and instantaneous device status reporting. I²C is a 2-wire serial interface with two bus lines required: a serial data line (SDA) and a serial clock line (SCL). Both SDA and SCL lines are open drain and must be connected to the positive supply voltage via a pull-up resistor.

The IC operates as a slave device, receiving control inputs from the master device such as a microcontroller. The SCL line is always driven by the master device. The I²C interface supports both standard mode (up to 100kb/s), and fast mode (up to 400kb/s).

All transactions begin with a start (S) condition and are terminated by a stop (P) condition. The start and stop conditions are always generated by the master. A high to low transition on the SDA line while SCL is high defines a start condition. A low to high transition on the SDA line when the SCL is high defines a stop condition (see Figure 6).

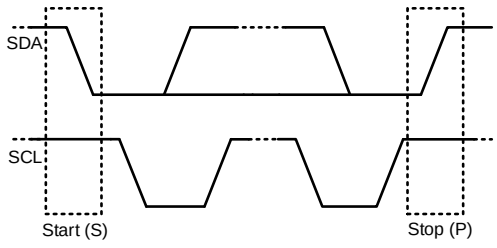


Figure 6: Start and Stop Conditions

For data validity, the data on the SDA line must be stable during the high period of the clock. The high or low state of the SDA line can only change when the clock signal on the SCL line is low. Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Data is first transferred with the most significant bit (MSB) (see Figure 7).

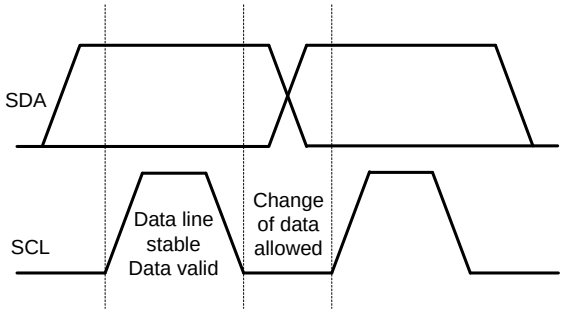


Figure 7: Bit Transfer on the I²C Bus

Each byte has to be followed by an acknowledge (ACK) bit, which is generated by the receiver, to signal to the transmitter that the byte was successfully received.

The ACK signal is defined as follows: the transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line low. The SDA line remains low during the high period of the ninth clock.

If SDA line is high during the ninth clock, this is defined as the not acknowledge (NACK) signal. The master can then generate either a stop condition to abort the transfer or a repeated start (Sr) condition to start a new transfer.

After the start signal is received, a slave address is sent. This address is 7 bits long, followed by the eighth bit as a data direction bit (bit R/W). A zero indicates a transmission (write), and a one indicates a request for data (read). Figure 8 shows the address bit arrangement.

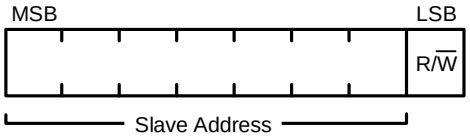


Figure 8: 7-Bit Address

See Figure 9 through Figure 13 for detailed signal sequences.

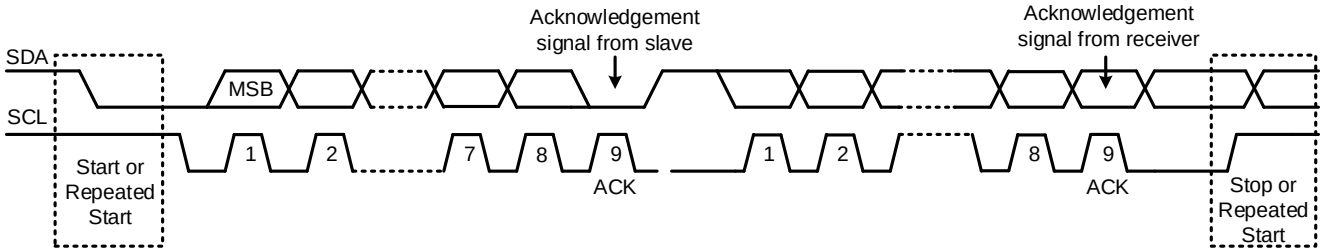


Figure 9: Data Transfer on the I²C Bus

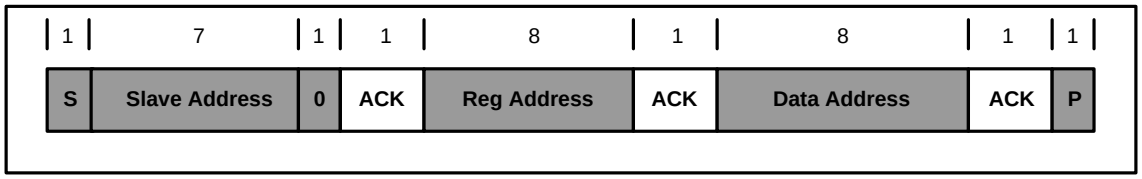


Figure 10: Single Write

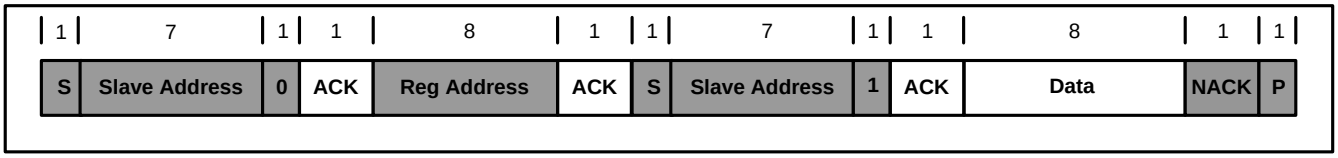


Figure 11: Single Read

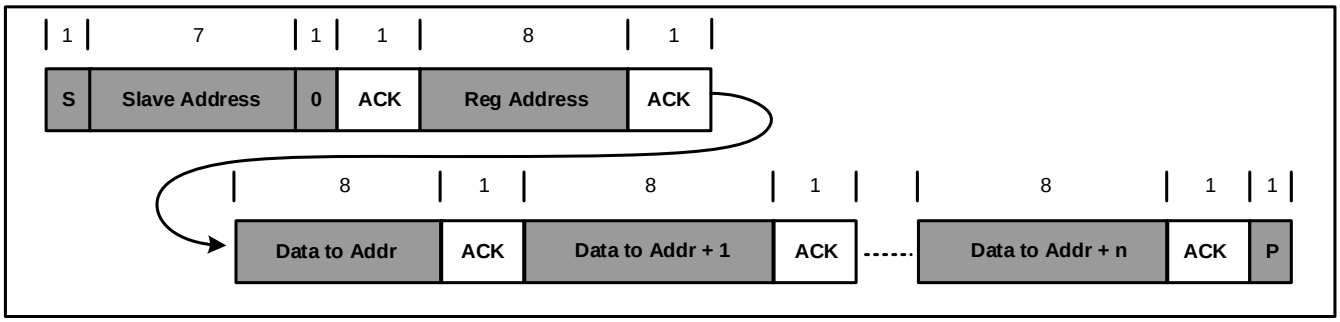


Figure 12: Multi-Write

Figure 13: Multi-Read

I²C REGISTER MAP

IC Address: 6Bh

Register Name	Address	R/W	Description
REG00h	0x00	R/W	Input voltage regulation setting and input current limit setting.
REG01h	0x01	R/W	Charge current setting and pre-charge current setting.
REG02h	0x02	R/W	Battery regulation voltage and termination current setting.
REG03h	0x03	R/W	Boost output current limit setting and cable impedance compensation.
REG04h	0x04	R/W	Boost output voltage setting and boost control.
REG05h	0x05	R	Status register.
REG06h	0x06	R	Fault register.
REG07h	0x07	R/W	Boost no-load setting and miscellaneous control.
REG08h	0x08	R/W	JEITA control.

REG00h

Bit	Name	POR	Reset by REG_RST	R/W	Description	Comment
7	REG_RST	0	Y	R/W	0: Keep current settings 1: Reset	This bit resets all registers to their default values. After a reset, this bit returns to 0 automatically.
6	EN_TIMER	1	Y	R/W	0: Disabled 1: Enabled	This bit enables the charge safety timer control. This bit is set to 1 by default.
5	VINMIN[2]	1	Y	R/W	200mV	These bits regulate the dynamic input voltage. They have a 4.45V offset, range between 4.45V and 4.8V, and are set to 200mV (4.65V) by default.
4	VINMIN[1]	0	Y	R/W	100mV	
3	VINMIN[0]	0	Y	R/W	50mV	
2	IINLIM[2]	0	Y	R/W	000: 500mA 001: 1000mA 010: 1500mA 011: 1800mA 100: 2100mA 101: 2400mA 110: 3000mA 111: 3500mA	These bits set the input current limit. They are set to 500mA by default.
1	IINLIM[1]	0	Y	R/W		
0	IINLIM[0]	0	Y	R/W		

REG01h

Bit	Name	POR	Reset by REG_RST	R/W	Description	Comment
7	ICC[4]	0	Y	R/W	1600mA	These bits set the charge current for a 10mΩ sensing resistor. They have a 500mA offset, range between 500mA and 3.6A, and are set to 1A by default. A scaling sense resistor scales the sett value at the same ratio.
6	ICC[3]	0	Y	R/W	800mA	
5	ICC[2]	1	Y	R/W	400mA	
4	ICC[1]	0	Y	R/W	200mA	
3	ICC[0]	1	Y	R/W	100mA	
2	EN_NTC	1	Y	R/W	0: Disabled 1: Enabled	This bit is set to 1 by default.
1	IPRE[1]	0	Y	R/W	01: 150mA 10: 250mA 11: 350mA	These bits set the pre-charge current with a 10mΩ sensing resistor. These bits range between 150mA and 350mA, with a 150mA default.
0	IPRE[0]	1	Y	R/W		

REG02h

Bit	Name	POR	Reset by REG_RST	R/W	Description	Comment
7	BATT_OVP_DIS	0	Y	R/W	0: Enable battery over-voltage protection (OVP) 1: Disable battery OVP	This bit is set to 0 by default.
6	BATT_REG[2]	0	Y	R/W	000: 3.6V 001: 4.1V 010: 4.2V 011: 4.3V 100: 4.35V 101: 4.4V 110: 4.45V	These bits set the regulated charge voltage. They are set to 010 by default.
5	BATT_REG[1]	1	Y	R/W		
4	BATT_REG[0]	0	Y	R/W		
3	JEITA_DIS	1	Y	R/W	0: JEITA enabled, NTC warm / cool decrease I_{CC} or V_{BATT_REG} 1: JEITA disabled, NTC warm / cool only reports status and INT	This bit is set to 1 by default.
2	ITERM[1]	0	Y	R/W	200mA	Charge termination current for a 10mΩ sensing resistor. These bits have a 100mA offset, range between 100mA and 400mA, and are set to 100mA by default.
1	ITERM[0]	0	Y	R/W	100mA	
0	CHG_EN	1	Y	R/W	0: Disable charge 1: Enable charge	This bit is set to 1 by default.

REG03h

Bit	Name	POR	Reset by REG_RST	R/W	Description	Comment
7	IOLIM[3]	1	Y	R/W	1600mA	These bits set the SYS output current limit. They have a 1A offset, range betwen 1A and 4A, and are set to 3A by default.
6	IOLIM[2]	0	Y	R/W	800mA	
5	IOLIM[1]	1	Y	R/W	400mA	
4	IOLIM[0]	0	Y	R/W	200mA	
3	RSYS_CMP[2]	0	Y	R/W	80mΩ	These bits set the SYS cable voltage drop compensation threshold. They are set to 60mΩ by default.
2	RSYS_CMP[1]	1	Y	R/W	40mΩ	
1	RSYS_CMP[0]	1	Y	R/W	20mΩ	
0	NO_LOAD	0	Y	R	0: Q2 load normal 1: Q2 no load	

REG04h

Bit	Name	POR	Reset by REG_RST	R/W	Description	Comment
7	VBOOST[2]	0	Y	R/W	-100mV	These bits set the boost regulation voltage at the PMID pin. They have a 5.2V offset, range between 5.05V and 5.225V, and are set to 5.15V by default.
6	VBOOST[1]	1	Y	R/W	-50mV	
5	VBOOST[0]	0	Y	R/W	25mV	
4	BST_EN	0	Y	R/W	0: Disable boost mode 1: Enable boost mode	This bit is set to 0 by default. Boost mode can be enabled only when V_{IN} < 2V.
3	Q2_EN	0	Y	R/W	0: Q2 is off 1: Q2 is on	This bit is set to 0 by default.
2	SYS_DSC	0	Y	R/W	0: Disable SYS discharge 1: Enable SYS discharge	This bit enables the SYS to GND discharge resistance (25Ω).
1	USB2_EN_ PLUG	1	Y	R/W	0: Disable USB2 plug-in detection 1: Enable USB2 plug-in detection	Enables the USB2 plug-in detection circuit. Toggle this bit for new detection.
0	USB2_ PLUG_IN	0	Y	R/W	0: USB2 is not plugged in 1: USB2 plug-in has been detected	After V_{SYS} is pulled up to 90% of V_{BATT}, detection starts. Once V_{SYS} drops to 75% V_{BATT}, the USB2 plug-in signal is asserted. Write 1 to this bit to reset it to 0. This bit should be cleared manually after a read to enable the next detection.

REG05h

An interrupt is asserted if any bit in REG 05h changes.

Bit	Name	POR	Reset by REG_RST	R/W	Description	Comment
7	CHIP_STAT[1]	0	Y	R	00: Idle mode 01: Charge mode 10: Boost mode 11: Power path and charge	
6	CHIP_STAT[0]	0	Y	R		
5	CHG_STAT[1]	0	Y	R	00: Not charging 01: Pre-charge 10: Constant current or constant voltage charge 11: Charge done	
4	CHG_STAT[0]	0	Y	R		
3	VPPM_STAT	0	Y	R	0: No VINPPM 1: VINPPM	
2	IPPM_STAT	0	Y	R	0: No IINPPM 1: INPPM	
1	USB1_PLUG_ IN	0	Y	R	0: USB1 is not plugged in 1: USB1 is plugged in	This bit is set to 1 when max (V_{IN_UV}, V_{BATT}+V_{HDRM}) < V_{IN} < V_{IN_OV}
0	RESERVED	0	Y	R		

REG06h

An interrupt is asserted if any bit in REG 06h changes.

Bit	Name	POR	Reset by REG_RST	R/W	Description	Comment
7	BATT_UVLO	0	Y	R	0: No battery under-voltage lockout (UVLO) has occurred 1: Battery UVLO has occurred	If the battery reaches the under-voltage lockout (UVLO) threshold, this bit is set to 1. This bit is reset to 0 once the battery is charged again.
6	SYS_SHORT	0	Y	R	0: Normal 1: A SYS short circuit has occurred	
5	BST_LMT	0	Y	R	0: Normal 1: Boost mode works in the Q2 current limit	
4	CHG_FAULT[1]	0	Y	R	00: Normal operation 01: A USB1 under-voltage (UV) condition has occurred 10: A USB1 over-voltage (OV) condition has occurred 11: The safety timer has expired	
3	CHG_FAULT[0]	0	Y	R		
2	NTC_FAULT[2]	0	Y	R	000: Normal 001: Warm 010: Cool 011: Cold 100: Hot	
1	NTC_FAULT[1]	0	Y	R		
0	NTC_FAULT[0]	0	Y	R		

REG07h

Bit	Name	POR	Reset by REG_RST	R/W	Description	Comment
7	NOLOAD_THR[1]	0	Y	R/W	00: 30mA 01: 50mA 10: 75mA 11: 100mA	These bits set the SYS no load current threshold. This bit is set to 00 by default.
6	NOLOAD_THR[0]	0	Y	R/W		
5	BATT_OVP	0	Y	R	0: The battery is operating normally 1: Battery over-voltage protection (OVP) has occurred	
4	NTC_STOP	1	Y	R/W	0: Only report in the register if NTC is outside its threshold 1: Suspend the charge and boost operation if NTC is outside its threshold	
3	VIN_OVP	0	Y	R/W	0: 6V 1: 11V	This bit sets the V_{IN} over-voltage protection (OVP) threshold.
2	SW_FREQ	0	Y	R/W	0: 700kHz 1: 1200kHz	This bit is set to 0 by default.
1	BST_IPK[1]	1	Y	R/W	00: 5A 01: 5.5A 10: 6A 11: 6.5A	These bits set the low-side switch peak current limit in boost mode. These bits are set to 11 by default.
0	BST_IPK[0]	1	Y	R/W		

REG08h

Bit	Name	POR	Reset by REG_RST	R/W	Description	Comment
7	JEITA_VSET	1	Y	R/W	0: V_{BATT_REG} - 100mV 1: V_{BATT_REG} - 200mV	This bit is set to 1 by default.
6	JEITA_ISET	1	Y	R/W	0: 14.3% of I_{CC} 1: 50% of I_{CC}	This bit is set to 1 by default.
5	VHOT	1	Y	R/W	0: 34% 1: 36%	This bit sets the hot threshold. This bit is set to 1 by default.
4	VWARM[1]	0	Y	R/W	00: 44% 01: 40% 10: 38% 11: 36%	These bits sets the warm threshold. These bits are set to 01 by default.
3	VWARM[0]	1	Y	R/W		
2	VCOOL[1]	1	Y	R/W	00: 72% 01: 68% 10: 64% 11: 60%	These bit sets the cool threshold. These bit are set to 11 by default.
1	VCOOL[0]	1	Y	R/W		
0	VCOLD	0	Y	R/W	0: 72% 1: 68%	This bit sets the cold threshold. This bit is set to 0 by default.

REG0Ah (6)

Bit	Name	POR	Reset by REG_RST	R/W	Description	Comment
7	TMR	0	N/A	N/A	0: The charge timer is 20hrs 1: The charge timer is 10hrs	This bit is set to 0 by default.
6	RESERVED	N/A	N/A	N/A	Reserved.	
5	RESERVED	N/A	N/A	N/A	Reserved.	
4	RESERVED	N/A	N/A	N/A	Reserved.	
3	VPRE	0	N/A	N/A	0: The pre-charge threshold is 3V 1: The pre-charge threshold is 2.5V	This bit is set to 0 by default.
2	RESERVED	N/A	N/A	N/A	Reserved.	
1	RESERVED	N/A	N/A	N/A	Reserved.	
0	RESERVED	N/A	N/A	N/A	Reserved.	

Note:

6) Register 0Ah is for the one-time programmable (OTP) only. It is not accessible to users.

OTP MAP

#	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
0x02	N/A	BATT_REG: 3.6V to 4.45V			N/A	N/A	N/A	N/A
0x07	NOLOAD_THR		N/A	NTC_STOP	VIN_OVP	N/A	N/A	N/A
0x0A	TMR	N/A	N/A	N/A	VPRE	N/A	N/A	N/A

OTP DEFAULT

OTP Items	Default
BATT_REG, bits[2:0]	4.2V
NOLOAD_THR, bits[1:0]	30mA
NTC_STOP	1: Suspend the charge and boost operation if NTC is outside its threshold
VIN_OVP	0: VIN_OVP = 6V
TMR	0: The charge timer is 20hrs
VPRE	0: The pre-charge threshold is 3V

APPLICATION INFORMATION

Setting the NTC Resistor

Figure 14 shows the different temperature thresholds (cold, cool, warm, and hot) that are preset by the internal voltage divider reference circuit.

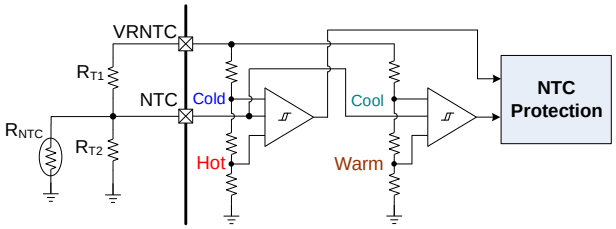


Figure 14: JEITA-Controlled NTC Protection Circuit

To set the NTC window for a given NTC thermistor, calculate R_{T1} and R_{T2} with Equation (6) and Equation (7), respectively:

$$R_{T1} = \frac{R_{NTC\_HOT} \times R_{NTC\_COLD} \times (V_{COLD} - V_{HOT})}{V_{COLD} \times V_{HOT} \times (R_{NTC\_COLD} - R_{NTC\_HOT})} \quad (6)$$

$$R_{T2} = \frac{R_{NTC\_HOT} \times R_{NTC\_COLD} \times (V_{COLD} - V_{HOT})}{V_{HOT} \times (1 - V_{COLD}) \times R_{NTC\_COLD} - V_{COLD} \times (1 - V_{HOT}) \times R_{NTC\_HOT}} \quad (7)$$

Where R_{NTC_HOT} is the value of the NTC resistor at the upper bound of its operating temperature range, and R_{NTC_COLD} is the value at the lower bound. V_{HOT} is the hot temperature threshold percentage, which can be set to 34% or 36% of V_{VRNTC}. V_{COLD} is the cold temperature threshold percentage, which can be set to 72% or 68% of V_{VRNTC}.

The warm and cool temperature thresholds can be calculated with Equation (8) and Equation (9), respectively:

$$V_{WARM} = \frac{R_{T2} // R_{NTC\_WARM}}{R_{T1} + R_{T2} // R_{NTC\_WARM}} \quad (8)$$

$$V_{COOL} = \frac{R_{T2} // R_{NTC\_COOL}}{R_{T1} + R_{T2} // R_{NTC\_COOL}} \quad (9)$$

Using the results from these calculations, choose the closest warm and cool thresholds in REG 08h.

If no external NTC is available, connect R_{T1} to R_{T2} to keep the voltage on NTC within the valid NTC window (e.g. R_{T1} = R_{T2} = 10kΩ).

Selecting the Inductor

Inductor selection requires a tradeoff between cost, size, and efficiency. A smaller-value inductance results a physically smaller inductor, but also results in greater current ripple, magnetic hysteretic losses, and output capacitance. A higher-value inductor benefits from lower ripple current and smaller output filter capacitors, but results in a greater inductor DC resistance (DCR) loss.

Table 2 shows recommended values when selecting an inductor

Table 2: Inductor Selection Guide

RS1 (mΩ)	Max Icc (A)	L (µH)
10	3.6	1
20	1.8	2.2
30	1.2	3.3
50	0.72	4.7

Choose an inductor that does not saturate under the worst-case load condition.

Selecting the PMID Capacitor (C_{PMID})

Select C_{PMID} based on the demand of the PMID current ripple for the mode being used.

In charge mode, C_{PMID} acts as the input capacitor of the buck converter in charge mode. The input current ripple can be calculated using Equation (10):

$$I_{RMS\_MAX} = I_{CC\_MAX} \times \frac{\sqrt{V_{BATT} \times (V_{IN} - V_{BATT})}}{V_{IN}} \quad (10)$$

In boost mode, C_{PMID} is the output capacitor of the boost converter. C_{PMID} keeps the system voltage ripple small and ensures feedback loop stability. The system current ripple can be estimated with Equation (11):

$$I_{RMS\_MAX} = I_{BATT} \times \frac{\sqrt{V_{BATT} \times (V_{SYS} - V_{BATT})}}{V_{SYS}} \quad (11)$$

Select the PMID capacitors based on the ripple current temperature rise, and ensure that the temperature rise does not exceed 10°C. For the best results, use ceramic capacitors with X5R dielectrics because of their low ESR and small temperature coefficients.

Compensate the Current-Sense Resistor

The soldering tin has resistance. For a 10mΩ resistor soldered on the PCB, the total resistance between the resistor pads is between 11mΩ and 12mΩ.

One method to compensate for this resistance consists of applying a resistor divider to the CSP/BATT pins (see Figure 15).

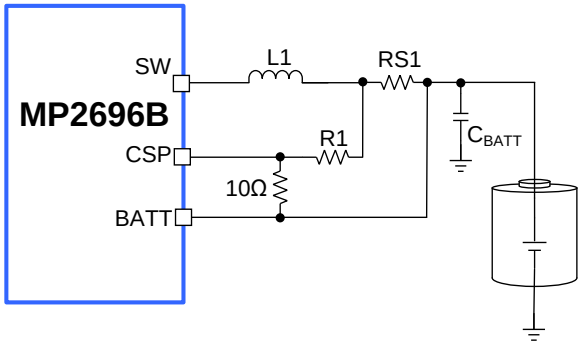


Figure 15: Current-Sense Compensation

After the PCB is assembled, apply a 2A DC current source between SW and BATT. Measure the voltage drop across the current-sense resistor on its PCB pads (V_{CS}). Calculate R1 with Equation (12):

$$R1 = \frac{V_{CS} - 2 \times RS1}{2 \times RS1} \times 10\Omega \quad (12)$$

PCB Layout Guidelines

Efficient PCB layout is critical to meet specified noise, efficiency, and stability requirements. For the best results, follow the guidelines below:

1. Place the PMID capacitor as close as possible to the PMID and PGND pins using a short copper plane connection. Place the PMID capacitor on the same layer as the IC.
2. Minimize the high-frequency current path loop between the PMID capacitor and the switching power MOSFETs (PMID pin to capacitor, capacitor to PGND pin).
3. Connect the IC's power pin to as many copper planes as possible to conduct heat away from the IC.
4. Place decoupling capacitors (e.g. the VCC pin capacitor) as close as possible to the IC pins, and make the connection as short as possible.
5. Ensure the number and physical size of the vias is sufficient for a current path.

TYPICAL APPLICATION CIRCUIT

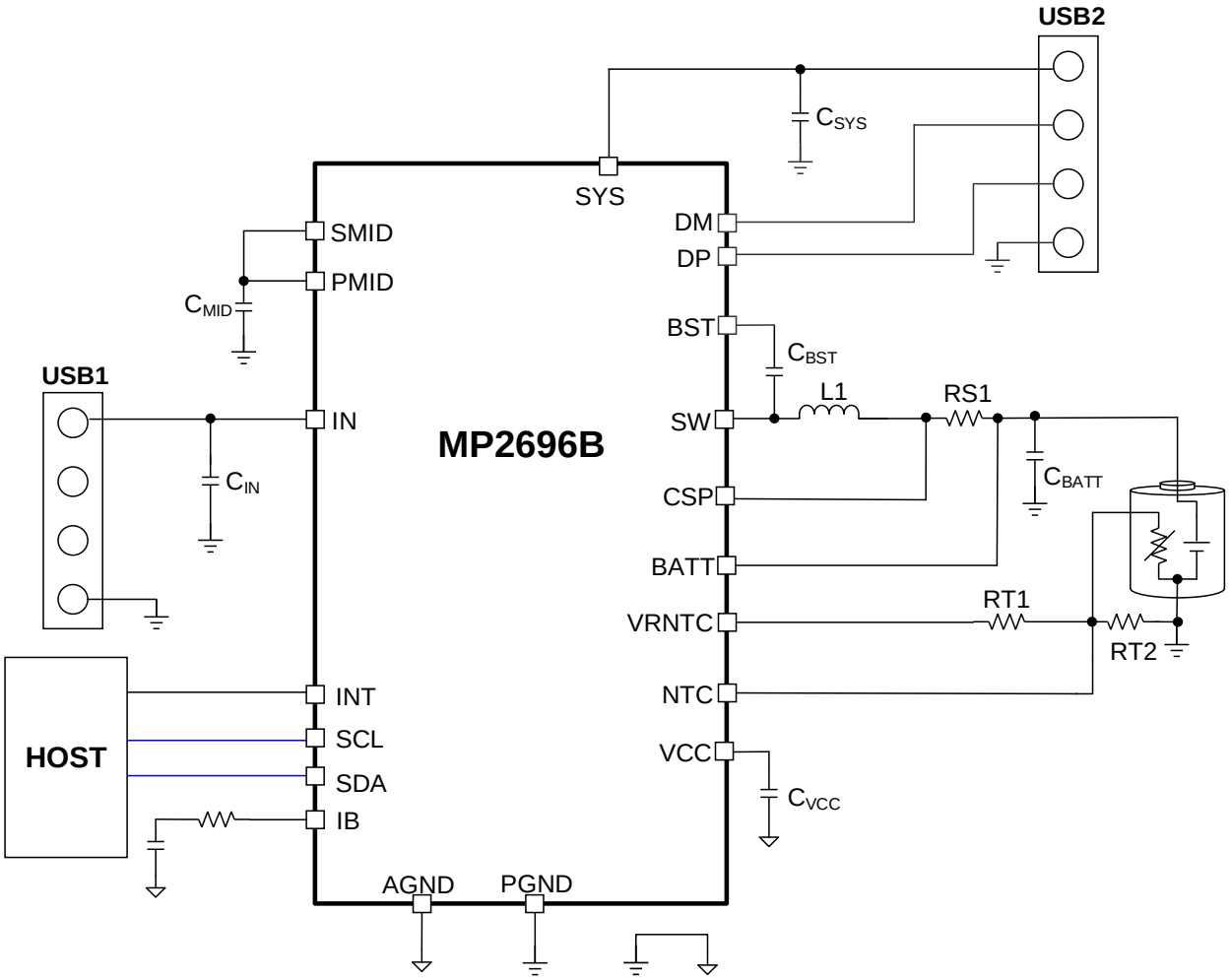


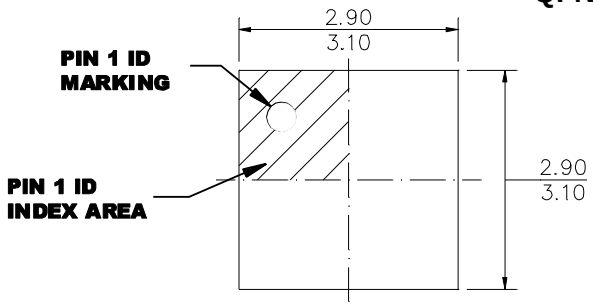
Figure 16: Typical Application Circuit for Power Bank

Table 3: Key BOM from Figure 16

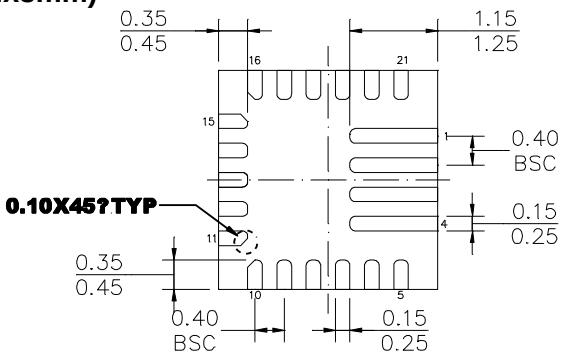
Qty	Ref	Value	Description	Package	Manufacturer
1	C_{IN}	1μF	Ceramic capacitor, 16V, X5R or X7R	0603	Any
1	C_{MID}	10μF	Ceramic capacitor, 16V, X5R or X7R	0805	Any
2	C_{SYS}	10μF	Ceramic capacitor, 16V, X5R or X7R	0805	Any
1	C_{BATT}	22μF	Ceramic capacitor, 10V, X5R or X7R	0805	Any
1	C_{VCC}	2.2μF	Ceramic capacitor, 6.3V, X5R or X7R	0603	Any
1	C_{BST}	470nF	Ceramic capacitor, 16V, X5R or X7R	0603	Any
1	L1	1μH	Inductor, 1μH, low DCR	SMD	Any
1	RS1	10mΩ	Film resistor, 1%	1206	Any

PACKAGE INFORMATION

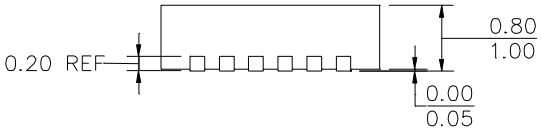
QFN-21 (3mmx3mm)



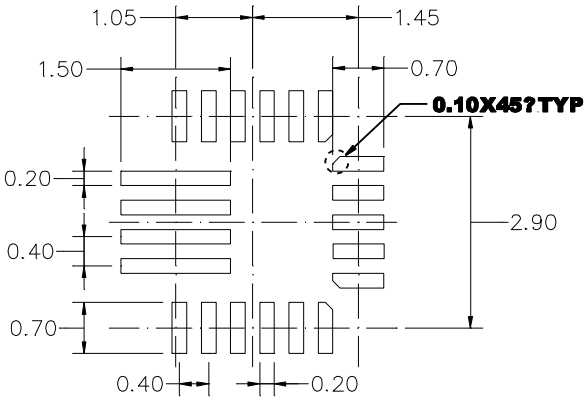
TOP VIEW



BOTTOM VIEW



SIDE VIEW

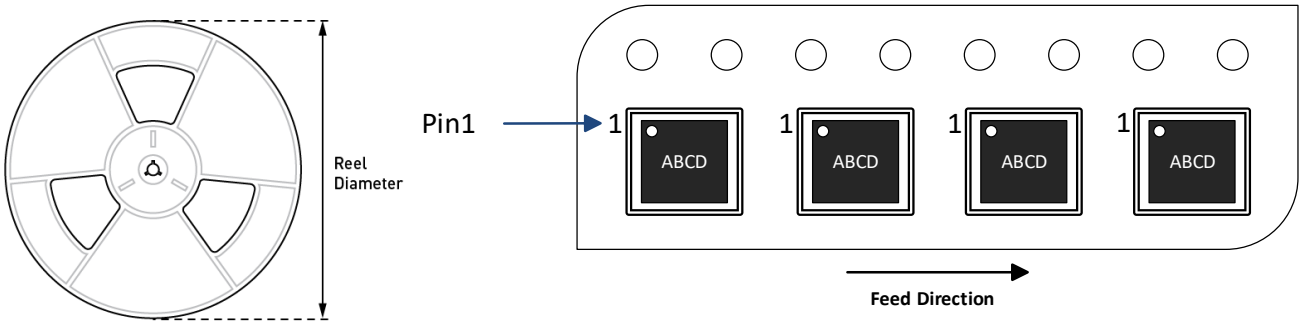


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/Reel	Quantity/ Tray	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2696BGQ-0000**	QFN-21 (3mmx3mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	4/16/2021	Initial Release	-