



# MP2695

## I<sup>2</sup>C-Controlled, Single-Cell Switching Charger with JEITA Profile

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### DESCRIPTION

The MP2695 is a highly integrated, flexible, switch-mode battery charging management device designed for a single-cell Li-ion and Li-polymer battery used in a wide range of portable applications.

The MP2695 integrates three battery-charging phases: pre-charge, constant-current, and constant-voltage charge. This device also manages the input power source by input current limit regulation and minimum input voltage regulation.

Using an I<sup>2</sup>C interface, the host can flexibly program the charge parameters. The device operating status can also be read in the registers.

Safety features include input over-voltage protection, battery under-voltage protection, thermal shutdown, and JEITA battery temperature monitoring.

The MP2695 is available in a 21-pin QFN (3mmx3mm) package.

### FEATURES

- 4.0V to 11V Operation Voltage Range
- Up to 16V Sustainable Input Voltage
- 500mA to 3.6A Programmable Charge Current
- 3.6V to 4.45V Programmable Charge Regulation Voltage with  $\pm 0.5\%$  Accuracy
- 100mA to 3A Programmable Input Current Limit with  $\pm 10\%$  Accuracy
- Minimum Input Voltage Loop for Maximum Adapter Power Tracking
- Ultra-Low 25 $\mu$ A Battery Discharge Current in Idle Mode
- Comprehensive Safety Features:
  - Fully-Customizable JEITA Profile with Programmable Temperature Threshold
  - Charge Safety Timer
  - Input Over-Voltage Protection
  - Thermal Shutdown
- Analog Voltage Output IB Pin for Battery Current Monitor
- Status and Fault Monitoring
- Available in a Small QFN-21 (3mmx3mm) Package

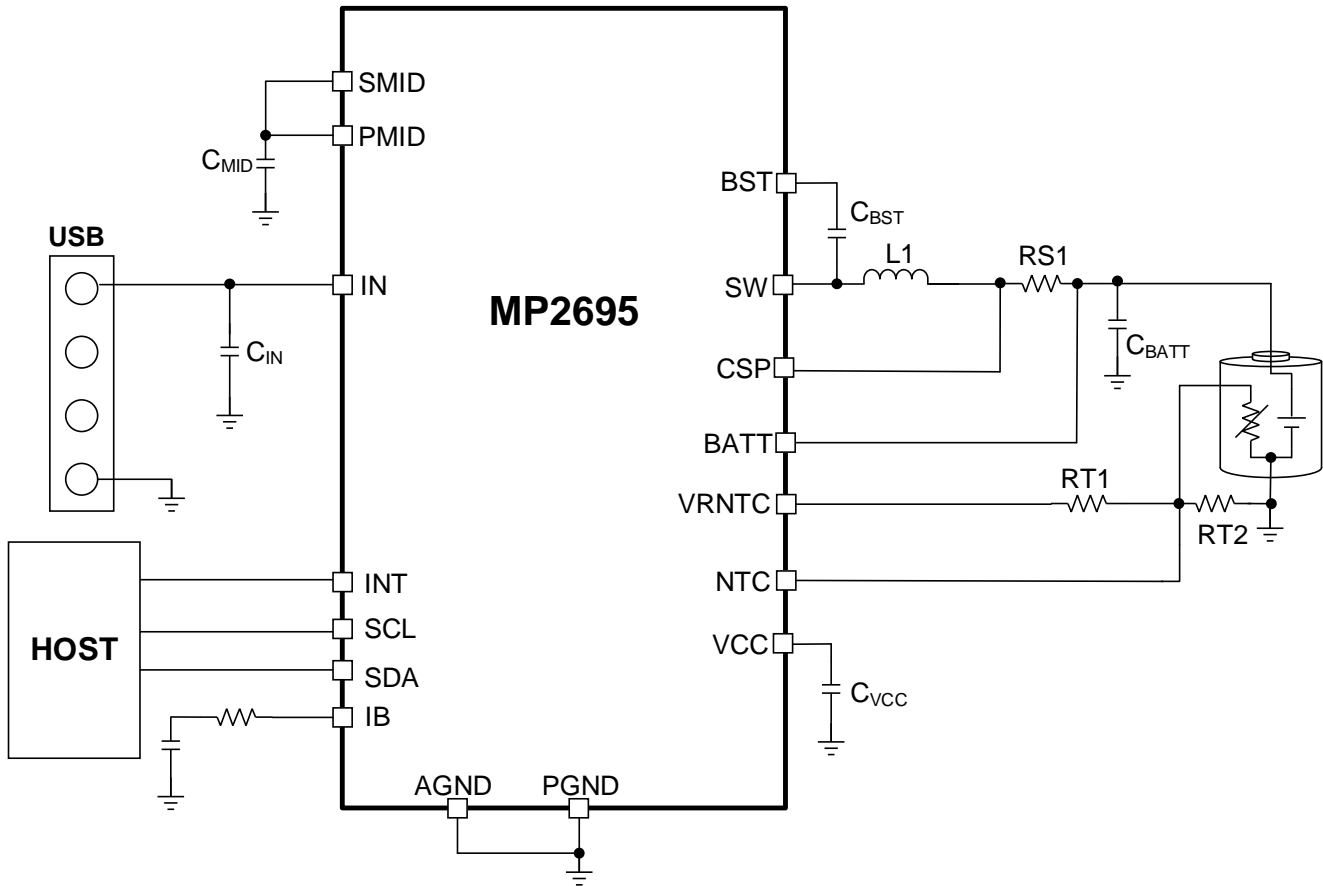
### APPLICATIONS

- Bluetooth Speakers
- Mobile Devices

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TYPICAL APPLICATION



### ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2695GQ-0000**	QFN21 (3mmx3mm)	See Below
EVKT-MP2695	Evaluation Kit	

\* For Tape & Reel, add suffix -Z (e.g. MP2695GQ-xxxx-Z).

\*\* “xxxx” is the register setting option. The factory default is “0000.” This content can be viewed in the I<sup>2</sup>C register map. Please contact an MPS FAE to obtain a value for “xxxx.”

### TOP MARKING

\_\_\_\_\_  
**BHXY**  
**LLL**

BHX: Product code of MP2695GQ

Y: Year code

LLL: Lot number

### EVALUATION KIT EVKT-MP2695

EVKT-MP2695 kit contents (items below can be ordered separately):

#	Part Number	Item	Quantity
1	EV2695-Q-00A	MP2695 evaluation board	1
2	EVKT-USB2I2C-02 bag	Includes one USB to I <sup>2</sup> C communication interface, one USB cable, and one ribbon cable	1
3	Online resources	Include datasheet, user guide, product brief, and GUI	1

Order directly from [MonolithicPower.com](http://MonolithicPower.com) or our distributors.

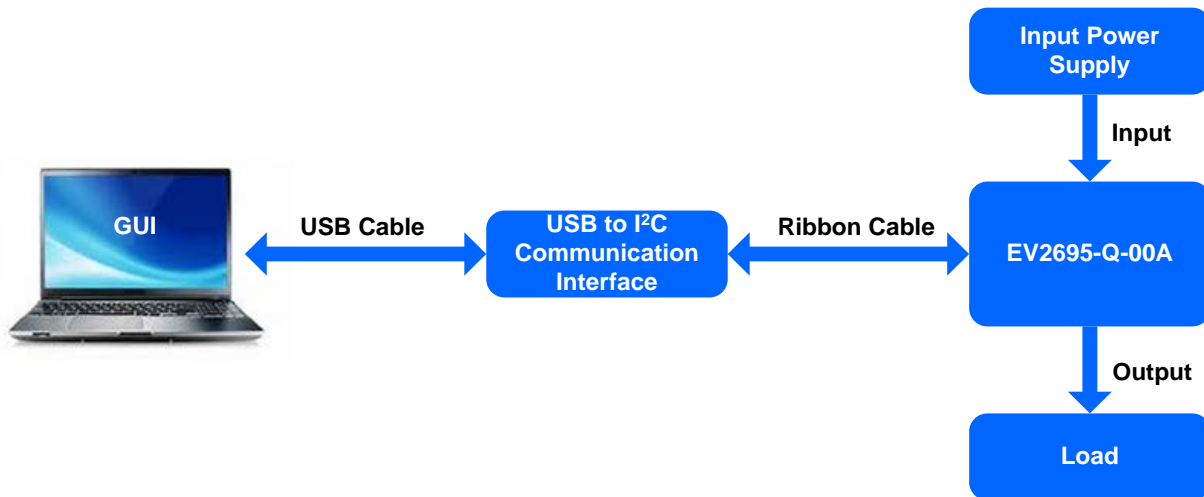
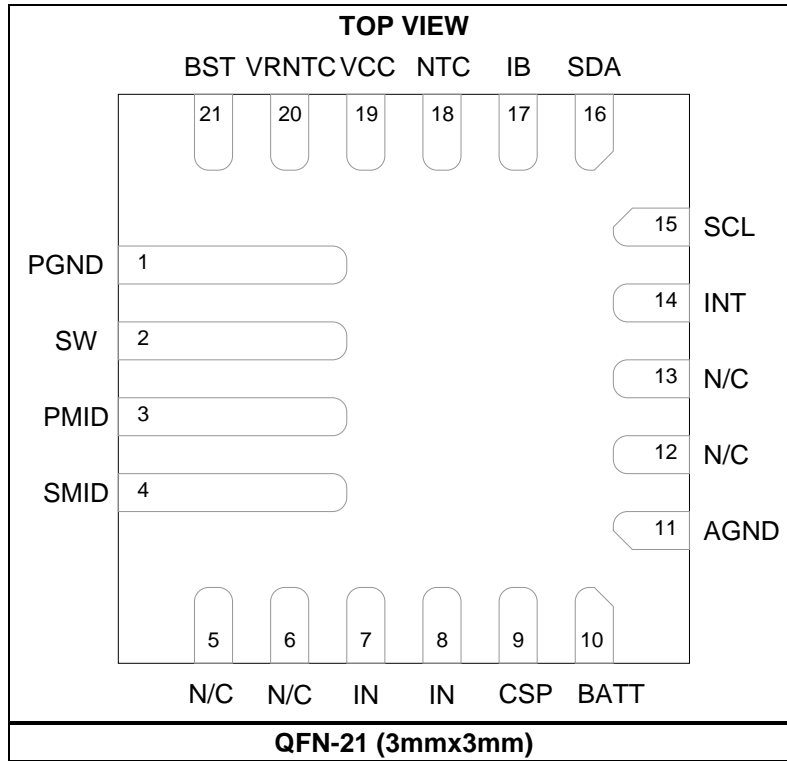


Figure 1: EVKT-MP2695 Evaluation Kit Set-Up

### PACKAGE REFERENCE



## PIN FUNCTIONS

Pin #	Name	I/O	Description
1	PGND	Power	<b>Power ground.</b>
2	SW	Power	<b>Switching output node.</b> Connect SW to the inductor.
3	PMID	Power	<b>High-side switching MOSFET drain.</b> Bypass PMID with ceramic capacitors from PMID to PGND as close to the IC as possible.
4	SMID	Power	<b>Connected to the drain of Q1 and Q2.</b> Short SMID to PMID on the PCB.
5, 6, 12, 13	N/C	-	<b>No connection.</b> Must be left open.
7, 8	IN	Power	<b>Power input of the IC.</b> Place ceramic capacitors from IN to PGND.
9	CSP	I	<b>Battery charge current-sense positive input.</b>
10	BATT	I	<b>Battery positive terminal.</b>
11	AGND	Power	<b>Analog ground.</b> Short to PGND on the PCB.
14	INT	O	<b>Open-drain interrupt output.</b> Connect INT to the logic rail through a 10kΩ resistor.
15	SCL	I	<b>I<sup>2</sup>C interface clock.</b> Connect SCL to the logic rail through a 10kΩ resistor.
16	SDA	I/O	<b>I<sup>2</sup>C interface data.</b> Connect SDA to the logic rail through a 10kΩ resistor.
17	IB	O	<b>Battery current indicator.</b> The IB voltage ( $V_{IB}$ ) indicates the charge current to the battery.
18	NTC	I	<b>Temperature-sense input.</b> Connect NTC to a negative temperature coefficient thermistor. Program the temperature window with a resistor divider from VRNTC to NTC to GND. Programmable JEITA thresholds are supported.
19	VCC	Power	<b>Internal circuit and the switch driver power supply.</b> Bypass to AGND with a ceramic capacitor as close to the IC as possible.
20	VRNTC	Power	<b>Reference voltage output for powering up NTC.</b>
21	BST	Power	<b>Bootstrap.</b> Connect a 470nF bootstrap capacitor between BST and SW to form a floating supply across the high-side power switch driver.

**ABSOLUTE MAXIMUM RATINGS** <sup>(1)</sup>

IN, PMID SMID to PGND .....	-0.3V to +16V
SW to PGND .....	-0.3V (-2V for 20ns) to ..... +14V (16V for 20ns)
BST to PGND.....	SW to SW + 5V
All other pins to AGND.....	-0.3V to +5V
Continuous power dissipation (T <sub>A</sub> = 25°C) <sup>(2)</sup> .....	2.5W
Junction temperature.....	150°C
Lead temperature (solder) .....	260°C
Storage temperature.....	-65°C to +150°C

**Recommended Operating Conditions** <sup>(3)</sup>

Supply voltage (V <sub>IN</sub> ) .....	4V to 11V
I <sub>IN</sub> .....	Up to 3A
I <sub>CC</sub> .....	Up to 3.6A
V <sub>BATT</sub> .....	Up to 4.5V
Operating junction temp (T <sub>J</sub> ) ....	-40°C to +125°C

**Thermal Resistance** <sup>(4)</sup>    **θ<sub>JA</sub>**    **θ<sub>JC</sub>**

QFN-21 (3mmx3mm) .....	50 .....	12... °C/W
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**ESD Ratings**

Human body model (HBM) <sup>(5)</sup> .....	2000V
Charged device model (CDM) <sup>(6)</sup> .....	250V

**Notes:**

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature T<sub>J</sub> (MAX), the junction-to-ambient thermal resistance θ<sub>JA</sub>, and the ambient temperature T<sub>A</sub>. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P<sub>D</sub> (MAX) = (T<sub>J</sub> (MAX) - T<sub>A</sub>) / θ<sub>JA</sub>. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on JESD51-7, 4-layer PCB.
- 5) Per ANSI/ESDA/JEDEC JS-001.
- 6) Per ANSI/ESDA/JEDEC JS-002.

## ELECTRICAL CHARACTERISTICS

$V_{IN} = 5.0V$ ,  $V_{BATT} = 3.5V$ ,  $R_{S1} = 10m\Omega$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
<b>Quiescent Current</b>						
Battery discharge current in idle mode	$I_{BATT\_IDLE}$	Idle mode		25	36	$\mu A$
Input quiescent current without switching	$I_{IN\_Q}$	$V_{IN} > V_{IN\_UVLO}$ , $V_{IN} > V_{BATT} + V_{HDRM}$ , charge disabled		0.6	1	mA
Input quiescent current when switching	$I_{IN\_QSW}$	$V_{IN} > V_{IN\_UVLO}$ , $V_{IN} > V_{BATT} + V_{HDRM}$ , charge enabled, BATT float		1		mA
<b>Power On/Off</b>						
IN operating range	$V_{IN\_OP}$	Converter switching	4		11	V
Input under-voltage lockout	$V_{IN\_UV}$	$V_{IN}$ falling	2.95	3.10	3.25	V
Input under-voltage lockout hysteresis		$V_{IN}$ rising		305		mV
Input vs. battery headroom	$V_{HDRM}$	$V_{IN}$ rising		200	310	mV
		$V_{IN}$ falling	10	80		mV
VCC LDO output voltage	$V_{VCC}$	$V_{IN} = 5V$ , $I_{VCC} = 30mA$	3.3	3.55	3.8	V
VCC under-voltage lockout	$V_{CC\_UV}$	VCC rising	1.9	2.1	2.3	V
VCC under-voltage lockout hysteresis				80		mV
<b>Power Path</b>						
IN to PMID FET (Q1) on resistance	$R_{ON\_Q1}$			25		m $\Omega$
High-side FET (Q2) on resistance	$R_{ON\_HS}$			15		m $\Omega$
Low-side FET (Q3) on resistance	$R_{ON\_LS}$			14		m $\Omega$
Peak current limit for high-side FET	$I_{HS\_PK}$	CC charge mode		6.5		A
		Pre-charge mode		1.3		A
Switching frequency	$f_{SW}$	$SW\_FREQ = 700kHz$		720		kHz
		$SW\_FREQ = 1200kHz$		1200		kHz

**ELECTRICAL CHARACTERISTICS (continued)**
 $V_{IN} = 5.0V$ ,  $V_{BATT} = 3.5V$ ,  $RS1 = 10m\Omega$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
<b>Charge Mode</b>						
Charge voltage regulation	$V_{BATT\_REG}$	BATT_REG range <sup>(7)</sup>	3.6		4.45	V
		BATT_REG[2:0] = 3.6V	3.582	3.6	3.618	V
		BATT_REG[2:0] = 4.1V	4.080	4.1	4.120	V
		BATT_REG[2:0] = 4.2V	4.179	4.2	4.221	V
		BATT_REG[2:0] = 4.3V	4.279	4.3	4.321	V
		BATT_REG[2:0] = 4.35V	4.328	4.35	4.372	V
		BATT_REG[2:0] = 4.4V	4.378	4.40	4.422	V
		BATT_REG[2:0] = 4.45V	4.428	4.45	4.472	V
Fast charge current	$I_{CC}$	ICC[4:0] = 3A	2.7	3	3.4	A
		ICC[4:0] = 1.5A	1.35	1.5	1.7	A
		ICC[4:0] = 0.5A	0.41	0.5	0.6	A
Charge termination current	$I_{TERM}$	ITERM[1:0] = 100mA	40	100	160	mA
		ITERM[1:0] = 200mA	100	200	300	mA
Recharge threshold below $V_{BATT\_REG}$	$V_{RECH}$	$V_{BATT}$ falling	100	200	320	mV
Pre-charge to fast charge threshold	$V_{BATT\_PRE}$	$V_{BATT}$ rising	2.9	3.0	3.1	V
Pre-charge to fast charge hysteresis		$V_{BATT}$ falling		290		mV
Pre-charge current	$I_{PRE}$	IPRE[1:0] = 150mA, $V_{BATT} = 1.8V$		150		mA
		IPRE[1:0] = 350mA, $V_{BATT} = 1.8V$		350		mA
Safety timer for charging cycle				20		hours
<b>Input Regulation</b>						
Input minimum voltage regulation	$V_{IN\_MIN}$	VINMIN[2:0] = 4.5V	4.41	4.51	4.61	V
		VINMIN[2:0] = 4.65V	4.56	4.66	4.76	V
Input current limit	$I_{IN\_LIM}$	IINLIM[2:0] = 3A	2.7	2.85	3	A
		IINLIM[2:0] = 1.5A	1.3	1.4	1.5	A
		IINLIM[2:0] = 0.5A	0.4	0.45	0.5	A
<b>Protection</b>						
Battery over-voltage threshold	$V_{BATT\_OVP}$		102	104	106	%
BATT over-voltage hysteresis				1.5		%
IN over-voltage protection	$V_{IN\_OVP}$	$V_{IN}$ rising, $V_{IN\_OVP} = 6V$	5.8	6	6.2	V
		$V_{IN}$ rising, $V_{IN\_OVP} = 11V$	10.6	11	11.4	V
IN over-voltage protection hysteresis		$V_{IN}$ falling		300		mV
<b>Thermal Shutdown And Temperature Control</b>						
Thermal shutdown rising threshold <sup>(7)</sup>	$T_{J\_SHDN}$	$T_J$ rising		150		$^\circ C$
Thermal shutdown hysteresis <sup>(7)</sup>				20		$^\circ C$



**ELECTRICAL CHARACTERISTICS (continued)**
**V<sub>IN</sub> = 5.0V, V<sub>BATT</sub> = 3.5V, R<sub>S1</sub> = 10mΩ, T<sub>A</sub> = 25°C, unless otherwise noted.**

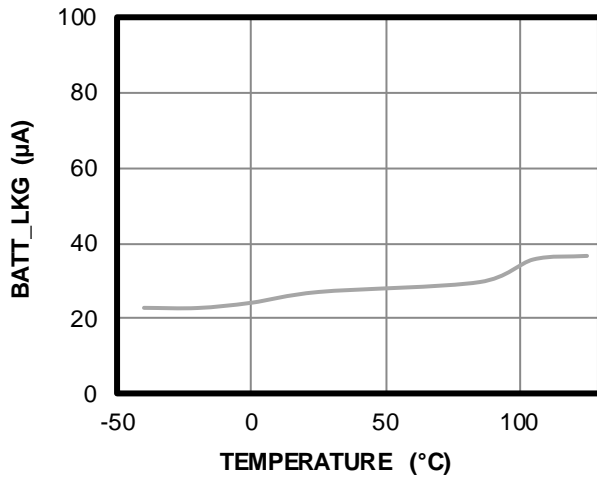
Parameters	Symbol	Condition	Min	Typ	Max	Units
VRNTC voltage	V <sub>VRNTC</sub>	V <sub>IN</sub> = 5V, I <sub>VRNTC</sub> = 100μA		3.5		V
NTC low-temp rising threshold	V <sub>COLD</sub>	As percentage of V <sub>VRNTC</sub> , V <sub>COLD</sub> [1:0] = 72%	72	73.1	74.3	%
NTC low-temp rising threshold hysteresis		As percentage of V <sub>VRNTC</sub>		1.6		%
NTC cool-temp rising threshold	V <sub>COOL</sub>	As percentage of V <sub>VRNTC</sub> , V <sub>COOL</sub> [1:0] = 60%	59.7	61	62.2	%
NTC cool-temp rising threshold hysteresis		As percentage of V <sub>VRNTC</sub>		1.6		%
NTC warm-temp falling threshold	V <sub>WARM</sub>	As percentage of V <sub>VRNTC</sub> , V <sub>WARM</sub> [1:0] = 40%	39.4	40.6	42	%
NTC warm-temp falling threshold hysteresis		As percentage of V <sub>VRNTC</sub>		1.6		%
NTC hot-temp falling threshold	V <sub>HOT</sub>	As percentage of V <sub>VRNTC</sub> , V <sub>HOT</sub> [1:0] = 36%	35.3	36.6	37.9	%
NTC hot-temp falling threshold hysteresis		As percentage of V <sub>VRNTC</sub>		1.6		%
<b>I<sup>2</sup>C Interface</b>						
Input high threshold level		SDA and SCL	1.3			V
Input low threshold level		SDA and SCL			0.4	V
Output low threshold level		I <sub>SINK</sub> = 5mA			0.3	V
I <sup>2</sup> C clock frequency	f <sub>SCL</sub>				400	kHz
<b>Battery Current Indicator</b>						
IB voltage output		I <sub>CC</sub> = 1A in charge mode	0.33	0.35	0.37	V

**Note:**

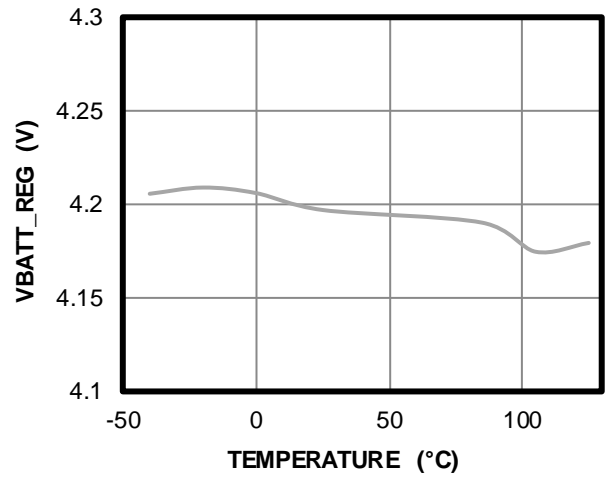
7) Guaranteed by design.

## TYPICAL CHARACTERISTICS

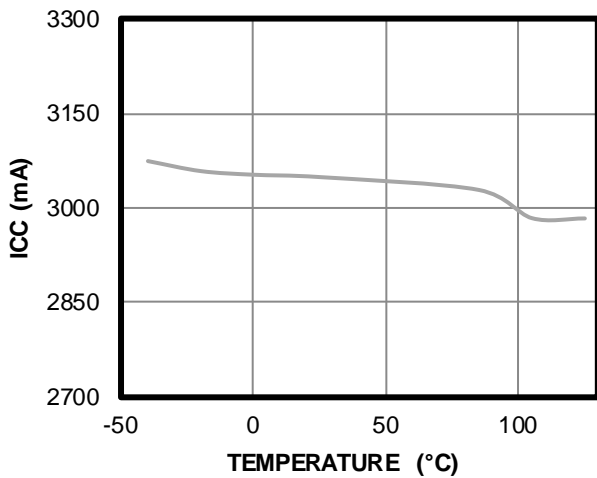
**I<sub>BATT\_LKG</sub> at BATT = 5V vs. Temperature**



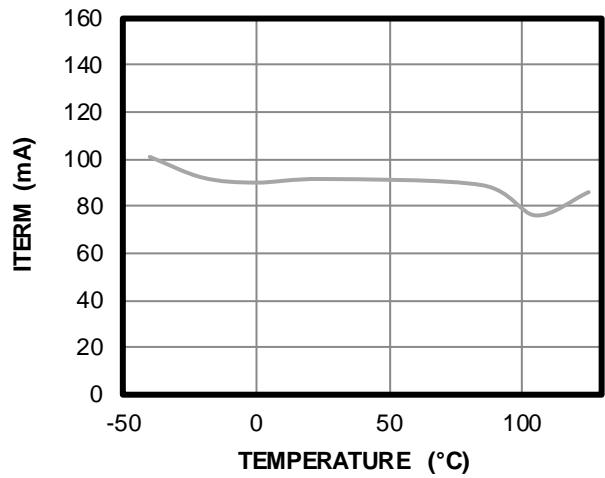
**V<sub>BATT\_REG</sub> = 4.2V vs. Temperature**



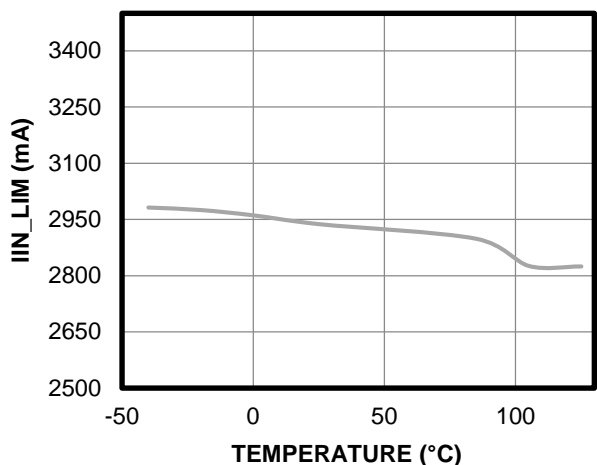
**I<sub>CC</sub> = 3A vs. Temperature**



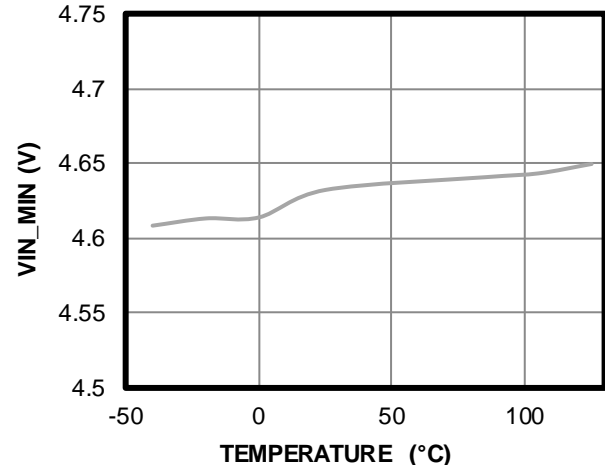
**I<sub>TERM</sub> = 100mA vs. Temperature**



**I<sub>IN\_LIM</sub> = 3A vs. Temperature**



**V<sub>IN\_MIN</sub> = 4.65V vs. Temperature**

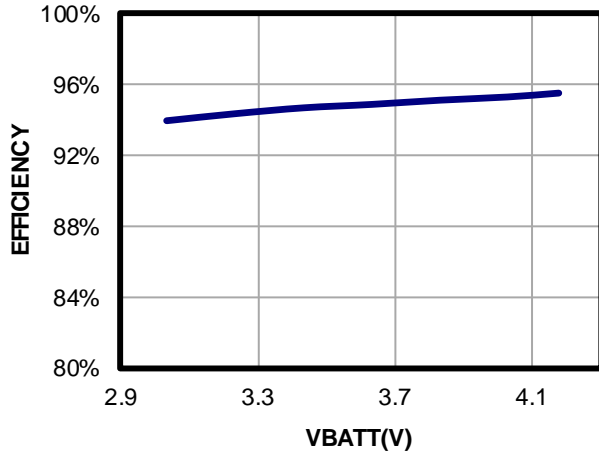


## TYPICAL PERFORMANCE CHARACTERISTICS

T<sub>A</sub> = 25°C, R<sub>S1</sub> = 10mΩ, L<sub>1</sub> = 1μH/6.5mΩ, battery simulator load, unless otherwise noted.

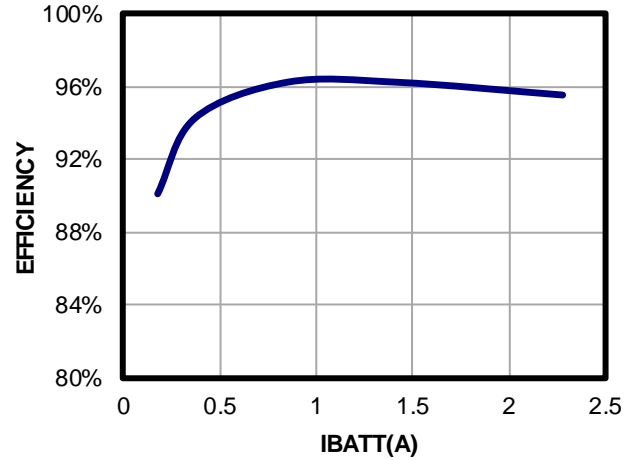
### Constant Current Charge Efficiency

V<sub>IN</sub> = 5V, I<sub>CHG</sub> = 2.5A



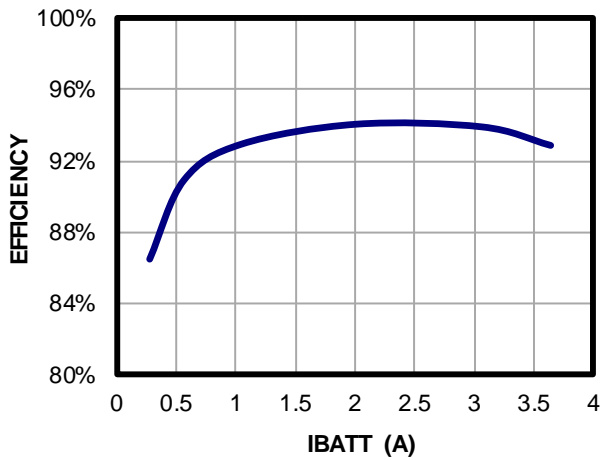
### Constant Voltage Charge Efficiency

V<sub>IN</sub> = 5V, V<sub>BATT</sub> = 4.2V



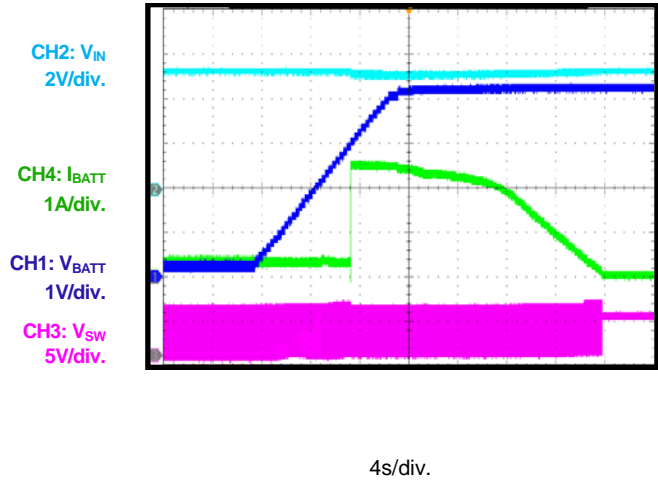
### Constant Voltage Charge Efficiency

V<sub>IN</sub> = 9V, V<sub>BATT</sub> = 4.2V



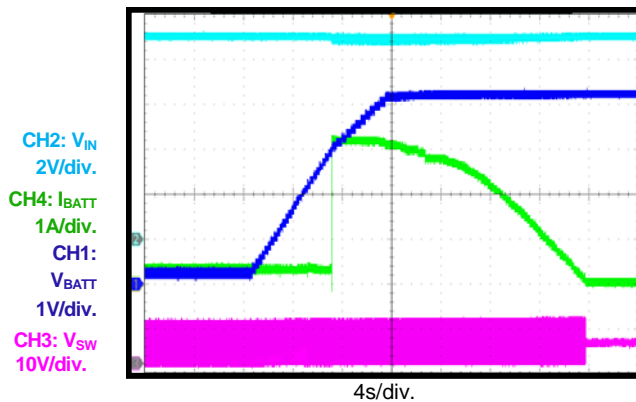
### Battery Charge Curve

V<sub>IN</sub> = 5V



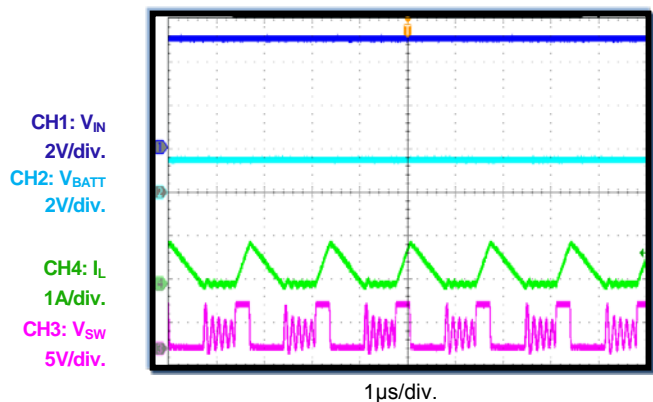
### Battery Charge Curve

V<sub>IN</sub> = 9V, I<sub>CC</sub> = 2.5A, V<sub>BATT-REG</sub> = 4.2V



### Pre-Charge Steady State

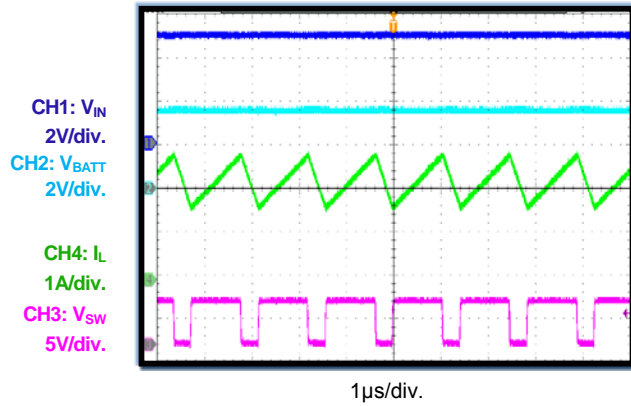
V<sub>IN</sub> = 5V, V<sub>BATT</sub> = 1.5V, I<sub>PRE</sub> = 150mA

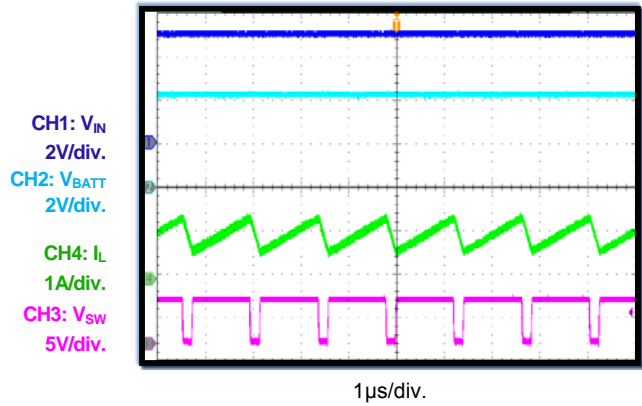


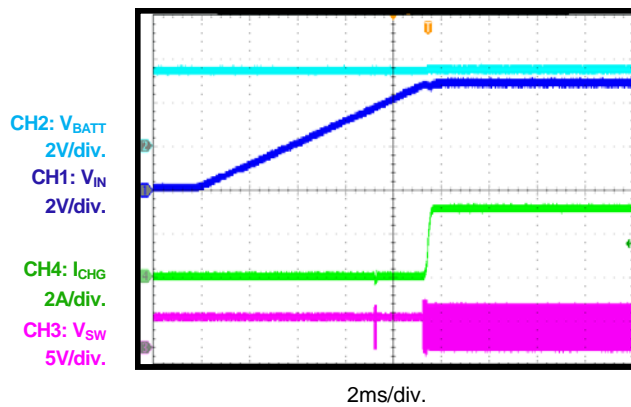
**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

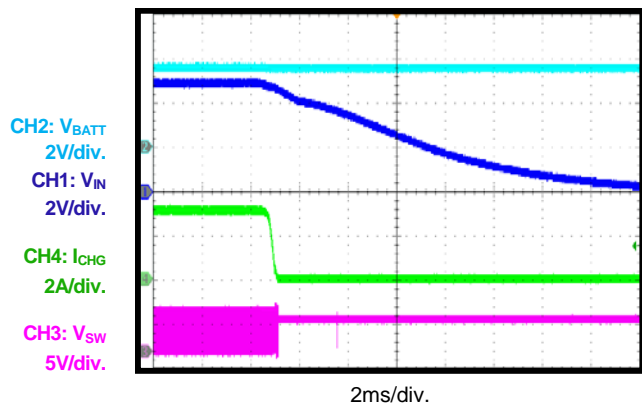
 T<sub>A</sub> = 25°C, R<sub>S1</sub> = 10mΩ, L<sub>1</sub> = 1μH/6.5mΩ, battery simulator load, unless otherwise noted.

**CC Charge Steady State**

 V<sub>IN</sub> = 5V, V<sub>BATT</sub> = 3.5V, I<sub>CC</sub> = 2A

**CV Charge Steady State**

 V<sub>IN</sub> = 5V, V<sub>BATT</sub> = 4.2V

**Power On, CC Charge Mode**

 V<sub>IN</sub> = 5V, V<sub>BATT</sub> = 3.5V, I<sub>CC</sub> = 3A

**Power Off, CC Charge Mode**

 V<sub>IN</sub> = 5V, V<sub>BATT</sub> = 3.5V, I<sub>CC</sub> = 3A


### FUNCTIONAL BLOCK DIAGRAM

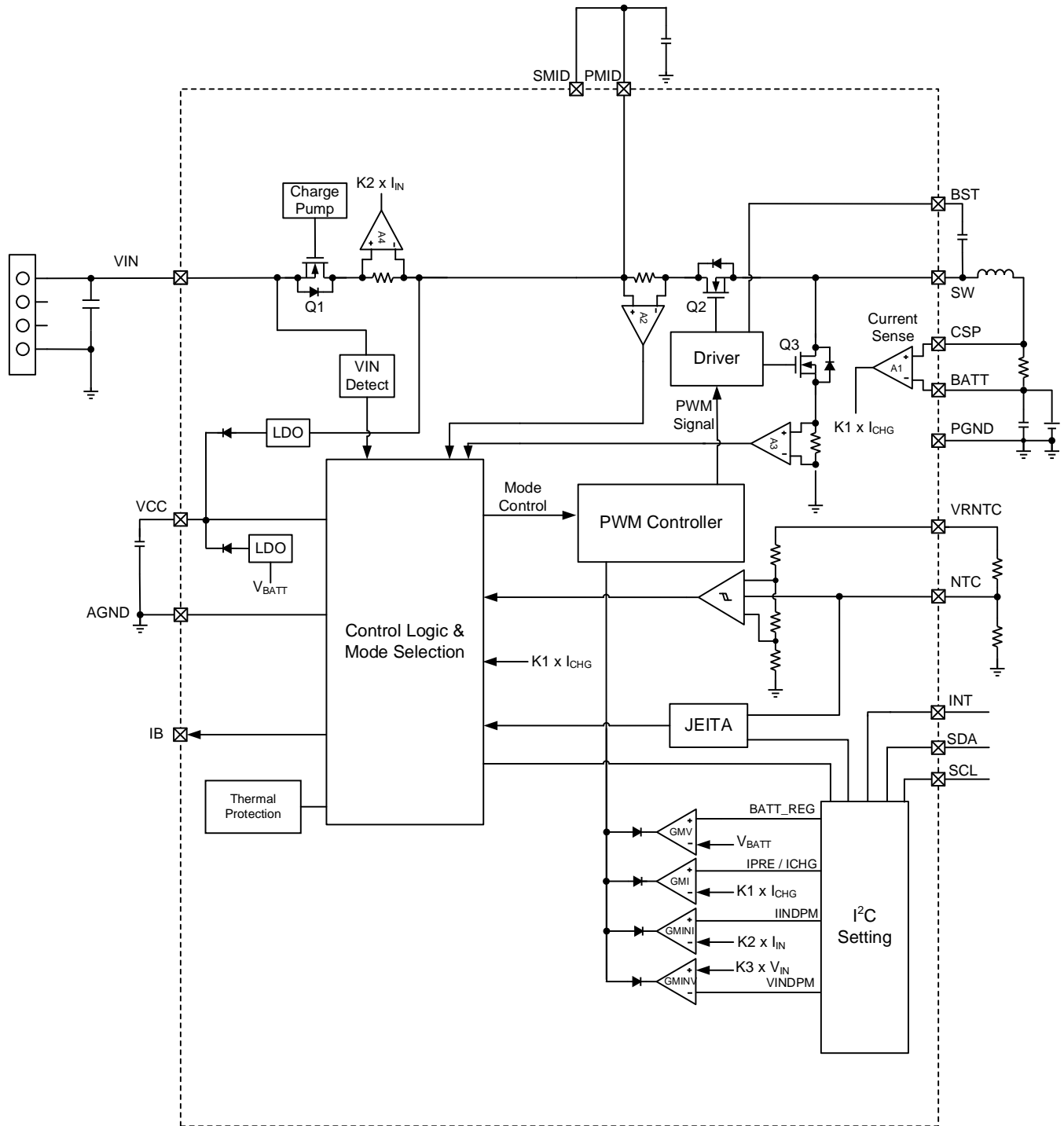


Figure 2: Functional Block Diagram

## OPERATION

### Introduction

The MP2695 is an I<sup>2</sup>C-controlled switching charger. The IC supports a precision Li-ion or Li-polymer charging system for single-cell applications. When no input is present, the IC operates at a low current to reduce power consumption from the battery.

### VCC Power Supply

VCC provides power for the internal bias circuit and the low-side switch driver. VCC is powered by whichever voltage is highest between PMID and BATT. When the VCC voltage rises above the V<sub>VCC\_UV</sub> threshold, the I<sup>2</sup>C interface is ready for communication, and all the registers reset to the default value. When the device is switching, VCC can provide up to 30mA for the external load.

### Battery Charging Profile

The IC can run a charging cycle autonomously without host involvement. The host can also control the charge operations and parameters via the registers.

A new charge cycle can start when the following conditions are met:

- V<sub>IN</sub> is above V<sub>IN\_UV</sub>
- V<sub>IN</sub> is below V<sub>IN\_OVP</sub>
- V<sub>IN</sub> is above V<sub>BATT</sub> + V<sub>HDRM</sub>
- NTC voltage is in the proper range (if NTC\_STOP is set to 1)
- No charge timer fault
- Charging is enabled (CHG\_EN = 1)
- No battery over-voltage

After the charge cycle has completed, unplug and re-insert VIN or toggle the CHG\_EN bit to start a new charge cycle.

### Charge Cycle

The IC checks the battery voltage (V<sub>BATT</sub>) to provide three main charging phases: pre-charge, constant-current (CC) charge, and constant-voltage (CV) charge (see Figure 3).

The IC regulates the voltage drop on the current-sense resistor (RS1) for the battery pre-charge and constant-current charge current. Table 1 shows the default value for a 10mΩ resistor.

**Table 1: Charge Current vs. Battery Voltage (RS1 = 10mΩ)**

Battery Voltage	Charge Current	Default Value	CHG_STAT
BATT < 3V	IPRE[1:0]	150mA	01
BATT > 3V	ICC[4:0]	1A	10

The charge current can be scaled by implementing different current-sense resistor values. The fast-charge current (I<sub>CC</sub>) can be calculated with Equation (1):

$$I_{CC} = \frac{ICC[4:0] * 10m\Omega}{RS1} \quad (1)$$

The pre-charge current (I<sub>PRE</sub>) can be calculated with Equation (2):

$$I_{PRE} = \frac{IPRE[4:0] * 10m\Omega}{RS1} \quad (2)$$

Note that the soldering tin for the current-sense resistor has resistance that must be compensated for.

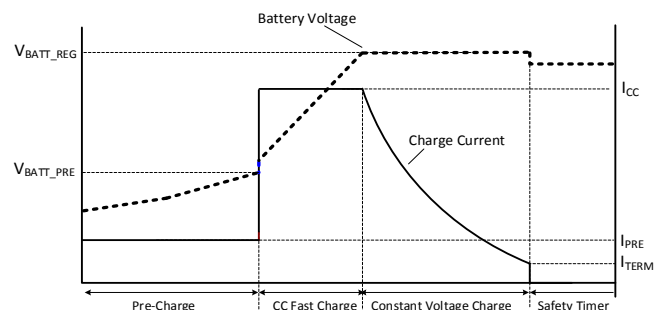
During the entire charging process, the actual charge current may be less than the register setting due to other loop regulations, such as the input current limit or the input voltage limit.

### Charge Termination

Charging terminates if the following conditions occur:

- The charge current is below the termination threshold for 20ms
- The IC works in a constant-voltage charge loop
- The IC is not in the input current loop or input voltage loop

After termination, the status register CHG\_STAT is set to 11, and an INT pulse is generated.



**Figure 3: Battery Charge Profile**

### Automatic Recharge

When the battery is fully charged and charging is terminated, the battery may be discharged because of system consumption or self-discharge. When  $V_{BATT}$  is discharged below the recharge threshold ( $V_{BATT\_REG} - 200mV$ ), the IC starts a new charging cycle automatically if the input power is valid. The timer resets when the auto-recharge cycle begins.

### Safety Timer

The IC provides a safety timer to prevent extended charging cycles caused by abnormal battery conditions. The safety timer feature can be disabled via the I<sup>2</sup>C.

The safety timer resets at the beginning of each new charging cycle. Two actions can restart the safety timer: starting a new charge cycle or toggling EN\_TIMER.

If the safety timer expires before the charge is complete, then an INT pulse is generated, the charge cycle stops, and CHG\_FAULT[1:0] becomes 11 (signaling a safety timer expiration). To clear this fault, unplug and reinsert VIN once the safety timer expires.

### Input Voltage Based and Input Current Based Power Management

The IC features both input current and input voltage based power management by continuously monitoring the input current and input voltage.

When the input current reaches the limit set by IINLIM[2:0], the charge current tapers off to keep the input current from increasing further.

If the preset input current limit is higher than the rating of the adapter, the backup input voltage based power management also works to prevent the input source from being overloaded. When the input voltage falls below the input voltage regulation threshold (set by VINMIN[2:0]) due to a heavy load, the charge current is also reduced to keep the input voltage from dropping further.

An INT pulse generates once the device enters a VINPPM or IINPPM condition.

### Thermistor Qualification

VRNTC is driven to match the VCC voltage when the IC is in charge mode. The IC continuously monitors the battery's temperature by measuring

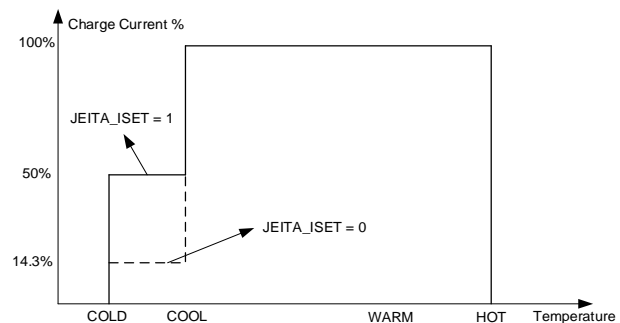
the voltage at the NTC pins. The NTC function can be disabled by setting EN\_NTC = 0.

When NTC\_STOP is set to 1, the NTC voltage should be within the  $V_{HOT}$  to  $V_{COLD}$  range for both charge operations. The IC resumes switching when the NTC voltage returns to within the  $V_{HOT}$  to  $V_{HOT}$  range.

When NTC\_STOP is set to 0, the IC only generates an interrupt (INT) signal and reports the NTC pin status if the NTC\_FAULT[2:0] bits have any changes.

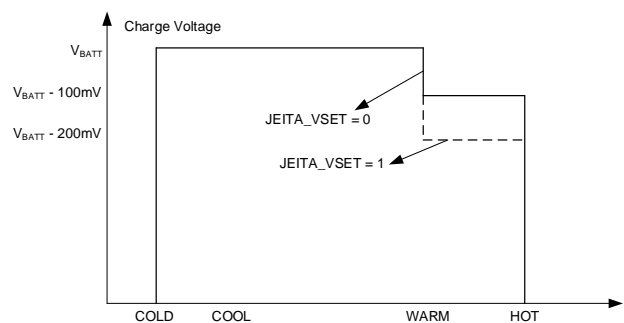
The JEITA profile is supported when the JEITA\_DIS bit is set to 0.

At a cool temperature ( $V_{COLD}$  to  $V_{COOL}$ ) range, the charge current is reduced according to the JEITA\_ISET[1:0] setting (see Figure 4).



**Figure 4: JEITA Profile – Charge Current**

At a warm temperature ( $V_{WARM}$  to  $V_{HOT}$ ) range, the charge voltage is reduced according to the JEITA\_VSET[1:0] setting (see Figure 5).



**Figure 5: JEITA Profile – Charge Voltage**

The HOT and COLD thresholds have two options in the register. The WARM and COOL thresholds have four options in the register, which offers accurate and flexible JEITA control.

### Interrupt (INT) to Host

A 50µs interrupt (INT) pulse is generated on the open drain (INT pin) if any of the following events occur:

- A good input source is detected
- The status register 05h changes
- The fault register 06h changes

### Battery Over-Voltage Protection (OVP)

If  $V_{BATT}$  exceeds 104% of  $V_{BATT\_REG}$ , then the IC stops charging, BATT\_OVP is set to 1, and an INT pulse is generated. An 800µA current source discharges the battery until it returns to the normal range.

Battery over-voltage protection (OVP) can be disabled by setting BATT\_OVP\_DIS to 1.

### Input Over-Voltage Protection (OVP)

If IN senses a voltage above the VIN\_OVP threshold, then the DC/DC converter shuts down.

The input OVP threshold can be 6V, 11V, or set via VIN\_OVP.

### Thermal Shutdown

The IC monitors the internal junction temperature to maximize power delivery and avoid overheating the chip. If the IC's junction temperature exceeds the threshold value (typically 150°C), then the converter shuts down. If the junction temperature drops to about 120°C, the MP2695 resumes normal operation.

### Battery Current Analog Output

The IC has an IB pin to monitor the real-time battery current. The IB voltage ( $V_{IB}$ ) is a fraction of the battery current. It indicates the current flowing into of the battery.

If using a 10mΩ current-sense resistor in charge mode, the IB voltage ( $V_{IB}$ ) can be calculated with Equation (3):

$$V_{IB} = I_{CHG} \times 0.36(V) \quad (3)$$

Note that scaling the current-sense resistor also scales the IB gain.

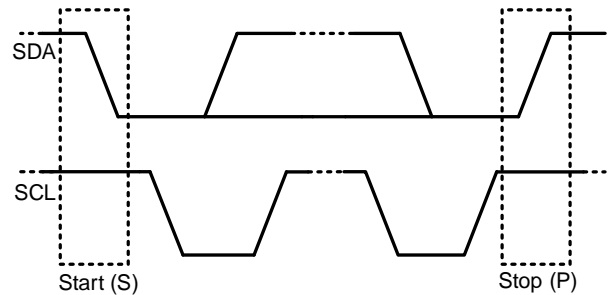
### Series Interface

The IC uses an I<sup>2</sup>C interface for setting the charging parameters and device status reporting. The I<sup>2</sup>C is a two-wire serial interface with two bus lines: a serial data line (SDA) and serial clock line

(SCL). Both SDA and SCL are open drains that must be connected to the positive supply voltage via a pull-up resistor.

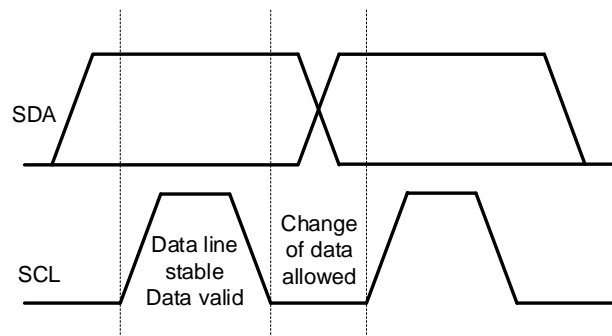
The IC operates as a slave device, receiving control inputs from the master device (e.g. a micro-controller). SCL is driven by the master device. The I<sup>2</sup>C interface supports both standard mode (up to 100 kbit/s) and fast mode (up to 400 kbit/s).

All transactions begin with a start (S) command and are terminated by a stop (P) command. Start and stop commands are generated by the master. A start command is defined as a high to low transition on SDA while SCL is high. A stop command is defined as a low to high transition on SDA while SCL is high. Figure 6 shows the start and stop commands.



**Figure 6: Start and Stop Commands**

For data validity, the data on SDA must be stable during the high clock period. The SDA high and low states only change if the clock signal on SCL is low. Every byte on SDA must be 8 bits long. The number of bytes transmitted per transfer is unrestricted. Data is transferred with the most significant bit (MSB) first.



**Figure 7: Bit Transfer on the I<sup>2</sup>C Bus**

To signal that a byte was successfully received by the transmitter, each byte has to be followed by an acknowledge (ACK) bit generated by the receiver.

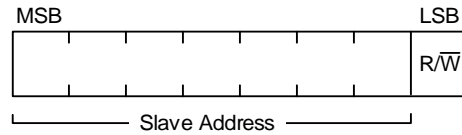


The ACK signal is defined as follows: the transmitter releases SDA during the ACK clock pulse and the receiver pulls SDA low. SDA remains low during the 9th clock's high period.

If SDA is high during the 9th clock, then the signal is defined as a not acknowledged (NACK) signal. The master then generates either a stop to abort the transfer or a repeated start to begin a new transfer.

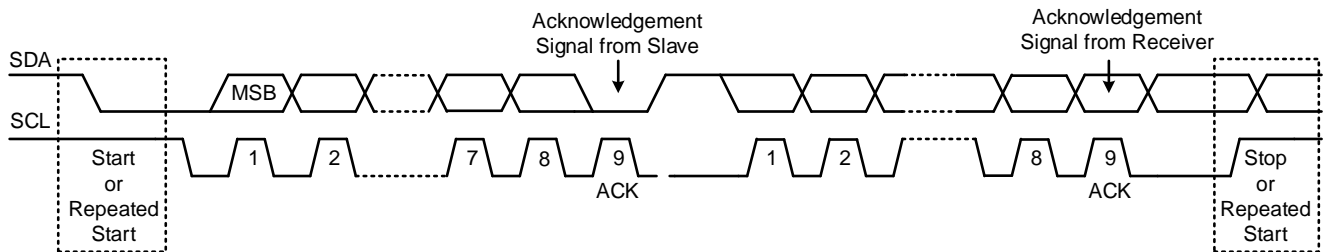
After the start signal, a slave address is sent. This address is 7 bits long, followed by an 8th data

direction bit (bit R/W). A 0 indicates a transmission (write), and a 1 indicates a request for data (read). Figure 8 shows the address arrangement.

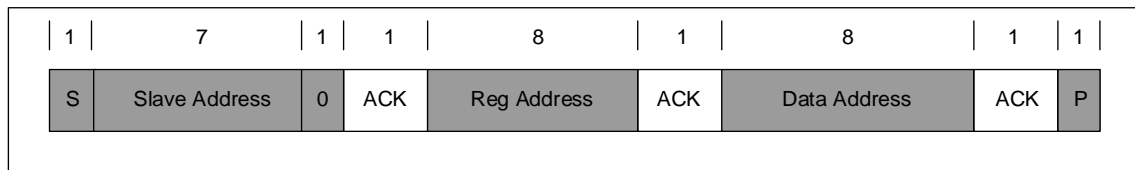


**Figure 8: 7-Bit Address**

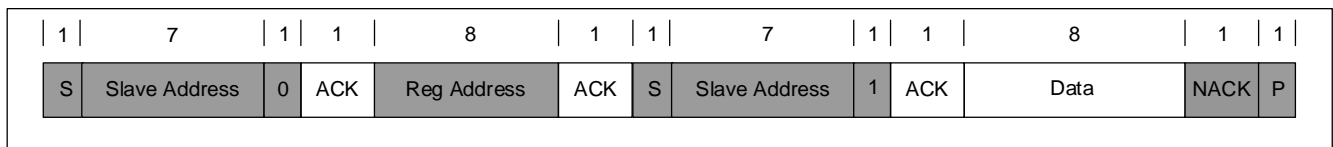
See Figure 9, Figure 10, Figure 11, Figure 12, and Figure 13 for detailed signal sequences.



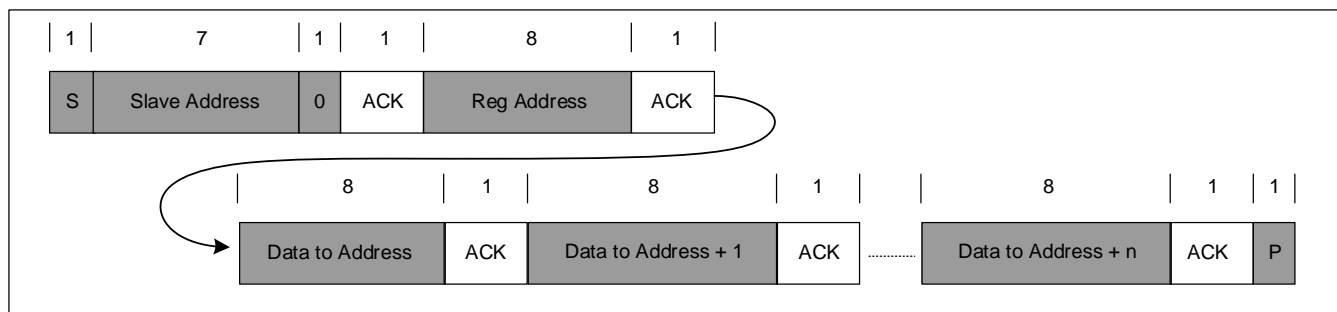
**Figure 9: Data Transfer on the I<sup>2</sup>C Bus**



**Figure 10: Single-Write**



**Figure 11: Single-Read**



**Figure 12: Multi-Write**

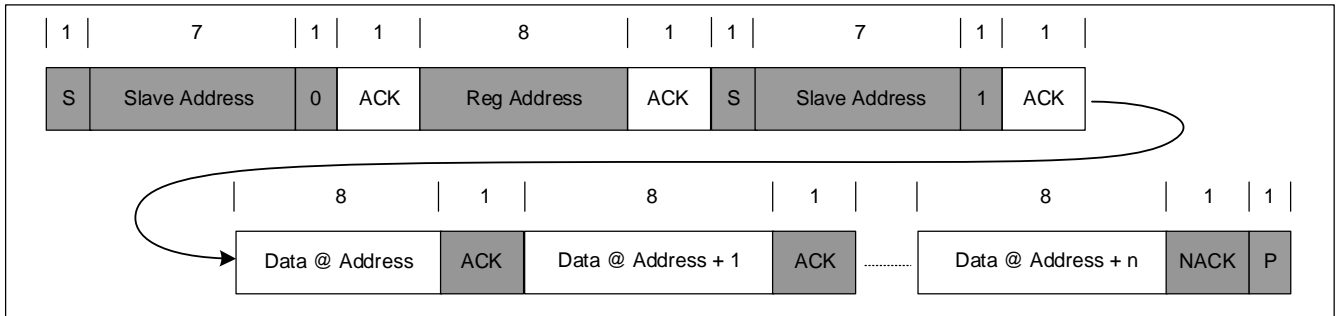


Figure 13: Multi-Read

## I<sup>2</sup>C REGISTER MAP

**IC Address: 6Bh**

Register Name	Address	R/W	Description
REG00h	0x00	R/W	Input voltage regulation setting and input current limit setting.
REG01h	0x01	R/W	Charge current setting and pre-charge current setting.
REG02h	0x02	R/W	Battery regulation voltage and termination current setting.
REG05h	0x05	R	Status register.
REG06h	0x06	R	Fault register.
REG07h	0x07	R/W	Miscellaneous control.
REG08h	0x08	R/W	JEITA control.

### REG 00h

Bit	Name	POR	Reset by REG_RST	R/W	Description	Comment
7	REG_RST	0	Y	R/W	0: Keeps current setting 1: Reset	Resets all registers to default. After reset, this bit returns to 0
6	EN_TIMER	1	Y	R/W	0: Disabled 1: Enabled (default)	Enables the safety timer
5	VINMIN[2]	1	Y	R/W	200mV (default)	Sets the input voltage dynamic regulation Offset: 4.45V Range: 4.45V to 4.8V Default: 4.65V (200mV)
4	VINMIN[1]	0	Y	R/W	100mV	
3	VINMIN[0]	0	Y	R/W	50mV	
2	IINLIM[2]	0	Y	R/W	000: 100mA 001: 500mA (default) 010: 1000mA 011: 1500mA 100: 1800mA 101: 2100mA 110: 2400mA 111: 3000mA	Sets the input current limit
1	IINLIM[1]	0	Y	R/W		
0	IINLIM[0]	1	Y	R/W		

**REG 01h**

Bit	Name	POR	Reset by REG_RST	R/W	Description	Comment
7	ICC[4]	0	Y	R/W	1600mA	Sets the charge current for the 10mΩ current-sense resistor Offset: 500mA Range: 500mA to 3.6A Default: 1A A scaling current-sense resistor scales the setting at the same ratio.
6	ICC[3]	0	Y	R/W	800mA	
5	ICC[2]	1	Y	R/W	400mA	
4	ICC[1]	0	Y	R/W	200mA	
3	ICC[0]	1	Y	R/W	100mA	
2	EN_NTC	1	Y	R/W	0: Disabled 1: Enabled (default)	
1	IPRE[1]	0	Y	R/W	01: 150mA (default) 10: 250mA 11: 350mA	Sets the pre-charge current for the 10mΩ current-sense resistor Range: 150mA to 350mA
0	IPRE[0]	1	Y	R/W		

**REG 02h**

Bit	Name	POR	Reset by REG_RST	R/W	Description	Comment
7	BATT_OVP_DIS	0	Y	R/W	0: Enabled (default) 1: Disabled	Enables OVP battery function
6	BATT_REG[2]	0	Y	R/W	000: 3.6V 001: 4.1V 010: 4.2V (default) 011: 4.3V 100: 4.35V 101: 4.4V 110: 4.45V	Sets the charge voltage regulation
5	BATT_REG[1]	1	Y	R/W		
4	BATT_REG[0]	0	Y	R/W		
3	JEITA_DIS	1	Y	R/W		
2	ITERM[1]	0	Y	R/W	200mA	Sets the charge termination current for the 10mΩ current-sense resistor Offset: 100mA Range: 100mA to 400mA
1	ITERM[0]	0	Y	R/W	100mA	
0	CHG_EN	1	Y	R/W	0: Disabled 1: Enabled (default)	Enables charge mode

**REG 05h**

Bit	Name	POR	Reset by REG_RST	R/W	Description	Comment
7	Reserved	N/A	N/A	N/A	N/A	
6	Reserved	N/A	N/A	N/A	N/A	
5	CHG_STAT[1]	0	Y	R	00: Not charging 01: Pre-charge 10: CC or CV charge 11: Charge complete	
4	CHG_STAT[0]	0	Y	R		
3	VPPM_STAT	0	Y	R	0: Does not enter V <sub>IN_LIM</sub> loop 1: Enters V <sub>IN_LIM</sub> loop	
2	IPPM_STAT	0	Y	R	0: Does not enter I <sub>IN_LIM</sub> loop 1: Enters I <sub>IN_LIM</sub> loop	
1	USB1_PLUG_IN	0	Y	R	0: Not plugged in 1: Plugged in	If (V <sub>IN_UV</sub> , V <sub>BATT</sub> + V <sub>HDRM</sub> ) < V <sub>IN</sub> < V <sub>IN_OVP</sub> , then this bit is set to 1.
0	Reserved	0	Y	R		

An interrupt signal is asserted when any bit in this register changes.

**REG 06h**

Bit	Name	POR	Reset by REG_RST	R/W	Description	Comment
7	BATT_UVLO	0	Y	R	0: No battery ULVO 1: Battery UVLO	If V <sub>BATT</sub> is below the UVLO threshold, then this bit is set to 1.  Once the battery is charged again, this bit resets to 0.
6	Reserved	N/A	N/A	N/A	N/A	
5	Reserved	N/A	N/A	N/A	N/A	
4	CHG_FAULT[1]	0	Y	R	00: Normal 01: USB1 UV 10: USB1 OV 11: Safety timer expiration	
3	CHG_FAULT[0]	0	Y	R		
2	NTC_FAULT[2]	0	Y	R	000: Normal 001: Warm 010: Cool 011: Cold 100: Hot	
1	NTC_FAULT[1]	0	Y	R		
0	NTC_FAULT[0]	0	Y	R		

An interrupt signal is asserted when any bit in this register changes.

**REG 07h**

Bit	Name	POR	Reset by REG_RST	R/W	Description	Comment
7	Reserved	N/A	N/A	N/A	N/A	
6	Reserved	N/A	N/A	N/A	N/A	
5	BATT_OVP	0	Y	R	0: Battery normal 1: Battery OVP	
4	NTC_STOP	1	Y	R/W	0: NTC out of window only reports in register 1: NTC out of window suspends charge operation	
3	VIN_OVP	0	Y	R/W	0: 6V 1: 11V	
2	SW_FREQ	0	Y	R/W	0: 700kHz (default) 1: 1200kHz	
1	Reserved	N/A	N/A	N/A	N/A	
0	Reserved	N/A	N/A	N/A	N/A	

**REG 08h**

Bit	Name	POR	Reset by REG_RST	R/W	Description	Comment
7	JEITA_VSET	1	Y	R/W	0: V <sub>BATT_REG</sub> - 100mV 1: V <sub>BATT_REG</sub> - 200mV	Default: V <sub>BATT_FULL</sub> - 200mV
6	JEITA_ISET	1	Y	R/W	0: 14.3% of ICC 1: 50% of ICC (default)	
5	VHOT	1	Y	R/W	0: 34% 1: 36% (default)	Sets the hot threshold
4	VWARM[1]	0	Y	R/W	00: 44% 01: 40% (default)	Sets the warm threshold
3	VWARM[0]	1	Y	R/W	10: 38% 11: 36%	
2	VCOOL[1]	1	Y	R/W	00: 72% 01: 68%	Sets the cool threshold
1	VCOOL[0]	1	Y	R/W	10: 64% 11: 60% (default)	
0	VCOLD	0	Y	R/W	0: 72% (default) 1: 68%	Sets the cold threshold

**REG 0Ah <sup>(8)</sup>**

Bit	Name	POR	Reset by REG_RST	R/W	Description	Comment
7	TMR	0	N/A	N/A	0: 20hrs (default) 1: 10hrs	Sets the timer duration
6	Reserved	N/A	N/A	N/A	N/A	
5	Reserved	N/A	N/A	N/A	N/A	
4	Reserved	N/A	N/A	N/A	N/A	
3	VPRE	0	N/A	N/A	0: 3V (default) 1: 2.5V	Sets the pre-charge threshold
2	Reserved	N/A	N/A	N/A	N/A	
1	Reserved	N/A	N/A	N/A	N/A	
0	Reserved	N/A	N/A	N/A	N/A	

**Note:**

8) Register 0Ah is for OTP only and is not accessible to users.

**OTP MAP**

#	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x02	N/A	BATT_REG (3.6V to 4.45V)			N/A	N/A	N/A	N/A
0x07	N/A	N/A	N/A	NTC_STOP	VIN_OVP	N/A	N/A	N/A
0x0A	TMR	N/A	N/A	N/A	VPRE	N/A	N/A	N/A

**OTP DEFAULT**

OTP items	Default
BATT_REG[2:0]	4.2V
NTC_STOP	1: NTC out of window suspends charge operation
VIN_OVP	0: VIN_OVP is 6V
TMR	0: Charge timer is 20hrs
VPRE	0: Pre-charge threshold is 3V

## APPLICATION INFORMATION

### NTC Function

The JEITA profile is supported for the battery temperature management. For a given NTC thermistor, select an appropriate  $R_{T1}$  and  $R_{T2}$  to set the NTC window.  $R_{T1}$  can be calculated with Equation (4):

$$R_{T1} = \frac{R_{NTC\_HOT} \times R_{NTC\_COLD} \times (V_{COLD} - V_{HOT})}{V_{COLD} \times V_{HOT} \times (R_{NTC\_COLD} - R_{NTC\_HOT})} \quad (4)$$

$R_{T2}$  can be calculated with Equation (5):

$$R_{T2} = \frac{R_{NTC\_HOT} \times R_{NTC\_COLD} \times (V_{COLD} - V_{HOT})}{V_{HOT} \times (1 - V_{COLD}) \times R_{NTC\_COLD} - V_{COLD} \times (1 - V_{HOT}) \times R_{NTC\_HOT}} \quad (5)$$

Where  $R_{NTC\_HOT}$  is the value of the NTC resistor at the upper bound of its operating temperature range, and  $R_{NTC\_COLD}$  is the value at its lower bound.  $V_{COLD}$  is the hot temperature threshold percentage, which can be selected as 72% or 68%.  $V_{HOT}$  is the cold temperature threshold percentage, which can be selected as 34% or 36%.

The warm temperature threshold ( $V_{WARM}$ ) can be calculated with Equation (6):

$$V_{WARM} = \frac{R_{T2} // R_{NTC\_WARM}}{R_{T1} + R_{T2} // R_{NTC\_WARM}} \quad (6)$$

The cool temperature threshold ( $V_{COOL}$ ) can be calculated with Equation (7):

$$V_{COOL} = \frac{R_{T2} // R_{NTC\_COOL}}{R_{T1} + R_{T2} // R_{NTC\_COOL}} \quad (7)$$

Choose the nearest warm/cool threshold in REG08h using the results from the calculations above.

If no external NTC is available, connect  $R_{T1}$  and  $R_{T2}$  to keep the voltage on NTC within the valid NTC window (e.g.  $R_{T1} = R_{T2} = 10k\Omega$ ).

### Selecting the Inductor

Inductor selection requires a tradeoff between cost, size, and efficiency. A lower inductance value means a smaller size, but results in higher current ripple, magnetic hysteretic losses, and output capacitances. A higher inductance value offers lower ripple current and smaller output filter capacitors, but results in higher inductor DC resistance (DCR) loss.

Table 2 shows the recommended values to choose the best inductor for the desired application.

**Table 2: Inductance Selection Guide**

RS1 (mΩ)	Max I <sub>CC</sub> (A)	L (μH)
10	3.6	1
20	1.8	2.2
30	1.2	3.3
50	0.72	4.7

Choose an inductor that does not saturate under the worst-case load condition.

### Selecting the PMID Capacitor (C<sub>PMID</sub>)

Select the PMID capacitor ( $C_{PMID}$ ) based on the demand of the PMID current ripple.

In charge mode,  $C_{PMID}$  acts as the input capacitor of the buck converter. The input current ripple ( $I_{RMS\_MAX}$ ) can be calculated with Equation (8):

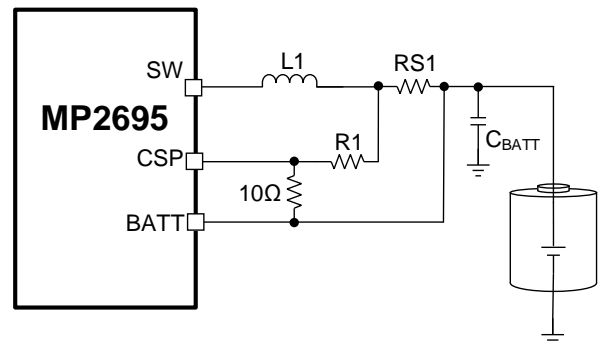
$$I_{RMS\_MAX} = I_{CC\_MAX} \times \frac{\sqrt{V_{BATT} \times (V_{IN} - V_{BATT})}}{V_{IN}} \quad (8)$$

Select the PMID capacitors based on the ripple current temperature rise not exceeding 10°C. For best results, use ceramic capacitors with X5R dielectrics, low ESR, and small temperature coefficients.

### Compensating in the Current-Sense Resistor

The soldering tin has resistance. For a 10mΩ resistor soldered on the PCB, the total resistance between resistor pads is about 11mΩ to 12mΩ.

One effective compensation method is to apply a resistor divider for the CSP/BATT pins (see Figure 14).



**Figure 14: Current-Sense Compensation**

After the PCB is assembled, apply a 2A DC current source between SW and BATT. Measure



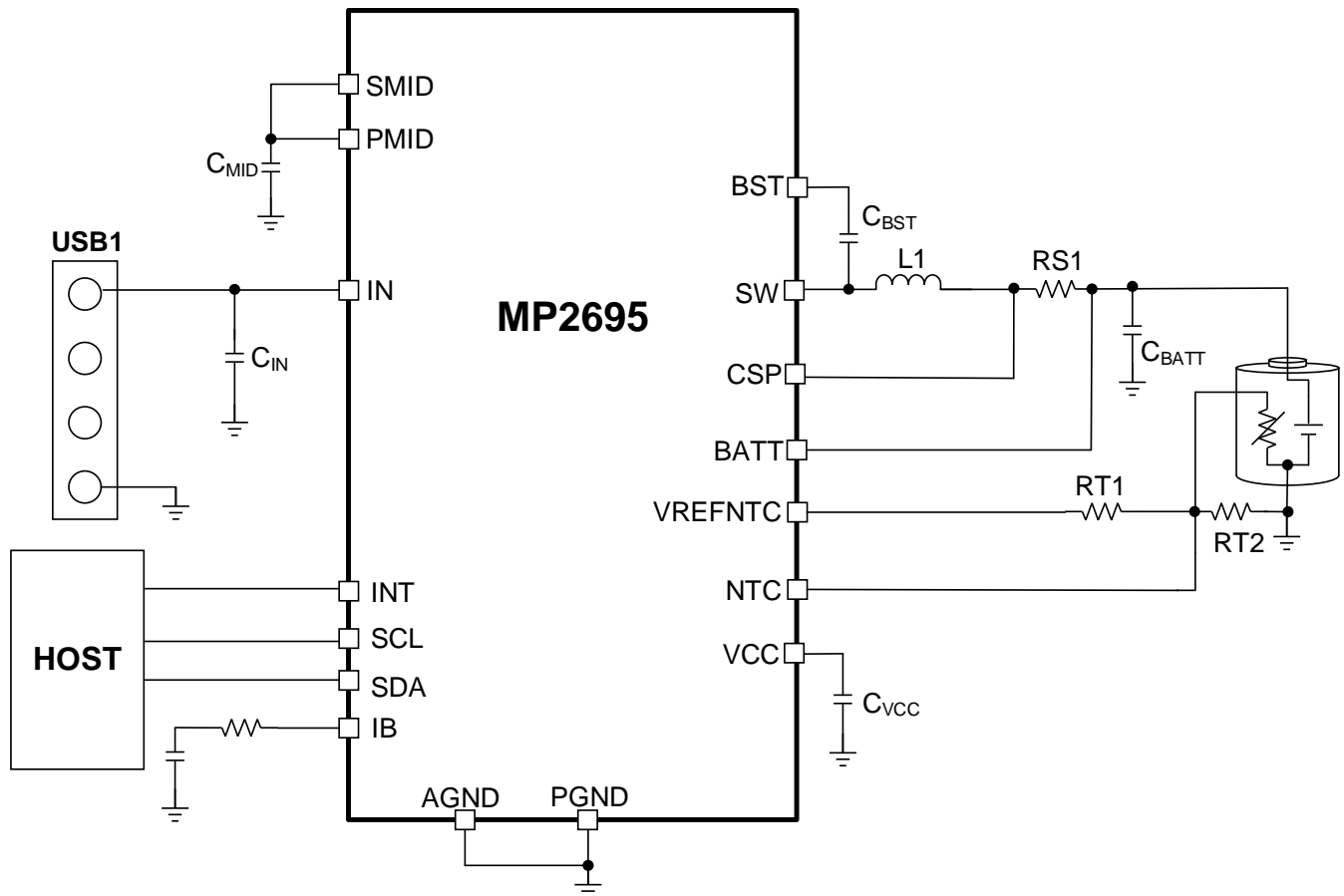
the voltage drop across the current-sense resistor on its PCB pads, which is  $V_{CS}$ . Then R1 can then be calculated with Equation (9):

$$R1 = \frac{V_{CS} - 2 \times RS1}{2 \times RS1} \times 10\Omega \quad (9)$$

### PCB Layout Guidelines

Efficient PCB layout is critical to meet specified noise, efficiency, and stability requirements. For the best performance, follow the guidelines below:

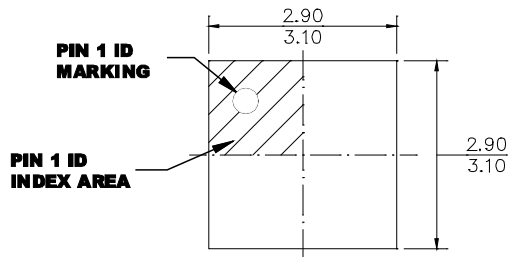
1. Place the PMID capacitor as close as possible to PMID and PGND.
2. Keep the PMID capacitor's return trace to the IC's PMID and PGND pins as short as possible.
3. Connect AGND to the ground of the PMID capacitor.
4. Keep the switching node short.
5. Connect the power pads for VIN, PMID, and PGND to as many coppers planes on the board as possible to improve thermal performance by conducting heat to the PCB.

**TYPICAL APPLICATION CIRCUIT**

**Figure 15: Typical Application Circuit for Power Bank**
**Table 3: Key BOM of Figure 15**

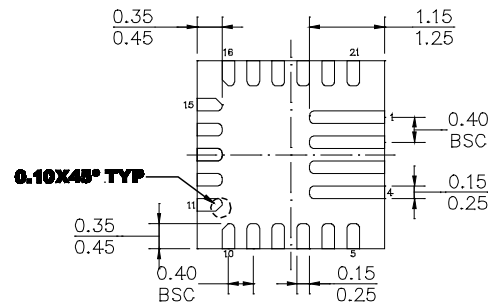
Qty	Ref	Value	Description	Package	Manufacturer
1	C <sub>IN</sub>	1 $\mu$ F	Ceramic capacitor, 16V, X5R or X7R	0603	Any
1	C <sub>MID</sub>	10 $\mu$ F	Ceramic capacitor, 16V, X5R or X7R	0805	Any
1	C <sub>BATT</sub>	22 $\mu$ F	Ceramic capacitor, 10V, X5R or X7R	0805	Any
1	C <sub>VCC</sub>	2.2 $\mu$ F	Ceramic capacitor, 6.3V, X5R or X7R	0603	Any
1	C <sub>BST</sub>	470nF	Ceramic capacitor, 16V, X5R or X7R	0603	Any
1	L1	1 $\mu$ H	Inductor, 1 $\mu$ H, low DCR	SMD	Any
1	RS1	10m $\Omega$	Film resistor, 1%	1206	Any

# PACKAGE INFORMATION

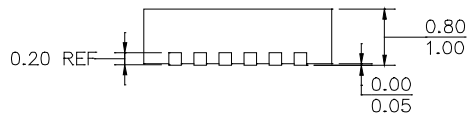
## QFN-21 (3mmx3mm)



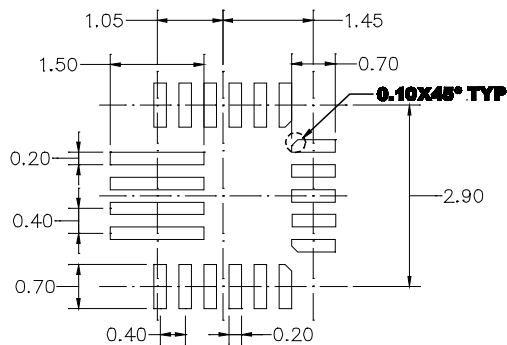
**TOP VIEW**



**BOTTOM VIEW**



**SIDE VIEW**



**RECOMMENDED LAND PATTERN**

**NOTE:**

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 3) JEDEC REFERENCE IS MO-220.
- 4) DRAWING IS NOT TO SCALE.

**REVISION HISTORY**

Revision #	Revision Date	Description	Pages Updated
1.0	04/11/2019	Initial Release	-
1.1	05/21/2021	Updated Tape & Reel suffix in the Ordering Information section from “-Z” to “-Z”	3
		Updated the I/O property of the IB, SCL, VRNTC, and BST pins in the Pin Functions table	5
		Changed the supply voltage range in the Recommended Operating Conditions section from “4.5V to +11V” to “4V to 11V” for consistency	6
		Changed IN OVP symbol in the Electrical Characteristics table from “V <sub>IN_OV</sub> ” to “V <sub>IN_OVP</sub> ” for consistency	8
		Updated graph titles	10–11
		Added the inductance and DCR information of L1 to the test conditions in the Typical Performance Characteristics section	11–12
		Changed “V <sub>IN_OV</sub> ” to “V <sub>IN_OVP</sub> ” for consistency; added abbreviation for battery voltage (V <sub>BATT</sub> ); updated the ICC default value in Table 1; updated descriptions for Equation 1 and Equation 2	14
		Updated the Safety Timer section ; added abbreviation for interrupt (INT)	15
		Updated description for Equation 3	16
		Updated I <sup>2</sup> C sections	16–18
		Updated I <sup>2</sup> C Register Map section	19–23
		Updated descriptions for Equations 4 through 9	24–25
		Updated Package Information	27
Formatting updates and clerical updates, like changed “current-sensing” to “current-sense”	All		

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