MP2652

I²C-Controlled, 2S to 5S Buck-Boost Charger with Reverse Source Mode

DESCRIPTION

The MP2652 is a buck-boost charger IC designed for battery pack with 2 cells to 5 cells in series. The device can accept a wide 4V to 22V input voltage (V_{IN}) range to charge the battery. The buck-boost topology allows the battery voltage (V_{BATT}) to be above or below V_{IN}.

When the input is present, the MP2652 operates in charge mode. It measures the battery voltage and charges the battery with four phases: constant current trickle charge, constant current pre-charge, constant current fast charge, and constant voltage charge. Other features include charge termination and auto-recharge.

The MP2652 also integrates an input current (I_{IN}) limit and V_{IN} limit to avoid overloading the input power source. This is compliant to the USB and power delivery (PD) specifications.

The MP2652 can also supply a wide 4V to 21V voltage range at the input when source mode is enabled. The device also has an output current (I_{IN_SRC}) limit with a high resolution in source mode.

The I²C/SMBus interface can configure the charge and discharge parameters, including the I_{IN} limit, V_{IN} limit, charge current, and battery-full regulation voltage in charge mode, as well as the output voltage (V_{IN_SRC}) and I_{IN_SRC} in source mode. The MP2652 can also use the registers to provide information on statuses and faults.

To guarantee safe operation, the device limits the die temperature to a configurable threshold. Other safety features include input over-voltage protection (OVP), battery OVP, thermal shutdown, and a configurable timer to prevent prolonged charging of a dead battery.

The MP2652 is available in a TQFN-30 (4mmx5mm) package.

FEATURES

- Buck-Boost Charger for 2-Cell to 5-Cell Series Battery Packs
- 4V to 22V Operation Input Voltage (V_{IN})
- Up to 26V Sustainable Voltage or 28V with External MOSFET
- Smooth Transition between Buck, Buck-Boost, and Boost Modes
- Configurable Maximum Input Current (I_{IN}) Limit and Minimum V_{IN} Limit
- Up to 6A Configurable Charge Current
- Configurable Battery-Full Voltage Up to 22V with 0.5% Accuracy
- Output Compatible with USB Power Delivery (PD) 3.0 Source Mode
- Configurable 4V to 21V Output Voltage (V_{IN_SRC}) with 20mV/Step
- Up to 6A of Output Current with 50mA/Step
- 375kHz to 770kHz Configurable f_{SW}
- I²C or SMBus Host Control Interface to Support Flexible Parameter Setting
- Input Power Source Status Indicator
- Integrated 10-Bit ADC for Monitoring in Both Charge Mode and Source Mode
- Analog Output Pin Monitors Charge Current
- Input and Battery OVP
- Output SCP in Source Mode
- Battery Missing and NTC Pin Floating Detection
- Integrated N-Channel MOSFET Driver for Input Power Pass Through or OVP
- Configurable JEITA for Battery Temperature Protection
- Thermal Regulation and Thermal Shutdown
- Available in a TQFN-30 (4mmx5mm) Package

APPLICATIONS

- Power Tools
- Wireless Speakers
- Drones
- Mobile Printers
- USB PD Multi-Cell Applications

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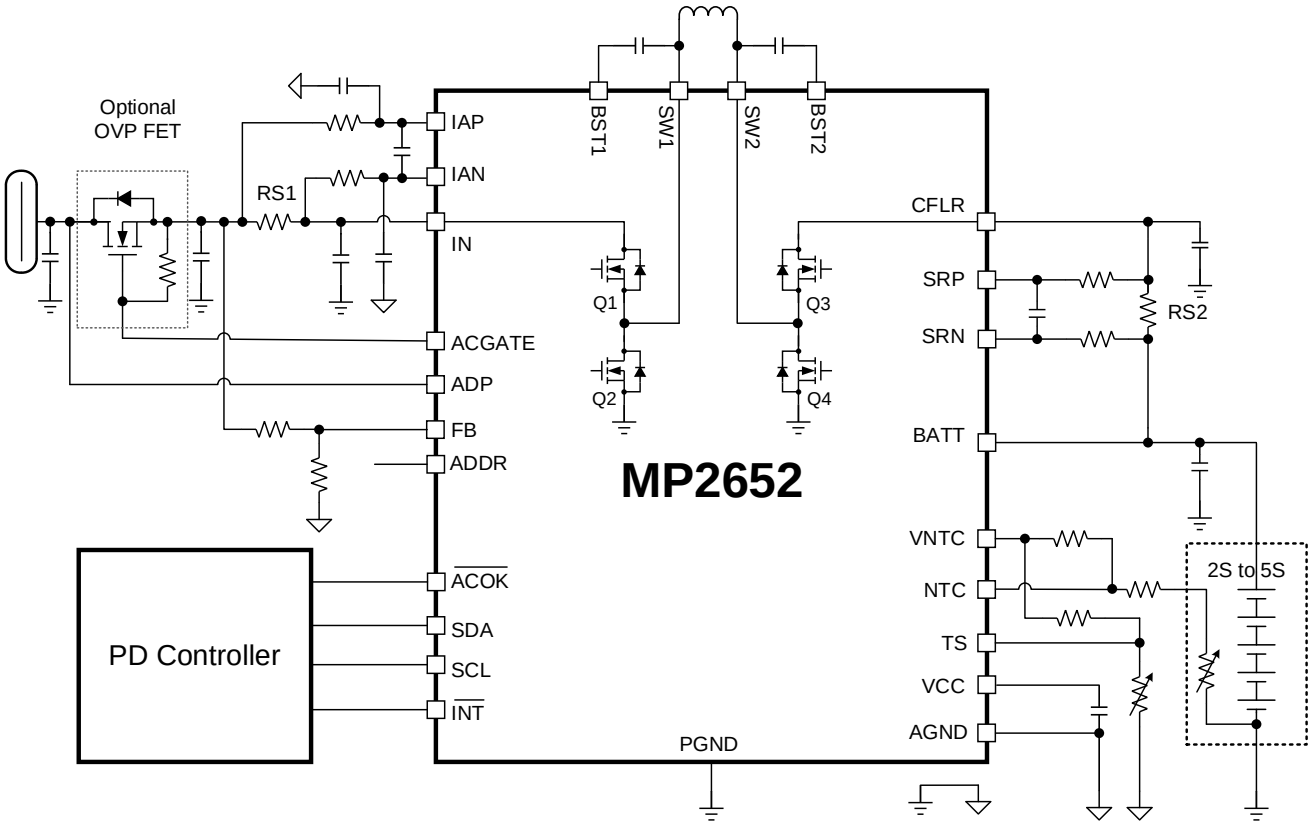
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP2652GVT-xxxx**	TQFN-30 (4mmx5mm)	*See Below*	1
MP2652GVT-0000***			
MP2652GVT-0200****			
MP2652GVT-0300****			
MP2652GVT-0400****			
EVKT-MP2652	Evaluation kit	-	-

* For Tape & Reel, add suffix -Z (e.g. MP2652GVT-xxxx-Z).

** “xxxx” is the register setting option. This content can be viewed in the I²C register map. Contact an MPS FAE to obtain an “xxxx” value.

*** The factory default “0000” code is for 5-cell applications.

**** The factory defaults “0200”, “0300”, and “0400” codes are for 2-cell applications, 3-cell applications, and 4-cell applications, respectively.

TOP MARKING

MPSYWW
MP2652
LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
MP2652: Part number
LLLLLL: Lot number

EVALUATION KIT (EVKT-MP2652)

EVKT-MP2652 kit contents (items below can be ordered separately):

#	Part Number	Item	Quantity
1	EVL2652-VT-00A	MP2652GVT-0000 evaluation board	1
2	EVKT-USBI2C-02 bag	Includes one USB-to-I²C communication interface, one USB cable, and one ribbon cable	1
3	Online resources	Include datasheet, user guide, product brief, and GUI	-

Order directly from MonolithicPower.com or our distributors.

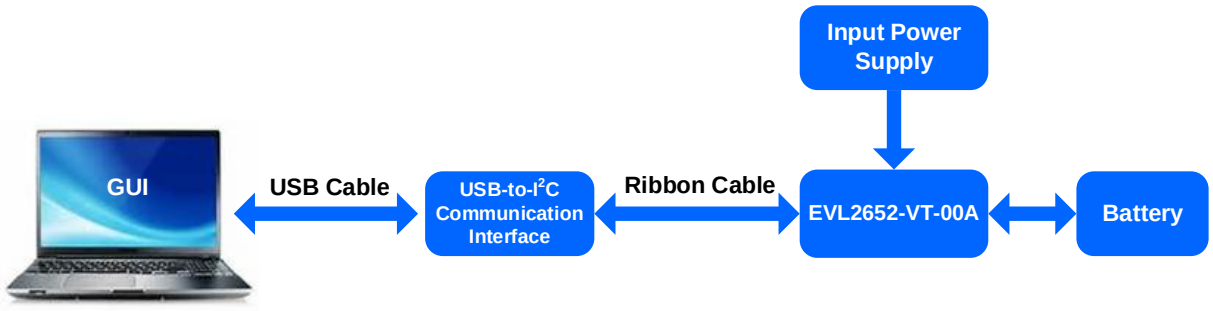

Figure 1: EVKT-MP2652 Evaluation Kit Set-Up

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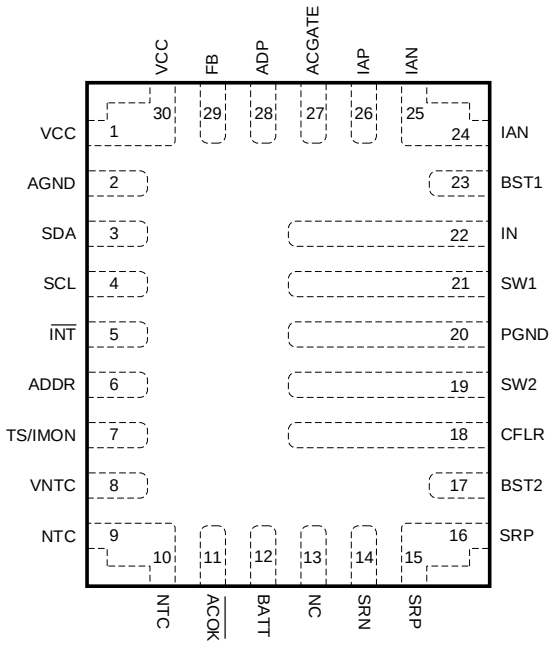
PACKAGE REFERENCE

TOP VIEW



TQFN-30 (4mmx5mm)

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PIN FUNCTIONS

Pin #	Name	Description
1, 30	VCC	**VCC low-dropout (LDO) regulator output.** Connect a 4.7µF ceramic capacitor from the VCC pin to AGND. VCC can provide a 3.6V output for the internal circuit and pulls up the open-drain pins (SCL, SDA, ACOK, INT).
2	AGND	**Analog ground.** All parameter settings refer to this ground.
3	SDA	**I²C/SMBus data.** Connect SDA to the logic rail through a 10kΩ resistor.
4	SCL	**I²C/SMBus clock.** Connect SCL to the logic rail through a 10kΩ resistor.
5	$\overline{\text{INT}}$	**Interrupt request output.** This pin is an open-drain structure that must be pulled up to VCC with an external 10kΩ resistor. This pin can be floated if it is not used.
6	ADDR	**Internal debugging pin.** Float this pin and do not use it.
7	TS/IMON	**Temperature sense/current monitor.** This pin can be set to be a temperature-sense pin (TS) or a current monitor pin (IMON). If this pin is configured to be the IMON pin, it monitors the battery current in charge or source mode.
8	VNTC	**Battery temperature-sense bias.** This pin is used for the voltage bias of the NTC and TS comparator's resistor divider.
9/10	NTC	**Negative temperature coefficient (NTC) thermistor pin.** The NTC pin is the battery's temperature-sense input.
11	$\overline{\text{ACOK}}$	**Input power good (PG) indication.** This pin has an open-drain output that indicates if the adapter is present. This pin must be externally pulled up to a voltage source.
12	BATT	**Battery voltage-sense pin.** BATT is the battery's positive terminal. Connect a 22µF ceramic capacitor from BATT to PGND, and place it as close as possible to the IC. Connect the battery as close to this pin as possible to improve V_{BATT} sense accuracy.
13	NC	**No connection.** Float this pin.
14	SRN	**Battery current-sense resistor negative terminal.**
15, 16	SRP	**Battery current-sense resistor positive terminal.**
17	BST2	**Bootstrap.** Connect a 100nF bootstrap capacitor between the BST2 and SW2 pins to form a floating supply across the power MOSFET driver to drive the power MOSFET's gate above the supply voltage.
18	CFLR	**DC/DC power stage output.** Connect two 22µF ceramic filter capacitors from CFLR to PGND, and place a 1µF capacitor as close as possible to the IC.
19	SW2	**Switching node.** SW2 is the middle point of the boost phase's half-bridge.
20	PGND	**Power ground.**
21	SW1	**Switching node.** SW1 is the middle point of the buck phase's half-bridge.
22	IN	**Input pin.** IN is the IC's power input. Connect two 10µF ceramic filter capacitors from IN to PGND, and place them as close as possible to the IC.
23	BST1	**Bootstrap.** Connect a 100nF bootstrap capacitor between the BST1 and SW1 pins to form a floating supply across the power switch driver to drive the power switch's gate above the supply voltage.
24, 25	IAN	**Input current-sense negative terminal.**
26	IAP	**Input current-sense positive terminal.**
27	ACGATE	**Input N-channel MOSFET gate driver.** ACGATE drives the external pass-through N-channel MOSFET. It is recommended to connect a 1MΩ resistor between ACGATE and the N-channel MOSFET's source port.
28	ADP	**Adapter voltage sense.** If ADP over-voltage protection (OVP) is triggered, the external OVP MOSFET (if used) and power stage turn off. The ADP pin also provides the IC's internal bias voltage. It is recommended to place three 10µF ceramic capacitors at ADP.

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PIN FUNCTIONS *(continued)*

Pin #	Name	Description
29	FB	**Feedback pin.** FB is the output voltage (V_{IN_SRC}) feedback pin in source mode. If V_{IN_SRC} at the IN pin is configured via the register in source mode, this pin is not functional. Leave this pin floating or connect it to AGND via a 10kΩ resistor.

ABSOLUTE MAXIMUM RATINGS (1)

ADP, ACGATE to PGND (DC) ..... -0.3V to +28V
IAP, IAN, IN to PGND (DC)..... -0.3V to +26V
IAP, IAN, IN to PGND (20ns) ..... -0.3V to +28V
IAP to IAN..... -3.6V to +3.6V
SW1, SW2 to PGND (DC) ..... -0.3V to +24V
SW1, SW2 to PGND (20ns)..... -2V to +28V
CFLR, BATT to PGND..... -0.3V to +24V
SRP, SRN to PGND ..... -0.3V to +24V
SRP to SRN..... -3.6V to +3.6V
VCC to AGND..... -0.3V to +4V
BST1 to SW1.....0 to 4V
BST2 to SW2.....0 to 4V
All others pins to AGND.....-0.3V to V_{CC} + 0.3V
Junction temperature (T_J) ..... 150°C
Lead temperature ..... 260°C
Continuous power dissipation (T_A = 25°C) (2)
.....3.29W
Storage temperature…. ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) 2kV
Charged-device model (CDM) 250V

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 4V to 22V
Input current (I_{IN})..... Up to 6A
Charge current (I_{CC}) ..... Up to 6A
Battery voltage (V_{BATT}) ..... Up to 22V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance θ_{JA} (4) θ_{JC} (5)

TQFN-30 (4mmx5mm)……...32……1.8 .... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) The simulated junction-to-ambient thermal resistance result and the simulation model is set up following JESD51-2 and JESD51-7.
5) The simulated junction-to-case (bottom) thermal resistance result.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, V_{BATT} = 3.7V/cell, 5-cell setting, RS1 and RS2 = 10mΩ,T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Power Characteristics						
Input voltage range	V_{IN}		4		22	V
ADP under-voltage lockout (UVLO) threshold	V_{ADP_UVLO}	ADP voltage (V_{ADP}) falling	2.4	2.6	3.05	V
ADP UVLO hysteresis		V_{ADP} rising		1		V
ADP over-voltage Protection (OVP) threshold	V_{ADP_OVP}	V_{ADP} rising	23	23.9	24.7	V
ADP OVP hysteresis		V_{ADP} falling		500		mV
ADP OVP recovery deglitch time		V_{ADP} falling		100		ms
Input under-voltage protection (UVP)	V_{IN_UVP}	V_{IN} falling, REG11h, bits[9:8] = 00	2.9	3.2	3.5	V
		V_{IN} falling, REG11h, bits[9:8] = 01	6	6.4	6.8	V
		V_{IN} falling, REG11h, bits[9:8] = 10	11.5	12	12.5	V
		V_{IN} falling, REG11h, bits[9:8] = 11	16.2	16.8	17.4	V
Input UVP threshold hysteresis		V_{IN} rising, REG11h, bits[9:8] = 01/10/11		328		mV
		V_{IN} rising, REG11h, bits[9:8] = 00		490		mV
Input UVP recovery deglitch time	t_{INUVP_DGL}	V_{IN} rising		30		ms
Input OVP threshold	V_{IN_OVP}	V_{IN} rising, REG11h, bits[7:6] = 00	6.9	7.25	7.6	V
		V_{IN} rising, REG11h, bits[7:6] = 01	10.8	11.25	11.7	V
		V_{IN} rising, REG11h, bits[7:6] = 10	17	17.65	18.25	V
		V_{IN} rising, REG11h, bits[7:6] = 11	22	22.45	23.15	V
Input OVP deglitch time	t_{INOVP_DGL}	V_{IN} rising, REG11h, bit[10] = 0		1		µs
		V_{IN} rising, REG11h, bit[10] = 1		15		ms
Input OVP hysteresis		V_{IN} falling		320		mV
Input OVP recovery deglitch time		V_{IN} falling		30		ms
DC/DC Converter						
Input quiescent current	I_{IN_Q}	V_{IN} = 5V, buck-boost and ACGATE driver are disabled, WD timer is disabled		550	620	µA
		$V_{IN_UVLO} < V_{IN} < V_{IN_OVP}$, buck-boost is disabled, ACGATE is enabled		1	1.2	mA
VCC low-dropout (LDO) regulator output voltage	V_{CC}	V_{IN} = 5V, I_{VCC} = 15mA		3.6		V
VCC LDO current limit	I_{VCC}	V_{IN} = 5V, V_{CC} = 3.3V		23		mA
IN to SW1 N-channel MOSFET (Q1) on resistance	R_{ON_Q1}			10		mΩ

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = 3.7V/cell, 5-cell setting, RS1 and RS2 = 10mΩ, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
SW1 to PGND N-channel MOSFET (Q2) on resistance	R_{ON_Q2}			8		mΩ
CFLR to SW2 N-channel MOSFET (Q3) on resistance	R_{ON_Q3}			8		mΩ
SW2 to PGND N-channel MOSFET (Q4) on resistance	R_{ON_Q4}			20		mΩ
Operation frequency	f_{SW}	REG0Eh, bits[6:4] = 000		375		kHz
		REG0Eh, bits[6:4] = 001		425		kHz
		REG0Eh, bits[6:4] = 010		475		kHz
		REG0Eh, bits[6:4] = 011		510		kHz
		REG0Eh, bits[6:4] = 100		550		kHz
		REG0Eh, bits[6:4] = 101		625		kHz
		REG0Eh, bits[6:4] = 110		700		kHz
		REG0Eh, bits[6:4] = 111		770		kHz
Battery Charger						
Battery charge voltage regulation range (6)	V_{BATT_REG}	2-cell MP2652-0200	6.8		9.34	V
		3-cell MP2652-0300	10.2		14.01	V
		4-cell MP2652-0400	13.6		18.68	V
		5-cell MP2652-0000	17		22	V
		T_A = 25°C, V_{BATT_REG} = 8.4V, MP2652-0200 (2-cell)	-0.5		+0.5	%
		T_A = 0 to 70°C, V_{BATT_REG} = 8.4V, MP2652-0200 (2-cell)	-0.7		+0.7	%

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = 3.7V/cell, 2-cell setting, RS1 and RS2 = 10mΩ, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Battery charge voltage regulation accuracy (6)		T_A = 25°C, V_{BATT_REG} = 12.6V, MP2652-0300 (3-cell)	-0.5		+0.5	%
		T_A = 0 to 70°C, V_{BATT_REG} = 12.6V, MP2652-0300 (3-cell)	-0.7		+0.7	%
		T_A = 25°C, V_{BATT_REG} = 16.8V, MP2652-0400 (4-cell)	-0.5		+0.5	%
		T_A = 0 to 70°C, V_{BATT_REG} = 16.8V, MP2652-0400 (4-cell)	-0.7		+0.7	%
		T_A = 25°C, V_{BATT_REG} = 21V, MP2652-0000 (5-cell)	-0.5		+0.5	%
		T_A = 0 to 70°C, V_{BATT_REG} = 21V, MP2652-0000 (5-cell)	-0.7		+0.7	%
Fast charge current range	I_{CC}	RS2 = 10mΩ, REG10h, bit[7] = 0	0		6.35	A
Fast charge current accuracy	I_{CC_ACC}	I_{CC} = 6A, REG14h, bits[13:6] = 0111 1000	5.79	6	6.2	A
		I_{CC} = 3A, REG14h, bits[13:6] = 0011 1100	2.84	3.0	3.14	A
		I_{CC} = 2A, REG14h, bits[13:6] = 0010 1000	1.88	2.0	2.13	A
		I_{CC} = 500mA, REG14h, bits[13:6] = 0000 1010	0.4	0.5	0.6	A
Pre-charge to fast charge threshold	V_{BATT_PRE}	REG0Bh, bit[12] = 1	2.9	3	3.1	V/cell
		REG0Bh, bit[12] = 0	2.45	2.55	2.6	V/cell
Pre-charge to fast charge deglitch time				30		ms
Pre-charge to fast charge hysteresis		2-cell MP2652-0200		160		mV
		3-cell MP2652-0300		240		mV
		4-cell MP2652-0400		315		mV
		5-cell MP2652-0000		400		mV
Pre-charge current range	I_{PRE}	RS2 = 10mΩ, REG10h, bit[7] = 0.	0		1.5	A
Pre-charge current accuracy		V_{BATT} = 5V, I_{PRE} = 300mA, REG0Fh, bits[7:4] = 0011	-20		20	%
		V_{BATT} = 5V, I_{PRE} = 500mA, REG0Fh, bits[7:4] = 0101	-15		15	%
Trickle charge (TC) to pre-charge threshold	V_{BATT_TC}	V_{BATT} rising		2		V/cell
TC to pre-charge hysteresis		V_{BATT} falling		200		mV/cell

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = 3.7V/cell, 5-cell setting, RS1 and RS2 = 10mΩ, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
TC current range	I_{TC}	RS2 = 10mΩ, REG10h, bit[7] = 0	0		750	mA
TC current accuracy		2-cell, V_{BATT} = 3V, REG0Fh, bits[11:8] = 0010, I_{TC} = 100mA	30	100	170	mA
Auto-recharge battery voltage threshold		V_{BATT} falling, V_{BATT_REG} = 4.2V/cell, REG10h, bit[11] = 0		120		mV/cell
Battery OVP threshold	V_{BATT_OVP}	V_{BATT} rising, V_{BATT_REG} = 4.2V/cell	170	230	300	mV/cell
Battery OVP hysteresis		V_{BATT} falling, V_{BATT_REG} = 4.2V/cell		113		mV/cell
Battery OVP deglitch time				30		ms
TC and pre-charge timer			1.8	2	2.2	hours
CC and CV charge timer		REG12h, bits[12:11] = 11	18	20	22	hours
Termination current accuracy	I_{TERM}	I_{TERM} = 100mA, REG0Fh, bits[3:0] = 0010	47	100	146	mA
		I_{TERM} = 200mA, REG0Fh, bits[3:0] = 0100	150	200	257	mA
		I_{TERM} = 400mA, REG0Fh, bits[3:0] = 1000	353	400	460	mA
Charge termination deglitch time	t_{TERM_DGL}			1		s
Pin Leakage Current						
SRP, SRN leakage current	$I_{LKG_SRP_SRN}$		-0.5		+0.5	μA
IAP, IAN leakage current	$I_{LKG_IAP_IAN}$		-0.5		+0.5	μA
Input Current Limit and Input Voltage Limit						
Input current limit range	I_{IN_LIM}	RS1 = 10mΩ, REG10h, bit[8] = 0	0		5.8	A
Input current limit regulation	I_{IN_LIM}	REG08h, bits[6:0] = 000 1010, I_{IN_LIM} = 0.5A	0.368	0.43	0.5	A
		REG08h, bits[6:0] = 001 0010, I_{IN_LIM} = 0.9A	0.768	0.82	0.9	A
		REG08h, bits[6:0] = 001 1110, I_{IN_LIM} = 1.5A	1.32	1.41	1.5	A
		REG08h, bits[6:0] = 011 1100, I_{IN_LIM} = 3.0A	2.76	2.87	2.98	A
		REG08h, bits[6:0] = 110 0100, I_{IN_LIM} = 5.0A	4.688	4.836	4.98	A

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = 3.7V/cell, 5-cell setting, RS1 and RS2 = 10mΩ, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Minimum input voltage regulation	V_{IN_MIN}	REG06h, bits[7:0] = 0011 1001, V_{IN_MIN} = 4.56V	4.44	4.58	4.72	V
		REG06h, bits[7:0] = 1000 0010, V_{IN_MIN} = 10.4V	10.19	10.4	10.61	V
		REG06h, bits[7:0] = 1010 1010, V_{IN_MIN} = 13.6V	13.33	13.6	13.87	V
		REG06h, bits[7:0] = 1110 0111, V_{IN_MIN} = 18.48V	18.11	18.48	18.85	V
Thermal Regulation and Protection						
Thermal shutdown rising threshold (7)	T_{J_SHDN}	T_J rising		150		°C
Thermal shutdown hysteresis (7)				20		°C
Thermal regulation threshold	T_{J_REG}	REG0Fh, bits[14:12] = 111		120		°C
Battery Temperature Monitoring						
Negative temperature coefficient (NTC) floating threshold	V_{NTC_FLT}	V_{NTC} rising, as a percentage of V_{VNTC}		95		%
NTC floating threshold hysteresis		V_{NTC} falling, as a percentage of V_{VNTC}		3		%
NTC cold temp threshold	V_{COLD}	V_{NTC} rising, as a percentage of V_{VNTC}, REG0Dh, bits[1:0] = 01	73.5	74.5	75.5	%
NTC cold temp threshold hysteresis		V_{NTC} falling, as a percentage of V_{VNTC},		1.2		%
NTC cool temp threshold	V_{COOL}	V_{NTC} rising, as a percentage of V_{VNTC},REG0Dh, bits[3:2] = 10	64.2	65.2	66.2	%
NTC cool temp threshold hysteresis		V_{NTC} falling, as percentage of V_{VNTC}		1.2		%
NTC warm temp threshold	V_{WARM}	V_{NTC} falling, as a percentage of V_{VNTC}, REG0Dh, bits[5:4] = 01	32.2	33.2	34.2	%
NTC warm temp threshold hysteresis		V_{NTC} rising, as percentage of V_{VNTC}		1.2		%
NTC hot temp threshold	V_{HOT}	V_{NTC} falling, as a percentage of V_{NTC}, REG0Dh, bits[7:6] = 10	22.6	23.6	24.6	%
NTC hot temp threshold hysteresis		V_{NTC} rising, as a percentage of V_{NTC}		1.2		%
TS hot	V_{TS_HOT}	REG0Dh, bits[12:10] = 100	12.24	14.95	15.66	%
VNTC voltage	V_{VNTC}		1.26	1.28	1.30	V

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = 3.7V/cell, 5-cell setting, RS1 and RS2 = 10mΩ, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Source Mode						
Output voltage in source mode	V_{IN_SRC}	I_{IN_SRC} = 0A, V_{BATT} = 7.6V, REG09h, bits[9:0] = 00 1111 1010	4.85	5.0	5.15	V
		I_{DSCHG} = 0A, V_{BATT} = 7.6V, REG09h, bits[9:0] = 01 1100 0010	8.82	9.0	9.18	V
		I_{DSCHG} = 0A, V_{BATT} = 7.6V, REG09h, bits[9:0] = 10 0101 1000	11.76	12.0	12.24	V
		I_{DSCHG} = 0A, V_{BATT} = 7.6V, REG09h, bits[9:0] = 10 1110 1110	14.7	15.0	15.3	V
		I_{DSCHG} = 0A, V_{BATT} = 7.6V, REG09h, bits[9:0] = 11 1110 1000	19.7	20.0	20.3	V
FB reference voltage for external setting	V_{FB}	REG09h, bits[9:0] = 11 1110 1000	1.194	1.206	1.228	V
		REG09h, bits[9:0] = 00 1111 1010	0.306	0.313	0.32	V
Output OVP in source mode	$V_{IN_SRC_OV}$	V_{BATT} = 7.4V, V_{IN_SRC} rising, percentage of discharge voltage setting, REG11h, bits[14:13] = 11		110		%
Output OVP hysteresis in source mode		V_{IN_SRC} falling		5		%
Output UVP in source mode	$V_{IN_SRC_UV}$	REG11h, bits[12:11] = 00		75		%
Output UVP hysteresis in source mode				5		%
Discharge output UV deglitch time		V_{IN_SRC} falling		10		ms
Discharge output UV recovery deglitch time		V_{IN_SRC} rising		30		ms
Output current regulation in discharge mode	I_{IN_SRC}	REG0Ah, bits[6:0] = 001 0010, V_{BATT} = 7.4V	0.9			A
		REG0Ah, bits[6:0] = 001 1110, V_{BATT} = 7.4V	1.5			A
		REG0Ah, bits[6:0] = 011 1111, V_{BATT} = 7.4V	3.0			A
Battery UVLO threshold	V_{BATT_UVLO}	V_{BATT} falling	2.5	2.6	2.7	V/cell
Battery UVLO hysteresis		V_{BATT} rising		280		mV
Battery low voltage threshold	V_{BATT_LOW}	V_{BATT} falling, REG0Bh, bits[10:9] = 10	3.1	3.2	3.3	V/cell
Battery low voltage hysteresis		V_{BATT} rising		200		mV/cell

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = 3.7V/cell, 5-cell setting, RS1 and RS2 = 10mΩ, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Battery low voltage deglitch time		V_{BATT} falling		30		ms
Battery standby current	$I_{BATT_STANDBY}$	V_{IN} = 0V, V_{BATT} = 8.4V, source mode disabled, WD_SET disabled, ACGATE_EN disabled, ADC_CONV disabled		33	39.5	µA
Battery quiescent current	I_{BATT_Q}	V_{IN} = 0V, V_{BATT} = 8.4V, WD_SET enabled, TMR_EN enabled, ADC_CONV disabled, source mode disabled, ACGATE_EN disabled			0.655	mA
		V_{IN}= 0V, V_{BATT} = 8.4V, WD_SET enabled, TMR_EN enabled, ADC_CONV enabled, source mode disabled, ACGATE_EN disabled			3.2	mA
Ultrasonic Mode (USM)						
USM regulation frequency	f_{USM}	REG07h, bit[8] = 1		30		kHz
ACGATE Driver						
ACGATE	V_{ACGATE}	Higher than V_{ADP} when enabled		6		V
		ACGATE disabled		0		V
Open-Drain Pin Characteristics (INT, ACOK)						
Low logic voltage threshold	V_L	Sink 10mA current			0.4	V
Analog-to-Digital Converter (ADC)						
Sample rate				50		kHz
ADC reference				1.28		V
ADC resolution				10		Bits
SMBus Interface (8)						
Input high threshold	V_{IH}	V_{PULL_UP} = 1.8V, SDA and SCL	1.3			V
Input low threshold	V_{IL}	V_{PULL_UP} = 1.8V, SDA and SCL			0.4	V
Output low threshold	V_{OL}	I_{SINK} = 1mA			0.4	V
Input leakage current	I_{LEAK}		-0.2		+0.2	µA
SMBus Timing Characteristics (7)						
SMBus clock frequency	f_{SCL}		10		400	kHz
Bus free time		Between a stop and start command	1.3			µs
Start command hold time after which first clock is generated			0.6			µs
Start command set-up time			0.6			µs
Stop command set-up time			0.6			µs

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = 3.7V/cell, 5-cell setting, RS1 and RS2 = 10mΩ, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Data hold time			0			ns
Data set-up time			100			ns
Clock low timeout			25		35	ms
Clock low period			1.3			µs
Clock high period			0.6			µs
Clock/data falling time					300	ns
Clock/data rising time					300	ns

Notes:

6) All minimum and maximum parameters are tested at T_A = 25°C. Over-temperature limits are guaranteed by characterization.
7) Not tested in production and guaranteed by design and characterization.
8) SMBus should cover I^2C specifications. The I^2C/SMBus lines are compatible with 1.8V/3.3V logic.

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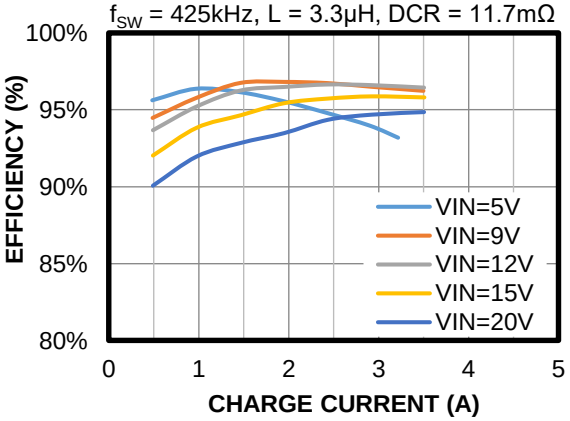
TYPICAL CHARACTERISTICS

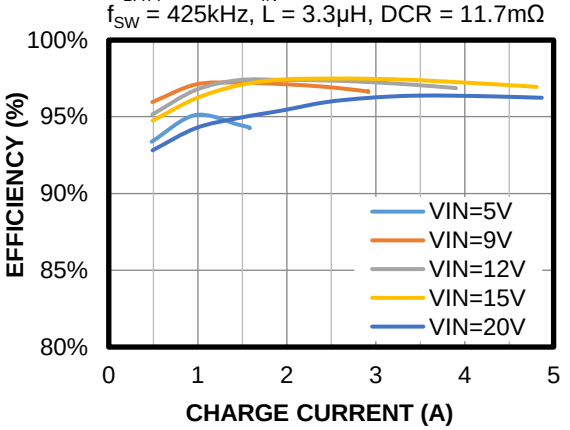
Efficiency vs. Charge Current

Charge mode with 2-cell battery,
V_{BATT} = 8V, V_{IN} = 5V, 9V, 12V, 15V, or 20V,
f_{SW} = 425kHz, L = 3.3µH, DCR = 11.7mΩ



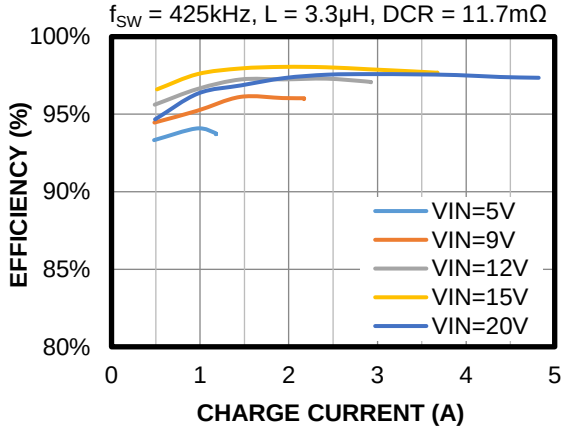
Efficiency vs. Charge Current

Charge mode with 3-cell battery,
V_{BATT} = 12V, V_{IN} = 5V, 9V, 12V, 15V, or 20V,
f_{SW} = 425kHz, L = 3.3µH, DCR = 11.7mΩ



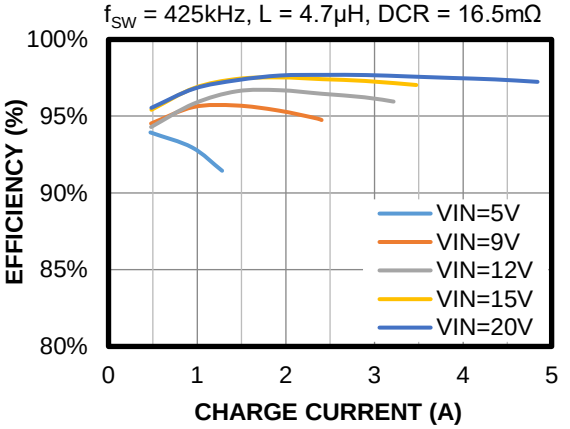
Efficiency vs. Charge Current

Charge mode with 4-cell battery,
V_{BATT} = 16V, V_{IN} = 5V, 9V, 12V, 15V,or 20V,
f_{SW} = 425kHz, L = 3.3µH, DCR = 11.7mΩ



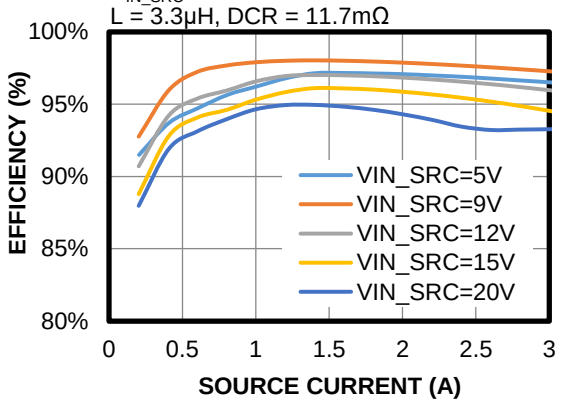
Efficiency vs. Charge Current

Charge mode with 5-cell battery,
V_{BATT} = 20V, V_{IN} = 5V, 9V, 12V, 15V, or 20V,
f_{SW} = 425kHz, L = 4.7µH, DCR = 16.5mΩ



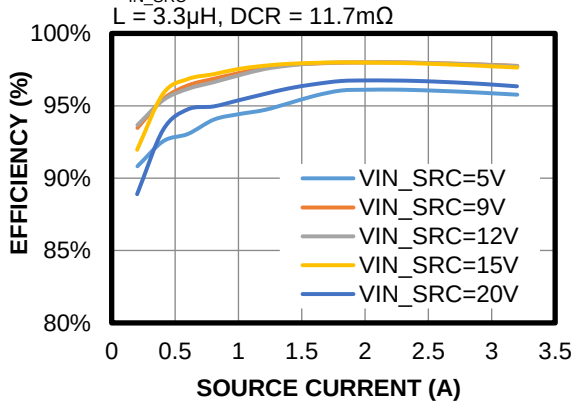
Efficiency vs. Source Current

Source mode with 2-cell battery,
V_{BATT} = 8V, f_{SW} = 425kHz,
V_{IN_SRC} = 5V, 9V, 12V, 15V, or 20V,
L = 3.3µH, DCR = 11.7mΩ



Efficiency vs. Source Current

Source mode with 3-cell battery,
V_{BATT} = 12V, f_{SW} = 425kHz,
V_{IN_SRC} = 5V, 9V, 12V, 15V, or 20V,
L = 3.3µH, DCR = 11.7mΩ



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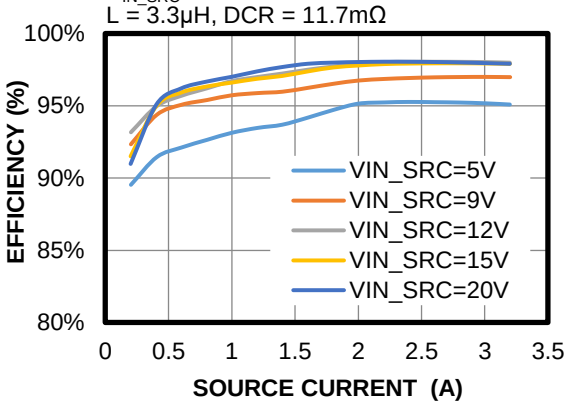
TYPICAL CHARACTERISTICS *(continued)*

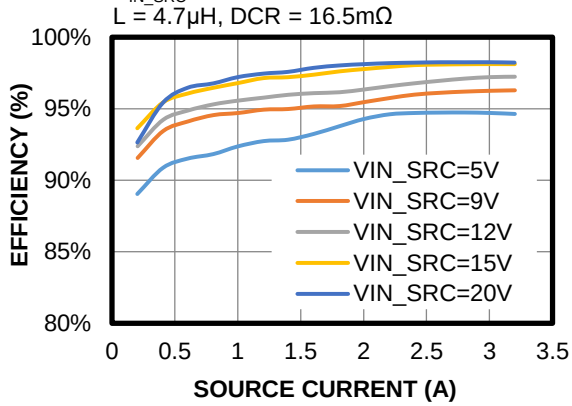
Efficiency vs. Source Current

Source mode with 4-cell battery,
V_{BATT} = 16V, f_{SW} = 425kHz,
V_{IN_SRC} = 5V, 9V, 12V, 15V, or 20V,
L = 3.3µH, DCR = 11.7mΩ



Efficiency vs. Source Current

Source mode with 5-cell battery,
V_{BATT} = 20V, f_{SW} = 425kHz,
V_{IN_SRC} = 5V, 9V, 12V,15V, or 20V,
L = 4.7µH, DCR = 16.5mΩ



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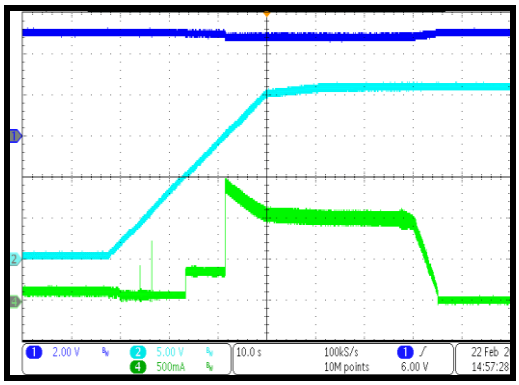
TYPICAL PERFORMANCE CHARACTERISTICS

C_{IN} = 10µF x 5pcs + 1µF, C_{CFLR} = 22µF x 2pcs + 1µF, C_{BATT} = 22µF x 2pcs, L = 4.7µH, f_{SW} = 425kHz, I_{IN_LIM} = 5000mA, I_{CC} = 3000mA, 5-cell application, V_{BATT_REG} = 21V.

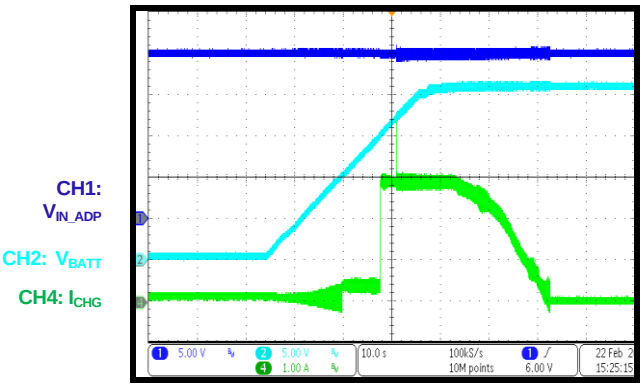
Charge Profile

V_{IN_ADP} = 5V, I_{IN_LIM} = 5A, I_{CC} = 3A,
V_{BATT_REG} = 21V, battery simulator = 10mV/step



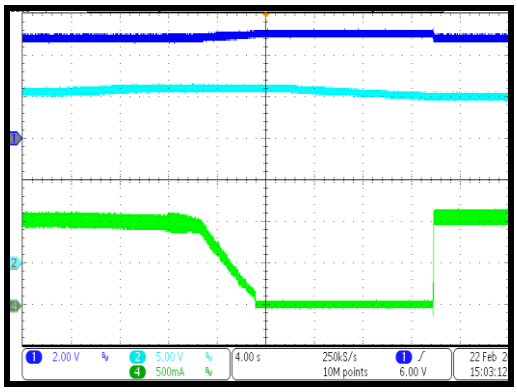
Charge Profile

V_{IN_ADP} = 20V, I_{IN_LIM} = 5A, I_{CC} = 3A,
V_{BATT_REG} = 21V, battery simulator = 10mV/step



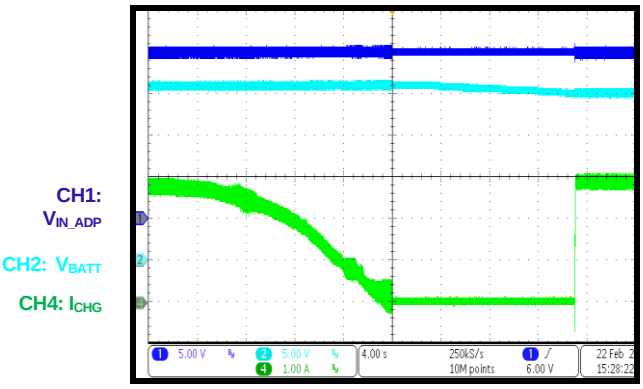
Auto-Recharge Profile

V_{IN_ADP} = 5V, I_{IN_LIM} = 5A, I_{CC} = 3A,
V_{BATT_REG} = 21V, battery simulator = 5mV/step



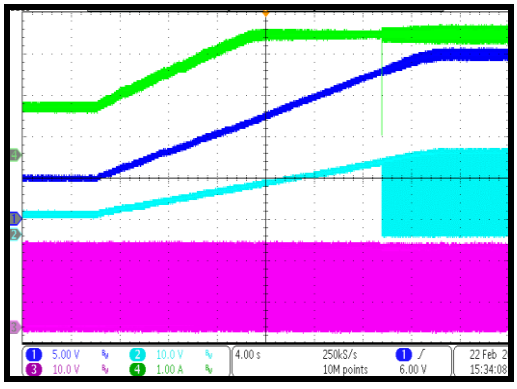
Auto-Recharge Profile

V_{IN_ADP} = 20V, I_{IN_LIM} = 5A, I_{CC} = 3A,
V_{BATT_REG} = 21V, battery simulator = 10mV/step



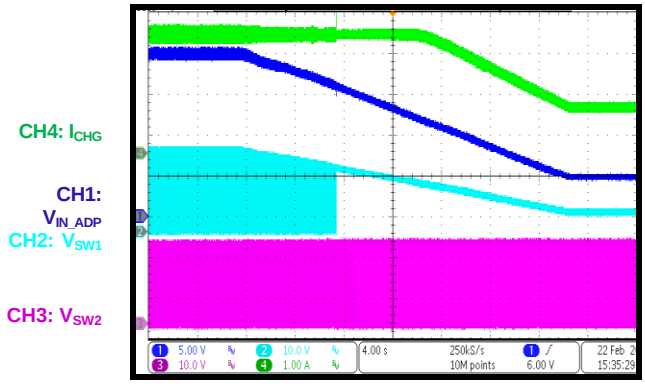
V_{IN_ADP} Step from 5V to 20V

V_{BATT} = 18.5V, I_{CC} = 3A, enable charge



V_{IN_ADP} Step from 20V to 5V

V_{BATT} = 18.5V, I_{CC} = 3A, enable charge



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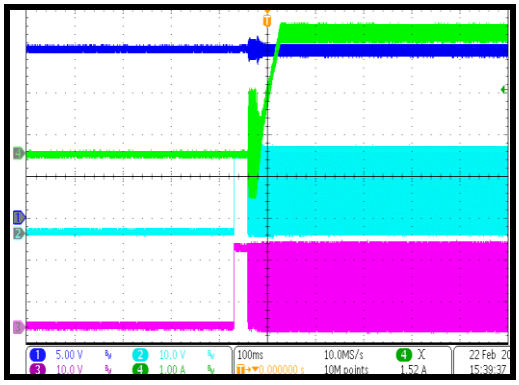
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

C_{IN} = 10µF x 5pcs + 1µF, C_{CFLR} = 22µF x 2pcs + 1µF, C_{BATT} = 22µF x 2pcs, L = 4.7µH, f_{SW} = 425kHz, I_{IN_LIM} = 5000mA, I_{CC} = 3000mA, 5-cell application, V_{BATT_REG} = 21V.

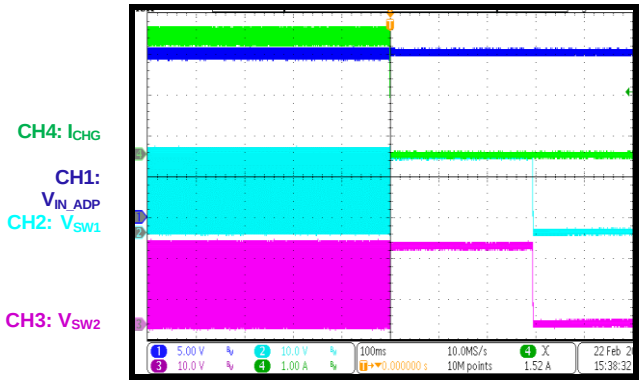
Charge Enabled

V_{IN_ADP} = 20V, I_{IN_LIM} = 18.5V, I_{CC} = 3A



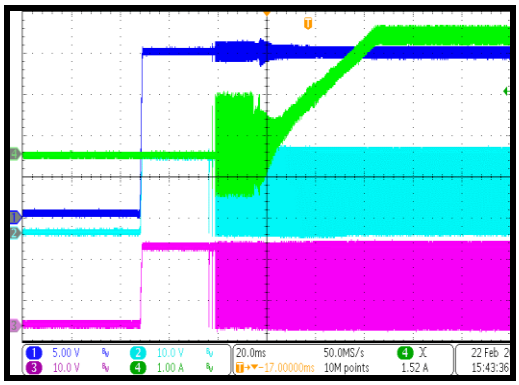
Charge Disabled

V_{IN_ADP} = 20V, I_{IN_LIM} = 18.5V, I_{CC} = 3A



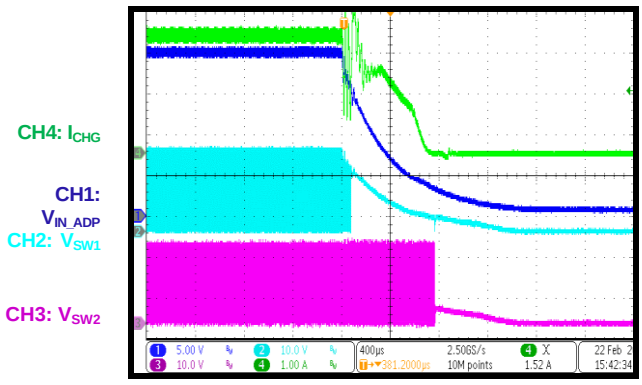
Input Power On

V_{IN_ADP} = 20V, V_{BATT} = 18.5V, I_{CC} = 3A



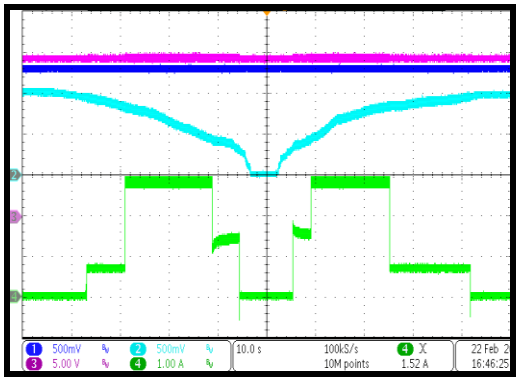
Input Power Off

V_{IN_ADP} = 20V, V_{BATT} = 18.5V, I_{CC} = 3A



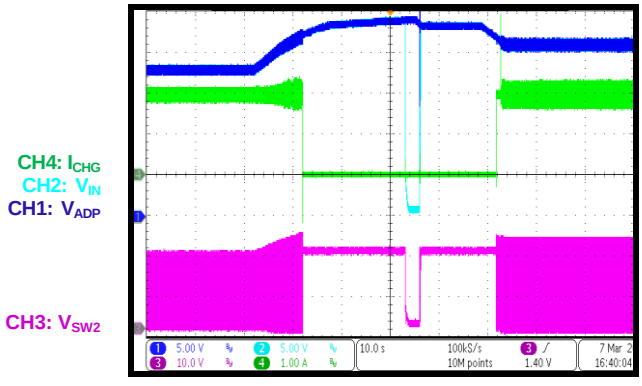
JEITA Compatible NTC Protection

V_{IN_ADP} = 12V, V_{BATT} = 19.3V, V_{BATT_REG} decreases by 320mV/cell in warm window, I_{CC} decreases by half in cool window



ADP and IN OV Protection

V_{BATT} = 18.5V, enable ACGATE driver with external N-channel pass through FET, V_{ADP} ramps up and down



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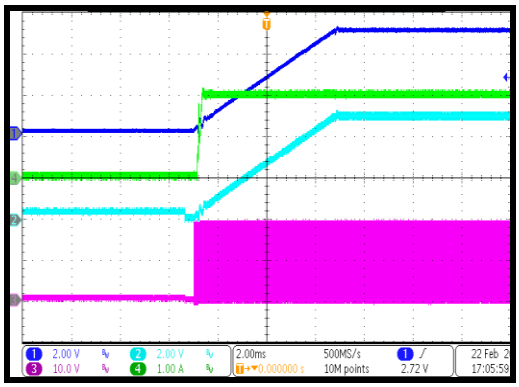
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

C_{IN} = 10µF x 5pcs + 1µF, C_{CFLR} = 22µF x 2pcs + 1µF, C_{BATT} = 22µF x 2pcs, L = 4.7µH, f_{SW} = 425kHz, I_{IN_LIM} = 5000mA, I_{CC} = 3000mA, 5-cell application, V_{BATT_REG} = 21V.

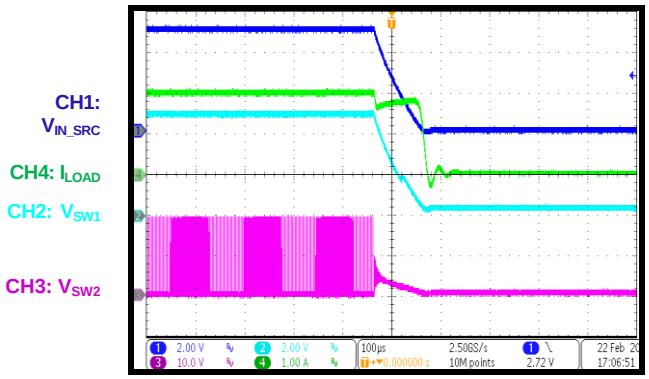
Source Mode Enabled

V_{BATT} = 18.5V, V_{IN_SRC} = 5V, I_{IN_SRC} = 2A (CC load)



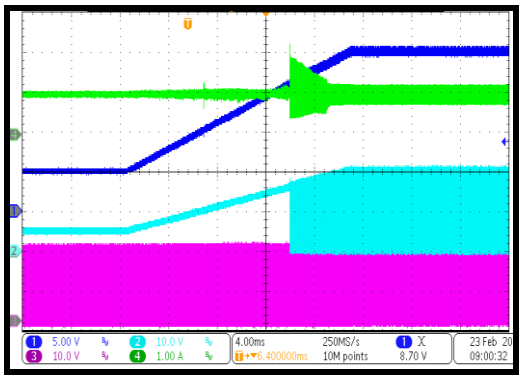
Source Mode Disabled

V_{BATT} = 18.5V, V_{IN_SRC} = 5V, I_{IN_SRC} = 2A(CC load)



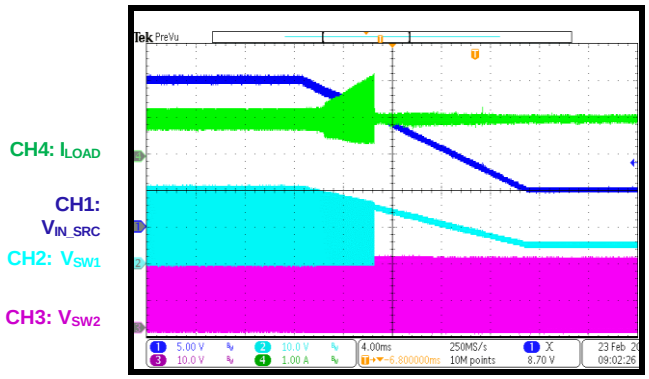
V_{IN_SRC} Step from 5V to 20V

V_{BATT} = 18.5V, V_{IN_SRC} = 5V to 20V, I_{IN_SRC} = 1A (CC load)



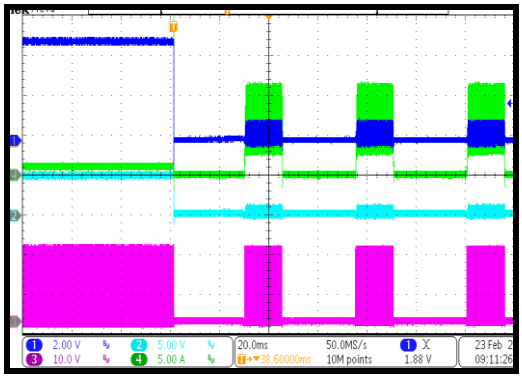
V_{IN_SRC} Step from 20V to 5V

V_{BATT} = 18.5V, V_{IN_SRC} = 20V to 5V, I_{IN_SRC} = 1A (CC load)



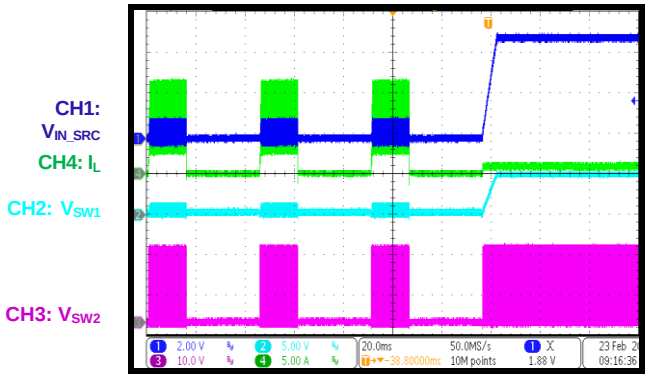
V_{IN_SRC} Short Protection

V_{BATT} = 18.5V, V_{IN_SRC} = 5V, I_{IN_SRC} = 1A (CC load)



V_{IN_SRC} Short Recovery

V_{BATT} = 18.5V, V_{IN_SRC} = 5V, I_{IN_SRC} = 1A (CC load)



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FUNCTIONAL BLOCK DIAGRAM

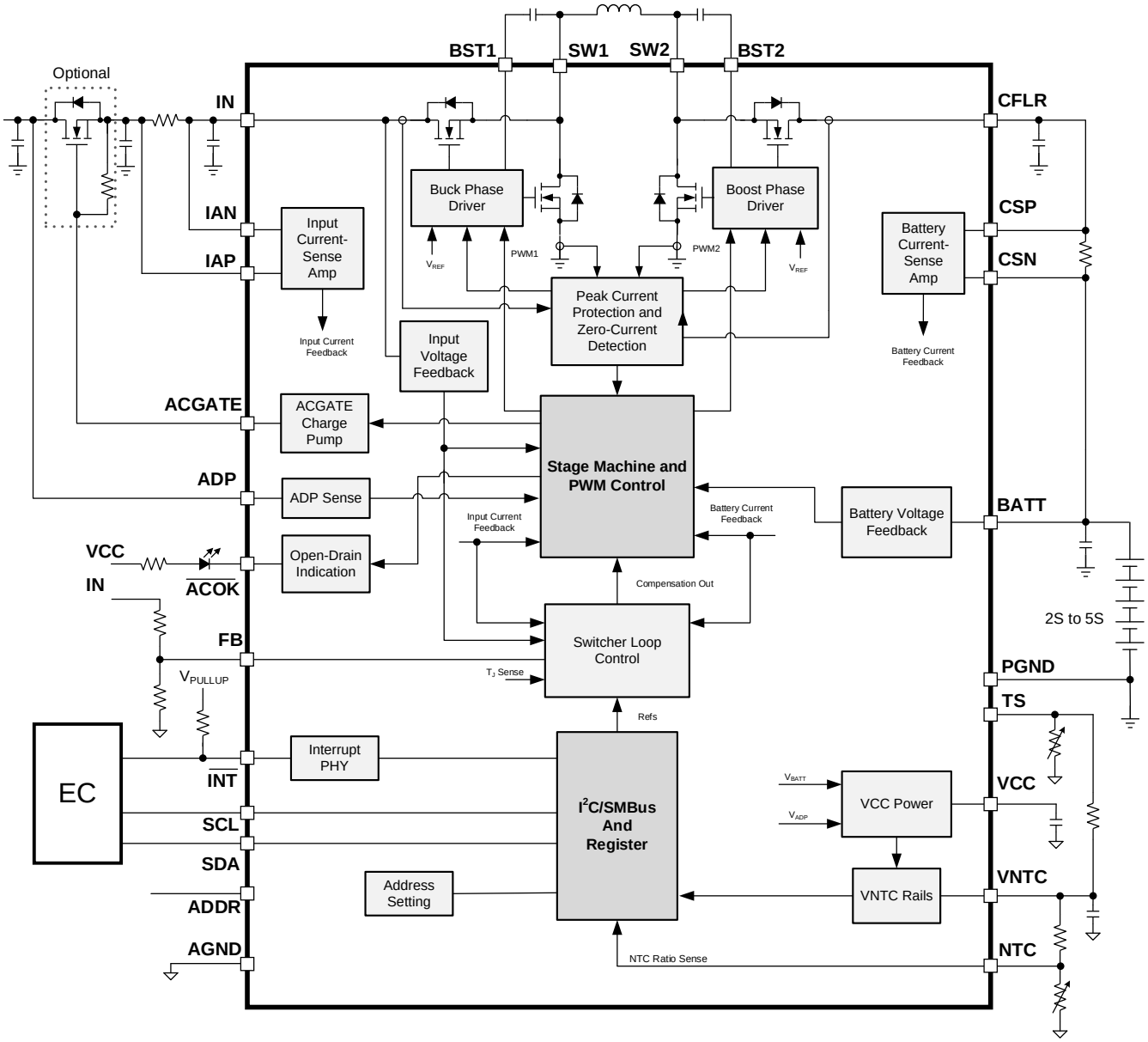

Figure 2: Functional Block Diagram

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OPERATION

Introduction

The MP2652 is a highly integrated buck-boost charger IC with four switching FETs (Q1, Q2, Q3, and Q4) for battery packs with 2 to 5 cells in series. It also integrates one N-channel MOSFET driver for higher input over-voltage protection (ADP OVP).

The MP2652 can operate in reverse to power the input from the battery. This function is compliant with USB power delivery (PD) source mode.

When input power is present, the MP2652 operates in charge mode. The buck-boost converter has three operating modes: boost mode when the input voltage (V_{IN}) is below the battery voltage (V_{BATT}); buck mode when V_{IN} exceeds V_{BATT}; and buck-boost mode when V_{IN} is almost equal to V_{BATT}. Figure 3 shows the power structure.

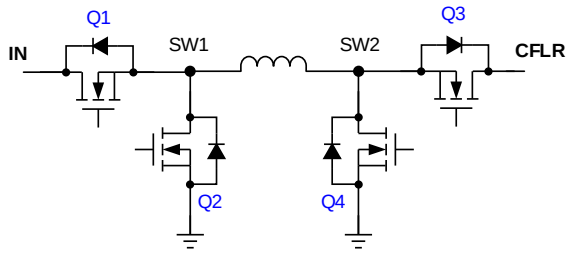

Figure 3: The MP2652's Power Stage

Table 1 shows the MOSFETs' modes while the device works in charge mode.

Table 1: MOSFET Operations in Charge Mode

MOSFET	Boost	Buck-Boost	Buck
Q1	On	Switching	Switching
Q2	Off	Switching	Switching
Q3	Switching	Switching	On
Q4	Switching	Switching	Off

Table 2 shows the MOSFETs' modes while the device works in source mode.

Table 2: MOSFET Operations in Source Mode

MOSFET	Boost	Buck-Boost	Buck
Q1	Switching	Switching	On
Q2	Switching	Switching	Off
Q3	On	Switching	Switching
Q4	Off	Switching	Switching

When the input is absent, the device operates in reverse to power the input from the battery via I²C/SMBus control. The MP2652 can provide a 4 to 21V output voltage (V_{IN_SRC}), with 20mV/step at the input. The device also has an output current (I_{IN_SRC}) limit with 50mA/step in this mode. This mode is called source mode in USB PD applications.

VCC Low-Dropout (LDO) Regulator Output

The MP2652 integrates a low-dropout (LDO) regulator to power the internal circuit, including the I²C block, FET driver, and bias current.

VCC is powered by the ADP pin's voltage (V_{ADP}) or V_{BATT}. When V_{ADP} exceeds its under-voltage lockout (UVLO) threshold (V_{ADP_UVLO}), VCC is powered by V_{ADP}, regardless of whether the MP2652 is in charge mode or source mode. When the input is absent or V_{ADP} is below V_{ADP_UVLO}, VCC is powered by V_{BATT}.

VCC can provide a 3.6V output to supply power to the internal circuit and open-drain pin's (SCL, SDA, ACOK, and INT) pull-up voltage. It is not recommended for VCC to power other circuits.

Input Power Status Indication

The MP2652 has both an $\overline{ACOK}$ pin and a status register bit, PG_STAT, to indicate whether the input power supply is present in charge mode. The $\overline{ACOK}$ pin is an open-drain structure that is pulled to AGND when $V_{IN_UVP} < V_{IN} < V_{IN_OVP}$.

The PG_STAT bit indicates when the power is good. This status is only valid in charge mode. PG_STAT is set to 1 when V_{IN} exceeds its under-voltage protection threshold (V_{IN_UVP}) but is below its over-voltage protection threshold (V_{IN_OVP}).

Input Over-Voltage Protection (OVP)

The MP2652 provides two input over-voltage protection (OVP) thresholds: the ADP OVP threshold (V_{ADP_OVP}) and V_{IN_OVP}.

The ADP pin senses the input voltage. If $V_{ADP} > V_{ADP_OVP}$, the ACGATE pin pulls low to turn off M1 immediately; at the same time, the switches turn off (see Figure 4 on page 22).

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The MP2652 reports the ADP OVP fault via the fault register bit, VADP_OV. There is a 100ms deglitch time to recover from ADP OVP.

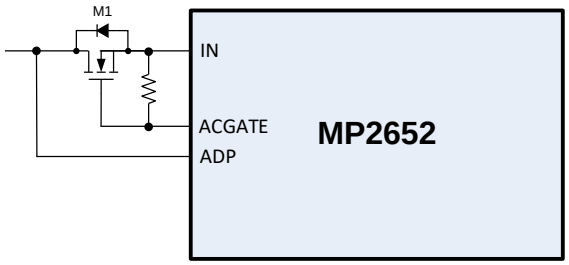

Figure 4: ACGATE Driver

When $V_{IN_OVP} < V_{IN} < V_{ADP_OVP}$, M1 turns on and the MP2652's switches are disabled. Then a fault is reported via VIN_OV (REG17h, bit[13]).

Input Current Limit and Input Voltage Limit Regulation

To meet the maximum current limit in the USB specification and avoid overloading the adapter, the MP2652 has both input current (I_{IN}) limit and V_{IN} limit regulation. If either the I_{IN} limit or V_{IN} limit is reached, the MP2652 regulates the duty cycle of Q1 and Q4 to limit the input power according to the setting.

Battery Charge Profile

In charge mode, the MP2652 regulates five control loops: V_{IN}, I_{IN}, charge current, battery-full regulation voltage, and the device's junction temperature (T_J).

Re-plugging the input power or toggling the battery charging control bit (REG12h, bit[0]) can restart a new charge cycle if none of the following faults are present:

- There is no thermistor fault
- There is no safety timer fault
- There is no battery over-voltage (OV) fault

The new charge cycle can start with any phase, since the phase depends on V_{BATT}.

The device provides four main charging phases: constant current trickle charge, constant current pre-charge, constant current (CC) fast charge, and constant voltage (CV) charge (see Figure 5).

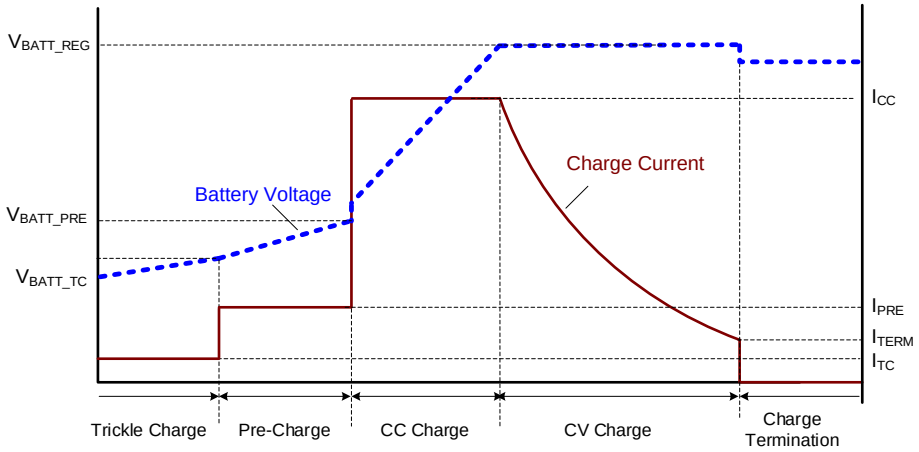

Figure 5: Charge Profile

Constant Current Trickle Charge (Phase 1)

When the input power qualifies as a good power supply, the IC checks V_{BATT} to determine whether trickle-charging is required. If V_{BATT} is below the trickle charge (TC) to pre-charge threshold (V_{BATT_TC}), a configurable trickle charging current is applied to the battery.

Constant Current Pre-Charge (Phase 2)

When V_{BATT} exceeds V_{BATT_TC}, the IC starts to safely pre-charge the deeply depleted battery until V_{BATT} reaches the pre-charge to fast charge threshold (V_{BATT_PRE}). If V_{BATT_PRE} is not reached before the pre-charge timer (about 2 hours) expires, the charge cycle stops, and a corresponding timeout fault signal is asserted. The pre-charge current can be configured via REG0Fh, bits[7:4], while V_{BATT_PRE} can be configured via REG0Bh, bit[12]. There are two options for this threshold: 2.5V/cell for $LiFePO_4$ batteries, and 3V/cell for Li-ion batteries.

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Constant Current (CC) Fast Charge (Phase 3)

When V_{BATT} exceeds V_{BATT_PRE} (set via REG0Bh, bit[12]), the IC enters the constant current (CC) fast charge phase. The fast charge current can be configured via REG14h, bits[13:6].

Constant Voltage (CV) Charge (Phase 4)

When V_{BATT} reaches the configurable battery-full voltage (V_{BATT_REG}, set via REG15h, bits[14:4]), the charge current begins to taper off.

The charge cycle is considered complete when the charge current reaches the termination threshold (I_{TERM}, set via REG0Fh, bits[3:0]), assuming the termination function is enabled. If I_{TERM} is not reached before the safety charge timer expires, then the charge cycle stops and a corresponding timeout fault signal is asserted (see the Safety Timer section on page 24 for more details).

Table 3 shows the battery-full voltage for different cell number applications.

Table 3 Battery-Full Voltage Range at Different Cells

Cell Number	Battery Cell Voltage Range	$V_{BATT_REG_MIN}$			$V_{BATT_REG_MAX}$		
		V_{BATT_REG} (mV)	Reg15h, Bits[14:4] (Dec)	Reg15h (Hex)	V_{BATT_REG} (mV)	Reg15h, Bits[14:4] (Dec)	Reg15h (Hex)
5-cell	3.4V to 4.4V	17000	340	0x1540	22000	440	0x1B80
2-cell	3.4V to 4.67V	6800	680	0x2A80	9340	934	0x3A60
3-cell	3.4V to 4.67V	10200	1020	0x3FC0	14010	1401	0x5790
4-cell	3.4V to 4.67V	13600	1360	0x5500	18680	1868	0x74C0

Automatic Recharge

When the battery is fully charged, charging is terminated and the battery may be discharged because of the system consumption or self-discharge. When V_{BATT} falls below the configurable recharge threshold, the IC automatically starts a new charging cycle without needing to manually restart a charging cycle if the input power is valid. The charge timer resets when the automatic recharge cycle begins.

Battery Over-Voltage Protection (OVP)

The IC has battery OVP. If V_{BATT} exceeds the battery OVP threshold (230mV higher than the battery regulation voltage per cell), charging is disabled. Battery OVP has a 30ms deglitch time. The switcher turns off during battery OVP.

Junction Thermal Regulation

The thermal regulation loop always monitors the IC's internal junction temperature (T_J). If T_J exceeds the temperature limit, the charge current is reduced to keep T_J at the regulated threshold.

There are multiple thermal regulation thresholds (from 80°C to 120°C) to help the system design meet the thermal requirement for different applications. The junction temperature's regulation threshold can be set via REG0Fh, bits[14:12].

Transitions Between Buck, Buck-Boost, and Boost Modes

The MP2652 always monitors the voltage on the IN and CFLR pins to automatically switch between different modes (see Figure 6).

When V_{IN} exceeds 90% of V_{BATT}, the MP2652 transitions from boost mode to buck-boost mode.

When V_{IN} drops below 75% of V_{BATT}, the MP2652 transitions from buck-boost mode to boost mode.

When V_{IN} drops below 120% of V_{BATT}, the MP2652 transitions from buck mode to buck-boost mode.

When V_{IN} exceeds 135% of V_{BATT}, the MP2652 transitions from buck-boost mode to buck mode.

Figure 6 on page 24 shows the transition thresholds between the modes.

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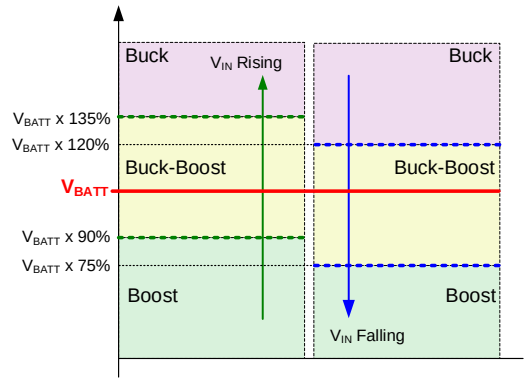

Figure 6: Mode Transition Threshold

Pulse-Skip Mode (PSM) Operation

The MP2652 utilizes pulse-skip mode (PSM) control to improve efficiency under light loads. In PSM, lighter loads mean the device skips more pulse width.

Ultrasonic Mode (USM)

The MP2652 provides ultrasonic mode (USM) control to ensure the switching pulse interval exceeds 30kHz, which can be disabled by setting REG07h, bit[8] to 0.

Cycle-by-Cycle MOSFET Current Limit

The MP2652 senses both the high-side and low-side MOSFET currents (HS-FET and LS-FET, respectively). During loop control, the device provides a valley current limit in buck mode and a peak current limit in boost mode for each cycle-by-cycle switching period. In buck mode, the next period does not start until the inductor current (I_L) drops to the valley current limit. Then I_L rises during the minimum on time to fold back the frequency after triggering the valley current limit.

Analog-to-Digital Converter (ADC) Conversion and Multiplexer

The MP2652 integrates a built-in, 10-bit successive approximation analog-to-digital converter (SAR ADC) with 50kSPS. A 10-channel multiplexer measures the device's parameters (see Table 4).

When the MP2652 works in charge mode and source mode, the ADC operates automatically. The ADC keeps running and each parameter is converted to a digital value every 370µs. When only the battery is present, the ADC converts values when ADC_CONV (REG0Eh, bit[7]) is set to 1.

Table 4: ADC Channels

Sink Mode	Source Mode
• V_{IN} • I_{IN} • V_{BATT} • Charge current • Battery temperature (NTC pin voltage ratio) • TS pin voltage ratio • Chip junction temperature	• V_{IN_SRC} • I_{IN_SRC} • V_{BATT} • Battery temperature (NTC pin voltage ratio) • TS pin voltage ratio • Chip junction temperature

Safety Timer

The IC provides both the pre-charge and CC/CV charge safety timer to prevent an extended charging cycle due to abnormal battery conditions. The total safety timer for both trickle charge and pre-charge is about 2 hours when V_{BATT} is below V_{BATT_PRE}.

The CC/CV charge safety timer starts when the battery enters the fast charge phase. The user can configure this time via REG12h, bits[12:11].

The two safety timers above can be disabled via REG12h, bit[13]. The safety timer does not operate in discharge mode.

The following actions restart the safety timer:

- Toggle CHG_EN (REG12h, bit[0]) or DC/DC_EN(REG12h, bit[6]) while V_{IN} is present.
- Toggle TMR_EN (REG12h, bit[13]) while V_{IN} is present.

The IC automatically suspends the timer if an NTC hot or cold fault occurs.

During input voltage, input current, or thermal regulation, the safety timer counts at a half-clock rate, as the actual charge current is likely to be below the register setting. For example, if the charger is in input current limit regulation (IIN_LIM_STAT = 1) throughout the whole charging cycle, and the safety timer is set to 20 hours, then the timer will expire in 40 hours. This half-clock rate feature can be disabled via TMR2X_EN (REG12h, bit[10]).

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Watchdog Timer

The MP2652 has a watchdog timer to monitor the I²C interface. If the watchdog timer is enabled, the host must periodically reset the watchdog timer reset bit before the watchdog timer expires. If the watchdog timer expires, some of the registers are reset to their default values. See the Register Map section on page 30 for more details.

The following actions reset the watchdog timer and force the device to recover from a watchdog timer fault:

- Write to watchdog timer reset bit.
- Write to the charge current register (REG14h).
- Write to the battery regulation voltage register (REG15h).

The watchdog timer can be disabled via REG12h, bits[8:7].

Battery Temperature Monitoring via the Negative Temperature Coefficient (NTC) Thermistor

Thermistor is the generic name given to thermally sensitive resistors. A negative temperature coefficient (NTC) thermistor is generally called a thermistor. Depending on the manufacturing method and the structure, the thermistor can have many shapes and characteristics. Unless otherwise specified, the thermistor resistance values are classified at a standard temperature of 25°C. The resistance of a temperature is solely a function of its absolute temperature.

Refer to the thermistor's datasheet to obtain the relevant parameters. Calculate the relationship between the resistance and absolute temperature of a thermistor with Equation (1):

$$R_1 = R_2 \times e^{\beta \times \left(\frac{1}{T1} - \frac{1}{T2}\right)} \quad (1)$$

Where R_1 is the resistance at the absolute temperature T_1, R_2 is the resistance at the absolute temperature T_2, and β is a constant that depends on the thermistor's material.

The MP2652 continuously monitors the battery's temperature by measuring the voltage at the NTC pin (V_{NTC}). This voltage is determined by the resistor divider since its ratio is produced by the NTC thermistor's resistance when the battery is under different temperatures (see Figure 7).

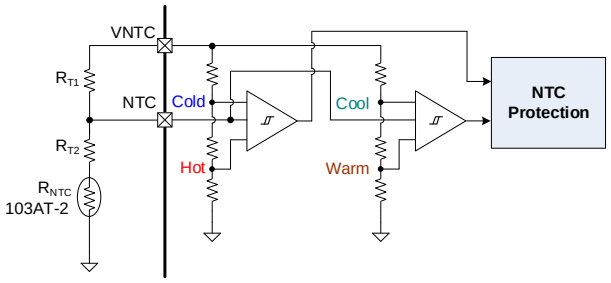

Figure 7: NTC Protection Circuit

The MP2652 internally sets a pre-determined upper and lower bound for V_{NTC} range. If V_{NTC} goes out of this range, the temperature is outside its safe operating limit. Then charging stops until the operating temperature returns into the safe range.

To satisfy the JEITA requirement, the MP2652 has four temperature thresholds: a cold battery threshold (0°C by default), a cool battery threshold (10°C by default), a warm battery threshold (45°C by default), and a hot battery threshold (60°C by default). For a given NTC thermistor, these temperatures correspond to V_{COLD}, V_{COOL}, V_{WARM}, and V_{HOT}, respectively. These thresholds can be configured via REG0Dh, bits[7:0]. When $V_{NTC} < V_{HOT}$ or $V_{NTC} > V_{COLD}$, charging is suspended and the timers are suspended. When $V_{HOT} < V_{NTC} < V_{WARM}$ or when $V_{COOL} < V_{NTC} < V_{COLD}$, the charging behavior is configured via REG0Ch, bits[14:4].

Figure 8 shows the JEITA control profile.

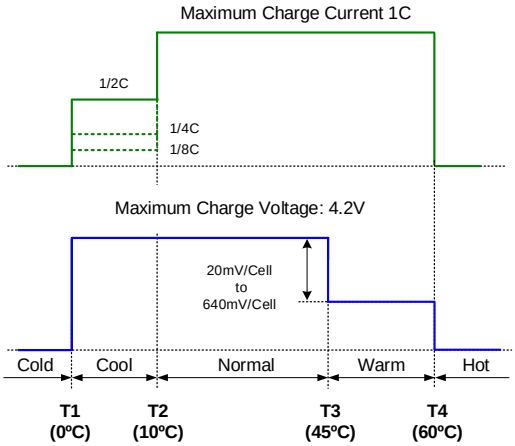

Figure 8: NTC Window

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The MP2652 also monitors the battery temperature in discharge mode. In this mode, NTC hot and NTC cold conditions are indicated but source mode switches as normal.

NTC Floating Detection

If V_{NTC} exceeds 95% of 1.28V in charge mode, an NTC float is detected, an interrupt (INT) asserts, and the corresponding status register changes. The switcher turns off when NTC is floating.

Battery Missing Detection

The MP2652 counts how often charging terminates every 10s. If charge termination occurs more than three times in 10s, the MP2652 reports that the battery is missing via the status register and initiates an INT signal.

TS/IMON Pin Function

The MP2652 has a TS/IMON pin that is either used for temperature monitoring (TS) or current monitoring (IMON). When REG10h, bit[12] = 0, this pin is configured for temperature monitoring. When REG10h, bit[12] = 1, this pin is configured for charge current monitoring.

TS Function

When the TS function is enabled, the TS pin senses the input connector's temperature via REG0Dh, bits[12:10].

When the TS pin reaches the TS hot threshold (V_{TS_HOT}), an INT signal asserts to indicate that a TS fault has occurred. In charging mode, the I_{IN} limit is reduced to 500mA, with 50mA/step every 62.5ms. When the IC recovers from a TS fault, the I_{IN} limit rises to its set value, with 50mA/step every 62.5ms.

By default, the triggered INT signal is masked by REG18h.

IMON Function

When the IMON function is used, the IMON pin represents the battery charge current with a gain of 0.1V/A, and there is a 100mV offset.

Thermal Shutdown

The IC continuously monitors the internal T_J to maximize power delivery and avoid overheating the chip. If T_J reaches 150°C, the pulse-width modulation (PWM) converter shuts down. Normal operation does not resume until T_J drops below 120°C.

Host Mode and Default Mode

The IC is a host-controlled device. After VCC power-on reset (POR), all the registers are set to their default settings.

Any write to the IC forces it to host mode. All the device parameters can be configured by the host. To keep the device in host mode, the host has to reset the watchdog timer regularly by writing 1 to REG12h, bit[9] before the watchdog timer expires. If the watchdog timer expires, the IC goes back into default mode.

Impedance Compensation to Accelerate Charging

Throughout the entire charging cycle, the CV charging stage takes a long time. To accelerate the charging cycle, it is recommended for the device to stay in the CC fast charge stage for as long as possible.

The IC allows the user to compensate the intrinsic resistance of the battery by adjusting the battery regulation voltage according to the charge current and internal resistance. In addition, a maximum allowed regulated voltage provides additional voltage ($V_{BATT_REG_ACT}$), estimated with Equation (2):

$$V_{BATT_REG_ACT} = V_{BATT_REG} + Min\ (V_{CLAMP}, I_{CHG_ACT} \times R_{BATT}) \quad (2)$$

Where V_{BATT_REG} is the battery regulation voltage set via REG15h, bits[14:4], and I_{CHG_ACT} is the real-time charge current during the operation.

Source Mode Operation

The MP2652 can operate in source mode to supply power to the IN pin using the battery. To ensure that the battery is not drained, the device does not enter this mode if the battery is below the configurable battery low threshold. Source mode operation can be enabled when REG12h, bit[3] = 1. When both charging and discharging are enabled, the discharge operation takes higher priority.

In source mode, the IC employs a fixed frequency (375kHz to 770kHz, configurable) switching regulator. This regulator switches from PWM operation to PSM under light loads.

V_{IN_SRC} is compliant with USB PD specifications. It can be set to 5V, 9V, 12V, 15V, or 20V, with

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20mV steps, via the digital-to-analog-converter (DAC) in the register or the external FB pin.

The I_{IN_SRC} limit can be configured via the I^2C/SMBus up to 5A, with 50mA/step. This is compliant with I^2C/SMBus specifications.

Discharge operation is enabled if both of the following conditions are met:

- $V_{BATT} > V_{BATT_LOW}$
- REG12h, bit[3] = 1

To meet PD timing specifications, V_{IN_SRC} should settle within 275ms.

In source mode, the switcher can work in buck mode, boost mode, or buck-boost mode, according to V_{BATT} and V_{IN_SRC}.

Over-Voltage Protection (OVP) in Source Mode

The MP2652 features output OVP in source mode. The IC continuously monitors V_{IN_SRC} in source mode in case it approaches the OVP threshold ($V_{IN_SRC_OV}$) in source mode. If $V_{IN_SRC} > V_{IN_SRC_OV}$, the PWM is disabled and an OV fault asserts in the status and fault registers. The PWM recovers once V_{IN_SRC} falls below $V_{IN_SRC_OV}$ with a hysteresis (see the Electrical Characteristics section starting on page 7 for more details).

Short-Circuit Protection (SCP) in Source Mode

In addition to output OVP, the MP2652 features output short-circuit protection (SCP). When the load current reaches the output current limit, V_{IN_SRC} begins to fall. If V_{IN_SRC} falls below $V_{IN_SRC_UV}$ for longer than 10ms, a source mode fault asserts. Source mode is disabled for 30ms, then it restarts.

Battery Standby Mode

If only the battery is connected, the input source is absent, and source mode is disabled, the VCC LDO stays on. The device's maximum consumed current ($I_{BATT_STANDBY}$) is 33μA, which extends the batteries runtime.

Battery Under-Voltage Protection (UVP)

In source mode, The MP2760 has two-level battery under-voltage protection.

The first level UVP in source mode is batt low. when $V_{BATT} < V_{BATT_LOW}$ for 30ms, the MP2760 generates an INT signal and reports that the battery voltage is low. Then the MP2652 turns off the buck-boost converter. The user can configure the batt low behavior via REG0Bh, bit[11]. When REG0Bh, bit[11] = 0, source mode restarts automatically when V_{BATT} exceeds V_{BATT_LOW} with 200mV/cell hysteresis. When REG0Bh, bit[11] = 1, source mode is latched, and the SRC_EN bit must be toggled to restart source mode.

If VBATT low is disabled by REG0Bh,bit[13], the second battery UVP, battery UVLO works. When V_{BATT} falls below the UVLO threshold ($V_{BATT} < V_{BATT_UVLO}$), the DC/DC converter turns off. When $V_{BATT} > V_{BATT_UVLO}$, the DC/DC converter starts switching again.

SMBus and I^2C Compatibility

The MP2652 has an SCL/SDA interface compatible with the SMBus/I^2C interface. In addition, the MP2652's registers are 16 bits, which are compatible with both SMBus and I^2C standards.

The system management bus (SMBus) is a two-wire, bidirectional, serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are externally pulled to a bus voltage when they are idle. Connecting to the line, a initiator device generates the SCL signal and device address, then arranges the communication sequence. This is based on I^2C operation principles.

The MP2652 interface is an SMBus target that supports both standard mode (100kHz) and fast mode (400kHz). The SMBus address is 0001 001x, where x is the read/write bit. The device receives control inputs from the initiator device, such as a microcontroller (MCU) or a digital signal processor.

Start and Stop Commands

All transactions begin with a start (S) command and are terminated by a stop (P) command. A start command is defined as a high-to-low transition on the SDA line while SCL is high. A stop command is defined as a low-to-high transition on the SDA line while the SCL is high (see Figure 9).

Start and stop commands are always generated by the initiator. The bus is considered busy after

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a start command; it is considered free after a stop command.

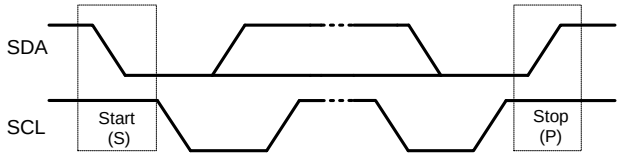

Figure 9: Start and Stop Commands

Data Validity

For data validity, the data on the SDA line must be stable during the high period of the clock. The high to low state of the SDA line can only change when the clock signal on the SCL line is low (see Figure 10).

When the bus is free, both lines are high. The SDA and SCL pins are open drains.

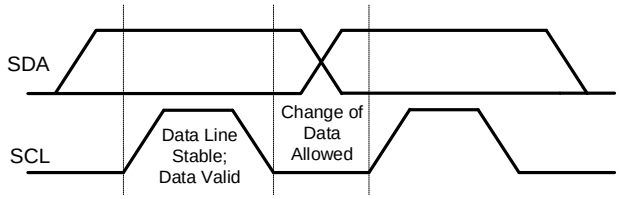

Figure 10: Data Validity

Interrupt to Host (INT)

The MP2652 has an alert mechanism that outputs an interrupt signal via the INT pin. If an interrupt is triggered, the device outputs a 256μs low-state INT pulse. The INT output is designed as an open-drain structure that must be externally pulled up to a voltage source for operation. The INT signal can be masked via the REG18h and REG19h registers.

SMBus Alert Response Address (ARA)

The SMBus alert response address (ARA) is a special address that can be used by the bus host.

If more than one target-only device is connected on the bus, and all the INT lines are connected together, a target-only device can signal to the host that it wants to talk through INT. The host processes the interrupt and simultaneously accesses all INT devices through the ARA. Only the device(s) that pull INT low acknowledge the ARA.

The host performs a modified receive byte operation. The 7-bit device address provided by the target transmission device is placed in the 7 most significant bits of the byte. The 8th bit can be a 0 or 1.

The SMBus ARA is 0001 100b.

Byte Format

Each byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte must be followed by an acknowledge (ACK) bit. Data is transferred with the most significant bit (MSB) first.

The acknowledge takes place after every byte. The ACK bit allows the receiver to signal to the transmitter that the byte was successfully received, then another byte can be sent. All clock pulses, including the acknowledge pulse (9th clock pulse), are generated by the initiator (see Figure 11).

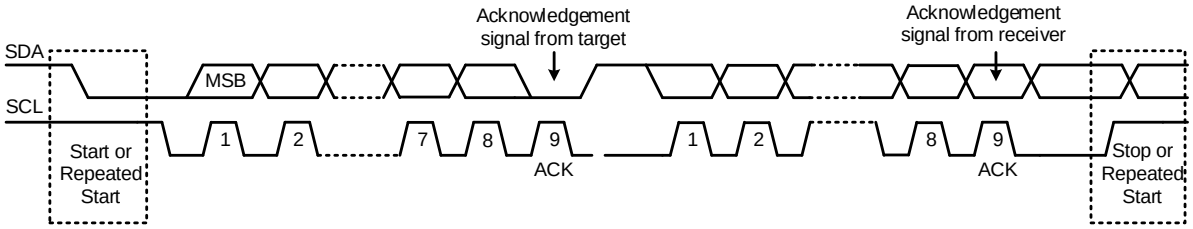

Figure 11: Acknowledge Bit

The transmitter releases the SDA line during the acknowledge clock pulse, so the receiver can pull the SDA line low. If the SDA line remains high during the 9th clock pulse, this is a not acknowledge (NACK) signal. The initiator can then generate either a stop command to abort the transfer or a repeated start command to start a transfer. After the start command, a target address is sent. This address is 7 bits long, followed by an 8th data direction bit (R/W).

A 0 indicates a transmission (write), and a 1 indicates a request for data (read). If the register address is not defined, the charger IC sends back NACK and returns to an idle state.

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Figure 12 shows the byte format. Figure 13 shows a single word write. Figure 14 shows a single word read.

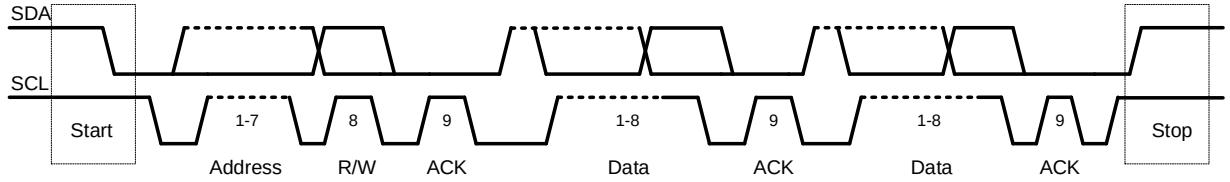

Figure 12: Byte Format

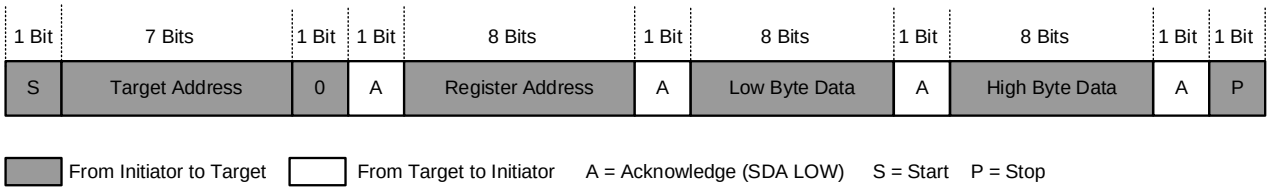

Figure 13: Singe-Word Write

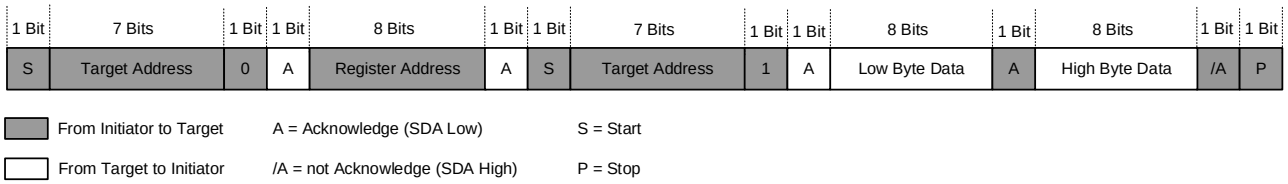

Figure 14: Single-Word Read

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REGISTER MAP

Register Name	Register Address	OTP (9)	R/W	Description
REG05h	0x05	Yes	R/W	Sets the device address. (10)
REG06h	0x06	Yes	R/W	Sets the minimum input voltage limit.
REG07h	0x07	Yes	R/W	Controls ultrasonic mode (USM).
REG08h	0x08	Yes	R/W	Sets the input current limit.
REG09h	0x09	No	R/W	Sets the output voltage in source mode.
REG0Ah	0x0A	No	R/W	Sets the battery impedance compensation and output current limit source mode.
REG0Bh	0x0B	Yes	R/W	Sets the battery low voltage threshold and battery discharge current regulation in source mode.
REG0Ch	0x0C	No	R/W	Sets the JEITA action.
REG0Dh	0x0D	Yes	R/W	Configures the temperature protections.
REG0Eh	0x0E	Yes	R/W	Configuration register 0.
REG0Fh	0x0F	Yes	R/W	Configuration register 1.
REG10h	0x10	Yes	R/W	Configuration register 2.
REG11h	0x11	Yes	R/W	Configuration register 3.
REG12h	0x12	Yes	R/W	Configuration register 4.
REG14h	0x14	Yes	R/W	Sets the charge current.
REG15h	0x15	Yes	R/W	Sets the battery-regulation voltage.
REG16h	0x16	No	R	Status and fault register 0.
REG17h	0x17	No	R	Status and fault register 1.
REG18h	0x18	No	R/W	INT mask setting register 0.
REG19h	0x19	No	R/W	INT mask setting register 1.
REG23h	0x23	No	R	Indicates the ADC result for the input voltage.
REG24h	0x24	No	R	Indicates the ADC result for the input current.
REG25h	0x25	No	R	Indicates the ADC result for the battery voltage.
REG27h	0x27	No	R	Indicates the ADC result for the battery current.
REG28h	0x28	No	R	Indicates the ADC result for the NTC voltage ratio.
REG29h	0x29	No	R	Indicates the ADC result for the TS voltage ratio.
REG2Ah	0x2A	No	R	Indicates the ADC result for the junction temperature.
REG2Bh	0x2B	No	R	Indicates the ADC result for the battery discharge current.
REG2Ch	0x2C	No	R	Indicates the ADC result for the input voltage in discharge mode.
REG2Dh	0x2D	No	R	Indicates the ADC result for the output current in discharge mode.

Notes:

9) OTP in this section means one-time programmable memory. The specific OTP bit refers to the register bit description.
10) The default Device Address is 69h.

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REGISTER MAP FOR THE MP2562VT-0000

REG05h: Device Address Setting

The REG05h register sets the device address, controls the watchdog, and selects the communication interface.

Bits	Access	Bit Name	Default	Description
15:10	N/A	RESERVED	0	Reserved.
9	R/W	WD_SET	1	When this bit is set to 0, the watchdog timer is automatically disabled when V_{IN} is absent. It is recommended to set this bit to 0. This bit is set to 1 by default. 0: Disabled 1: Enabled
8	R	TLOW_EN	0	To be compliant with the SMBus, the I^2C initiator pulls SCL low for longer than 25ms to make the device release SDA (reset the communication). It is reset when the watchdog resets. This bit is set to 0 by default. This bit can be configured via the OTP. 0: Disabled (I^2C) 1: Enabled (SMBus)
7	N/A	RESERVED	1	Reserved.
6	R	ADDR[3]	1	Determines the highest 4 bits of the device's address. The default is 4'b 1101. These bits can be configured via the OTP.
5	R	ADDR[2]	1	
4	R	ADDR[1]	0	
3	R	ADDR[0]	1	
2	R	RESERVED	0	Reserved.
1	R	RESERVED	0	
0	R	RESERVED	1	

REG06h: Input Minimum Voltage Limit Setting

The REG06h register sets the minimum input voltage limit.

Bits	Access	Name	Default	Description
15:8	N/A	RESERVED	0	Reserved.
7	R/W	V_{IN_MIN}[6]	0	Sets the minimum V_{IN} limit. These bits are reset when the watchdog resets. These bits can be configured via the OTP. Range: 4.0V (0011 0010) to 20.4V (1111 1111) Default: 4.48V (0011 1000) LSB: 80mV V_{IN_MIN} = DEC(Bits[7:0]) x 80 (mV)
6	R/W	V_{IN_MIN}[6]	0	
5	R/W	V_{IN_MIN}[5]	1	
4	R/W	V_{IN_MIN}[4]	1	
3	R/W	V_{IN_MIN}[3]	1	
2	R/W	V_{IN_MIN}[2]	0	
1	R/W	V_{IN_MIN}[1]	0	
0	R/W	V_{IN_MIN}[0]	0	

REG07h: USM Mode Control

The REG07h register enables ultrasonic mode (USM).

Bit	Access	Name	Default	Description
15:9	N/A	RESERVED	0	Reserved.

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8	R/W	USM_EN	0	Enables USM. When the device enters PFM and there is no load, the frequency should be >30kHz, and the dummy load is modulated to discharge the output. This bit is reset when watchdog resets. This bit is set to 0 by default. This bit can be configured via the OTP. 0: Disabled 1: Enabled
7:5	N/A	RESERVED	0	Reserved. Do not change this bit value.
4	N/A	RESERVED	1	Reserved. Do not change this bit value.
3:0	N/A	RESERVED	0	Reserved. Do not change this bit value.

REG08h: Input Current Limit Setting

The REG08h register sets the input current limit.

Bit	Access	Name	Default	Description
15:7	N/A	RESERVED	0	Reserved.
6	R/W	I_{IN_LIM}[6]	0	Sets the input current limit. These bits are reset when the watchdog resets. These bits can be configured via the OTP. Range: Up to 6A (111 1000) Default: 500mA (000 1010) LSB: 50mA I_{IN_LIM} = DEC(Bits[6:0]) x 50 (mA) When RS1 changes to 5mΩ, the internal gain should also be changed via REG10h, bit[8] so that the LSB stays unchanged.
5	R/W	I_{IN_LIM}[5]	0	
4	R/W	I_{IN_LIM}[4]	0	
3	R/W	I_{IN_LIM}[3]	1	
2	R/W	I_{IN_LIM}[2]	0	
1	R/W	I_{IN_LIM}[1]	1	
0	R/W	I_{IN_LIM}[0]	0	

REG09h: Output Voltage Setting in Source Mode

The REG09h register sets the output voltage in source mode.

Bit	Access	Name	Default	Description
15:12	N/A	RESERVED	0	Reserved.
11	R/W	$V_{IN_SRC_OS}$	0	When this bit is enabled, V_{IN_SRC} is DEC(Bits[9:0]) + 0.64V. Keep this bit set to 0 in charge mode. This bit is set to 0 by default. 0: 0V 1: 0.64V
10	R/W	$V_{IN_SRC_CFG}$	0	This bit determines the method to configure V_{IN_SRC} in source mode. This bit is set to 0 by default. 0: Configured via register bit V_{IN_SRC}[9:0] 1: Configured via the FB pin
9	R/W	V_{IN_SRC}[9]	0	Sets V_{IN_SRC} in source mode. Range: Up to 20.46V (11 1111 1111) Default: 4.98V LSB: 20mV V_{IN_SRC} = DEC(Bits[9:0]) x 20 (mV) When REG09h, bit[11] = 1, then V_{IN_SRC} is DEC (Bits[9:0]) x 20 (mV) + 0.64V. The maximum V_{IN_SRC} is 21V.
8	R/W	V_{IN_SRC}[8]	0	
7	R/W	V_{IN_SRC}[7]	1	
6	R/W	V_{IN_SRC}[6]	1	
5	R/W	V_{IN_SRC}[5]	1	
4	R/W	V_{IN_SRC}[4]	1	
3	R/W	V_{IN_SRC}[3]	1	
2	R/W	V_{IN_SRC}[2]	0	
1	R/W	V_{IN_SRC}[1]	0	
0	R/W	V_{IN_SRC}[0]	1	

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REG0Ah: Battery Impedance Compensation and Output Current Limit Setting in Source Mode

The REG0Ah register sets the battery impedance compensation, battery-full regulation voltage, and the output current (I_{IN_SRC}) limit in source mode.

Bit	Access	Bit Name	Default	Description
15	N/A	RESERVED	0	Reserved.
14	N/A	RESERVED	0	Reserved.
13	R/W	BATTR[2]	0	Sets the predicted battery internal impedance and cable impedance. These bits are reset when watchdog resets. Range: 0mΩ/cell to 350mΩ/cell Default: 0mΩ/cell LSB: 50mΩ/cell BATTR = DEC(Bits[13:11]) x 50 (mΩ/cell)
12	R/W	BATTR[1]	0	
11	R/W	BATTR[0]	0	
10	R/W	V_{CLAMP}[2]	0	Sets the maximum compensation voltage, which should be added to the original battery-full regulation voltage if the IR compensation function is used. These bits are reset when the watchdog resets. Range: 0mV/cell to 420mV/cell Default: 0mV/cell LSB: 60mV/cell V_{CLAMP} = DEC(Bits[10:8]) x 60 (mV/cell)
9	R/W	V_{CLAMP}[1]	0	
8	R/W	V_{CLAMP}[0]	0	
7	N/A	RESERVED	0	Reserved.
6	R/W	I_{IN_SRC}[6]	0	Sets the I_{IN_SRC} limit in source mode. These bits are reset when the watchdog resets. Range: 0A to 6A Default: 2A LSB: 50mA I_{IN_SRC} = DEC(Bits[6:0]) x 50 (mA) When RS1 changes to 5mΩ, the internal gain should also be changed via REG10h, bit[8] so that the LSB is unchanged.
5	R/W	I_{IN_SRC}[5]	1	
4	R/W	I_{IN_SRC}[4]	0	
3	R/W	I_{IN_SRC}[3]	1	
2	R/W	I_{IN_SRC}[2]	0	
1	R/W	I_{IN_SRC}[1]	0	
0	R/W	I_{IN_SRC}[0]	0	

REG0Bh: Battery Low Voltage Setting and Battery Discharge Current Regulation in Source Mode

The REG0Bh register sets the low battery voltage thresholds, as well as the battery discharge current regulation in source mode.

Bit	Access	Name	Default	Description
15:14	N/A	RESERVED	NA	Reserved
13	R/W	V_{BATT_LOW}_EN	1	This bit enables the battery low-voltage protection. It is reset when watchdog resets. This bit is set to 1 by default. This bit can be configured via the OTP. 0: Disabled 1: Enabled
12	R/W	V_{BATT_PRE}	1	Sets the pre-charge to CC charge threshold. This bit is set to 1 by default. 0: 2.55V/cell 1: 3V/cell

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11	R/W	BATTLOW_ACT	0	Determines the behavior of battery low-voltage protection when REG0Bh, bit[13] is set to 1. If $V_{BATT} < V_{BATT_LOW}$ (which is set via REG0Bh, bits[10:9]), INT asserts and the DC/DC converter can also be latched off optionally. This bit is reset when the watchdog resets. This bit is set to 0 by default. This bit can be configured via the OTP. 0: Generate INT and disable the DC/DC converter 1: Generate INT and latch off the DC/DC converter Charging the battery or toggling the SRC_EN bit clears the DSCHG_FLT bit. Then the source can be enabled again. When source mode is disabled, the BATTLOW comparator does not operate.
10	R/W	V_{BATT_LOW}[1]	0	Sets the low battery voltage threshold for battery low-voltage protection. These bits are set to 00 by default. 00: 3V/cell 01: 3.1V/cell 10: 3.2V/cell 11: 3.3V/cell
9	R/W	V_{BATT_LOW}[0]	0	
8	R/W	$I_{BATT_DSCHG_EN}$	0	Enables battery discharge current regulation in source mode. This bit is set to 0 by default. 0: Disabled 1: Enabled
7	R/W	I_{BATT_DSCHG}[7]	1	Sets the battery discharge current in source mode. Range: Up to 12.75A Default: 6.4A LSB: 50mA $I_{BATT_DIS_LIM}$ = DEC(Bits[7:0]) x 50 (mA)
6	R/W	I_{BATT_DSCHG}[6]	0	
5	R/W	I_{BATT_DSCHG}[5]	0	
4	R/W	I_{BATT_DSCHG}[4]	0	
3	R/W	I_{BATT_DSCHG}[3]	0	
2	R/W	I_{BATT_DSCHG}[2]	0	
1	R/W	I_{BATT_DSCHG}[1]	0	
0	R/W	I_{BATT_DSCHG}[0]	0	

REG0Ch: JEITA Action Setting

The REG0Ch register controls the IC's action during JEITA protection.

Bit	Access	Bit Name	Default	Description
15	N/A	RESERVED	0	Reserved.
14	R/W	WARM_ACT[1]	0	Determines the device's behavior if NTC warm protection occurs. These bits are reset when the watchdog resets. 00: No action 01: Only reduce V_{BATT_REG} 10: Only reduce I_{CC} 11: Reduce both V_{BATT_REG} and I_{CC}
13	R/W	WARM_ACT[0]	1	
12	R/W	COOL_ACT[1]	1	Determines the device's behavior if NTC cool protection occurs. These bits are reset when the watchdog resets. 00: No action 01: Only reduce V_{BATT_REG} 10: Only reduce I_{CC} 11: Reduce both V_{BATT_REG} and I_{CC}
11	R/W	COOL_ACT[0]	0	

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10	R/W	JEITA_VSET[4]	1	Sets the decrement value for the battery-full voltage if NTC cool or warm protection occurs. The battery-full voltage can be set via REG15h. These bits are reset when the watchdog resets. Range: Up to 620mV/cell Default: 320mV/cell LSB: 20mV/cell JEITA_VSET = V_{BATT_REG} - DEC([Bits[10:6]) x 20 (mV/cell)
9	R/W	JEITA_VSET[3]	0	
8	R/W	JEITA_VSET[2]	0	
7	R/W	JEITA_VSET[1]	0	
6	R/W	JEITA_VSET[0]	0	
5	R/W	JEITA_ISET[1]	0	Sets the scaling value of the constant current (CC) charge current. The CC charge current can be set via REG14h. These bits are reset when the watchdog resets. These bits are set to 01 by default. 00: 1/2 times 01: 1/4 times 10: 1/8 times 11: 1/16 times
4	R/W	JEITA_ISET[0]	1	
3:0	N/A	RESERVED	0	Reserved.

REG0Dh: Temperature Protection Setting

The REG0Dh register sets the JEITA thresholds and includes the control bits for temperature protection.

Bit	Access	Bit Name	Default	Description
15	R/W	TS_EN	1	Enables the external temperature sense function. This bit is set to 1 by default. 0: Disabled 1: Enabled
14	NA	RESERVED	0	Reserved. Do not change this bit value.
13	R/W	TS_ACT	0	When TS_OPTION (REG0Dh, bit[14]) is set to 0, this bit determines the device's behavior if a TS over-temperature (OT) condition occurs. An INT asserts after TS OT occurs, and an additional I_{IN} regulation can be executed optionally. This bit is reset when the watchdog resets. This bit is set to 0 by default. This bit can be configured via the OTP. 0: Only deliver INT when reaching the TS threshold 1: Deliver INT and take the TS action
12	R/W	V_{TS_HOT}[2]	1	Sets the TS OT threshold, which is a percentage of V_{NTC}. These bits are set to 100 by default. Assume that the thermistor is 103AT, and the pull-up resistor is 10kΩ. 000: 9.68% (100°C) 001: 10.62% (95°C) 010: 11.98% (90°C) 011: 13.29% (85°C) 100: 14.95% (80°C) 101: 16.74% (75°C) 110: 18.74% (70°C) 111: 21.11% (65°C)
11	R/W	V_{TS_HOT}[1]	0	
10	R/W	V_{TS_HOT}[0]	0	
9	R/W	NTC_EN	1	Enables NTC protection. This bit is set to 1 by default. 0: Disabled 1: Enabled

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8	R/W	NTC_ACT	1	Determines the device's behavior if NTC protection occurs. An INT asserts when NTC protection occurs, and additional actions can be taken optionally. This bit is set to 1 by default. This bit can be configured via the OTP. 0: Only deliver INT when the NTC threshold is reached 1: Deliver INT and take JEITA action
7	R/W	V_{HOT}[1]	1	Sets the NTC hot temperature threshold, which is a percentage of V_{NTC}. These bits are set to 10 by default. Assume that the thermistor is 103AT. 00: 29.63% (50°C) 01: 26.46% (55°C) 10: 23.6% (60°C) 11: 21.03% (65°C)
6	R/W	V_{HOT}[0]	0	
5	R/W	V_{WARM}[1]	0	Sets the NTC warm temperature threshold, which is a percentage of V_{NTC}. These bits are set to 01 by default. Assume that the thermistor is 103AT. 00: 36.86% (40°C) 01: 33.2% (45°C) 10: 29.61% (50°C) 11: 26.45% (55°C)
4	R/W	V_{WARM}[0]	1	
3	R/W	V_{COOL}[1]	1	Sets the NTC cool temperature threshold, which is a percentage of V_{NTC}. These bits are set to 10 by default. Assume that the thermistor is 103AT. 00: 74.68% (0°C) 01: 70.12% (5°C) 10: 65.2% (10°C) 11: 59.9% (15°C)
2	R/W	V_{COOL}[0]	0	
1	R/W	V_{COLD}[1]	0	Sets the NTC cold temperature threshold, which is a percentage of V_{NTC}. These bits are set to 01 by default. Assume that the thermistor is 103AT. 00: 78.82% (-5°C) 01: 74.5% (0°C) 10: 70.12% (5°C) 11: 65.29% (10°C)
0	R/W	V_{COLD}[0]	1	

REG0Eh: Configuration Register 0

The REG0Eh register controls certain ADC options and sets the switching frequency.

Bit	Access	Bit Name	Default	Description
15:9	N/A	RESERVED	0	Reserved.
8	N/A	RESERVED	0	Reserved.
7	R/W	ADC_CONV	0	Determines the behavior for ADC conversion when only a battery is present. 0: Disable the ADC 1: Continuous ADC conversion

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6	R/W	SW_FREQ[2]	0	Sets the buck-boost converter's switching frequency. These bits are reset when the watchdog resets. These bits are set to 001 by default. These bits can be configured via the OTP. 000: 375kHz 001: 425kHz 010: 475kHz 011: 510kHz 100: 550kHz 101: 625kHz 110: 700kHz 111: 770kHz
5	R/W	SW_FREQ[1]	0	
4	R/W	SW_FREQ[0]	1	
3	NA	RESERVED	1	Reserved. Do not change this bit value.
2:0	NA	RESERVED	0	Reserved. Do not change this bit value.

REG0Fh: Configuration Register 1

The REG0Fh register sets the junction temperature, trickle charge current, pre-charge current, and termination current.

Bit	Access	Bit Name	Default	Description
15	R/W	TJ_REG_EN	1	Enables the junction temperature's OT regulation. This bit is reset when watchdog resets. This bit is set to 1 by default. This bit can be configured via the OTP. 0: Disabled 1: Enabled
14	R/W	T_{J_REG}[2]	1	Sets the junction temperature's (T_J) regulation point. These bits are reset when the watchdog resets. These bits are set to 111 by default. 000: 80°C 001: 90°C 010: 95°C 011: 100°C 100: 105°C 101: 110°C 110: 115°C 111: 120°C
13	R/W	T_{J_REG}[1]	1	
12	R/W	T_{J_REG}[0]	1	
11	R/W	I_{TC}[3]	0	Sets the trickle-charge current. These bits are reset when the watchdog resets. These bits can be configured via the OTP. Range: 0mA to 750mA Default: 100mA LSB: 50mA I_{TC} = DEC(Bits[11:8]) x 50 (mA)
10	R/W	I_{TC}[2]	0	
9	R/W	I_{TC}[1]	1	
8	R/W	I_{TC}[0]	0	
7	R/W	I_{PRE}[7]	0	Sets the pre-charge current. These bits are reset when the watchdog resets. These bits can be configured via the OTP. Range: Up to 1.5A Default: 400mA LSB: 100mA I_{PRE} = DEC(Bits[7:4]) x 100 (mA)
6	R/W	I_{PRE}[6]	1	
5	R/W	I_{PRE}[5]	0	
4	R/W	I_{PRE}[4]	0	
3	R/W	I_{TERM}[3]	0	Sets the termination current. These bits are reset when the watchdog resets. These bits can be configured via the OTP. Range: Up to 750mA Default: 200mA LSB: 50mA I_{TERM} = DEC(Bits[3:0]) x 50 (mA)
2	R/W	I_{TERM}[2]	1	
1	R/W	I_{TERM}[1]	0	
0	R/W	I_{TERM}[0]	0	

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REG10h: Configuration Register 2

The REG10h register sets some control bits and sets the battery cell number.

Bit	Access	Bit Name	Default	Description
15	NA	RESERVED	0	Reserved.
14	R/W	ACGATE_CTRL	0	Controls the ACGATE. It can force ACGATE to turn on external MOSFET when it is set to 1. This bit is set to 0 by default, and the ACGATE state depends on the ADP voltage. 0: Do not force ACGATE on 1: Force ACGATE on
13	NA	RESERVED	0	Reserved. Do not change this bit
12	R/W	TS/IMON	0	Configures the function of the TS/IMON pin. This bit is reset when the watchdog timer resets. This bit is set to 0 by default. This bit can be configured via the OTP. 0: Act as the TS function 1: Act as the IMON function
11	R/W	VRECH	1	Sets the automatic recharge threshold, which is below the battery-full voltage. This bit is reset when watchdog timer resets. This bit is set to 1 by default. This bit can be configured via the OTP. 0: 100mV/cell 1: 200mV/cell
10	R/W	BAT_NUM[1]	0	Sets the battery cells in series. These bits are reset when the watchdog timer resets. These bits are set to 00 by default. These bits can be configured via the OTP. 00: 5 cells 01: 2 cells 10: 3 cells 11: 4 cells
9	R/W	BAT_NUM[0]	0	
8	R/W	IN_RSNS	0	Sets the I_{IN} sense gain. This bit should be set according to the external sense resistor (RS1). This bit is reset when the watchdog timer resets. This bit is set to 0 by default. This bit can be configured via the OTP. 0: 10mΩ sense FET adopted 1: 5mΩ
7	R/W	IBATT_RSNS	0	Sets the battery current-sense gain. This bit should be set according to external sense resistor (RS2). This bit is reset when the watchdog timer resets. This bit is set to 0 by default. This bit can be configured via the OTP. 0: 10mΩ sense FET adopted 1: 5mΩ
6	R/W	ACGATE_EN	1	Enables the ACGATE driver. This bit is set to 1 by default. 0: Disable the ACGATE driver 1: Enable ACGATE driver
5	N/A	RESERVED	0	Reserved. Do not change the value of this bit.
4:0	N/A	RESERVED	0	Reserved. Do not change the value of these bits.

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REG11h: Configuration Register 3

The REG11h register sets the system's voltage protections and input voltage protections in charge mode, as well as battery over-voltage protection (OVP).

Bit	Access	Bit Name	Default	Description
15	N/A	RESERVED	0	Reserved.
14	R/W	$V_{IN_SRC_OV}$[1]	1	Sets the over-voltage (OV) threshold for the source V_{IN_SRC}. These bits are set to 11 by default. 00: 106% 01: 120% 10: 115% 11: 110%
13	R/W	$V_{IN_SRC_OV}$[0]	1	
12	R/W	$V_{IN_SRC_UV}$[1]	0	Sets the under-voltage (UV) threshold for the source V_{IN_SRC}. These bits are set to 00 by default. 00: 75% 01: 80% 10: 85% 11: 30%
11	R/W	$V_{IN_SRC_UV}$[0]	0	
10	R/W	$t_{IN_OVP_DGL}$	0	Sets the deglitch time for input OVP in charging mode. This bit is set to 0 by default. 0: 1µs 1: 15ms
9	R/W	V_{IN_UVP}[1]	0	Sets the input under-voltage protection (UVP) threshold. These bits are reset when the watchdog timer resets. These bits are set to 00 by default. These bits can be configured via the OTP. 00: 3.2V 01: 6.4V 10: 12V 11: 16.8V
8	R/W	V_{IN_UVP}[0]	0	
7	R/W	V_{IN_OVP}[1]	1	Sets the input OVP threshold. These bits are reset when the watchdog timer resets. These bits are set to 11 by default. These bits can be configured via the OTP. 00: 7.25V 01: 11.25V 10: 17.65V 11: 22.45V
6	R/W	V_{IN_OVP}[0]	1	
5	N/A	RESERVED	1	Reserved. Do not change the value of this bit.
4	N/A	RESERVED	0	Reserved. Do not change the value of this bit.
3	R/W	BATTOVP_EN	1	Enables battery OVP. This bit is set to 1 by default. 0: Disabled 1: Enabled
2	R/W	BATT_DUMMY	0	Enables the BATT dummy load. This bit is set to 0 by default. 0: Disabled 1: Enabled
1:0	R/W	RESERVED	0	Reserved. Do not change the value of these bits.

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REG12h: Configuration Register 4

The REG12h register sets some control bits for the charge timer, watchdog timer, and on/off control for charge and source mode.

Bit	Access	Bit Name	Default	Description
15	N/A	RESERVED	0	Reserved. Do not change this bit value.
14	N/A	RESERVED	0	Reserved. Do not change this bit value.
13	R/W	TMR_EN	1	Enables the charging safety timers (both the TC/pre-charge timer and CC/CV charge timer). This bit is reset when the watchdog resets. This bit is set to 1 by default. This bit can be configured via the OTP. 0: Disabled 1: Enabled
12	R/W	CHG_TMR[1]	1	Sets the CC/CV timer. This bit is reset when the watchdog resets. These bits are set to 11 by default. 00: 5 hours 01: 8 hours 10: 12 hours 11: 20 hours
11	R/W	CHG_TMR[0]	1	
10	R/W	TMR2X_EN	1	Controls the charge timer's speed during input voltage, input current, or thermal regulation. This bit is reset when the watchdog resets. This bit is set to 1 by default. 0: The timer counts at a normal clock rate 1: The timer counts at a half-clock rate
9	R/W	WTD_RST	0	Resets the I^2C watchdog timer. This bit returns to 0 after it is reset. This bit is reset when the watchdog resets. This bit is set to 0 by default. 0: Normal 1: Reset
8	R/W	WTD[1]	0	Sets the I^2C watchdog timer. These bits are reset when the watchdog resets. These bits are set to 00 by default. These bits can be configured via the OTP. 00: Disable the timer 01: 40s 10: 80s 11: 175s
7	R/W	WTD[0]	0	
6	R/W	DC/DC_EN	1	Enables the DC/DC converter. This bit is reset when the watchdog resets. This bit is set to 0 by default. This bit can be configured via the OTP. 0: Disabled 1: Enabled
5	N/A	RESERVED	0	Reserved. Do not change this bit value.
4	R/W	TERM_EN	1	Enables charge termination. This bit is reset when the watchdog resets. This bit is set to 1 by default. 0: Disabled 1: Enabled
3	R/W	SRC_EN	0	Enables source mode configuration. SRC_EN can override the charge enable function. This bit is reset when the watchdog resets. This bit is set to 0 by default. 0: Disable source mode 1: Enable source mode

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2	R/W	REG_RST	0	Sets the register reset setting. This bit resets to 0 after the register is reset. This bit is set to 0 by default. This bit is reset when the watchdog resets. 0: Keep the current register setting 1: Reset to the default register value and reset the safety timer
1	R/W	IINLIM_EN	1	Enables the I_{IN} limit loop (IIN_LIM). This bit is reset when the watchdog resets. This bit is set to 1 by default. 0: Disabled 1: Enabled
0	R/W	CHG_EN	1	Configures charge mode. SRC_EN overrides the CHG_EN enable function. This bit is reset when the watchdog resets. This bit is set to 1 by default. This bit can be configured via the OTP. 0: Charge disabled 1: Charge enabled

REG14h: Charge Current Setting

The REG14h register sets the battery constant fast charge current.

Bit	Access	Bit Name	Default	Description
15:14	N/A	RESERVED	0	Reserved.
13	R/W	I_{CC}[7]	0	Sets the charge current. These bits are reset when the watchdog resets. These bits can be configured via the OTP. Range: 0A to 6A Default: 2A LSB: 50mA I_{CC} = DEC(Bits[13:6]) x 50 (mA)
12	R/W	I_{CC}[6]	0	
11	R/W	I_{CC}[5]	1	
10	R/W	I_{CC}[4]	0	
9	R/W	I_{CC}[3]	1	
8	R/W	I_{CC}[2]	0	
7	R/W	I_{CC}[1]	0	
6	R/W	I_{CC}[0]	0	
5:0	N/A	RESERVED	0	Reserved.

REG15h: Battery Regulation Voltage Setting

The REG15h register sets the battery-full regulation voltage.

Bit	Access	Bit Name	Default	Description
15	NA	RESERVED	0	Reserved.

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14	R/W	V_{BATT_REG}[10]	0	Sets the charge-full voltage. These bits are reset when the watchdog resets. These bits can be configured via the OTP. The default is 4.2V/cell while BAT_NUM = 5-cell, and the charge-full voltage is 21V. Charge-Full Voltage = DEC(REG15h, Bits[14:4]) x 10 (mV)) For 5-cell applications: When BAT_NUM (REG10h, bits[10:9]) = 00 for a 5-cell battery pack, V_{BATT_REG}[10:0] (REG15h, bits[14:4]) sets the cell voltage with a range between 3.4V and 4.4V. The charge-full voltage is V_{BATT_REG} x BAT_NUM. For example: for a 5-cell application with 4.2V/cell, V_{BATT_REG} = 4.2V, and the charge-full voltage is 21V. For 2-cell to 4-cell applications: When BAT_NUM (REG10h, bits[10:9]) = 01/10/11 for 2-cell to 4-cell battery packs, V_{BATT_REG}[10:0] (REG15h, bits [14:4]) sets the charge-full voltage, with a range between 3.4V/cell to 4.67V/cell. For example: for a 4-cell application with 4.2V/cell, V_{BATT_REG} = 16.8V, and the charge-full voltage is 16.8V.
13	R/W	V_{BATT_REG}[9]	0	
12	R/W	V_{BATT_REG}[8]	1	
11	R/W	V_{BATT_REG}[7]	1	
10	R/W	V_{BATT_REG}[6]	0	
9	R/W	V_{BATT_REG}[5]	1	
8	R/W	V_{BATT_REG}[4]	0	
7	R/W	V_{BATT_REG}[3]	0	
6	R/W	V_{BATT_REG}[2]	1	
5	R/W	V_{BATT_REG}[1]	0	
4	R/W	V_{BATT_REG}[0]	0	
3:0	R/W	RESERVED	0	Reserved.

REG16h: Status and Fault Register 0

The REG16h register indicates the charge status and TS hot fault status.

Bit	Access	Bit Name	Default	Description
15	R	MD_STAT[1]	0	Indicates the DC/DC converter's status. These bits assert INT when the state changes. 00/10: Idle 01/11: Operation
14	R	MD_STAT[0]	0	
13	R	PG_STAT	0	Indicates the power good (PG) status. This bit asserts INT when it changes from 0 to 1. 0: V_{IN} not power good 1: V_{IN} power good
12	R	SWITCH_STAT[1]	0	Indicates the DC/DC converter's operation mode. 00: Idle 01: Buck 10: Buck-Boost 11: Boost
11	R	SWITCH_STAT[0]	0	
10	R	BATT MISS_STAT	0	Indicates whether the battery is missing. This bit asserts INT when it changes from 0 to 1. 0: Normal operation 1: Battery missing
9	N/A	RESERVED	0	Reserved.
8	R	CHG_STAT[2]	0	Indicates the charging status. These bits assert INT when the state changes. 000: No charging 001: Trickle charge 010: Pre-charge 011: CC charge 100: CV charge 101: Charge termination
7	R	CHG_STAT[1]	0	
6	R	CHG_STAT[0]	0	

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5	R	VIN_MIN_STAT	0	Indicates whether the IC is within the V_{IN} loop. This bit asserts INT when it changes from 0 to 1. 0: Not within the input voltage limit 1: Within the input voltage limit
4	R	IIN_LIM_STAT	0	Indicates whether the IC stays within the I_{IN} loop This bit asserts INT when it changes from 0 to 1. 0: Not within the input current limit 1: Within the input current limit
3	N/A	RESERVED	0	Reserved.
2	N/A	RESERVED	0	Reserved.
1	R	TS_FAULT	0	Indicates whether a TS-related fault occurs. This bit asserts INT if a hot TS fault occurs. 0: Normal operation 1: A TS hot fault has occurred
0	N/A	RESERVED	0	Reserved.

REG17h: Status and Fault Register 1

The REG17h register indicates the faults in charge and source mode.

Bit	Access	Bit Name	Default	Description
15	R	VIN_SRC_OV	0	Indicates whether output over-voltage protection (OVP) has occurred in source mode. This bit asserts INT if output OVP occurs. 0: Normal operation 1: OVP has occurred at VIN in source mode.
14	R	VIN_SRC_UV	0	Indicates whether output under-voltage protection (UVP) has occurred in source mode. This bit asserts INT if output UVP occurs. 0: Normal operation 1: UVP has occurred at VIN in source mode
13	R	VIN_OV	0	Indicates whether input OVP has occurred in charging mode. This bit asserts INT if input OVP occurs. 0: Normal operation 1: Input OVP has occurred in charge mode
12	R	VADP_OV	0	Indicates whether ADP OVP has occurred in charging mode. This bit asserts INT if V_{ADP} OVP occurs. 0: Normal operation 1: V_{ADP} OVP has occurred
11	N/A	RESERVED	0	Reserved.
10	N/A	RESERVED	0	Reserved.
9	N/A	RESERVED	0	Reserved.
8	R	VBATT_OV	0	Indicates whether battery OVP occurs in charge mode. It asserts INT when battery OVP occurs. 0: Normal operation 1: Battery OVP has occurred in charge mode

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<table>
<tr><td>7</td><td>R</td><td>VBATT_LOW</td><td>0</td><td>Indicates whether there is a low battery voltage in source mode. This bit asserts INT if a BATT_LOW condition occurs.

0: Normal operation
1: Discharge stops due to BATT_LOW</td></tr>
<tr><td>6</td><td>R</td><td>WTD_EXP</td><td>0</td><td>Indicates whether the watchdog timer has expired.

0: Normal operation
1: The watchdog timer has expired</td></tr>
<tr><td>5</td><td>R</td><td>CHG_TMR_EXP</td><td>0</td><td>Indicates whether the charge safety timer has expired. This bit asserts INT if the timer expires.

0: Normal operation
1: The charge safety timer has expired</td></tr>
<tr><td>4</td><td>R</td><td>THERM_SHDN</td><td>0</td><td>Indicates whether thermal shutdown has occurred. This bit asserts INT if thermal shutdown occurs.

0: Normal operation
1: Thermal shutdown has occurred</td></tr>
<tr><td>3</td><td>R/W</td><td>RESERVED</td><td>0</td><td>Reserved.</td></tr>
<tr><td>2</td><td>R</td><td>NTC_FAULT[2]</td><td>0</td><td rowspan="3">Indicates whether an NTC fault has occurred in charge mode or source mode. These bits assert INT if any fault occurs.

<table><tr><th colspan="2">Charge Mode</th><th colspan="2">Source Mode</th></tr><tr><td>000</td><td>Normal</td><td>000</td><td>Normal</td></tr><tr><td>001</td><td>NTC Cold</td><td>001</td><td>NTC Cold</td></tr><tr><td>010</td><td>NTC Cool</td><td>100</td><td>NTC Hot</td></tr><tr><td>011</td><td>NTC Warm</td><td>111</td><td>NTC Float</td></tr><tr><td>100</td><td>NTC Hot</td><td>-</td><td>-</td></tr><tr><td>111</td><td>NTC Float</td><td>-</td><td>-</td></tr></table></td></tr>
<tr><td>1</td><td>R</td><td>NTC_FAULT[1]</td><td>0</td></tr>
<tr><td>0</td><td>R</td><td>NTC_FAULT[0]</td><td>0</td></tr>
</table>

REG18h: INT Mask Setting Register 0

The REG18h register controls the INT mask.

Bit	Access	Bit Name	Default	Description
15	NA	RESERVED	0	Reserved.
14	NA	RESERVED	0	Reserved.
13	R/W	VIN_SRC_FAULT	0	For any fault that is masked, INT does not assert if that fault occurs. However, the fault bit is still set. These bits are reset when the watchdog timer resets. 0: Masked 1: Not masked
12	R/W	VIN_OV_FAULT	0	
11	R/W	PG_STAT	0	
10	R/W	BATT_OV_FAULT	0	
9	NA	RESERVED	0	Reserved.
8	NA	RESERVED	0	Reserved.
7	R/W	BATT_LOW_FAULT	0	For any fault that is masked, INT does not assert if that fault occurs. However, the fault bit is still set. These bits are reset when the watchdog timer resets. 0: Masked 1: Not masked
6	R/W	BATT_MISS_STAT	0	
5	R/W	THERM_SHDN	0	
4	R/W	TS_FAULT	0	
3	R/W	NTC_FAULT	0	
2	R/W	CHG_TMR_FAULT	0	
1	R/W	MD_STAT	0	
0	R/W	CHG_STAT	0	

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REG19h: INT Mask Setting Register 1

The REG19h register controls the INT mask for the input power path.

Bit	Access	Bit Name	Default	Description
15:3	NA	RESERVED	0	Reserved
2	R/W	TJREG_STAT	0	For any fault that is masked, INT does not assert if that fault occurs. However, the fault bit is still set. These bits are reset when the watchdog timer resets. 0: Masked 1: Not masked
1	R/W	VIN_MIN_STAT	0	
0	R/W	IIN_LIM_STAT	0	

REG23h: ADC Result of the Input Voltage

The REG23h register indicates the ADC's input voltage result.

Bit	Access	Bit Name	Default	Description
15:10	N/A	RESERVED	N/A	Reserved.
9	R	V_{IN_ADC}[9]	N/A	Indicates the ADC's V_{IN} conversion. LSB: 20mV V_{IN_ADC} = DEC(Bits[9:0]) x 20 (mV)
8	R	V_{IN_ADC}[8]	N/A	
7	R	V_{IN_ADC}[7]	N/A	
6	R	V_{IN_ADC}[6]	N/A	
5	R	V_{IN_ADC}[5]	N/A	
4	R	V_{IN_ADC}[4]	N/A	
3	R	V_{IN_ADC}[3]	N/A	
2	R	V_{IN_ADC}[2]	N/A	
1	R	V_{IN_ADC}[1]	N/A	
0	R	V_{IN_ADC}[0]	N/A	

REG24h: ADC Result of the Input Current

The REG24h register indicates the ADC's input current results.

Bit	Access	Bit Name	Default	Description
15:10	N/A	RESERVED	N/A	Reserved.
9	R	I_{IN_ADC}[9]	N/A	Indicates the ADC's I_{IN} conversion. LSB: 6.25mA I_{IN_ADC} = DEC(Bits[9:0]) x 6.25 (mA)
8	R	I_{IN_ADC}[8]	N/A	
7	R	I_{IN_ADC}[7]	N/A	
6	R	I_{IN_ADC}[6]	N/A	
5	R	I_{IN_ADC}[5]	N/A	
4	R	I_{IN_ADC}[4]	N/A	
3	R	I_{IN_ADC}[3]	N/A	
2	R	I_{IN_ADC}[2]	N/A	
1	R	I_{IN_ADC}[1]	N/A	
0	R	I_{IN_ADC}[0]	N/A	

REG25h: ADC Result of the Battery Voltage Per Cell

The REG25h register indicates the ADC's battery voltage per cell result.

Bit	Access	Bit Name	Default	Description
15:10	N/A	RESERVED	N/A	Reserved.

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9	R	V_{BATT_ADC}[9]	N/A	Indicates the ADC's conversion for the battery voltage per cell. The real battery voltage is the read value multiplied by the number of cells. LSB: 5mV/cell V_{BATT_ADC} = DEC(Bits[9:0]) x 5 (mV/cell)
8	R	V_{BATT_ADC}[8]	N/A	
7	R	V_{BATT_ADC}[7]	N/A	
6	R	V_{BATT_ADC}[6]	N/A	
5	R	V_{BATT_ADC}[5]	N/A	
4	R	V_{BATT_ADC}[4]	N/A	
3	R	V_{BATT_ADC}[3]	N/A	
2	R	V_{BATT_ADC}[2]	N/A	
1	R	V_{BATT_ADC}[1]	N/A	
0	R	V_{BATT_ADC}[0]	N/A	

REG27h: ADC Result of the Battery Charge Current

The RE27h register indicates the ADC's battery charge current result.

Bit	Access	Bit Name	Default	Description
15:10	N/A	RESERVED	N/A	Reserved.
9	R	I_{BATT_ADC}[9]	N/A	Indicates the ADC's conversion for the charge current via the external 10mΩ sense resistor. LSB: 12.5mA I_{BATT_ADC} = DEC(Bits[9:0]) x 12.5 (mA)
8	R	I_{BATT_ADC}[8]	N/A	
7	R	I_{BATT_ADC}[7]	N/A	
6	R	I_{BATT_ADC}[6]	N/A	
5	R	I_{BATT_ADC}[5]	N/A	
4	R	I_{BATT_ADC}[4]	N/A	
3	R	I_{BATT_ADC}[3]	N/A	
2	R	I_{BATT_ADC}[2]	N/A	
1	R	I_{BATT_ADC}[1]	N/A	
0	R	I_{BATT_ADC}[0]	N/A	

REG28h: ADC Result of the NTC Sense Ratio

The REG28h register indicates the ADC's NTC sense ratio result.

Bit	Access	Bit Name	Default	Description
15:10	N/A	RESERVED	N/A	Reserved.
9	R	NTC_{ADC}[9]	N/A	Indicates the ADC's conversion for the NTC voltage, as a percentage of V_{NTC}. The real battery temperature can be recalculated according to external divider and thermistor datasheet. LSB: 1/1024 NTC_{ADC} = DEC(Bits[9:0]) x 1/1024 x 100%
8	R	NTC_{ADC}[8]	N/A	
7	R	NTC_{ADC}[7]	N/A	
6	R	NTC_{ADC}[6]	N/A	
5	R	NTC_{ADC}[5]	N/A	
4	R	NTC_{ADC}[4]	N/A	
3	R	NTC_{ADC}[3]	N/A	
2	R	NTC_{ADC}[2]	N/A	
1	R	NTC_{ADC}[1]	N/A	
0	R	NTC_{ADC}[0]	N/A	

REG29h: ADC Result of the TS Sense Ratio

The REG29h register indicates the ADC's TS sense ratio result.

Bit	Access	Bit Name	Default	Description
15:10	N/A	RESERVED	N/A	Reserved.

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9	R	TS_{ADC}[9]	N/A	Indicates the ADC's conversion for the TS voltage, as a percentage of V_{NTC}. LSB: 1/1024 TS_{ADC} = DEC(Bits[9:0]) x 1/1024 x 100%
8	R	TS_{ADC}[8]	N/A	
7	R	TS_{ADC}[7]	N/A	
6	R	TS_{ADC}[6]	N/A	
5	R	TS_{ADC}[5]	N/A	
4	R	TS_{ADC}[4]	N/A	
3	R	TS_{ADC}[3]	N/A	
2	R	TS_{ADC}[2]	N/A	
1	R	TS_{ADC}[1]	N/A	
0	R	TS_{ADC}[0]	N/A	

REG2Ah: ADC Result of the Junction Temperature

The REG2Ah register indicates the ADC's junction temperature result.

Bit	Access	Bit Name	Default	Description
15:10	N/A	RESERVED	N/A	Reserved.
9	R	T_{J_ADC}[9]	N/A	Indicates the ADC's conversion for the junction temperature. LSB: 1 T_{J_ADC} = 314 - 0.5703 x DEC(Bits[9:0])
8	R	T_{J_ADC}[8]	N/A	
7	R	T_{J_ADC}[7]	N/A	
6	R	T_{J_ADC}[6]	N/A	
5	R	T_{J_ADC}[5]	N/A	
4	R	T_{J_ADC}[4]	N/A	
3	R	T_{J_ADC}[3]	N/A	
2	R	T_{J_ADC}[2]	N/A	
1	R	T_{J_ADC}[1]	N/A	
0	R	T_{J_ADC}[0]	N/A	

REG2Bh: ADC Result of the Battery Discharge Current

The REG2Bh register indicates the ADC's battery discharge current result.

Bit	Access	Bit Name	Default	Description
15:10	N/A	RESERVED	N/A	Reserved.
9	R	$I_{BATT_DIS_ADC}$[9]	N/A	Indicates the ADC's conversion for the battery discharge charge current. Offset: 900mA LSB: 12.5mA $I_{BATT_DIS_ADC}$ = DEC(Bits[9:0]) x 12.5 (mA) - 900
8	R	$I_{BATT_DIS_ADC}$[8]	N/A	
7	R	$I_{BATT_DIS_ADC}$[7]	N/A	
6	R	$I_{BATT_DIS_ADC}$[6]	N/A	
5	R	$I_{BATT_DIS_ADC}$[5]	N/A	
4	R	$I_{BATT_DIS_ADC}$[4]	N/A	
3	R	$I_{BATT_DIS_ADC}$[3]	N/A	
2	R	$I_{BATT_DIS_ADC}$[2]	N/A	
1	R	$I_{BATT_DIS_ADC}$[1]	N/A	
0	R	$I_{BATT_DIS_ADC}$[0]	N/A	

REG2Ch: ADC Result of Input Voltage in Source Mode

The REG2Ch register indicates the ADC's input voltage in source mode result.

Bit	Access	Bit Name	Default	Description
15:10	N/A	RESERVED	N/A	Reserved.

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9	R	$V_{IN_SRC_ADC}$[9]	N/A	Indicates the ADC's V_{IN_SRC} conversion at the IN pin in source mode. LSB: 20mV $V_{IN_SRC_ADC}$ = DEC(Bits[9:0]) x 20 (mV)
8	R	$V_{IN_SRC_ADC}$[8]	N/A	
7	R	$V_{IN_SRC_ADC}$[7]	N/A	
6	R	$V_{IN_SRC_ADC}$[6]	N/A	
5	R	$V_{IN_SRC_ADC}$[5]	N/A	
4	R	$V_{IN_SRC_ADC}$[4]	N/A	
3	R	$V_{IN_SRC_ADC}$[3]	N/A	
2	R	$V_{IN_SRC_ADC}$[2]	N/A	
1	R	$V_{IN_SRC_ADC}$[1]	N/A	
0	R	$V_{IN_SRC_ADC}$[0]	N/A	

REG2Dh: ADC Result of Output Current in Source Mode

The REG2Dh register indicates the ADC's output current in source mode result.

Bit	Access	Bit Name	Default	Description
15:10	N/A	RESERVED	N/A	Reserved.
9	R	$I_{IN_SRC_ADC}$[9]	N/A	Indicates the ADC's I_{IN_SRC} conversion in source mode. LSB: 6.25mA $I_{IN_SRC_ADC}$ = DEC(Bits[9:0]) x 6.25 (mA)
8	R	$I_{IN_SRC_ADC}$[8]	N/A	
7	R	$I_{IN_SRC_ADC}$[7]	N/A	
6	R	$I_{IN_SRC_ADC}$[6]	N/A	
5	R	$I_{IN_SRC_ADC}$[5]	N/A	
4	R	$I_{IN_SRC_ADC}$[4]	N/A	
3	R	$I_{IN_SRC_ADC}$[3]	N/A	
2	R	$I_{IN_SRC_ADC}$[2]	N/A	
1	R	$I_{IN_SRC_ADC}$[1]	N/A	
0	R	$I_{IN_SRC_ADC}$[0]	N/A	

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APPLICATION INFORMATION

Selecting the Input Capacitor

The input capacitor absorbs the maximum ripple current from the PWM converter. The input current (I_{IN}) is discontinuous in buck mode. The input capacitor's RMS ripple current (I_{CIN_RMS}) can be calculated with Equation (3):

$$I_{CIN_RMS} = I_{CHG} \times \frac{\sqrt{V_{BATT} \times (V_{IN} - V_{BATT})}}{V_{IN}} \quad (3)$$

The worst-case RMS ripple current occurs at a 50% duty cycle. Typically, V_{BATT} is between 15V and 20V for the 5-cell battery configuration, which means the worst-case condition occurs when V_{IN} is 20V.

Low-ESR ceramic capacitors with X7R or X5R dielectrics are recommended to be the input decoupling capacitor. These capacitors should be placed as close as possible to the IN and PGND pins, and their voltage rating must exceed the normal V_{IN} level. A capacitor with a minimum 35V voltage is recommended for up to 20V V_{IN}. It is recommended to use 1 x 1μF and 5 x 10μF capacitors for an I_{IN} limit up to 3A.

Ceramic capacitors show a DC-bias effect that reduces the capacitor's effective capacitances. The effect may lead to a significant capacitance drop, especially at higher input voltages with small capacitor packages. Choose a higher voltage rating or nominal capacitance to obtain the required value at the relevant operation point.

VCC Decoupling Capacitor

VCC is an internal LDO output. Place an external 4.7μF decoupling capacitor between VCC and AGND, and as close to these pins as possible.

Selecting the Inductor

The MP2652 can operate in buck mode or boost mode, which means that the inductor current is equal to either the charging current (I_{CHG}) or I_{IN}. The inductor's saturation current should exceed the larger value between I_{IN} and I_{CHG}, plus half the ripple current. The inductor current ripples in buck mode and boost mode can be calculated with Equation (4) and Equation (5), respectively:

$$I_{RIPPLE_BUCK} = \frac{V_{BATT} \times (V_{IN} - V_{BATT})}{V_{IN} \times f_{SW} \times L} \quad (4)$$

$$I_{RIPPLE_BOOST} = \frac{V_{IN} \times (V_{BATT} - V_{IN})}{V_{BATT} \times f_{SW} \times L} \quad (5)$$

The inductor ripple current (I_{RIPPLE}) depends on V_{IN}, the CFLR pin's voltage (V_{CFLR}), the switching frequency (f_{SW}), and the inductance (*L*). The inductance (*L*) in buck mode can be estimated with Equation (6):

$$L = \frac{V_{BATT} \times (V_{IN} - V_{BATT})}{I_{RIPPLE_BUCK} \times V_{IN} \times f_{SW}} \quad (6)$$

The required inductance (*L*) in boost mode can be calculated with Equation (7):

$$L = \frac{V_{IN} \times (V_{BATT} - V_{IN})}{V_{BATT} \times f_{SW} \times I_{RIPPLE_BOOST}} \quad (7)$$

The MP2652 has a configurable f_{SW} from 375kHz to 770kHz. Higher switching frequencies means that smaller-value inductors can be used. The inductor saturation current should exceed I_{CHG} plus half of the ripple current.

The maximum input ripple current occurs when the duty cycle is 50%.

For example, the battery charging voltage ranges from 12V to 16V for a 4-cell battery pack. For a 20V adapter voltage, a 12V V_{BATT} gives the maximum inductor ripple current.

Another example is a 3-cell battery with a V_{BATT} range between 9V and 13.2V. For a 20V adapter voltage, a 10V V_{BATT} gives the maximum inductor ripple current.

Generally, the inductor ripple is designed to be between 20% and 40% of the maximum charging current. For practical designs, there is a tradeoff between inductor size and efficiency. The recommend inductance is 4.7μH for 2 to 4 cells in series (see Table 5).

Table 5: Recommended Inductance

Cell Number	5-Cell	2-Cell	3-Cell	4-Cell
L (μH)	4.7	3.3		

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Selecting the Output Capacitor

The output capacitor (C_{BATT}) should have a sufficient ripple current rating to absorb the output AC current.

In the boost mode operation, I_{OUT} is discontinuous and dominates the output RMS ripple current (I_{CBATT_BOOST}) can be calculated with Equation (8)

$$I_{CBATT_BOOST} = I_{CHG} \times \frac{\sqrt{V_{IN} \times (V_{BATT} - V_{IN})}}{V_{IN}} \quad (8)$$

The worst-case output RMS ripple current occurs at the lowest VBUS input voltage. The CFLR voltage is approximately 8V for the 2-cell battery packs, so the worst-case scenario occurs when the voltage is 5V in source mode. Low-ESR ceramic capacitors with X7R or X5R dielectrics are recommended for the output decoupling capacitor. This capacitor should be placed as close as possible to the CFLR and PGND pins.

The capacitor's voltage rating must exceed the normal V_{BATT} level. A capacitor with a minimum 35V voltage rating is recommended for the 5-cell battery configuration.

Current Sense

The MP2652 has current loops to limit the current and improve the current accuracy and loop stability. An external current-sense resistor is required to sense the average current. Figure 15 shows a recommended connection.

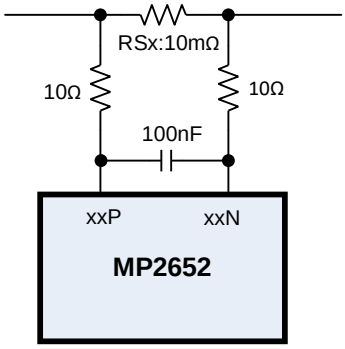

Figure 15: Input or Output Current-Sense Circuit

1. The I_{IN} loop limits the current drawn from the USB port or adapter, and I_{IN} is sensed through the IAP and IAN pins.
2. The battery current loop limits the charge current and discharge current. The battery current is sensed through the SRP and SRN pins.

Selecting the Resistive Divider for NTC Thermistor Temperature

In real-word applications, an external NTC thermistor is placed close to the battery to sense the battery's temperature. The MP2652 measures the battery temperature by monitoring the voltage ratio between the NTC and VNTC pins (see Figure 7 on page 25). Every temperature corresponds to a voltage ratio. The MP2652 has four temperature thresholds to satisfy JEITA requirements.

For a given NTC thermistor, the NTC hot and cold temperature points can be calculated with Equation (9) and Equation (10), respectively:

$$\frac{R_{T2} + R_{NTC_HOT}}{R_{T1} + R_{T2} + R_{NTC_HOT}} = \frac{V_{HOT}}{V_{VNTC}} \quad (9)$$

$$\frac{R_{T2} + R_{NTC_COLD}}{R_{T1} + R_{T2} + R_{NTC_COLD}} = \frac{V_{COLD}}{V_{VNTC}} \quad (10)$$

Where R_{NTC_HOT} is the thermistor value at the expected hot temperature protection point, and R_{NTC_COLD} is the thermistor value at the expected cold temperature protection point.

By default, V_{HOT} / V_{VNTC}, V_{WARM} / V_{VNTC}, V_{COOL} / V_{VNTC} and V_{COLD} / V_{VNTC} are 23.6%, 33.2%, 65.2% and 74.5%, respectively.

Consider a 103AT NTC thermistor on the battery pack, where the thermistor parameters are $R_{25°C}$ = 10kΩ, and β_factor = 3435K. If R_{T1} = 9.845kΩ and R_{T2} = 60Ω, the expected temperature thresholds (T_{HOT} = 60°C, T_{WARM} = 45°C, T_{COOL} = 10°C, and T_{COLD} = 0°C) can be determined.

For simplification, a 10kΩ R_{T1} can be used and R_{T2} can be replaced with a wire.

Design Example

Table 6 on page 51 shows a design example following the application guidelines for the specifications below.

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Table 6: Design Example

V_{IN}	5V to 20V
V_{BATT_REG}	21V
f_{SW}	425kHz
I_{CC}	2A
V_{IN_SRC}	5V to 20V

Figure 17 on page 52 and Figure 18 on page 53 show the detailed application schematics. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section starting on page 17. For more device applications, refer to the related evaluation board datasheet.

PCB Layout Guidelines

Efficient PCB layout is critical for specified noise, efficiency, and stability requirements. A 4-layer PCB is recommended. For the best results, refer to Figure 16 and follow the guidelines below:

1. Place the output capacitors as close to CFLR and PGND as possible. Place a small-sized (e.g. 0603), 1µF capacitor closer to the CFLR and PGND pins than the other 22µF capacitors.
2. Place the input capacitors as close to IN and PGND as possible. Place a small-sized (e.g. 0603), 1µF capacitor closer to the IN and PGND pins than the other 10µF capacitors.
3. Tie the ground connections for the input and output capacitors to the IC ground with a short copper trace connection or PGND plane.
4. Route the connection between CFLR/IN and its 1µF capacitor on the same layer with the IC. The connection to PGND must be on the same layer as the IC. Keep this routing loop as small as possible.
5. Connect AGND to PGND and to each decoupling capacitor via a single-point connection.
6. Place the VCC decoupling capacitor and the bootstrap capacitors next to the IC, and keep their trace connections as short as possible.
7. Use a Kelvin connection for the current-sense resistor.
8. Route the current-sense wires (IAP and IAN, SRP and SRN) away from switching nodes, such as SW1 and SW2.

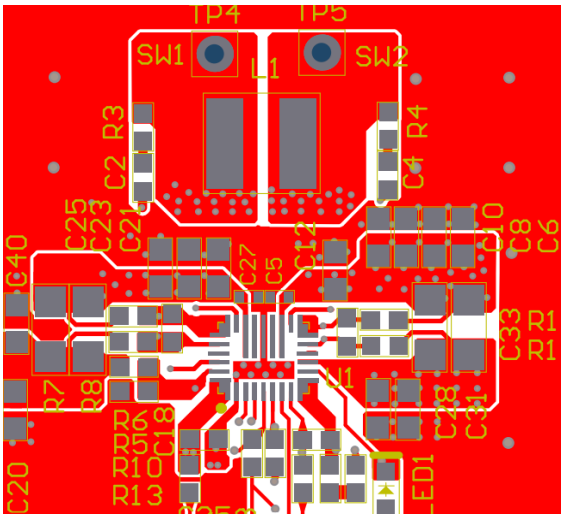

Figure 16: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS

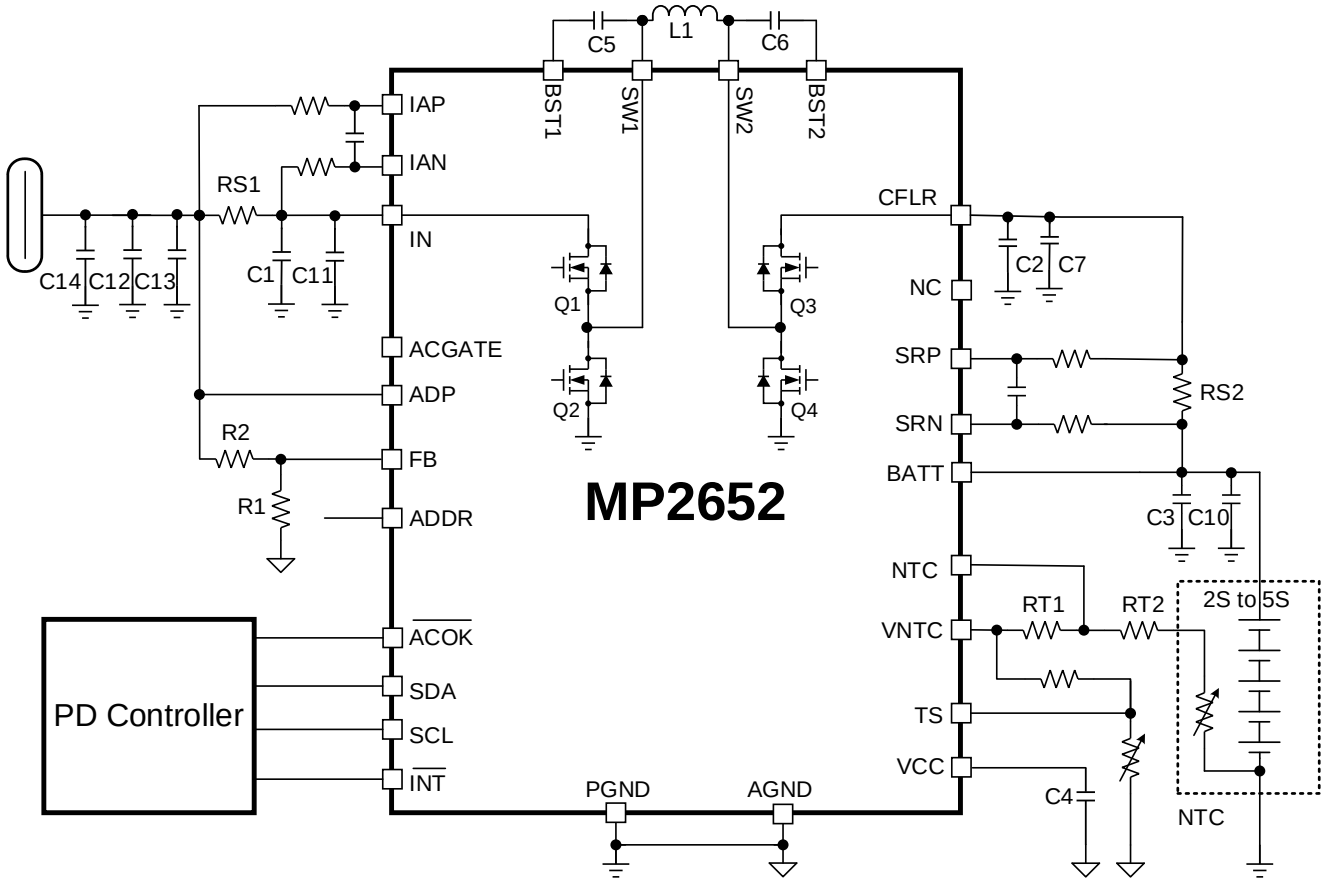

Figure 17: Typical Application Circuit

Table 7: Key BOM for Figure 17

Qty	Ref	Value	Description	Package	Manufacturer
5	C1, C11, C12, C13, C14	10µF	Ceramic capacitor, 35V, X5R	0805	Any
4	C2, C3, C7, C10	22µF	Ceramic capacitor, 35V, X5R	0805	Any
1	C4	4.7µF	Ceramic capacitor, 10V, X5R or X7R	0603	Any
2	C5, C6	100nF	Ceramic capacitor, 25V, X5R or X7R	0603	Any
1	L1	4.7µH	Inductor, 4.7µH, low DCR, I_{SAT} > 7.5A	SMD	Any
2	RS1, RS2	10mΩ	Film resistor, 1%	2512	Any

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TYPICAL APPLICATION CIRCUITS *(continued)*

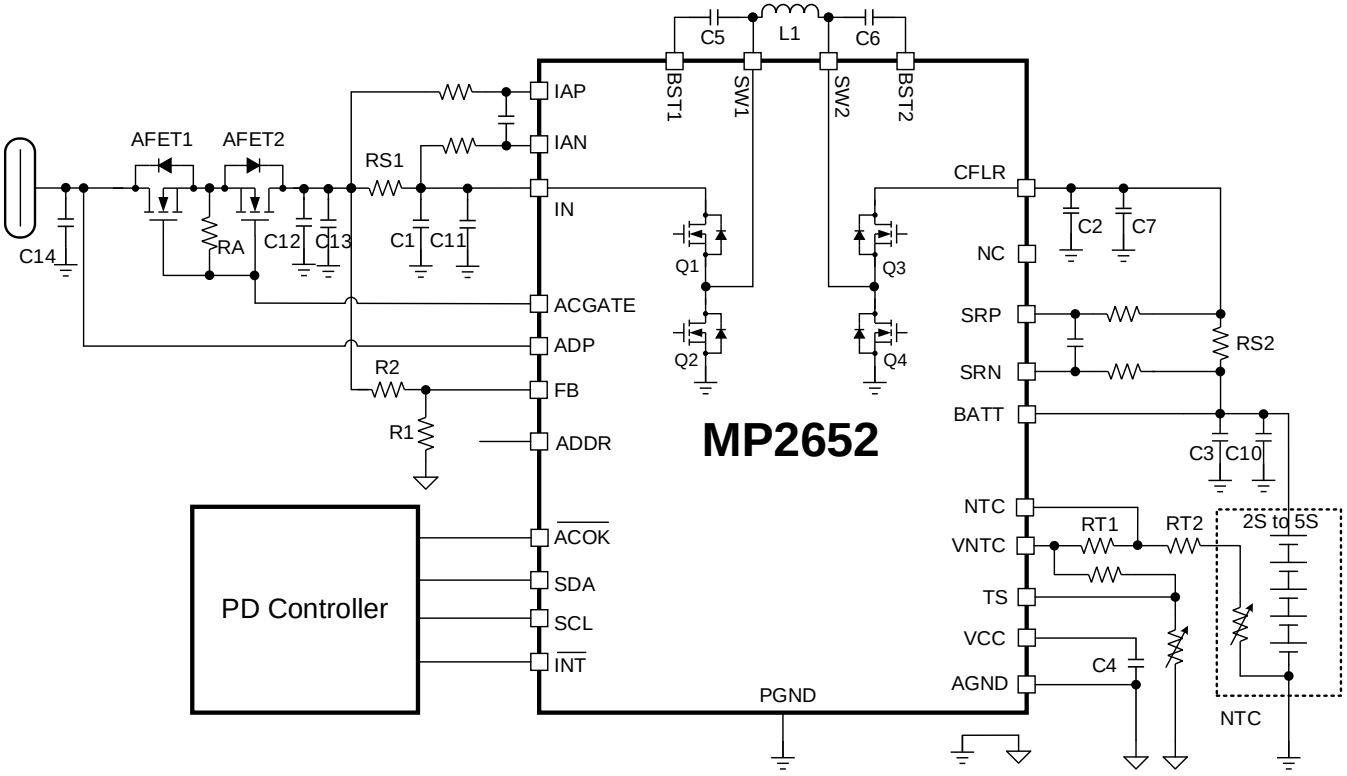

Figure 18: Typical Application Circuit

Table 8: Key BOM for Figure 18

Qty	Ref	Value	Description	Package	Manufacturer
5	C1, C11, C12, C13, C14	10µF	Ceramic capacitor, 35V, X5R	0805	Any
4	C2, C3, C7, C10	22µF	Ceramic capacitor, 35V, X5R	0805	Any
1	C4	4.7µF	Ceramic capacitor, 10V, X5R or X7R	0603	Any
2	C5, C6	100nF	Ceramic capacitor, 25V, X5R or X7R	0603	Any
1	L1	4.7µH	Inductor, 4.7µH, low DCR, I_{SAT} > 7.5A	SMD	Any
2	RS1, RS2	10mΩ	Film resistor, 1%	2512	Any
2	RA	5MΩ	Film resistor, 5%	0603	Any
2	AFET1, AFET2,	30V, 5.1mΩ, 20A	N-channel MOSFET (SISA14DN-T1-GE3)	Power PAK 1212-8	Vishay

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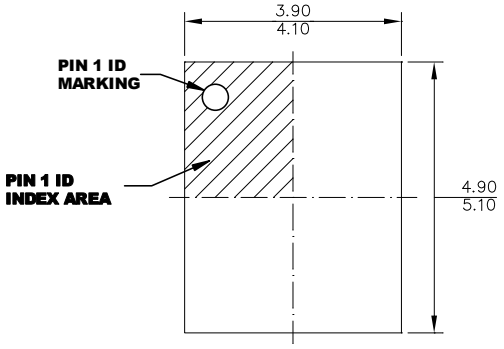
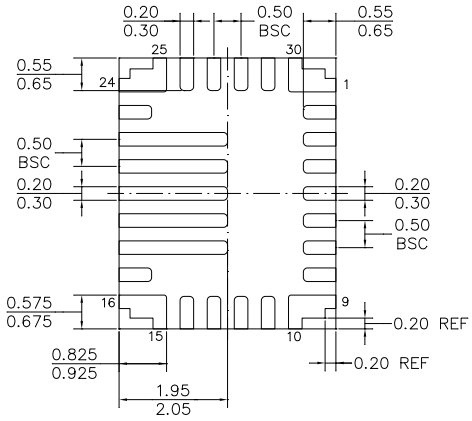
PACKAGE INFORMATION

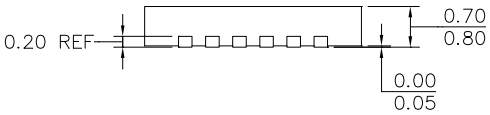
TQFN-30 (4mmx5mm)



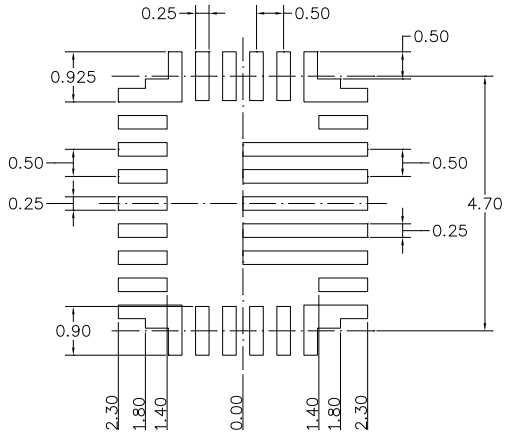
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

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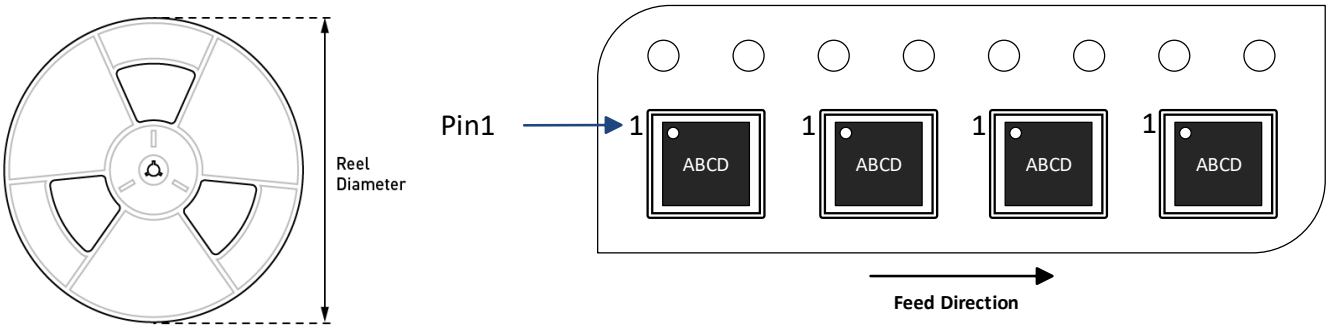

Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2652GVT-xxxx-Z	TQFN-30 (4mmx5mm)	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	2/13/2026	Initial Release	-

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