MP2623

Stand-Alone, 2A, 1- or2-Cell Switching LiFePO$_4$ Battery Charger

The Future of Analog IC Technology

DESCRIPTION

The MP2623 is a monolithic, DC-DC, step-down, switching charger for a 1-or-2-cell serial LiFePO$_4$ battery. It has an integrated high-side power MOSFET that can output up to a 2A charge current. It also has peak-current–mode control for fast loop response and easy compensation.

The MP2623 uses a sense resistor to control a programmable charge current, and accurately regulates the charge current and the charge voltage using two control loops.

The MP2623 has multiple fault-condition protections that include cycle-by-cycle current limiting and thermal shutdown. Other safety features include battery temperature monitoring and protection, charge status indication and a programmable timer to halt charging after a set time period.

The MP2623 requires a minimal number of readily-available external components.

The MP2623 is available in a 4mm×4mm 16-pin QFN package.

FEATURES

- Charges 1- and 2-Cell LiFePO$_4$ Battery Packs
- Wide Operating-Input Range
- Programmable Charging Current of up to 2A
- ±0.75% V_{BATT} Accuracy
- 0.2Ω Integrated Power MOSFET
- Up to 90% Efficiency
- Fixed 1.1MHz Frequency
- Preconditioning for Fully-Depleted Batteries
- Charging Status Indicator
- Input Supply Fault Indicator
- Thermal Shutdown
- Cycle-by-Cycle Over-Current Protection
- Battery Temperature Monitor and Protection

APPLICATIONS

- Power Tools and Portable Equipment
- Handheld Terminals
- LiFePO$_4$ Battery Chargers

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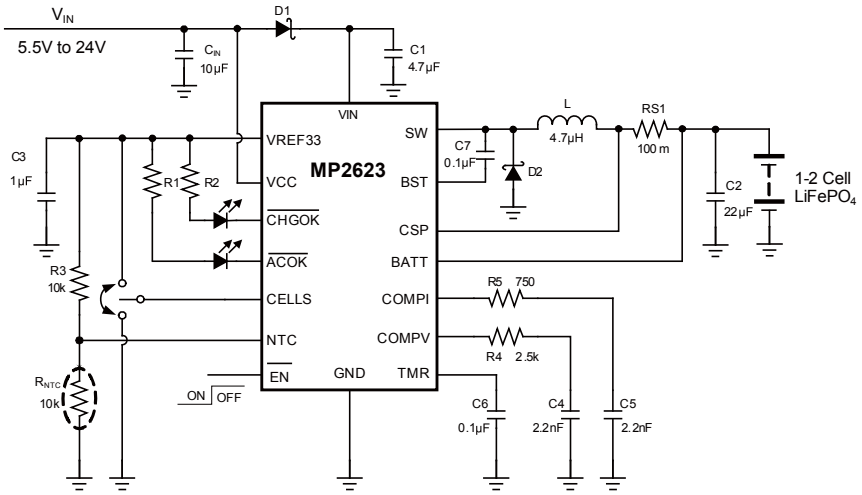
TYPICAL APPLICATION



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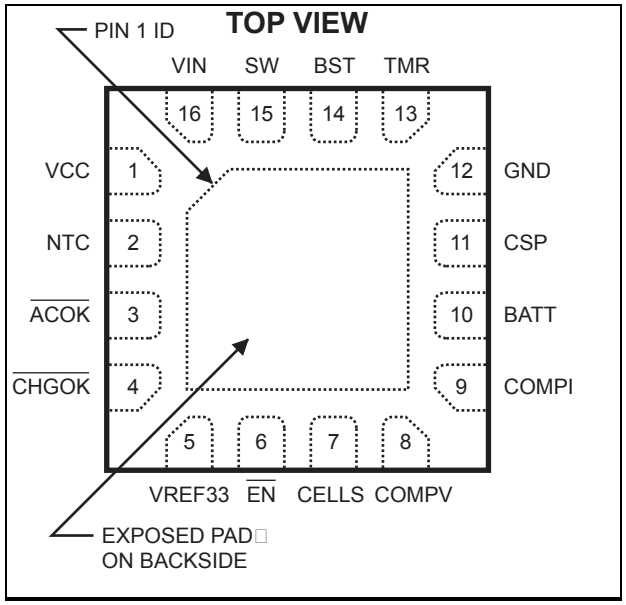
ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2623GR	QFN16 (4×4mm)	MP2623

*For Tape & Reel, add suffix –Z (e.g. MP2623GR–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage VCC, VIN 26V
V_{SW} ..... -0.3V to (V_{IN} + 0.3V)
V_{BST} ..... V_{SW} + 6V
V_{CSP}, V_{BATT}, ...-0.3V to +18V
$V_{\overline{ACOK}}$, $V_{\overline{CHGOK}}$, ...-0.3V to +26V
All Other Pins .....-0.3V to +6V
Continuous Power Dissipation (T_A = 25°C) (2)
..... 2.7W
Junction Temperature .....150°C
Lead Temperature .....260°C
Storage Temperature..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} .....5V to 24V
Operating Junction Temp. (T_J) -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN16 (4x4mm) ..... 46 ..... 10... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(MAX)=(T_J(MAX)-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7 4-layer board.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 19V, T_A = 25°C, CELLS=0V, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Battery-terminal voltage	V_{BATT}	CELLS=0V	3.573	3.6	3.627	V
		CELLS=Float	7.146	7.2	7.254	
CSP，BATT current	I_{CSP},I_{BATT}	Charging disabled		1		μA
Switch-on resistance	$R_{DS(ON)}$			0.2		Ω
Switch leakage		$\overline{EN}$= 4V, V_{SW} = 0V		0	1	μA
Peak-current limit	CC(5)			4.1		A
	TRICKLE			2		A
CC current	I_{CC}	RS1=100mΩ	1.8	2.0	2.2	A
Trickle-charge current	$I_{TRICKLE}$			10%		I_{CC}
Trickle-charge voltage threshold	V_{TC}			2.52		V/cell
Trickle-charge hysteresis				300		mV/cell
Termination current threshold	I_{BF}		5%	10%	15%	I_{CC}
Oscillator frequency	f_{SW}	CELLS=0V, V_{BATT} =3.2V		1100		kHz
Fold-back frequency		V_{BATT} =0V		350		kHz
Maximum duty cycle			90			%
Maximum current-sense voltage (CSP to BATT)	V_{SENSE}		170	200	230	mV
Minimum ON time (5)	t_{ON}			100		ns
Under-voltage lockout threshold, rising	V_{IN}		3.1	3.3	3.5	V
Under-voltage lockout threshold, hysteresis				300	1000	mV
Open-drain sink current		V_{DRAIN} =0.3V	5			mA
Dead battery indicator		In trickle mode C_{TMR}=0.1μF		30		min
Recharge threshold for V_{BATT}	V_{RECHG}			3.42		V/cell
Recharge hysteresis				100		mV
NTC low-temp rising threshold		R_{NTC}=NCP18X103, 0°C	70.5	73.5	76.5	%of VREF33
NTC high-temp falling threshold		R_{NTC}=NCP18X103, 50°C	27.5	29.5	31.5	%of VREF33
VIN min. head-room (reverse blocking)		V_{IN}−V_{BATT}		180		mV

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 19V, T_A = 25°C, CELLS=0V, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
$\overline{EN}$ input low voltage					0.4	V
$\overline{EN}$ input high voltage			1.8			V
$\overline{EN}$ input current		$\overline{EN}$=4V		4		µA
		$\overline{EN}$=0V		0.2		
Supply current (shutdown)		$\overline{EN}$=4V		0.5		mA
		$\overline{EN}$=4V, Consider VREF33 pin output current, R_3=10k,R_{NTC}=10k		0.665		mA
Supply current (quiescent)		$\overline{EN}$=0V, CELLS=0V			2.0	mA
Thermal shutdown (5)				150		°C
VREF33 output voltage				3.3		V
VREF33 load regulation		I_{LOAD} =0 to 10mA		30		mV

Notes:

5) Guaranteed by design.

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PIN FUNCTIONS

Pin #	Name	Description
1	VCC	IC Supply Voltage.
2	NTC	Thermistor Input. Connect a resistor from this pin to VREF33, and the thermistor from this pin to ground.
3	$\overline{\text{ACOK}}$	Valid Input Supply Indicator. Open drain output. Add a pull-up resistor. Logic LOW indicates the presence of a valid input supply.
4	$\overline{\text{CHGOK}}$	Charging Status Indicator. Open drain output. Add a pull-up resistor. Logic LOW indicates normal charging. Logic HIGH indicates either a completed charge process or a fault-suspended process.
5	VREF33	Internal Linear Regulator, 3.3V Reference Output. Bypass to GND with a 1μF ceramic capacitor.
6	$\overline{\text{EN}}$	On/Off Control Input.
7	CELLS	Command Input. Indicates the number of LiFePO$_4$ battery cells. Connect to VREF33 or float for 2-cell operation. Ground for 1-cell operation.
8	COMPV	V-LOOP Compensation. Decouple this pin with a capacitor and a resistor.
9	COMPI	I-LOOP Compensation. Decouple this pin with a capacitor and a resistor.
10	BATT	Positive Battery Terminal.
11	CSP	Battery-Charge Current-Sense–Positive Input. Connect a resistor RS1 between CSP and BATT. The full charge current is: $I_{CHG}(A)=\frac{200mV}{RS1(m\Omega)}$.
12	GND	Ground. Voltage reference for the regulated output voltage. Place this node outside of the path of the switching diode (D2) to the input ground to prevent switching current spikes from inducing voltage noise.
13	TMR	Set-Safe–Time Period. A 0.1μA current charges and discharges the external capacitor decoupled to GND. The capacitor value programs the time period.
14	BST	Bootstrap. Requires a charged capacitor to drive the power switch's gate above the supply voltage. Connect a capacitor between SW and BST pins to form a floating supply across the power switch driver.
15	SW	Switch Output.
16	VIN	Regulator Input Voltage. The MP2623 regulates a 5V-to-24V input to a voltage suitable for charging either a 1- or 2-cell LiFePO$_4$ battery. Requires capacitors to prevent large voltage spikes from appearing at the input.

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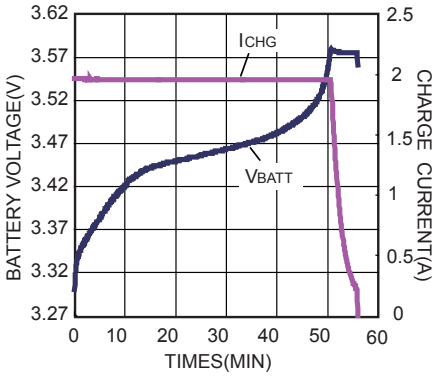
TYPICAL PERFORMANCE CHARACTERISTICS

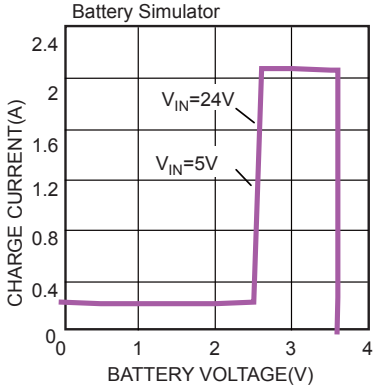
V_{IN}=5V/ 9V, C1=4.7µF, C2=22µF, L=4.7µH, RS1=100mΩ, Real/Simulation Battery Load, T_A=25°C, unless otherwise noted.

1 Cell Battery Charge Curve

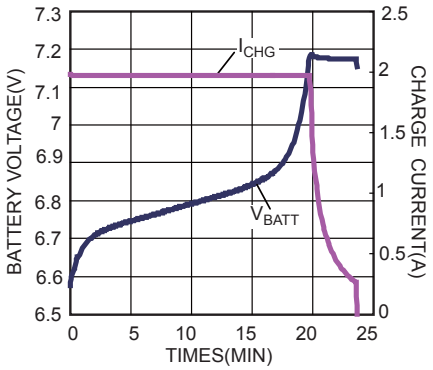


1 Cell Charge Current vs. Battery Voltage

Battery Simulator

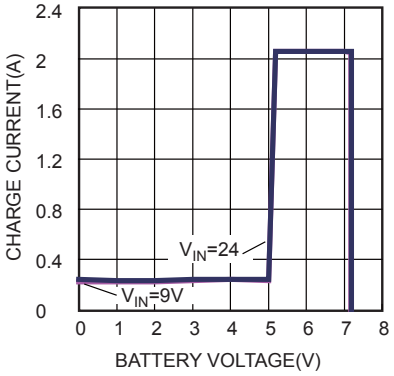


2 Cells Battery Charge Curve

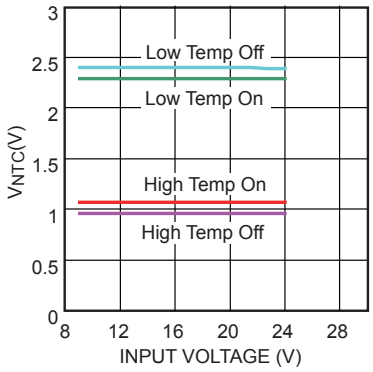


2 Cells Charge Current vs. Battery Voltage

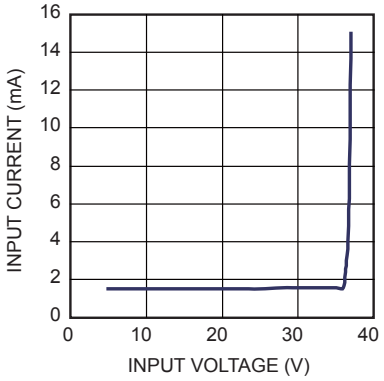
Battery Simulator



NTC Control Window

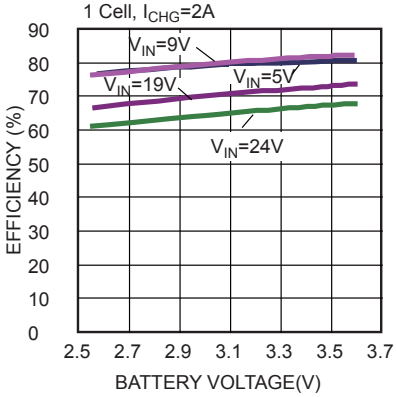


Breakdown Voltage



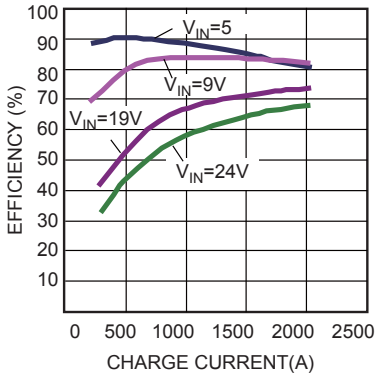
Efficiency vs. Battery Voltage

1 Cell, I_{CHG}=2A



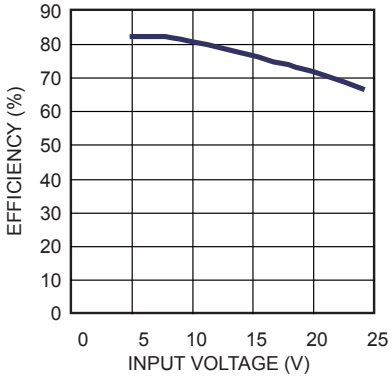
Efficiency vs. I_{CHG}

1 Cell, V_{BATT}=3.6V



Efficiency vs. V_{IN}

1 Cell, V_{BATT}=3.4V, I_{CHG}=2A



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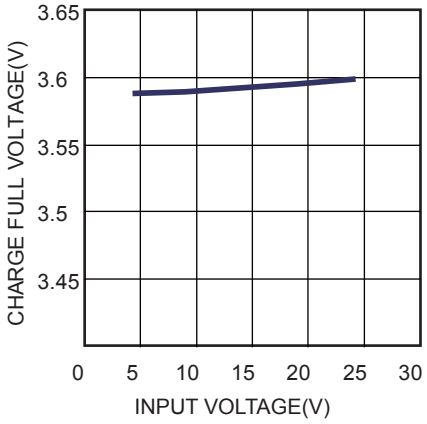
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=5V/ 9V, C1=4.7µF, C2=22µF, L=4.7µH, RS1=100mΩ, Real/Simulation Battery Load, T_A=25°C, unless otherwise noted.

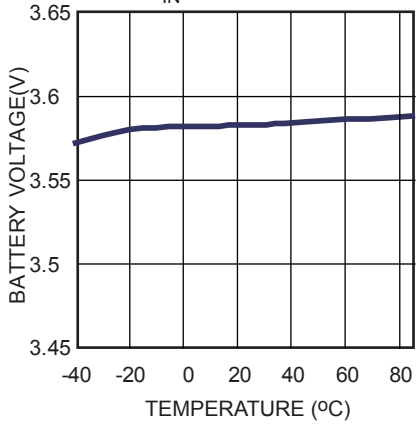
BATT Float Voltage vs. V_{IN}

1 Cell



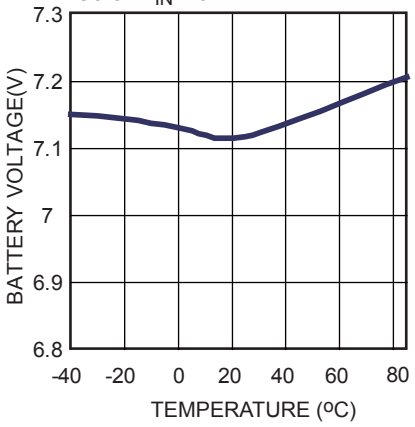
BATT Charge Full Voltage vs. Temperature

1 Cell V_{IN}=19V

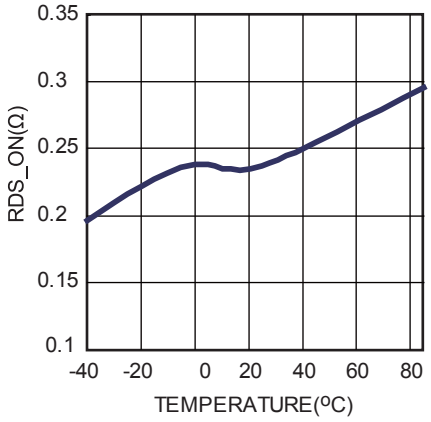


BATT Charge Full Voltage vs. Temperature

2 Cells V_{IN}=19V

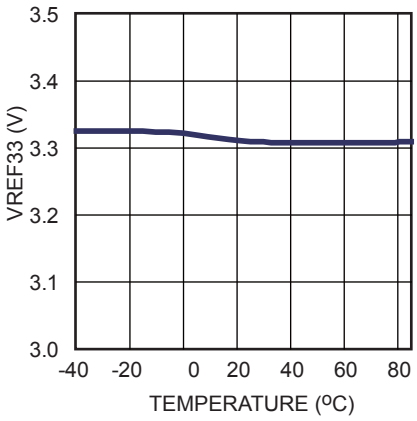


RDS_ON vs. Temperature



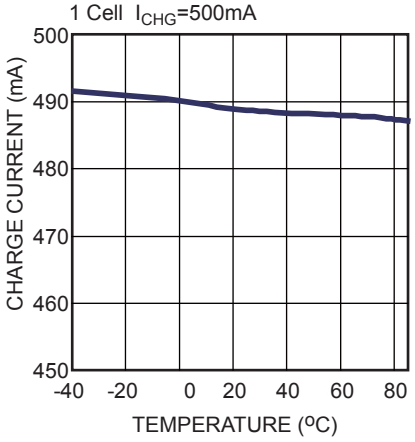
VREF33 vs. Temperature

V_{IN}=19V



Constant Current Charge vs. Temperature

1 Cell I_{CHG}=500mA



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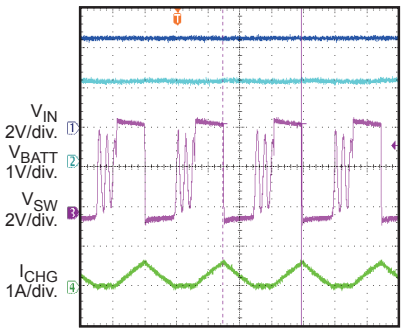
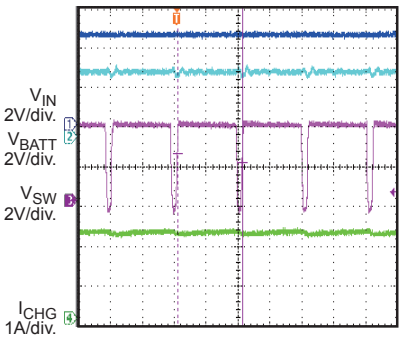
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=5V/ 9V, C1=4.7µF, C2=22µF, L=4.7µH, RS1=100mΩ, Real/Simulation Battery Load, T_A=25°C, unless otherwise noted.

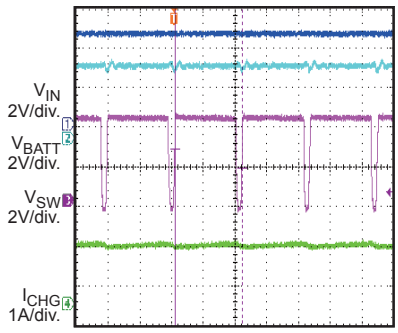
Steady State Waveform
1 Cell, V_{BATT}=2V



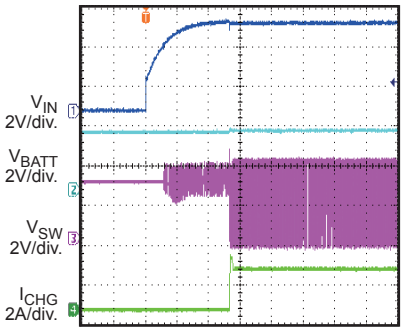
Steady State Waveform
1 Cell, V_{BATT}=3.2V



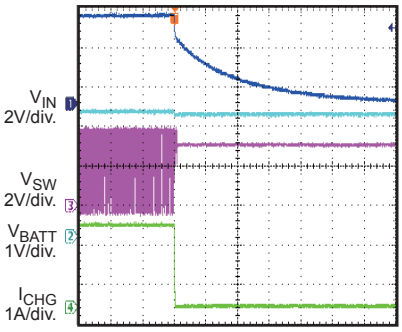
Steady State Waveform
1 Cell, V_{BATT}=3.6V



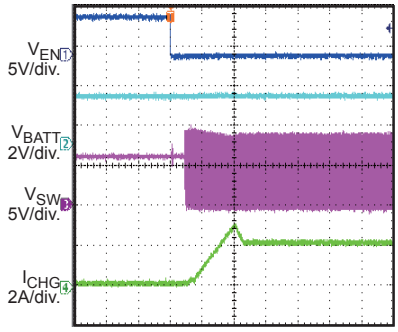
Power On Waveform
1 Cell, I_{CHG}=2A,V_{BATT}=3V



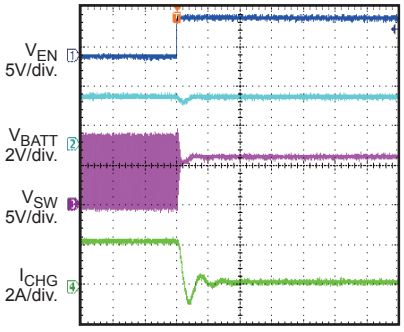
Power Off Waveform
1 Cell, I_{CHG}=2A,V_{BATT}=3V



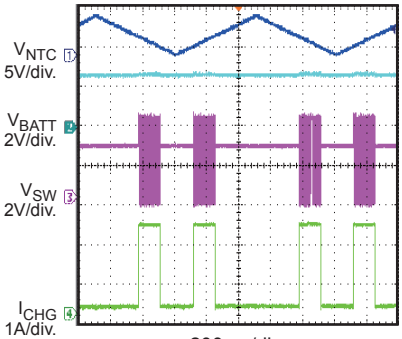
EN On Waveform
1 Cell, I_{CHG}=2A,V_{BATT}=3V



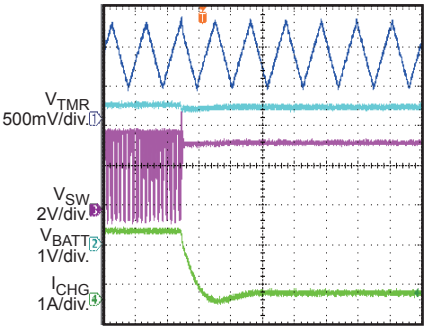
EN Off Waveform
1 Cell, I_{CHG}=2A,V_{BATT}=3V



NTC Control,
1 Cell, I_{CHG}=2A, V_{BATT}=2.5V, Battery Simulator



Timer Out
1 Cell,I_{CHG}=2A, V_{BATT}=3.5V, C_{TIMER}=47pF, Battery Simulator



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FUNCTIONAL BLOCK DIAGRAM

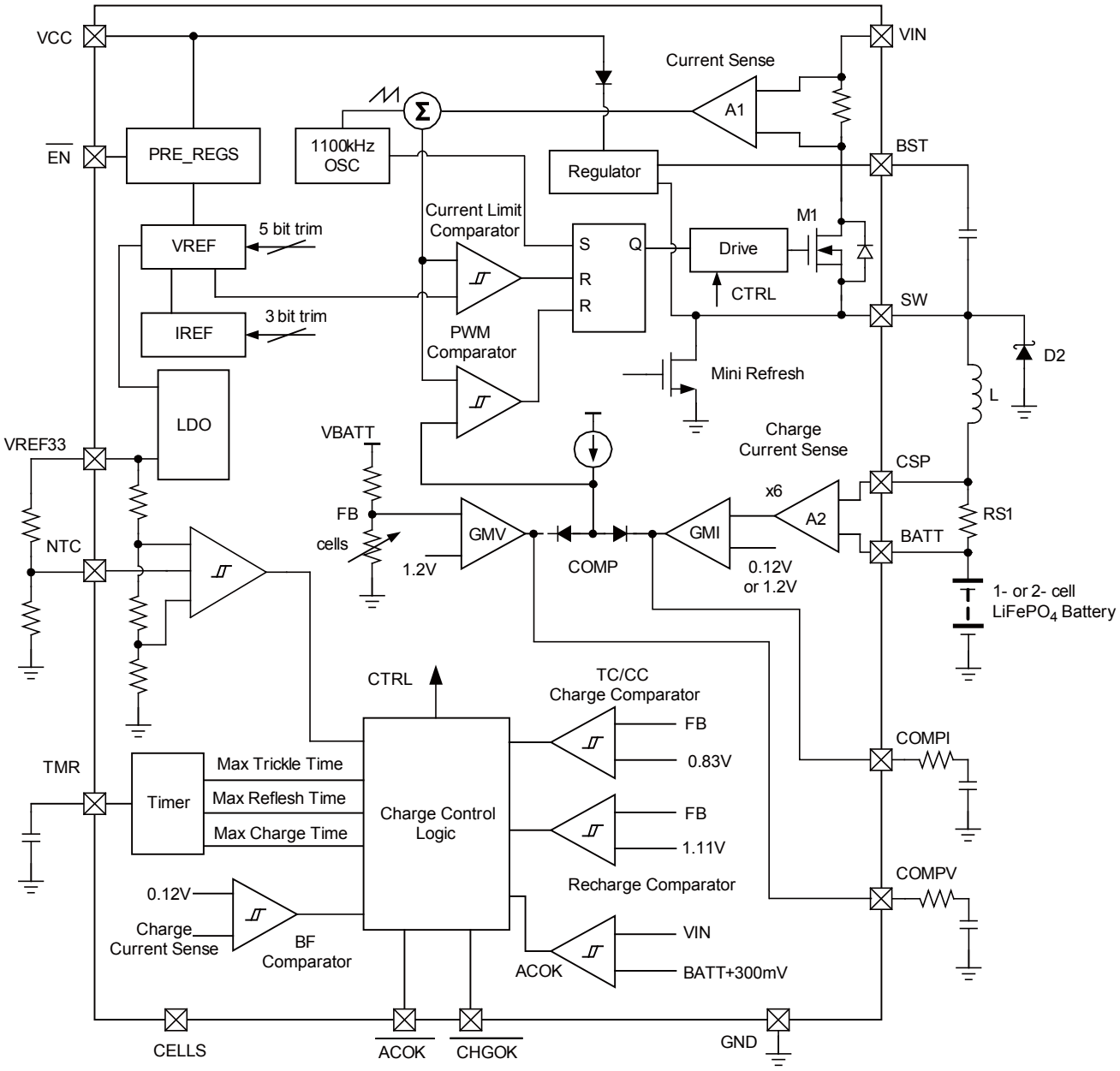

Figure 1: Functional Block Diagram

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OPERATION

The MP2623 is a peak-current–mode controlled switching charger for use with LiFePO$_4$ batteries.

At the beginning of each cycle, M1 is off and the COMP voltage exceeds the output of the current-sense amplifier (A1). The PWM comparator's output is low, and the rising edge of the 1.1MHz CLK signal sets the RS flip-flop that turns on M1; this connects the SW pin and the inductor to the input supply.

A1 senses and amplifies the inductor current: The PWM comparator then compares the sum of this signal and the ramp compensator signal against the COMP signal. When the sum of the A1 output and the ramp compensator exceeds the COMP voltage, the RS flip-flop resets and turns M1 off. The external switching diode (D2) then conducts the inductor current. If the sum of the A1 output and the ramp compensator does not exceed the COMP voltage, then the falling edge of the CLK resets the flip-flop.

The MP2623 uses COMP to select the smaller value of GMI and GMV to implement either current-loop control or voltage-loop control. Current-loop control triggers when the battery voltage goes low, which results in the GMV output saturating. The GMI compares the charge current (as a voltage sensed through RS1) against the reference voltage to regulate the charge current to a constant value. When the battery voltage charges up to the reference voltage, the output of GMV goes low and initiates voltage loop control to control the duty cycle to regulate the output voltage.

The MP2623 has an internal linear regulator—VREF33—to power internal circuitry. It can also power external circuitry as long as the load does not exceed the maximum current (30mA). Connect a 1µF bypass capacitor from VREF33 to GND to ensure stability.

Charge Cycle (Mode change: Trickle→ CC→ CV)

At the start of a charging cycle, the MP2623 monitors V_{BATT}. If V_{BATT} is lower than the trickle-charge threshold, V_{TC} (typically 2.52V/cell), the charging cycle will start in trickle-charge mode (10% of the RS1-programmed constant-charge current, I_{CC}) until the battery voltage reaches V_{TC}.

If the charge stays in the trickle-charge mode until the time-out condition triggers, charging terminates and will not resume until either the input power or the EN signal refreshes. Otherwise, GMI regulates the charge current to the level set by RS1. The charger operates in constant-current–charging mode. The COMPI voltage—regulated by GMI—determines the switching duty cycle.

When the battery voltage triggers constant-voltage mode, GMV regulates the COMP pin and the duty cycle. When the charge current drops to the battery-full threshold, I_{BF} (typically 10% I_{CC}), the battery is defined as fully-charged, the charger stops charging, and CHGOK goes high to indicate the charge-full condition. If the total charge time exceeds the timer period, charging terminates at once and will resume when either the input power or EN signal can restart the charger.

Figure 2 shows the typical charge profile of the MP2623.

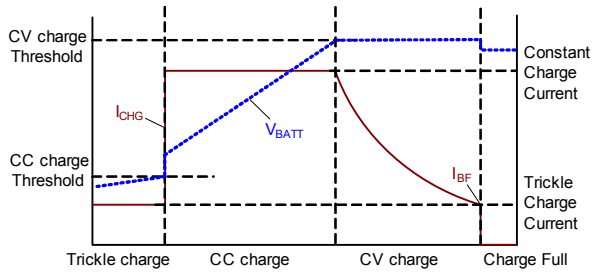

Figure 2: Li-Ion Battery Charging Profile

Automatic Recharge

After the battery completely recharges, the charger removes all the blocks besides the battery voltage monitor to reduce the leakage current from the input or the battery. If the battery voltage drops below 3.42V/Cell, the circuit will automatically recharge the battery using soft-start. The timer will then restart to avoid triggering a false fault.

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Charger Status Indication

MP2623 has two open-drain status outputs: $\overline{ACOK}$ and $\overline{CHGOK}$. The $\overline{ACOK}$ pin goes low when the IC supply voltage (VCC) exceeds the under-voltage lockout threshold and the regulated voltage VIN is 300mV higher than V_{BATT} to make sure the regulator can operate normally. $\overline{CHGOK}$ indicates charge status. Table 1 describes $\overline{ACOK}$ and $\overline{CHGOK}$ outputs under different charge conditions.

Table 1—Charging Status Indication

$\overline{ACOK}$	$\overline{CHGOK}$	Charger Status
low	low	In charging
low	high	End of charge, NTC fault, timer out, thermal shutdown, $\overline{EN}$ disable
high	high	V_{IN}–V_{BATT}<0.3V. V_{CC}<UVLO,

Timer Operation

MP2623 uses an internal timer to limit the charge period during both the trickle charge and the total charge cycle. The MP2623 terminates charging once the charge time exceeds the time limit. A good battery should fully recharge within the allotted time period; otherwise the battery has a fault. An external capacitor at the TMR pin programs the time period.

The trickle mode charge time is:

$$t_{TRICKLE_TMR} = 30\,mins \times \frac{C_{TMR}}{0.1\mu F}$$

The total charge time is:

$$t_{TOTAL_TMR} = 3hours \times \frac{C_{TMR}}{0.1\mu F}$$

When time-out occurs, the charger is suspended. Only refreshing the input power or EN signal can restart the charge cycle.

Negative Thermal Coefficient (NTC) Thermistor

The MP2623 has a built-in NTC-resistance window comparator that allows the MP2623 to sense the battery temperature through the thermistor included in the battery pack. Connect a resistor with an appropriate value from VREF33 to the NTC pin, and connect the thermistor from the NTC pin to GND. A resistor divider determines the voltage on the NTC pin as a function of the battery temperature. Charging halts when the NTC voltage falls below the lower NTC window threshold. Charging resumes when the voltage is within the NTC window range.

Application with Power Selector

MP2623 is a stand-alone, switching charger. Typically, VIN receives power from the adapter input, V_{IN}, through a diode that blocks the battery voltage to VCC. For power selector application, however, V_{IN} powers the system and charges the battery simultaneously so the user can start-up a device with a drained battery when it is connected to an adapter. Replace the diode from the stand-alone switching charger circuit with a MOSFET to improve system efficiency and reduce voltage drop of the block device.

An additional MOSFET between VIN and the battery allows the battery to charge even in the absence of an adapter or connection to an invalid adapter. Figure 3 shows a typical application circuit with power-path management. When the adapter input is invalid or absent, the block diode is replaced by a MOSFET controlled by $\overline{ACOK}$ signal.

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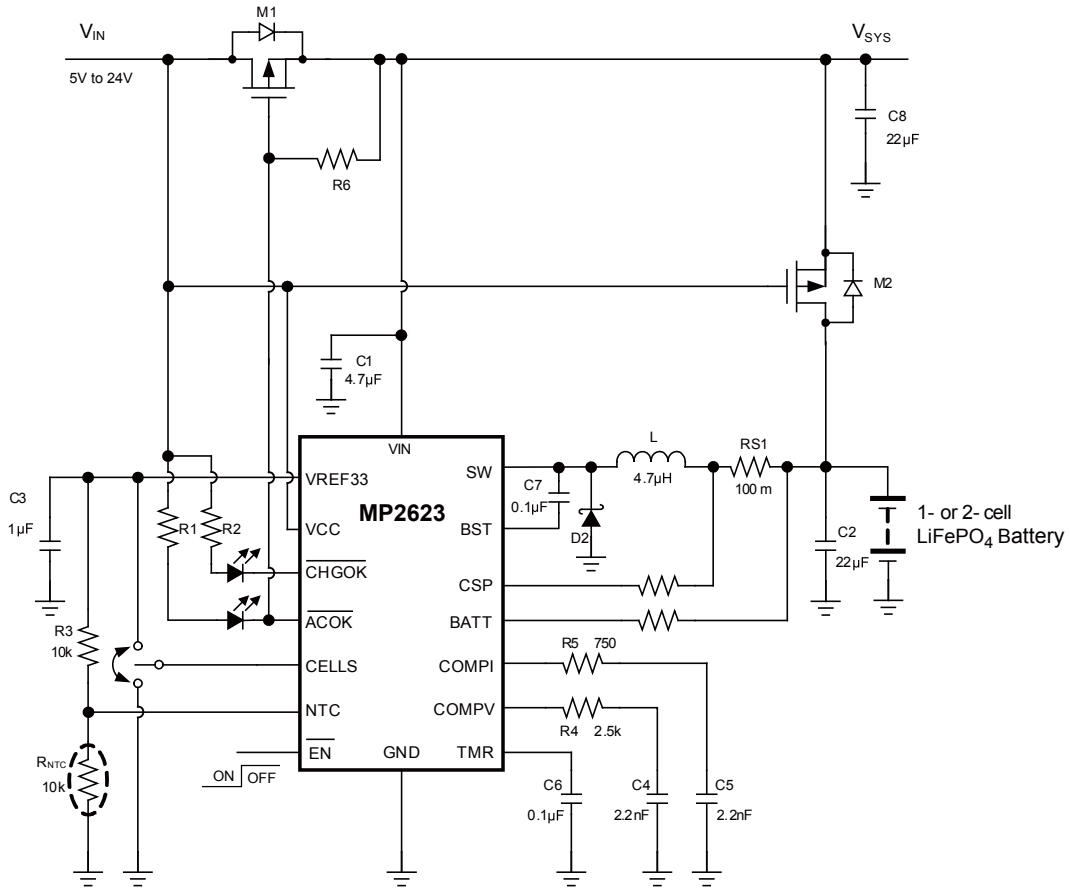

Figure 3: MP2623 with Power Selector

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OPERATION FLOW CHART

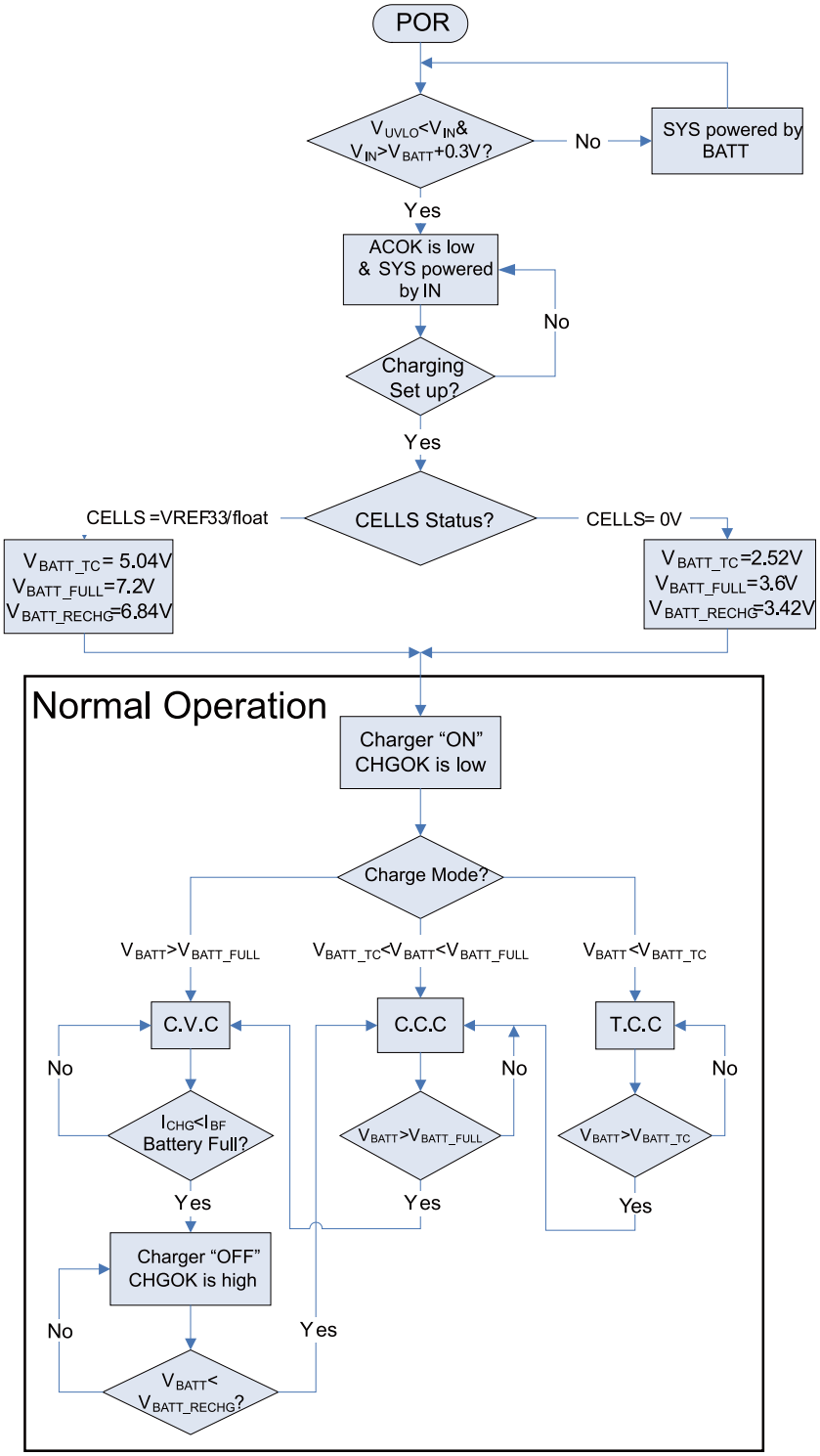

Figure 4: Normal Charging Operation Flow Chart

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OPERATION FLOW CHART *(continued)*

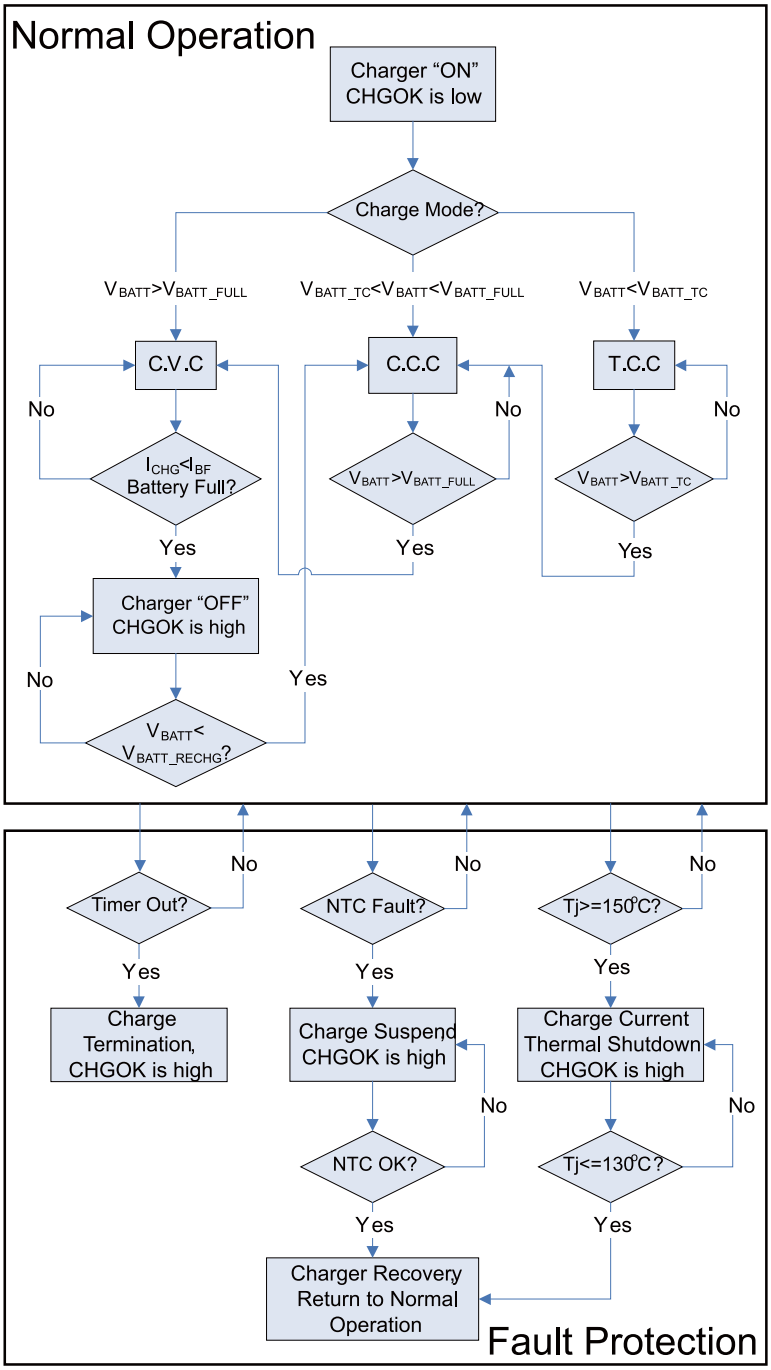

Figure 5: Fault-Protection Flow Chart

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APPLICATION INFORMATION

Setting the Charge Current

RS1 sets the MP2623 charge current (See Typical Application). Determine the current with the following equation:

$$I_{CHG}(A) = \frac{200mV}{RS1(m\Omega)} \quad (1)$$

Selecting the Inductor

Use a 1μH-to-10μH inductor for most applications. Calculate the inductance value from the following equation.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (2)$$

Where ΔI_L is the inductor ripple current. Choose ΔI_L to be approximately 30% of the maximum charge current, 2A. V_{OUT} is the 1- or 2-cell battery voltage.

The maximum inductor peak current is:

$$I_{L(MAX)} = I_{CHG} + \frac{\Delta I_L}{2} \quad (3)$$

Under light-load conditions (below 100mA), use a larger inductor value to improve efficiency.

Select an inductor with a DC resistance of less than 200mΩ to optimize efficiency.

NTC Function

Figure 6 shows that the low temperature threshold and high-temperature threshold are preset internally to 73.5%·VREF33 and 29.5%·VREF33, respectively, using a resistor divider. For a given NTC thermistor, we can select appropriate R3 and R6 resistors to set the NTC window.

For the thermistor (NCP18XH103) noted in the electrical characteristic previous,

At 0°C, R_{NTC_Cold} = 27.445k;

At 50°C, R_{NTC_Hot} = 4.1601k.

Assuming that the NTC window is between 0°C and 50°C, we can derive the following equations:

$$\frac{R6 // R_{NTC_Cold}}{R3 + R6 // R_{NTC_Cold}} = \frac{V_{TH_Low}}{VREF33} = 73.5\% \quad (4)$$

$$\frac{R6 // R_{NTC_Hot}}{R3 + R6 // R_{NTC_Hot}} = \frac{V_{TH_High}}{VREF33} = 29.5\% \quad (5)$$

According to equation (4) and equation (5), R3 = 9.63k and R6 = 505k.

Simplifying, select R3=10k and R6 no connect to approximate the estimate.

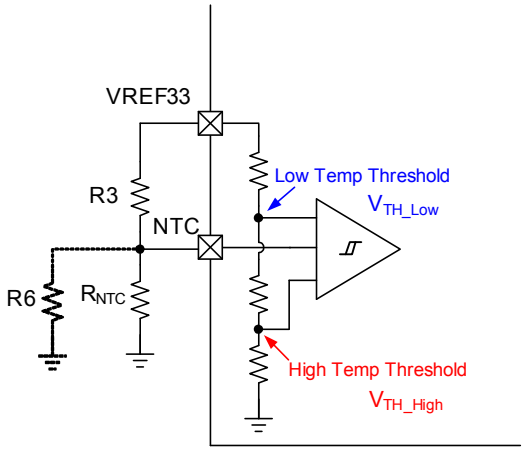

Figure 6: NTC function block

Selecting the Input Capacitor

The input capacitor reduces the surge current drawn from the input and the switching noise from the device. Chose an input capacitor with an impedance at the switching frequency less than the input source impedance to prevent a high-frequency switching current. Use ceramic capacitors with X5R or X7R dielectrics with low ESR and small temperature coefficients. A 4.7μF capacitor is sufficient for most applications.

Selecting the Output Capacitor

The output capacitor limits output voltage ripple and ensures regulator-loop stability. The output capacitor impedance should be low at the switching frequency. Use ceramic capacitors with X5R or X7R dielectrics.

PC Board Layout

Connect the high frequency and high current paths (GND, IN, and SW) to the device with short, wide, and direct traces. Place the input capacitor as close as possible to the IN and GND pins. Place the external feedback resistors next to the FB pin. Keep the switching node SW short and away from the feedback network.

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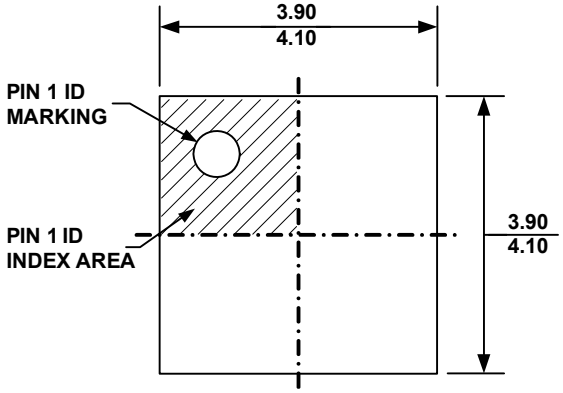
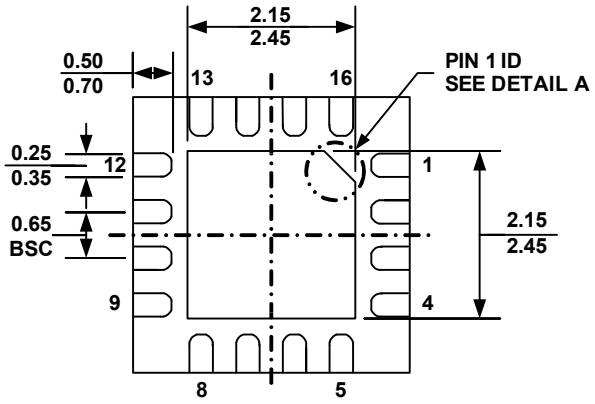
PACKAGE INFORMATION

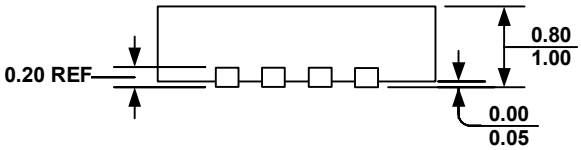
QFN16 (4 x 4mm)



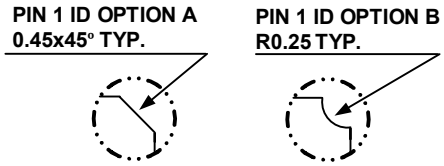
TOP VIEW



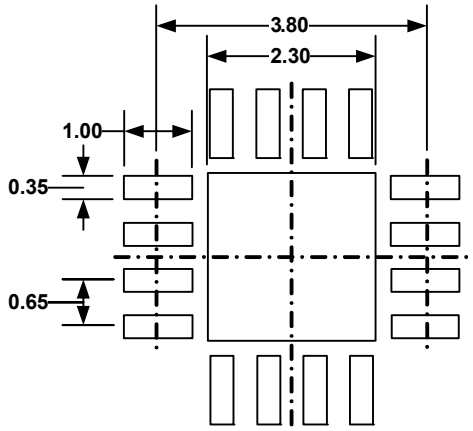
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) JEDEC REFERENCE IS MO-220, VARIATION VGGC.
5) DRAWING IS NOT TO SCALE

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