MP2618

2A, 24V Input, 600kHz 2-3 Cell Switching Li-Ion Battery Charger With System Power Path Management

The Future of Analog IC Technology

DESCRIPTION

The MP2618 is a monolithic switching charger for 2-3 cell Li-Ion battery packs with a built-in internal power MOSFET. It achieves up to 2A charge current with current mode control for fast loop response and easy compensation. The charge current can be programmed by sensing the current through an accurate sense resistor.

MP2618 regulates the charge voltage and charge current using two control loops to realize high accuracy CC charge and CV charge.

The system power path management function ensures continuous supply to the system by automatically selecting the input or the battery. Power path management separates charging current from system load. When the MP2618 realizes current sharing of the input current, charge current will drop down according to the increase of the system current.

Fault condition protection includes cycle-by-cycle current limiting, and thermal shutdown. Other safety features include battery temperature monitoring, charge status indication and programmable timer to cease the charging cycle.

The MP2618 is available in a 28-pin, 4mmx5mm QFN package.

FEATURES

- Charges 2-3 cell Li-Ion battery packs
- Wide Operating Input Range
- Up to 2A Programmable Charging Current
- Power Path Management with Current Sharing
- ±0.75% V_{BATT} Accuracy
- 0.28Ω Internal Power MOSFET Switch
- Up to 90% Efficiency
- Fixed 600kHz Frequency
- Preconditioning for fully depleted batteries
- Charging Operation Indicator
- Input Supply and battery fault indicator
- Thermal Shutdown
- Cycle-by-Cycle Over Current Protection
- Battery Temperature Monitor and Protection

APPLICATIONS

- Netbook PC
- Distributed Power Systems
- Chargers for 2-Cell or 3-Cell Li-Ion Batteries
- Pre-Regulator for Linear Regulators

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TYPICAL APPLICATION

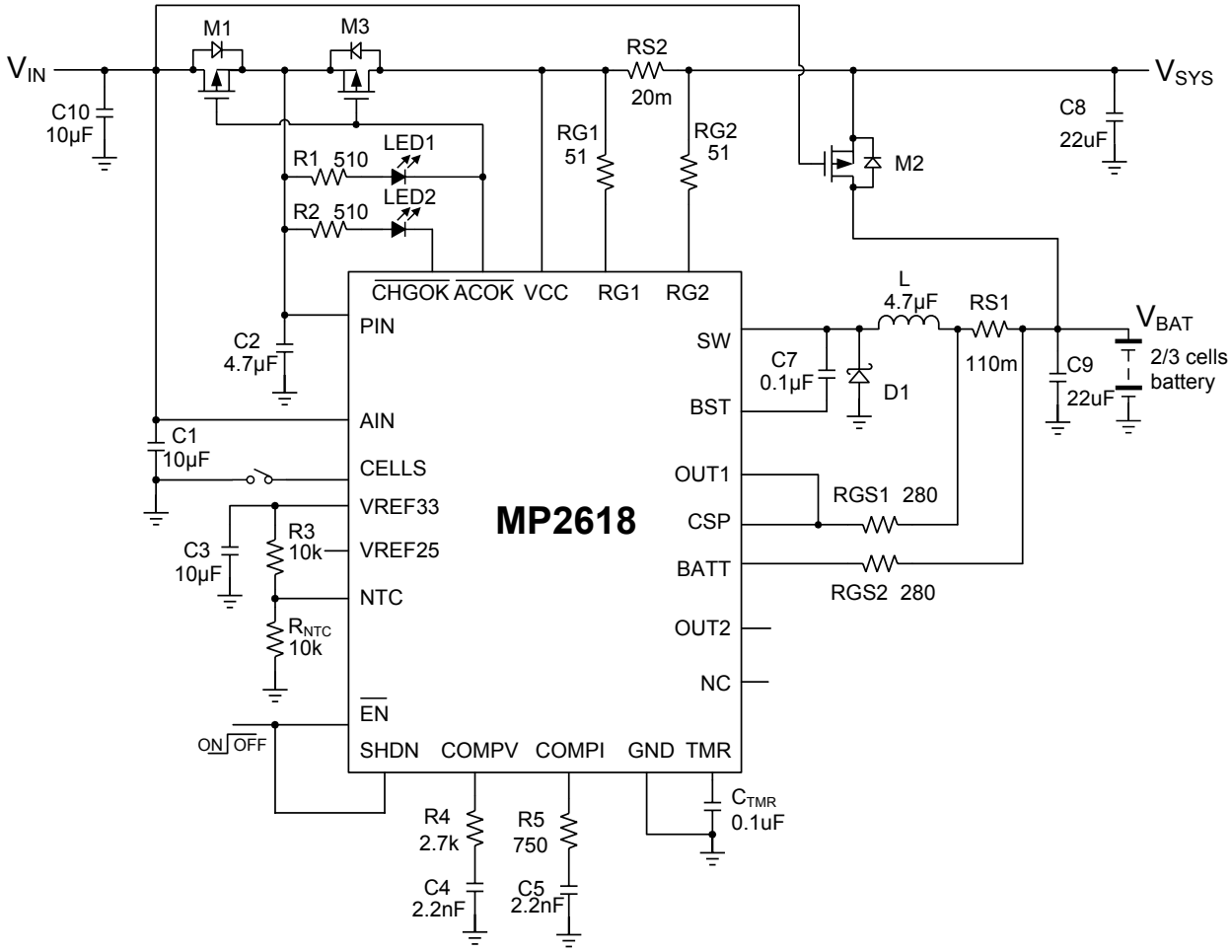

Figure 1—Typical Application Circuit

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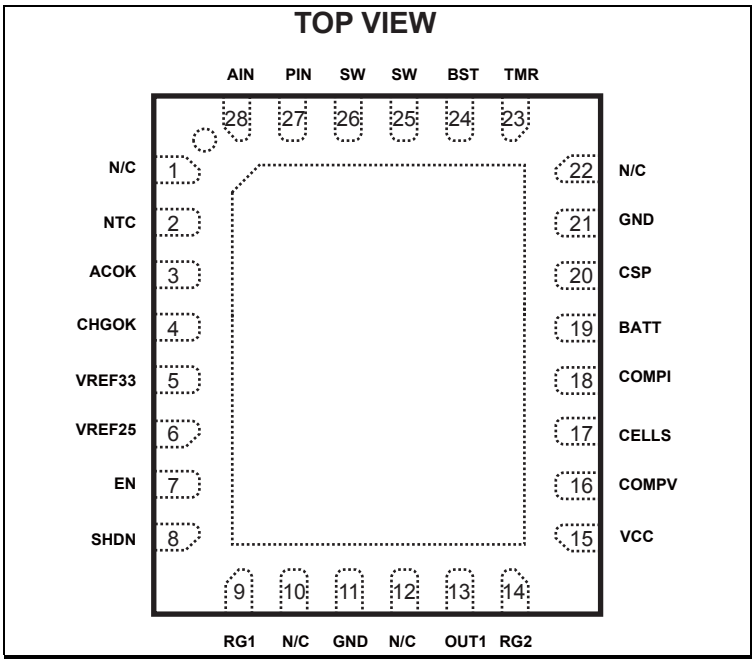
ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature (T_A)
MP2618EV	4mmx5mm QFN28	2618EV	-20°C to +85°C

* For Tape & Reel, add suffix –Z (eg. MP2618EV–Z).
For RoHS compliant packaging, add suffix –LF (eg. MP2618EV–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} 26V
V_{SW} ..... -0.3V to V_{IN} + 0.3V
V_{BS} ..... V_{SW} + 6V
V_{CSP}, V_{BATT}, ... -0.3V to +18V
All Other Pins ..... -0.3V to +6V
Continuous Power Dissipation (T_A = +25°C) (2) 3.1W
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... -65°C to +150°C
VCC, RG1, RG2 to GND ..... -0.3V to +42V
Max Differential Input Voltage (RG1 to RG2). 5V

Recommended Operating Conditions (3)

Supply Voltage V_{IN} ..... 5.5V to 24V
VCC, RG1, RG2 to GND ..... 2.5V to 40V
Operating Junct. Temp. (T_J) ..... -20°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
4mmx5mm QFN28	40	9	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB

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ELECTRICAL CHARACTERISTICS

V_{IN} = 19V, T_A = +25°C, CELLS=0V, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Terminal Battery Voltage	V_{BATT}	CELLS=0V	8.337	8.4	8.463	V
		CELLS= Float	12.505	12.6	12.695	
CSP, BATT Current	I_{CSP},I_{BATT}	Charging disabled		1		μA
Switch On Resistance	$R_{DS(ON)}$			0.28		Ω
Switch Leakage		$\overline{EN}$ = 4V, V_{SW} = 0V		0	10	μA
Peak Current Limit		CC Mode		4.1		A
		Trickle Mode		2		A
CC current	I_{CC}	RS1=100mΩ	1.8	2.0	2.2	A
Trickle charge current	$I_{TRICKLE}$			10%		Icc
Trickle charge voltage threshold				3		V/Cell
Trickle charge hysteresis				350		mV/Cell
Termination current threshold	IBF		5%	10%	15%	Icc
Oscillator Frequency	f_{SW}	V_{FB} = 1.2V		600		kHz
Fold-back Frequency		V_{FB} = 0V		190		kHz
Maximum Duty Cycle		V_{FB} = 1.2V	90			%
Maximum current Sense Voltage (CSP to BATT)	V_{SENSE}		170	200	230	mV
Minimum On Time	t_{ON}	V_{FB} = 1.5V		100		ns
Under Voltage Lockout Threshold Rising			3	3.2	3.4	V
Under Voltage Lockout Threshold Hysteresis				200	1000	mV
Open-drain sink current		Vdrain=0.3V	5			mA
Dead-battery indication		Stay at trickle charge, C_{TMR}=0.1μF		30		min
Termination delay		Time after I_{BF} reached, C_{TMR}=0.1μF		1		Min
Recharge threshold at Vbatt	Vrechg			4.0		V/cell
Recharge Hysteresis				100		mV/Cell
NTC Low Temp Rising Threshold		R_{NTC}=NCP18XH103 (0°C)		73		%of VREF33
		Recovery Hysteresis		3		
NTC High Temp Falling Threshold		R_{NTC}=NCP18XH103, (50°C)		30		%of VREF33
		Recovery Hysteresis		2		
Vin min head-room (reverse blocking)		Vin-Vbatt		180		mV
$\overline{EN}$ Input Low Voltage					0.4	V
$\overline{EN}$ Input High Voltage			1.8			V

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 19V, T_A = +25°C, CELLS=0V, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
$\overline{EN}$ Input Current		$\overline{EN}$ = 4V		4		µA
		$\overline{EN}$ = 0V		0.2		
Supply Current (Shutdown)		$\overline{EN}$ = 4V		0.5		mA
		$\overline{EN}$ = 4V, Consider VREF33 pin output current. R_3=10k,R_{NTC}=10k		0.665		mA
Supply Current (Quiescent)	I_{AIN}	$\overline{EN}$ = 0V, CELLS=0V			2.0	mA
Thermal Shutdown				150		°C
VREF25 output voltage				2.5		V
VREF33 output voltage				3.3		V
VREF33 load regulation		I_{LOAD}=0 to 10mA		30		mV
Input Current Sense Section						
Supply Voltage	V_{CC}		2.5		40	V
Supply Current	I_{IN}	I_{LOAD}= 0A, V_{CC} = 40V		12	30	µA
Common Mode Input Voltage(5)	V_{IN_CM}	V_{CC} > VIN Low		1.4		V
		V_{CC} > VIN High		40		V
OUT1 Input Offset Voltage	V_{OS1}			0.4	2	mV
Input Bias Current	I_{RG1}, I_{RG2}			4	20	nA
OUT1 Current Accuracy	I_{RG1}/I_{GS}	V_{SENSE} = 100mV		±2	±5	%
No-Load OUT1 Error		V_{SENSE} = 0V		0.1	1	µA
Low-Level OUT1 Error		V_{SENSE} = 5mV		0.3	2	µA
Shutdown Supply Current	$I_{IN(SHDN)}$	V_{SHDN} = 3V		3	6	µA
SHDN Threshold Voltage	$V_{TH_SHUTDOWN}$	(Low → High)	0.7	0.9	1.2	V
SHDN Hysteresis				30		mV
OUT1 Rise, Fall Time (5)	t_R	V_{SENSE} = 40mV, R_{GS} = 20kΩ, R_{OUT} = 100kΩ, R_{G1} = R_{G2} = 2kΩ, C_{GS} = 100pF, C_{OUT} = 100pF, 10% to 90%		17		µs
	t_F			29		µs
OUT1 Output Voltage Range	V_{GS}			V_{CC} – 0.15	24	V
Maximum OUT1 Current (5)	I_{GS}			500		µA

Notes:

5) Input common mode range cannot exceed the supply voltage.

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PIN FUNCTIONS

Pin #	Name	Description
1,10,12,22	NC	No Connection
2	NTC	Thermistor Input. Connect a resistor from this pin to the pin VREF33 and the Thermistor from this pin to ground.
3	$\overline{\text{ACOK}}$	Valid Input Supply Indicator. A logic LOW on this pin indicates the presence of a valid input supply.
4	$\overline{\text{CHGOK}}$	Charging status Indicator. A logic LOW indicates charging operation. The pin will become an open drain once the charging is stopped.
5	VREF33	Internal linear regulator 3.3V reference output. Bypass to GND with a 1μF ceramic capacitor.
6	VREF25	Internal linear regulator 2.5V reference output.
7	$\overline{\text{EN}}$	On/Off Control Input.
8	SHDN	Shutdown control of current sense amplifier. Connect this pin to $\overline{\text{EN}}$.
9	RG1	Gain Resistor of current sense amplifier.
11, 21	GND, Exposed Pad	Ground. This pin is the voltage reference for the regulated output voltage. For this reason care must be taken in its layout. This node should be placed outside of the D1 to C1 ground path to prevent switching current spikes from inducing voltage noise into the part. Connect exposed pad to ground plane for optional thermal performance.
13	OUT1	Output for Driving Resistor Load.
14	RG2	Gain Resistor of current sense amplifier.
15	VCC	Power Input of current sense amplifier.
16	COMPV	VLOOP Compensation. Decouple this pin with a capacitor and a resistor.
17	CELLS	Command Input for the Number of Li-Ion Cells. Make this pin float for 3-cell operation or connect this pin to ground for 2-cell operation.
18	COMPI	ILOOP Compensation. Decouple this pin with a capacitor and a resistor.
19	BATT	Positive Battery Terminal.
20	CSP	Battery Current Sense Positive Input. Connect a resistor RS1 between CSP and BATT.
23	TMR	Set time constant. 0.1uA charge and discharge the external cap. Connect TMR pin to GND to disable the internal timer.
24	BST	Bootstrap. This capacitor is needed to drive the power switch's gate above the supply voltage. It is connected between SW and BST pins to form a floating supply across the power switch driver.
25, 26	SW	Switch Output.
27	PIN	Power Supply Voltage. The MP2618 operates from a +5.5V to +24V unregulated input. C1 is needed to prevent large voltage spikes from appearing at the input.
28	AIN	Controller Supply Voltage.

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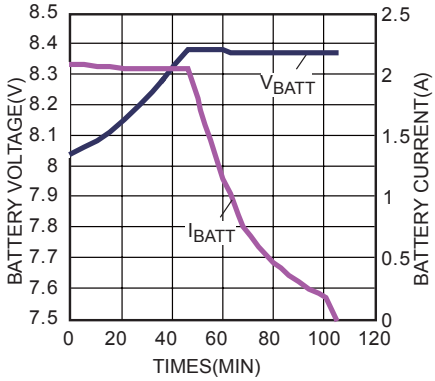
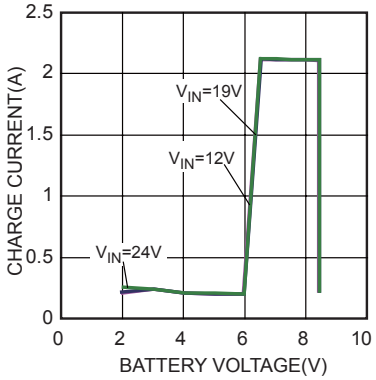
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=19V, C1=10µF, C2=4.7µF, C9=22µF, L=4.7µH, RS1=110mΩ, RS2=20mΩ, Real Battery Load, T_A=25ºC, unless otherwise noted.

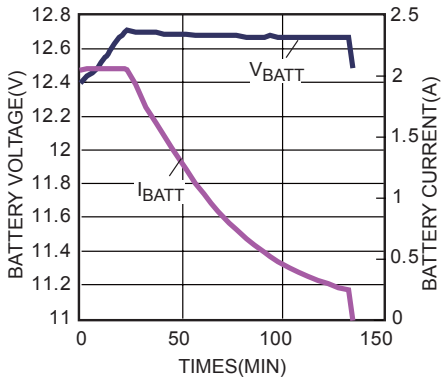
2 Cells Battery Charge Curve



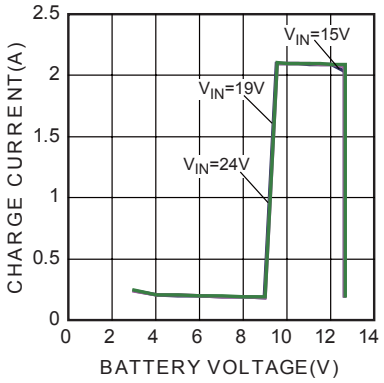
2 Cells I_{CHG} vs. V_{BATT} Curve



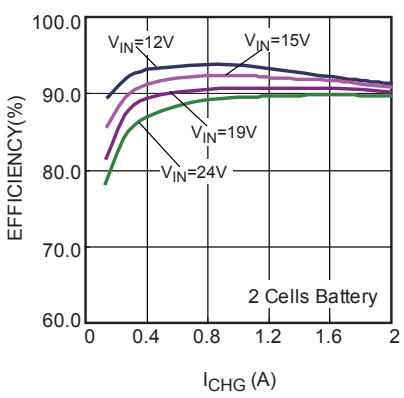
3 Cells Battery Charge Curve



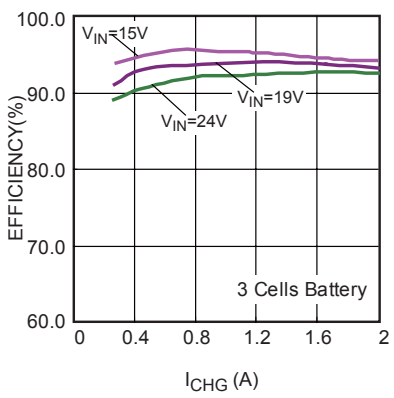
3 Cells I_{CHG} vs. V_{BATT} Curve



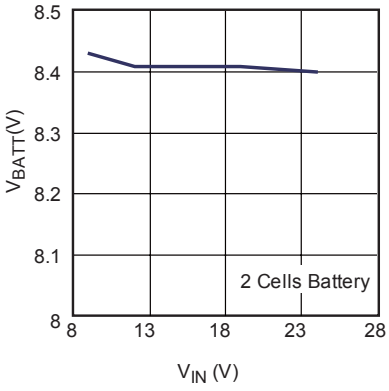
Effciency vs. I_{CHG}



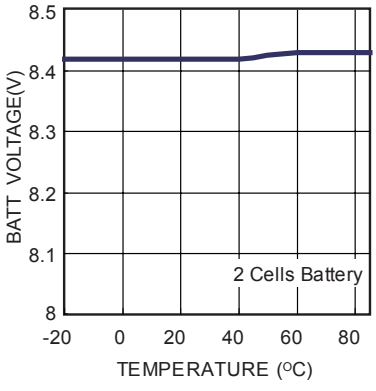
Effciency vs. I_{CHG}



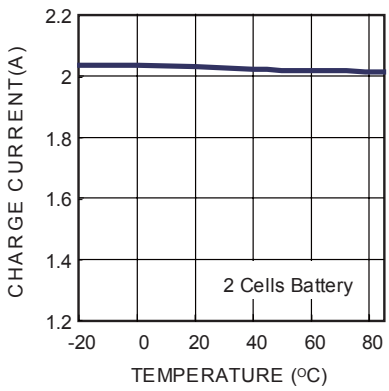
BATT Float Voltage vs. V_{IN}



BATT Float Voltage vs. Temperature



Charge Current vs. Temperature



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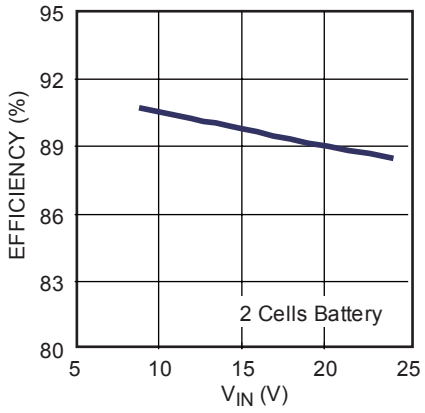
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

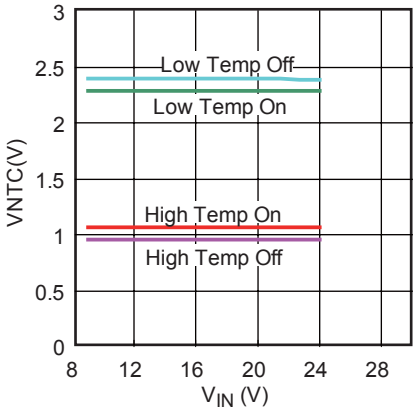
V_{IN}=19V, C1=10µF, C2=4.7µF, C9=22µF, L=4.7µH, RS1=110mΩ, RS2=20mΩ, Real Battery Load, T_A=25ºC, unless otherwise noted.

Efficiency vs. V_{IN}

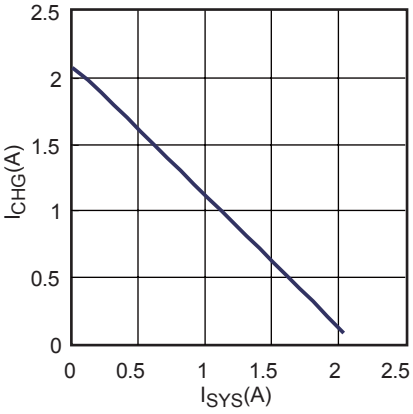
V_{BATT}=7.4V, I_{CHG}=2A



NTC Control Window



Current Sharing



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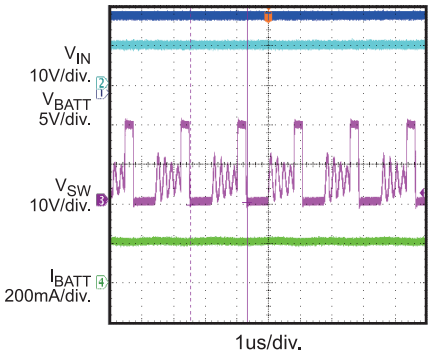
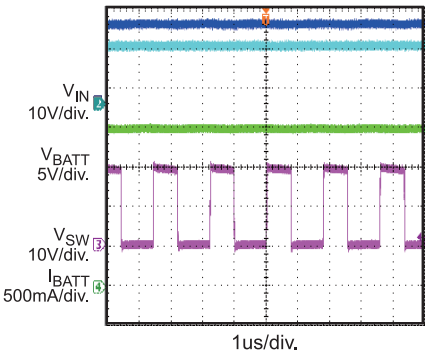
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=19V, C1=10µF, C2=4.7µF, C9=22µF, L=4.7µH, RS1=110mΩ, RS2=20mΩ, Real Battery Load, T_A=25ºC, unless otherwise noted.

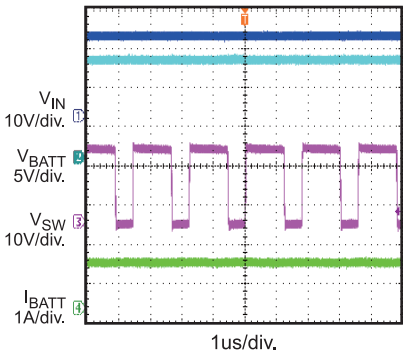
Trickle Charge
2 Cells, I_{CHG} = 2A, V_{BATT} = 5V



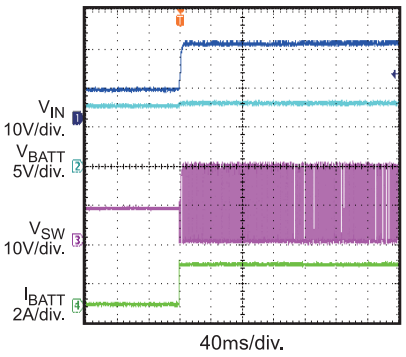
CC Charge
2 Cells, I_{CHG} = 2A, V_{BATT} = 7.4V



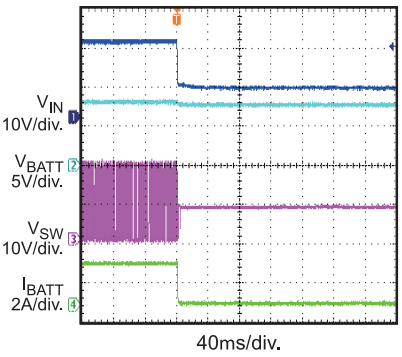
CV Charge
2 Cells, I_{CHG} = 2A, V_{BATT} = 8.4V



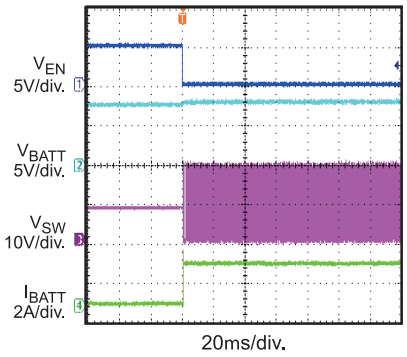
Power On
2 Cells, I_{CHG} = 2A, V_{BATT} = 8V



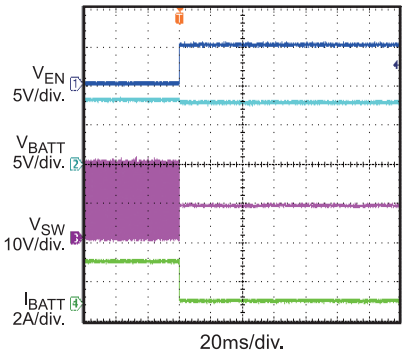
Power Off
2 Cells, I_{CHG} = 2A, V_{BATT} = 8V



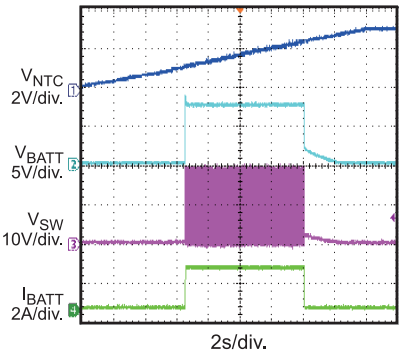
EN On
2 Cells, I_{CHG} = 2A, V_{BATT} = 8V



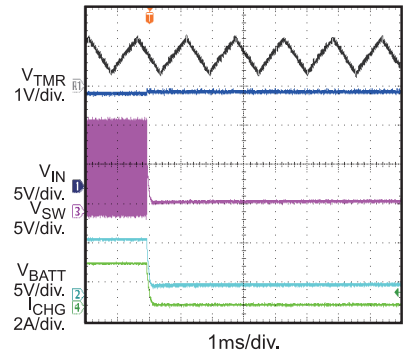
EN Off
2 Cells, I_{CHG} = 2A, V_{BATT} = 8V



NTC Control
2 Cells, I_{CHG} = 2A, V_{BATT} = 7.4V



Timer Out
V_{IN} = 12V,2 Cells, I_{CHG} = 2A, V_{BATT} = 7.4V, C_{TMR}=1nF



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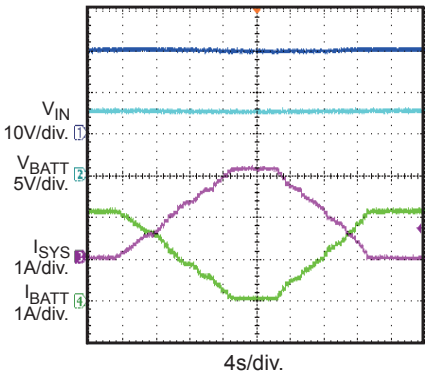
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=19V, C1=10µF, C2=4.7µF, C9=22µF, L=4.7µH, RS1=110mΩ, RS2=20mΩ, Real Battery Load, T_A=25ºC, unless otherwise noted.

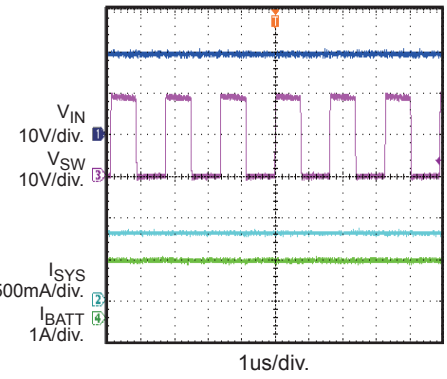
Power Path Management_Current Sharing

2 Cells, I_{CHG} = 2A, V_{BATT} = 7.4V



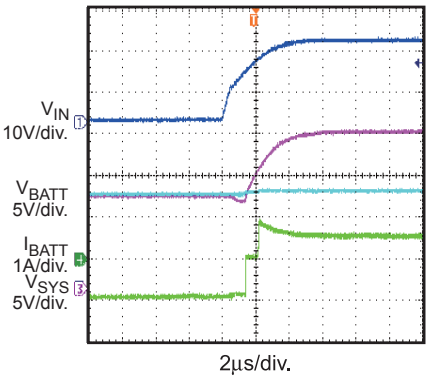
Power Path Management_Steady State

2 Cells, I_{CHG} = 2A, V_{BATT} = 8V, I_{SYS}=0.8A



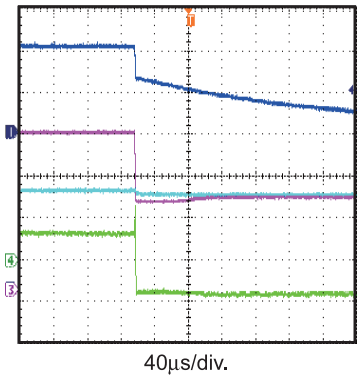
Power Path Management_Power On

3 Cells, I_{CHG} = 2A, V_{BATT} = 12V, SYS load=10Ω



Power Path Management_Power Off

3 Cells, I_{CHG} = 2A, V_{BATT} = 12V, SYS load=10Ω



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OPERATION

The MP2618 is a peak current mode controlled switching charger for use with Li-Ion batteries.

Figure 2 shows the block diagram. At the beginning of a cycle, M1 is off. The COMP voltage is higher than the current sense result from amplifier A1's output and the PWM comparator's output is low. The rising edge of the 600 kHz CLK signal sets the RS Flip-Flop. Its output turns on M1 thus connecting the SW pin and inductor to the input supply.

The increasing inductor current is sensed and amplified by the Current Sense Amplifier A1. Ramp compensation is summed to the output of A1 and compared to COMP by the PWM comparator.

When the sum of A1's output and the Slope Compensation signal exceeds the COMP voltage, the RS Flip-Flop is reset and M1 turns off. The external switching diode D1 then conducts the inductor current.

If the sum of A1's output and the Slope Compensation signal does not exceed the COMP voltage, then the falling edge of the CLK resets the Flip-Flop.

The MP2618 have two internal linear regulators power internal circuit, VREF33 and VREF25. The output of 3.3V reference voltage can also power external circuitry as long as the maximum current (50mA) is not exceeded. A 1μF bypass capacitor is required from VREF33 to GND to ensure stability.

Charge Cycle (Mode change: Trickle→ CC→ CV)

The battery current is sensed via RS1 (Figure 2) and amplified by A2. The charge will start in "trickle charging mode" (10% of the R_{SEN} programmed current I_{CC}) until the battery voltage reaches 3V/cell. If the charge stays in the "trickle charging mode" till "timer out" condition triggered, and the charge is terminated. Otherwise, the output of A2 is then regulated to the level set by RS1. The charger is operating at "constant current charging mode." The duty cycle of the switcher is determined by the COMPI voltage that is regulated by the amplifier GMI.

When the battery voltage reaches the "constant voltage mode" threshold, the amplifier GMV will regulate the COMP pin, and then the duty cycle. The charger will then operate in "constant voltage mode."

Automatic Recharge

Once the battery charging current drops below the termination threshold, the charger will cease charging and the $\overline{CHGOK}$ pin becomes an open drain. If for some reason, the battery voltage is lowered to 4.0V/Cell, recharge will automatically kick in.

Charger Status Indication

MP2618 has two open-drain status outputs: $\overline{CHGOK}$ and $\overline{ACOK}$. The $\overline{ACOK}$ pin pulls low when an input voltage is greater than battery voltage 300mV and over the under voltage lockout threshold. $\overline{CHGOK}$ is used to indicate the status of the charge cycle. Table 1 describes the status of the charge cycle based on the $\overline{CHGOK}$ and $\overline{ACOK}$ outputs.

Table 1—Charging Status Indication

$\overline{ACOK}$	$\overline{CHGOK}$	Charger status
low	low	In charging
low	high	End of charge, NTC fault, timer out, thermal shutdown $\overline{EN}$ disable
high	high	V_{IN} –V_{BAT}<0.3V. V_{IN}<UVLO

Timer Operation

MP2618 uses internal timer to terminate the charge if the timer times out. The timer duration is programmed by an external capacitor at the TMR pin.

The trickle mode charge time is:

$$T_{TICKLE_TMR} = 30mins \times \frac{C_{TMR}}{0.1uF}$$

The total charge time is:

$$T_{TOTAL_TMR} = 3hours \times \frac{C_{TMR}}{0.1uF}$$

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Negative Thermal Coefficient (NTC) Thermistor

The MP2618 has a built-in NTC resistance window comparator, which allows MP2618 to sense the battery temperature via the thermistor packed internally in the battery pack to ensure a safe operating environment of the battery. A resistor with appropriate value should be connected from VREF33 to NTC pin and the thermistor is connected from NTC pin to GND. The voltage on NTC pin is determined by the resistor divider whose divide ratio depends on the battery temperature. When the voltage of pin NTC falls out of NTC window range, MP2618 will stop the charging. The charger will restart if the temperature goes back into NTC window range.

Power Path Management

MP2618 can implement a switching charger circuit with power path management function, which realizes the current sharing of the charger and system load. In other words, MP2618 senses the system current and feeds it back, then reduces charge current according to the increase of the system current.

However, after the charge current decrease to 0, the system current can only be limited by the adapter.

The system current is satisfied first and always. It chooses the adapter as its power source when the adapter plugs in, and the battery is the backup power source when the adapter is removed.

Figure 3 to Figure 6 shows the charge profile, operation waveform and flow chart, respectively.

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BLOCK DIAGRAM

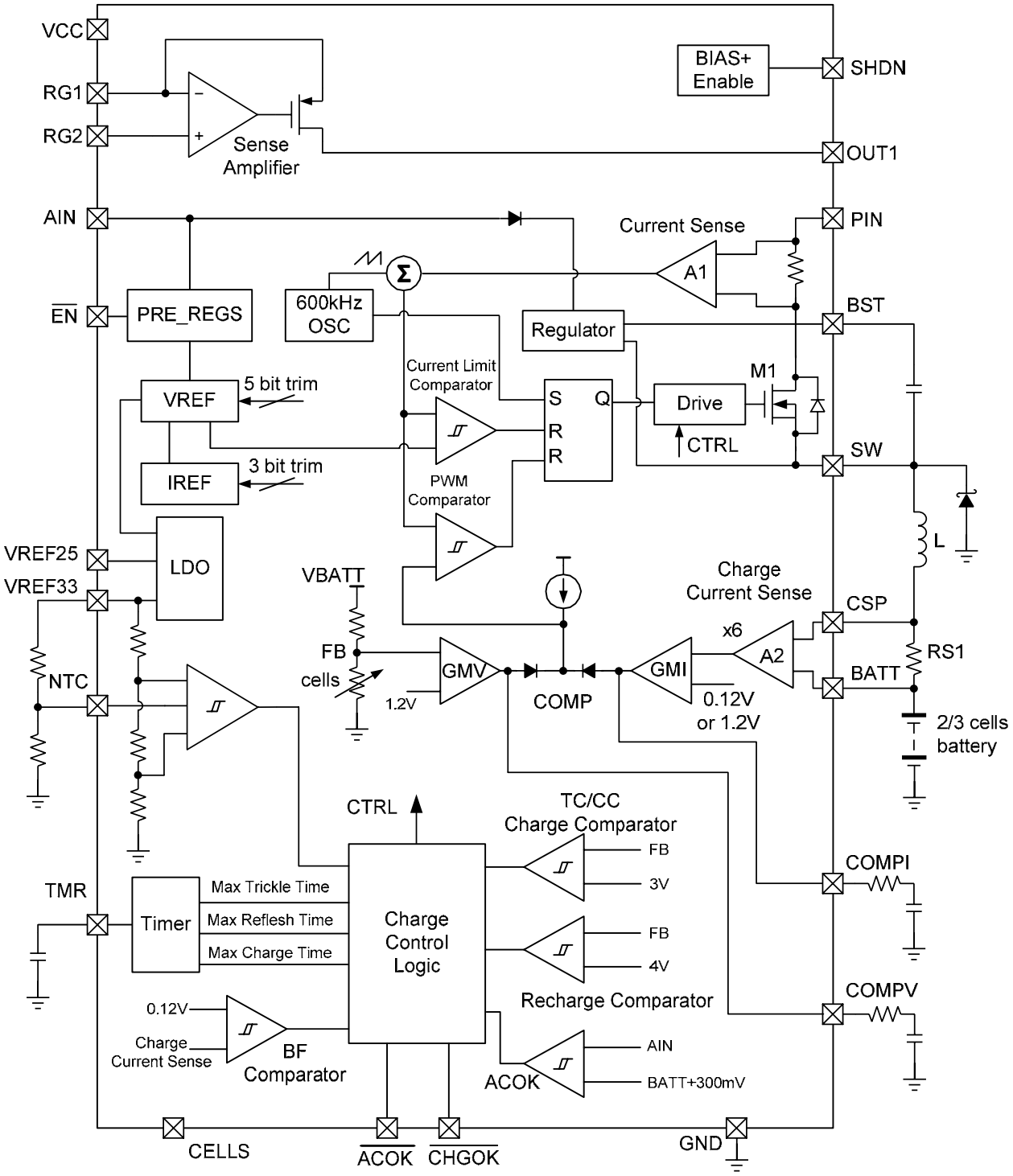

Figure 2—Function Block Diagram

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CHARGE PROFILE AND POWER PATH MANAGEMENT FUNCTION

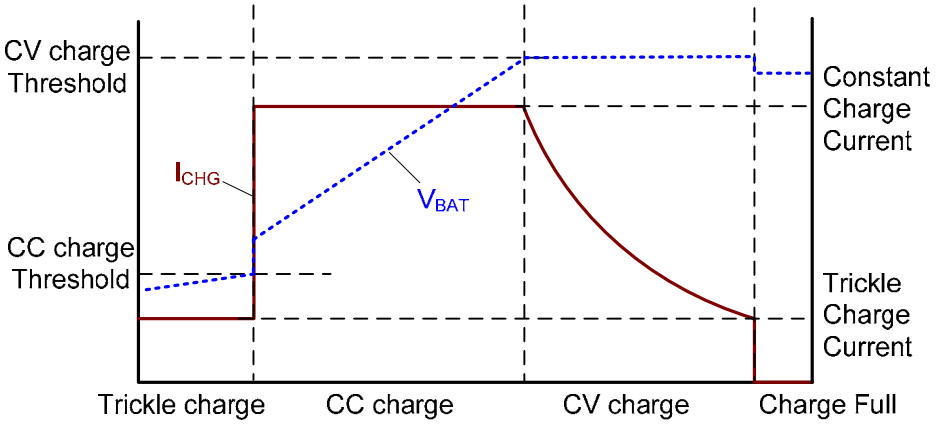

Figure 3—Li-Ion Battery Charge Profile

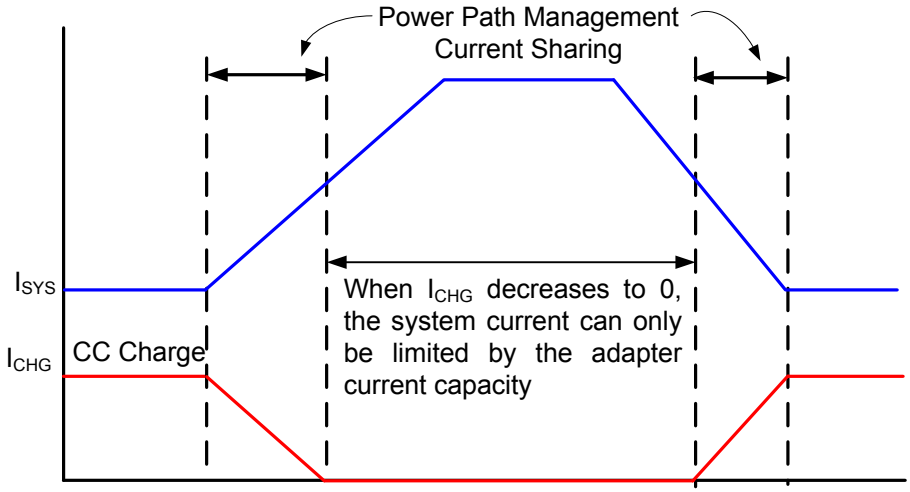

Figure 4 — Power Path Management Function- Current Sharing

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OPERATION FLOW CHART

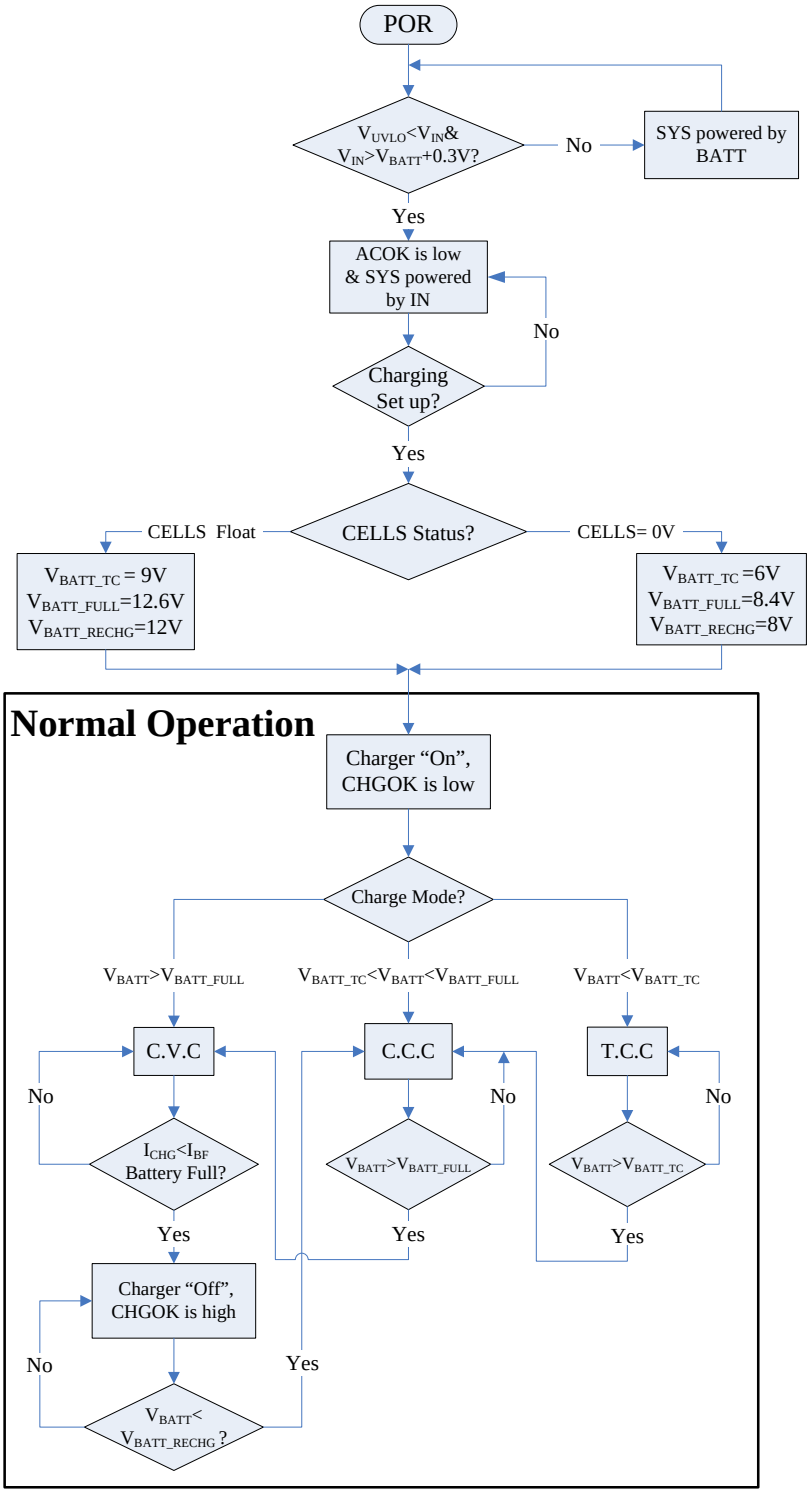

Figure 5— Normal Charging Operation Flow Chart

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OPERATION FLOW CHART *(continued)*

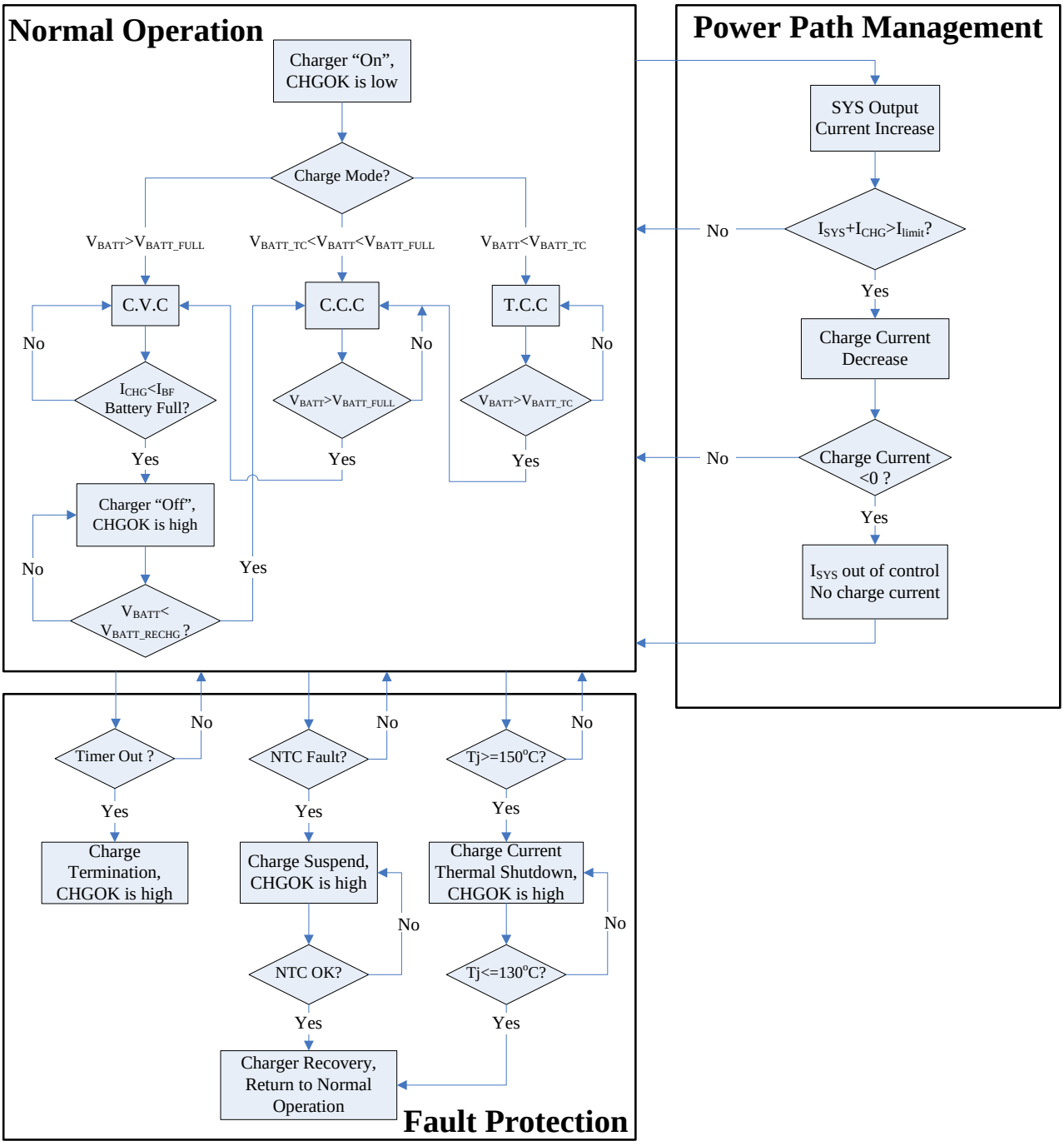

Figure 6— Power Path Management Operation and Fault Protection Flow Chart

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APPLICATION INFORMATION

Setting the Charge Current

1. Standalone Switching Charger

The charge current of MP2618 is set by the sense resistor RS1. The charge current programmable formula is as following:

$$I_{CHG}(A)=\frac{200mV}{RS1(m\Omega)} \quad (1)$$

2. Switching Charger with Power Path Management

Figure 7 shows the charge current sharing with the system current.

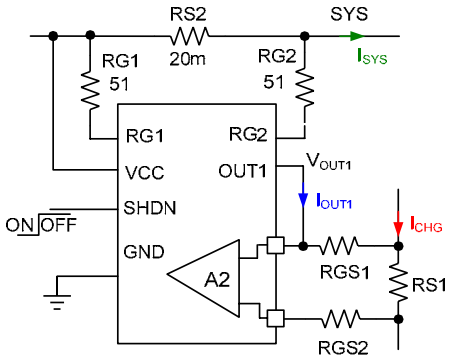

Figure 7— Charge current sharing with System current

The gain of the system current is set as:

$$Gain=\frac{RGS1}{RG1} \quad (2)$$

The voltage of OUT1 pin, V_{OUT1} can be calculated from:

$$V_{OUT1}=I_{SYS}\times RS2\times Gain=\frac{I_{SYS}\times RS2\times RGS1}{RG1} \quad (3)$$

When the system current increased ΔI_{SYS}, to satisfy the charge current decreased ΔI_{SYS} accordingly, the relationship should be:

$$\Delta I_{BAT}=\frac{\Delta V_{OUT1}}{RS1}=\frac{\Delta I_{SYS}\times RS2\times RGS1}{RS1\times RG1} \quad (4)$$

Because $\Delta I_{SYS}=\Delta I_{BAT}$, we can get:

$$\frac{RS1}{RS2}=\frac{RGS1}{RG1} \quad (5)$$

RGS1/2 causes the charge current sense error as it changes the sense gain of A2, which can be calculated from:

$$G_{A2}=\frac{12.3(k\Omega)}{2(k\Omega)+RGS(k\Omega)} \quad (6)$$

The charge current is set as:

$$I_{CHG}(A)=\frac{1230}{G_{A2}\times RS1(m\Omega)} \quad (7)$$

Then the influence of R_{GS1} to the charge current is:

$$I_{CHG}(A)=\frac{2000+RGS(\Omega)}{10\times RS1(m\Omega)} \quad (8)$$

To decrease the power loss of the sensing circuit, choose RS2 as small as possible, 20m is recommended. Too small R_{G1} results in too big current sense error of the system current, 50Ω is at least.

Substitute these two values into equation (5), then the calibrated charge current set formula in power path application is got from equation (8):

$$I_{CHG}(A)=\frac{2000+2.5\times RS1(m\Omega)}{10\times RS1(m\Omega)} \quad (9)$$

Following table is the calculated RS1 and RGS1 value for setting different charge current.

Table2—I_{CHG} Set in Power Path Application

I_{CHG}(A)	RGS(Ω)	RS1(mΩ)
2	280	110
1.5	402	160
1	665	260
0.8	909	360
0.5	2k	800

If choose different RS2 and RG1, re-calculated from equation (5) and equation (8), then get the different equation (9) and the table.

Also, any relationship between ΔI_{SYS} and ΔI_{BATT} can be realized by re-calculate equation (4), (5) and (8).

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Selecting the Inductor

A 1μH to 10μH inductor is recommended for most applications. The inductance value can be derived from the following equation.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (10)$$

Where ΔI_L is the inductor ripple current. V_{OUT} is the 2/3 cell battery voltage.

Choose inductor current to be approximately 30% if the maximum charge current, 2A. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{CHG} + \frac{\Delta I_L}{2} \quad (11)$$

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency.

For optimized efficiency, the inductor DC resistance is recommended to be less than 200mΩ.

NTC Function

As Figure 8 shows, the low temperature threshold and high temperature threshold are preset internally via a resistive divider, which are 73%·VREF33 and 30%·VREF33. For a given NTC thermistor, we can select appropriate R3 and R6 to set the NTC window.

In detail, for the thermistor (NCP18XH103) noted in above electrical characteristic,

At 0ºC, R_{NTC_Cold} = 27.445k;

At 50ºC, R_{NTC_Hot} = 4.1601k.

Assume that the NTC window is between 0ºC and 50ºC, the following equations could be derived:

$$\frac{R6//R_{NTC_Cold}}{R3 + R6//R_{NTC_Cold}} = \frac{V_{TH_Low}}{VREF33} = 73\% \quad (12)$$

$$\frac{R6//R_{NTC_Hot}}{R3 + R6//R_{NTC_Hot}} = \frac{V_{TH_High}}{VREF33} = 30\% \quad (13)$$

According to equation (12) and equation (13), we can find that R3 = 9.63k and R6 = 505k.

To be simple in project, making R3=10k and R6 no connect will approximately meet the specification.

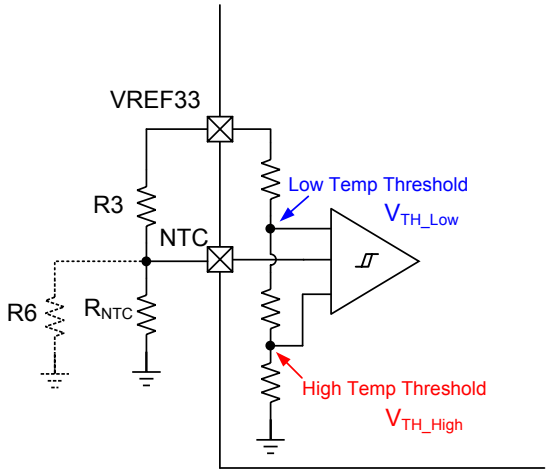

Figure 8— NTC function block

Selecting the Input Capacitor

The input capacitor reduces the surge current drawn from the input and also the switching noise from the device. The input capacitor impedance at the switching frequency should be less than the input source impedance to prevent high frequency switching current passing to the input. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 4.7μF capacitor is sufficient.

Selecting the Output Capacitor

The output capacitor keeps output voltage ripple small and ensures regulation loop stability. The output capacitor impedance should be low at the switching frequency. Ceramic capacitors with X5R or X7R dielectrics are recommended.

PC Board Layout

The high frequency and high current paths (GND, IN and SW) should be placed to the device with short, direct and wide traces. The input capacitor needs to be as close as possible to the IN and GND pins. The external feedback resistors should be placed next to the FB pin. Keep the switching node SW short and away from the feedback network.

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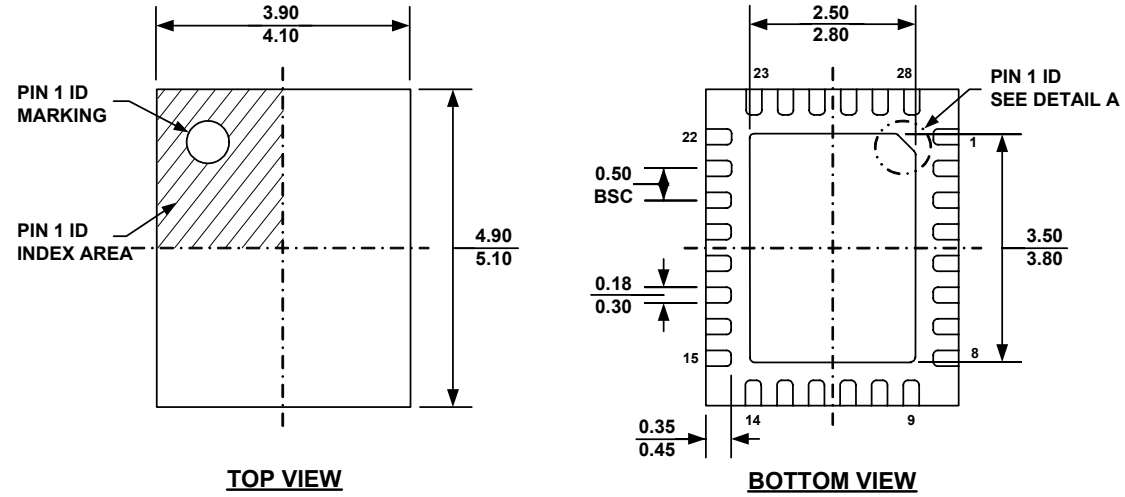
PACKAGE INFORMATION

QFN28 (4mm x 5mm)



NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-220, VARIATION VHGD-3.
5) DRAWING IS NOT TO SCALE.

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