MP2499A

36V, 3A Max, High-Efficiency, Synchronous, Step-Down Converter with Output Line Drop Compensation

DESCRIPTION

The MP2499A is a synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs. The MP2499A offers a very compact solution that achieves a maximum of 3A of continuous output current with built-in, output, line drop compensation.

The MP2499A uses synchronous mode operation to achieve high efficiency over the output current load range. Current-mode operation provides fast transient response and eases loop stabilization.

Full protection features include over-current protection (OCP) and thermal shutdown.

The MP2499A requires a minimal number of readily available, standard, external components and is available in a space-saving QFN-13 (2.5mmx3mm) package.

FEATURES

- Wide 5V to 36V Continuous Operating Input Range
- 85mΩ/55mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- High-Efficiency Synchronous Mode Operation
- Default 270kHz Switching Frequency
- Synchronizes to a 200kHz to 2.4MHz External Clock
- Internal Soft Start
- Output Line Drop Compensation
- Accurate Continuous Output Current Limit with External Resistor
- Over-Current Protection (OCP) and Hiccup
- Thermal Shutdown
- Output Adjustable from 0.8V
- Available in a QFN-13 (2.5mmx3mm) Package

APPLICATIONS

- USB-Dedicated Charging Ports (DCP)
- Automotive Cigarette Lighter Adapters
- USB Chargers
- USB PD Applications

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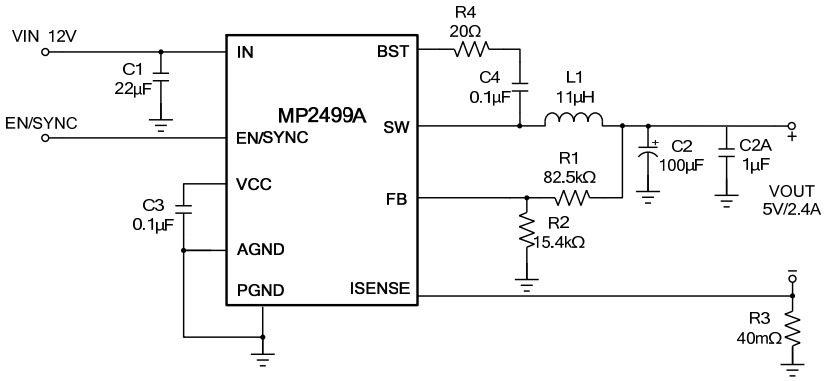
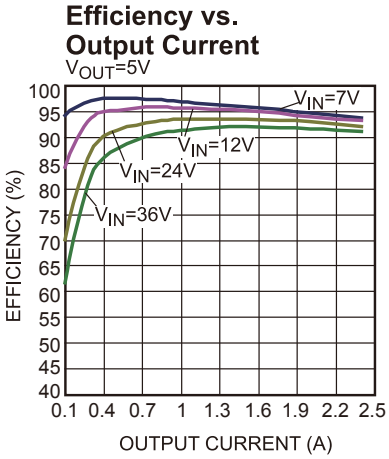
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2499AGQB	QFN-13 (2.5mmx3mm)	*See Below*

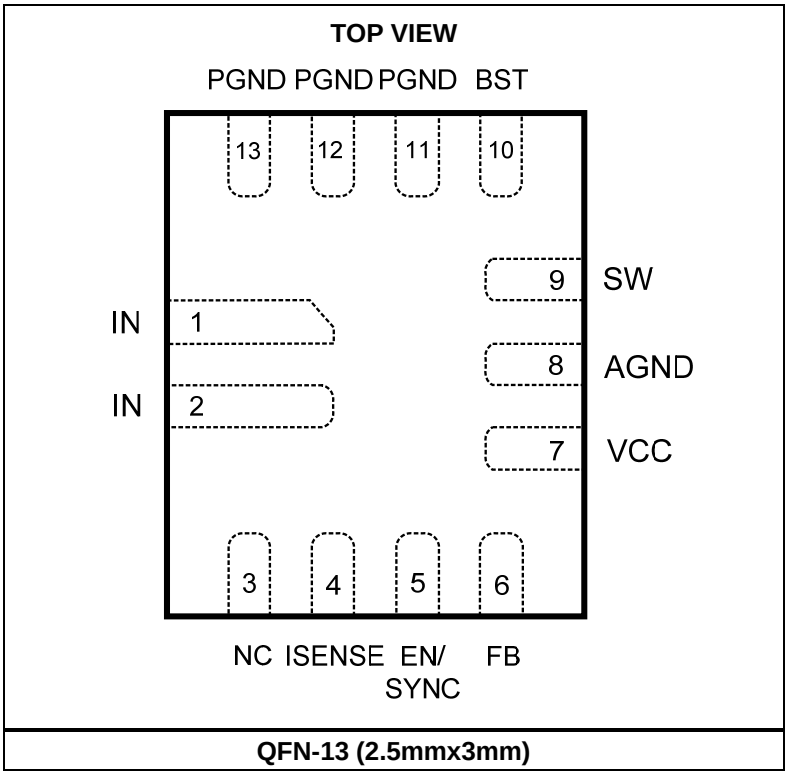
* For Tape & Reel, add suffix –Z (e.g. MP2499AGQB–Z).

TOP MARKING

BJQ
YWW
LLL

BJQ: Product code of MP2499AGQB
Y: Year code
WW: Week code
LLL: Lot number

PACKAGE REFERENCE



QFN-13 (2.5mmx3mm)

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PIN FUNCTIONS

Package Pin #	Name	Description
1, 2	IN	**Supply voltage.** The MP2499A operates from a 5V to 36V input rail. A capacitor (C1) is required to decouple the input rail. Connect IN using a wide PCB trace.
3	NC	**No connection.** Leave NC floating.
4	ISENSE	**Output current sense.** Connect a resistor from ISENSE close to AGND to sense the output current and set the continuous output current-limit threshold.
5	EN/SYNC	**Enable/synchronize.** Drive EN/SYNC high to enable the MP2499A. Drive EN/SYNC low to disable the MP2499A. EN/SYNC cannot be floated. Apply an external clock to EN/SYNC to change the switching frequency.
6	FB	**Feedback.** Connect FB to the tap of an external resistor divider from the output to GND to set the output voltage. The frequency foldback comparator lowers the oscillator frequency when the FB voltage is below 240mV to prevent current limit runaway during a short-circuit fault condition.
7	VCC	**Bias supply.** Decouple VCC with a 0.1 - 0.22μF capacitor. The capacitor should not exceed 0.22μF.
8	AGND	**Analog ground.**
9	SW	**Switch output.** Connect SW using a wide PCB trace.
10	BST	**Bootstrap.** Connect a capacitor between SW and BST to form a floating supply across the high-side switch driver. Place a 20Ω resistor between the SW and BST capacitor to reduce SW voltage spikes.
11 - 13	PGND	**System ground.** PGND is the reference ground of the regulated output voltage. PGND requires special care during the PCB layout. For best results, connect PGND with copper traces and vias.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... -0.3V to 40V
V_{SW} ..... -0.3V (-5V for <10ns) to 41V (43V for <10ns)
V_{BST} ..... V_{SW} + 6V
All other pins ..... -0.3V to 6V (2)
Continuous power dissipation (T_A = +25°C) (3)
QFN-13 (2.5mmx3mm) 2.08W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to 150°C

Recommended Operating Conditions

Continuous supply voltage (V_{IN}) ..... 5V to 36V
Output voltage (V_{OUT}) ..... 0.8V to D_{MAX} x V_{IN}
Operating junction temp. (T_J) .... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-13 (2.5mmx3mm)	60	13 ... °C/W

NOTES:

1) Absolute maximum ratings are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
2) For details on EN/SYNC's ABS max rating, please refer to the EN/SYNC Control section on page 10.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C (5), unless otherwise noted. Typical values are at T_J = +25°C.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{SHDN}	V_{EN} = 0V			10	μA
Supply current (quiescent)	I_Q	V_{EN} = 2V, V_{FB} = 1V		0.7	0.9	mA
HS switch on resistance	R_{ON_HS}	V_{BST-SW} = 5V		85	150	mΩ
LS switch on resistance	R_{ON_LS}	V_{CC} = 5V		55	105	mΩ
Switch leakage	I_{LKG_SW}	V_{EN} = 0V, V_{SW} = 12V			1	μA
Current limit	I_{LIMIT}	Under 40% duty cycle	4	6	8	A
Oscillator frequency	f_{SW}	V_{FB} = 750mV	200	270	340	kHz
Foldback frequency	f_{FB}	V_{FB} < 240mV, and OC (V_{COMP} is high)		70		kHz
Maximum duty cycle (6)	D_{MAX}	V_{FB} = 750mV, 250kHz		97		%
Minimum on time (6)	t_{ON_MIN}			70		ns
Sync frequency range	f_{SYNC}		0.2		2.4	MHz
ISENSE reference voltage	V_{ISENSE}		94	118	142	mV
Line drop compensation current	I_{SINK}	I_O = 2.4A, R_{SENSE} = 40mΩ, T_J = 25°C	4	6	8	μA
Feedback voltage	V_{FB}	T_J = 25°C	780	792	804	mV
		T_J = -40°C to 85°C	776	792	808	
Feedback current	I_{FB}	V_{FB} = 820mV		10	100	nA
EN/SYNC rising threshold	V_{EN_RISING}		1.15	1.4	1.65	V
EN/SYNC falling threshold	$V_{EN_FALLING}$		1.05	1.25	1.45	V
EN/SYNC threshold hysteresis	V_{EN_HYS}			150		mV
V_{IN} under-voltage lockout threshold rising	$INUV_{RISING}$		4.2	4.5	4.8	V
V_{IN} under-voltage lockout threshold-falling	$INUV_{FALLING}$		4	4.3	4.6	V
V_{IN} under-voltage lockout threshold hysteresis	$INUV_{HYS}$			200		mV
VCC regulator	V_{CC}	I_{CC} = 0mA	4.6	4.9	5.2	V
VCC load regulation		I_{CC} = 5mA		1.5	4	%
Soft-start period	t_{SS}	V_{OUT} from 10% to 90%		1.6		ms
Thermal shutdown (6)				170		°C
Thermal hysteresis (6)				30		°C

NOTES:

5) Not tested in production, guaranteed by over-temperature correlation.
6) Guaranteed by design and engineering sample characterization.

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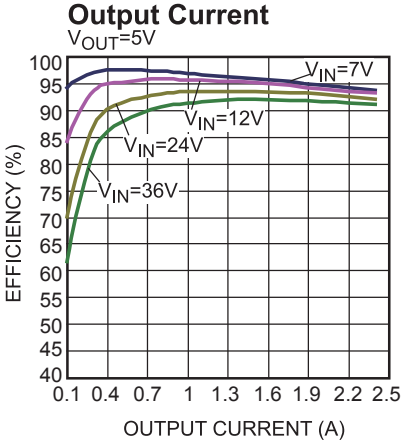
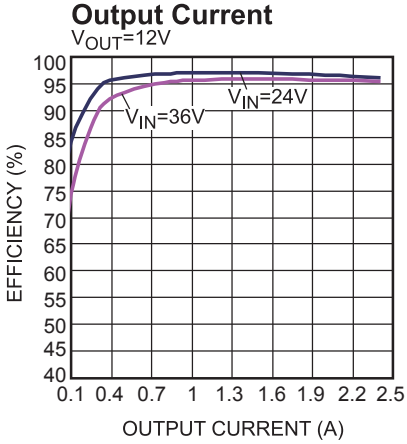
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, L = 11µH, T_A = +25°C, unless otherwise noted.

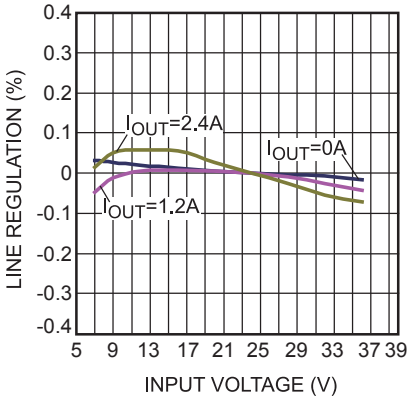
Efficiency vs. Output Current



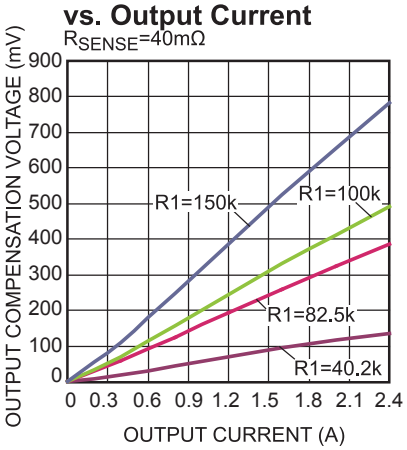
Efficiency vs. Output Current



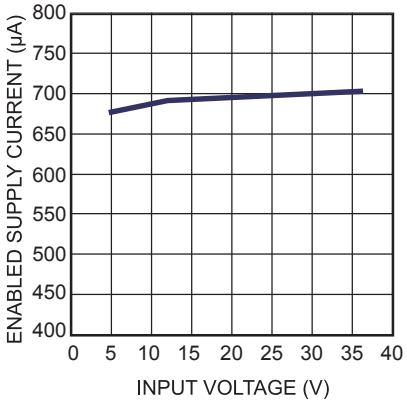
Line Regulation



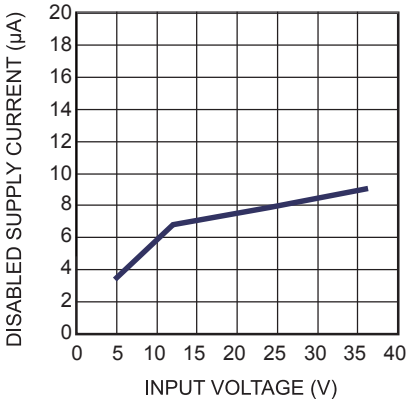
Line Drop Compensation vs. Output Current



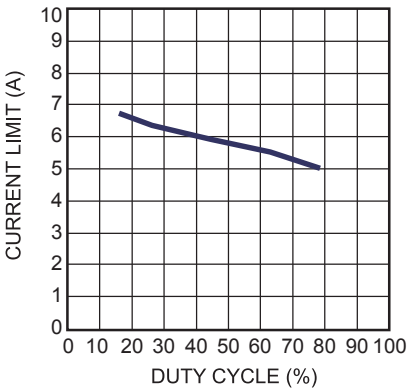
Enabled Supply Current vs. Input Voltage



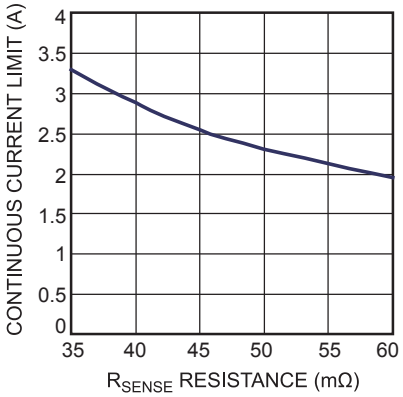
Disabled Supply Current vs. Input Voltage



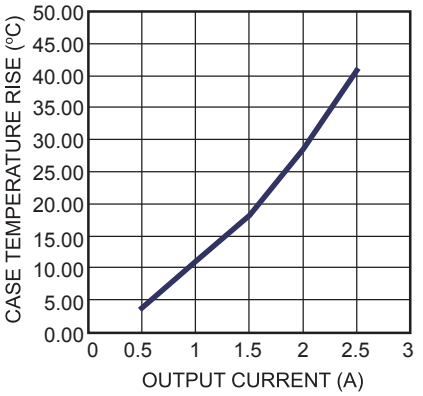
Current Limit vs. Duty Cycle



Continuous Output Current Limit vs. R_{SENSE}



Case Temperature Rise vs. Output Current



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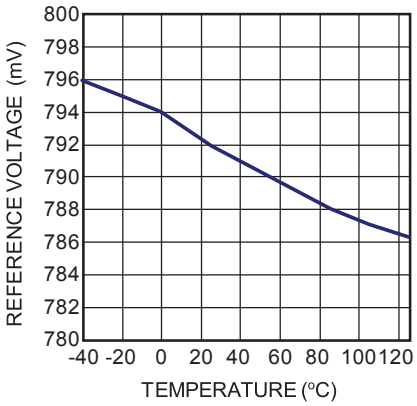
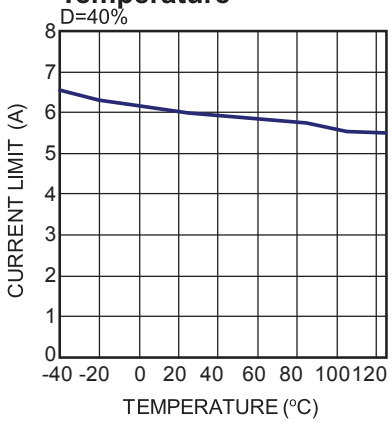
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 11µH, T_A = +25°C, unless otherwise noted.

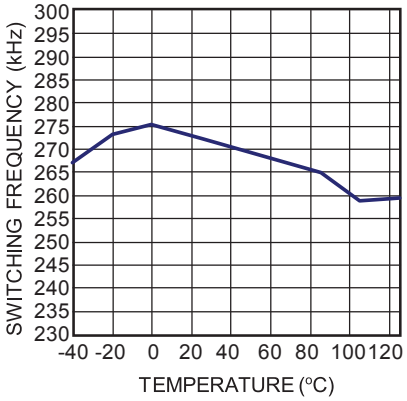
Reference Voltage vs. Temperature



Current Limit vs. Temperature



Switching Frequency vs. Temperature



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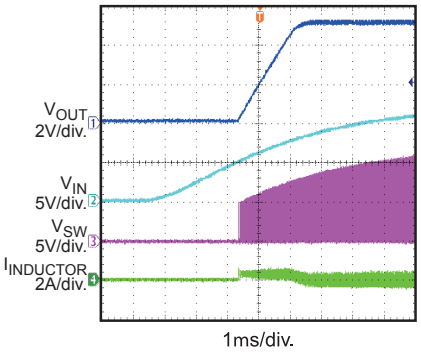
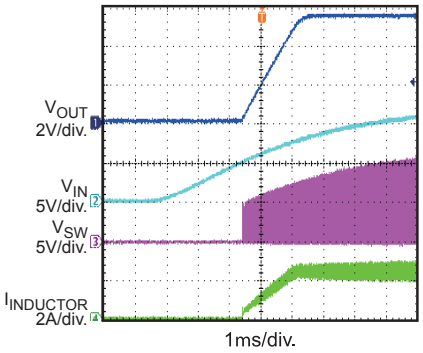
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 11µH, T_A = +25°C, unless otherwise noted.

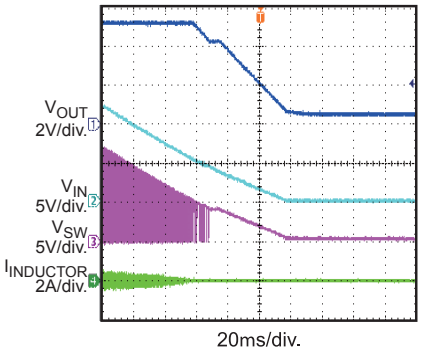
Start-Up through V_{IN}
I_{OUT} = 0A



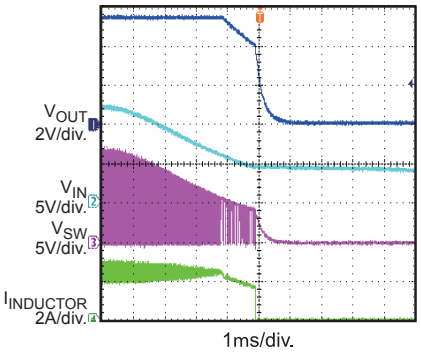
Start-Up through V_{IN}
I_{OUT} = 2.4A



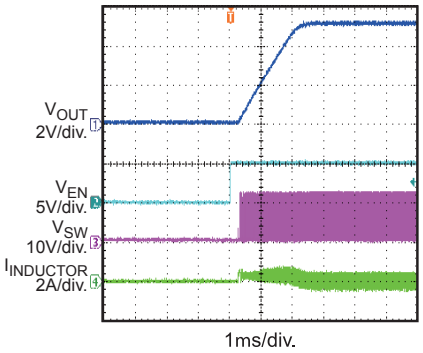
Shutdown through V_{IN}
I_{OUT} = 0A



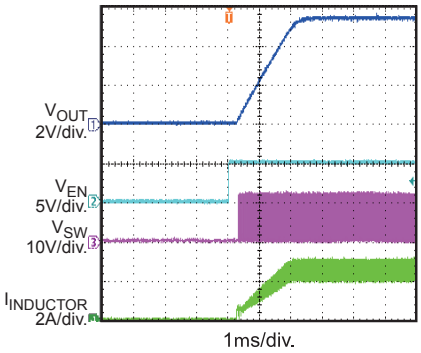
Shutdown through V_{IN}
I_{OUT} = 2.4A



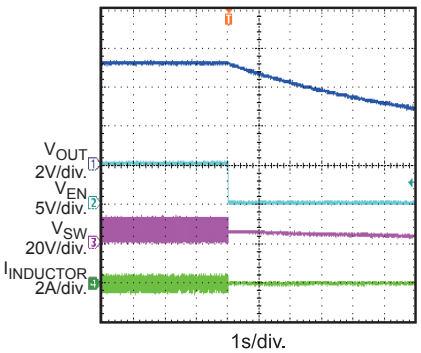
Start-Up through EN/SYNC
I_{OUT} = 0A



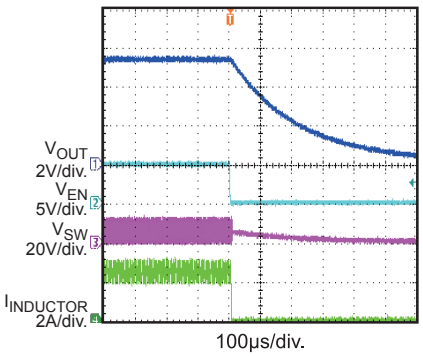
Start-Up through EN/SYNC
I_{OUT} = 2.4A



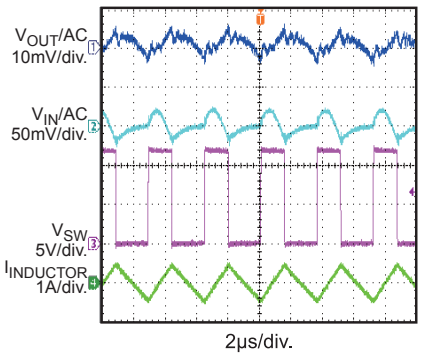
Shutdown through EN/SYNC
I_{OUT} = 0A



Shutdown through EN/SYNC
I_{OUT} = 2.4A



Output Voltage Ripple
I_{OUT} = 0A



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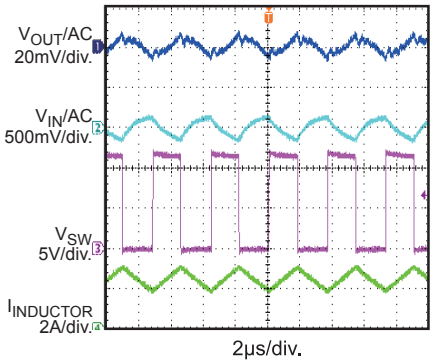
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 11µH, T_A = +25°C, unless otherwise noted.

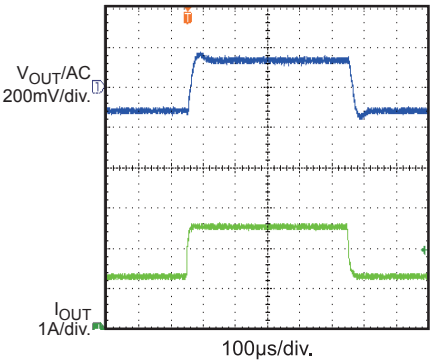
Output Voltage Ripple

I_{OUT} = 2.4A



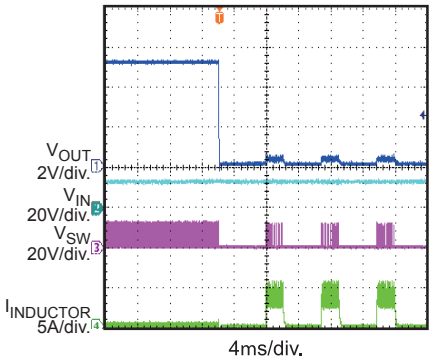
Load Transient Response

I_{OUT} = 1.2A-2.4A



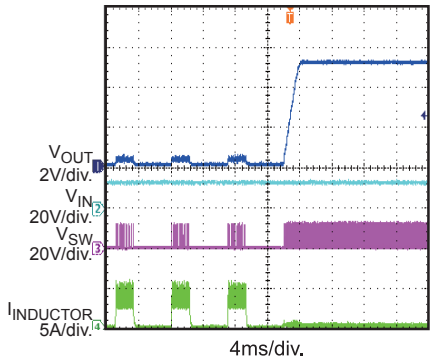
Short-Circuit Entry

I_{OUT} = 0A



Short-Circuit Recovery

I_{OUT} = 0A



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BLOCK DIAGRAM

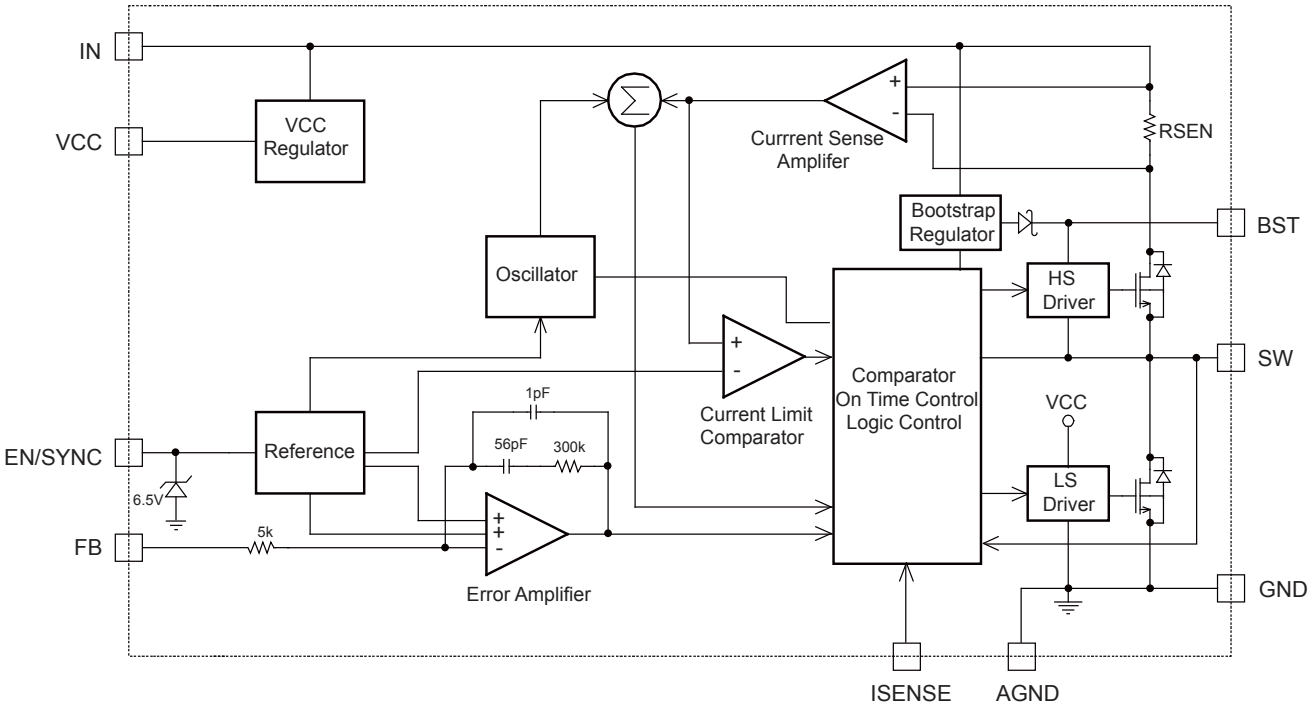

Figure 1: Functional Block Diagram

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OPERATION

The MP2499A is a high-frequency, synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs. The MP2499A offers a very compact solution that achieves 3A max of continuous output current with built-in output line drop compensation.

The MP2499A operates in a fixed-frequency, peak-current-control mode to regulate the output voltage. An internal clock initiates a pulse-width modulation (PWM) cycle. The integrated high-side power MOSFET (HS-FET) turns on and remains on until its current reaches the value set by the error amplifier (EA) COMP voltage (V_{COMP}). When the power switch is off, it remains off until the next clock cycle begins. If the current in the power MOSFET does not reach the current value set by V_{COMP} within 97% of one PWM period, the power MOSFET is forced off.

Internal Regulator

The 5V internal regulator powers most of the internal circuitries. This regulator takes the V_{IN} input and operates in the full V_{IN} range. When V_{IN} exceeds 5.0V, the output of the regulator is in full regulation. When V_{IN} falls below 5.0V, the output of the regulator decreases following V_{IN}. A 0.1µF decoupling ceramic capacitor is needed at VCC.

Error Amplifier (EA)

The EA compares the FB voltage against the internal 0.8V reference (REF) and outputs a V_{COMP} value. This V_{COMP} controls the power MOSFET current. The optimized internal compensation network minimizes the external component count and simplifies the control loop design.

Enable/SYNC Control (EN/SYNC)

EN/SYNC is a digital control pin that turns the regulator on and off. Drive EN/SYNC high to turn on the regulator. Drive EN/SYNC low to turn off the regulator. EN/SYNC cannot be floated.

EN/SYNC is clamped internally using a 6.5V series Zener diode (see Figure 2). Connect the EN/SYNC input through a pull-up resistor to any voltage connected to IN. The pull-up resistor limits the EN/SYNC input current below 150µA.

For example, with 12V connected to V_{IN}, $R_{PULLUP} \geq (12V - 6.5V) \div 150\mu A = 36.7k\Omega$.

Connecting EN/SYNC to a voltage source directly without a pull-up resistor requires limiting the voltage amplitude to ≤6V to prevent damage to the Zener diode.

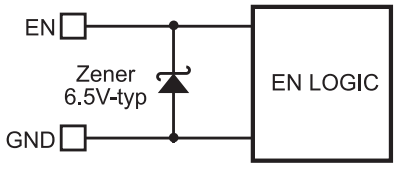

Figure 2: 6.5V Type Zener Diode

Connect an external clock with a range of 200kHz to 2.4MHz to synchronize the internal clock rising edge to the external clock rising edge. The pulse width of the external clock signal should be less than 3µs.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MP2499A UVLO comparator monitors the output voltage of the internal regulator (VCC). The UVLO rising threshold is about 4.5V, while its falling threshold is 4.3V.

Internal Soft Start (SS)

Soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage that ramps up from 0 - 1.2V. When SS is lower than REF, SS overrides REF, so the error amplifier uses SS as the reference. When SS exceeds REF, the error amplifier uses REF as the reference. The SS time is set to 1.6ms internally.

Output Line Drop Compensation

The MP2499A can compensate for an output voltage drop, such as high impedance caused by a long trace, to maintain a fairly constant load-side voltage.

The MP2499A uses the sensed load current through the external sensing resistor (R_{SENSE}) to sink a current (I_{SINK}) at FB. Calculate I_{SINK} with Equation (1):

$$I_{SINK} = \frac{I_{LOAD} \cdot R_{SENSE}}{16.5k} \quad (1)$$

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This current flows through the feedback resistor (R1) and generates V_{COMP} (see Figure 3).

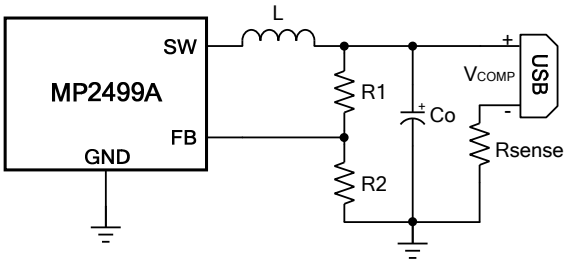

Figure 3: Output Line Drop Compensation

Calculate V_{COMP} with Equation (2):

$$V_{COMP} = I_{LOAD} \cdot R_{SENSE} \left(\frac{R1}{16.5k} - 1 \right) \quad (2)$$

The line drop compensation voltage amplitude increases linearly as the load current increases. Setting a different R1 value can produce different voltages to compensate for the cable drop voltage (see Figure 4). When the load current is 2.4A, R1 is 82.5kΩ, R_{SENSE} is 40mΩ, and V_{COMP} is 384mV.

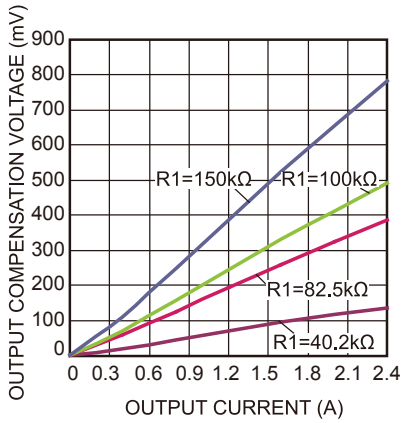

Figure 4: Output Line Drop Compensation at Different R1 Values

Over-Current Protection (OCP) and Hiccup

The MP2499A uses a cycle-by-cycle over-current limit when the inductor current peak value exceeds the current limit threshold. If the output voltage drops until FB is below the under-voltage (UV) threshold (typically 30% below the reference), the MP2499A enters hiccup mode to restart the part periodically. This protection mode is especially useful when the output is dead-shorted to ground. The average short-circuit current is reduced greatly to alleviate thermal issues and protect the regulator. The MP2499A exits hiccup mode once the over-current condition is removed.

The MP2499A also has a continuous output current limit. A current sensing resistor senses the load current to protect the output from an over-current condition. If output over-current is detected (ISENSE voltage exceeds 118mV) and the output voltage drops until FB is 30% below the reference, the MP2499A enters hiccup mode. The MP2499A enters hiccup mode when the soft start finishes, over-current occurs (internal cycle-by-cycle inductor peak current limit or external sensed continuous output current limit), and FB falls below the under-voltage (UV) threshold.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 170°C, the entire chip shuts down. When the temperature drops below its lower threshold (typically 140°C), the chip is enabled again.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. A dedicated internal regulator charges and regulates the bootstrap capacitor voltage to ~5V (see Figure 5). When the voltage between the BST and SW nodes drops below regulation, a PMOS pass transistor connected from V_{IN} to BST turns on. The charging current path is from V_{IN} to BST to SW. The external circuit should provide enough voltage headroom to facilitate charging. As long as V_{IN} is higher than SW significantly, the bootstrap capacitor remains charged.

When the HS-FET is on, $V_{IN} \approx V_{SW}$, so the bootstrap capacitor cannot charge. When the low-side MOSFET (LS-FET) is on, V_{IN} - V_{SW} reaches its maximum for fast charging. When there is no inductor current, $V_{SW} = V_{OUT}$, so the difference between V_{IN} and V_{OUT} can charge the bootstrap capacitor. The floating driver has its own UVLO protection with a rising threshold of 2.2V and hysteresis of 150mV. Place a 20Ω resistor between the SW and BST capacitor to reduce SW voltage spikes.

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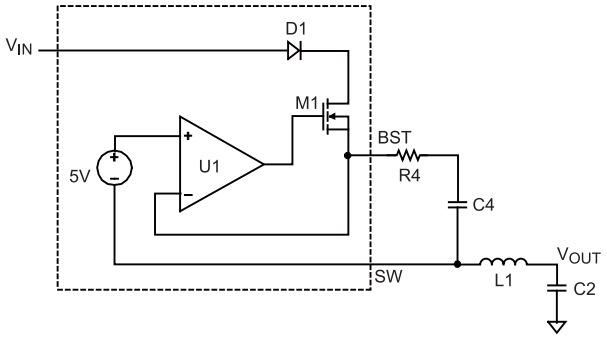

Figure 5: Internal Bootstrap Charging Circuit

Start-Up and Shutdown

If both V_{IN} and EN/SYNC exceed their respective thresholds, the chip starts up. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Three events can shut down the chip: EN/SYNC low, V_{IN} low, and thermal shutdown. In the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. The EA V_{COMP} and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

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APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage (see Figure 6). The feedback resistor (R1) sets the feedback loop bandwidth with the internal compensation capacitor. R1 should be around 82.5kΩ. R2 can then be calculated with Equation (2):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.792V} - 1} \quad (2)$$

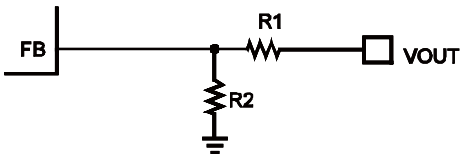

Figure 6: Feedback Network

Selecting the Inductor

For most applications, use a 10 - 20μH inductor with a DC current rating at least 25% higher than the maximum load current. For the highest efficiency, an inductor with a small DC resistance is recommended. For most designs, the inductance value can be derived from Equation (3):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (3)$$

Where ΔI_L is the inductor ripple current.

Set the inductor ripple current to be approximately 40% of the maximum load current. The maximum inductor peak current can be calculated with Equation (4):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (4)$$

Setting the Continuous Output Current Limit

The MP2499A has a programmable continuous output current limit, which is set by an external resistor (R_{SENSE}). The current limit can be calculated with Equation (5):

$$I_{CC_LIMIT} = \frac{V_{ISENSE}}{R_{SENSE}} \quad (5)$$

Where V_{ISENSE} = 118mV.

Choose a different R_{SENSE} to set a different continuous output current limit. If R_{SENSE} = 40mΩ, then the current limit is 2.95A.

Setting the Line Drop Compensation

The MP2499A can generate a V_{COMP} value to compensate for the line drop at the output (see Figure 3).

V_{COMP} can be calculated with Equation (6):

$$V_{COMP} = I_{LOAD} \cdot R_{SENSE} \left(\frac{R1}{16.5k} - 1 \right) \quad (6)$$

When the load current is 2.4A, R1 is 82.5kΩ, R_{SENSE} is 40mΩ, and V_{COMP} is 384mV.

Setting the V_{IN} UVLO

The MP2499A has an internal, fixed, under-voltage lockout (UVLO) threshold. The rising threshold is 4.5V, while the falling threshold is about 4.3V. For applications requiring a higher UVLO point, an external resistor divider between EN/SYNC and IN can be used to achieve a higher equivalent UVLO threshold (see Figure 7).

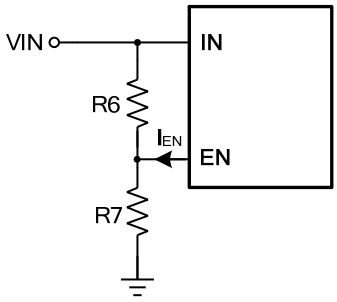

Figure 7: Adjustable UVLO using EN/SYNC Divider

The UVLO threshold can be calculated with Equation (7) and Equation (8):

$$INUV_{RISING} = \left(1 + \frac{R6}{R7}\right) \cdot V_{EN_RISING} - I_{EN} \cdot R6 \quad (7)$$

$$INUV_{FALLING} = \left(1 + \frac{R6}{R7}\right) \cdot V_{EN_FALLING} - I_{EN} \cdot R6 \quad (8)$$

Where V_{EN_RISING} = 1.4V, $V_{EN_FALLING}$ = 1.25V, and I_{EN} = 7μA.

When choosing R6, ensure that it is large enough to limit the current flow into EN/SYNC below 150μA.

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Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are recommended for their low ESR and small temperature coefficients. For CLA applications, a 100µF electrolytic capacitor and two 10µF ceramic capacitors are recommended.

Since C1 absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (9):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (9)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (10):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (10)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 1µF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (11):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (11)$$

Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (12)$$

Where L_1 is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and the capacitance causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (13):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (13)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (14):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (14)$$

The characteristics of the output capacitor affect the stability of the regulation system. The MP2499A can be optimized for a wide range of capacitance and ESR values.

BST Resistor and External BST Diode

A 20Ω resistor in series with the BST capacitor is recommended to reduce SW voltage spikes. A higher resistance is better for SW spike reduction but compromises efficiency.

An external BST diode can enhance the efficiency of the regulator when the duty cycle is high (>65%). A power supply between 2.5 - 5V can be used to power the external bootstrap diode. VCC or VOUT is recommended for this power supply in the circuit (see Figure 8).

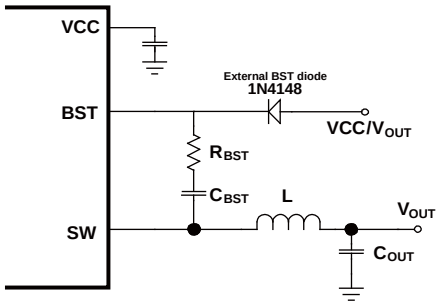

Figure 8: Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is IN4148, and the recommended BST capacitor value is 0.1 - 1µF.

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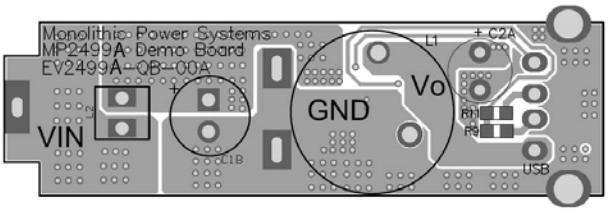
PCB Layout Guidelines [7]

Efficient PCB layout is critical for stable operation, especially for the input capacitor and VCC capacitor placement. For best results, refer to Figure 9 and follow the guidelines below.

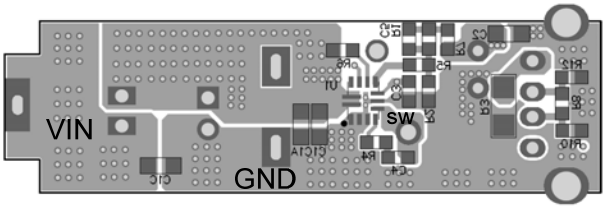
1. Place the ceramic input capacitors as close to IN and PGND as possible.
2. Keep the connection of the input capacitor and IN as short and wide as possible.
3. Place the VCC capacitor as close to VCC and AGND as possible.
4. Make the trace length of the VCC pin to the VCC capacitor anode to the VCC capacitor cathode to the chip's AGND pin as short as possible.
5. Use a large ground plane to connect to PGND directly.
6. Add vias near PGND if the bottom layer is a ground plane.
7. Route SW and BST away from sensitive analog areas such as FB.
8. Place the feedback resistor close to the chip to ensure that the trace connecting to FB is as short as possible.

NOTE:

7) The recommended layout is based on the Typical Application Circuit shown in Figure 10.



Top Layer



Bottom Layer

Figure 9: Recommended Layout

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TYPICAL APPLICATION CIRCUIT

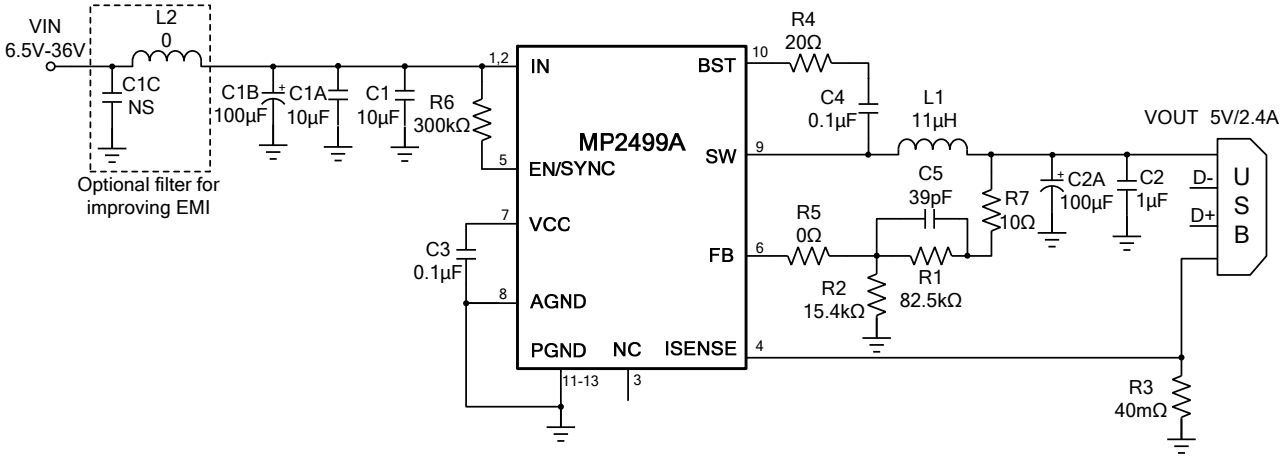

Figure 10: CLA Typical Application Circuit

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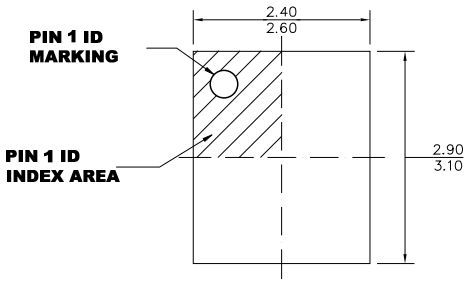
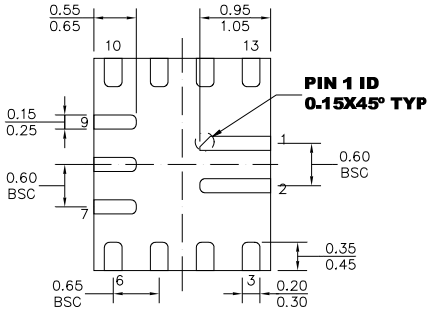
PACKAGE INFORMATION

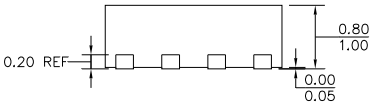
QFN-13 (2.5mmx3mm)



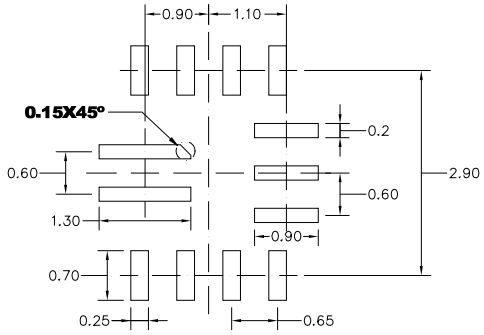
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

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2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
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