MP2499

Integrated 100V Load Dump Protection 2A, 100kHz Step Down Regulator with Programmable Output Current

END OF LIFE

DESCRIPTION

The MP2499 is a monolithic step-down switch mode converter with a programmable output current limit and an integrated input over-voltage protection switch. It achieves 2.0A continuous output current over a wide input supply range with excellent load and line regulation.

The maximum output current can be programmed by sensing current through the inductor DC resistance (DCR) or an accurate sense resistor.

Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown.

The MP2499 can survive high-voltage transients such as those found in automotive and industrial applications.

The MP2499 requires a minimum number of readily available standard external components. The MP2499 is available in a 16-pin SOIC package.

FEATURES

- Replaces External Transorb
- Supports 12V/24V Systems
- Input Surge Protection Up to 100V
- Programmable Output Current up to 2.0A
- Output Adjustable
- Fixed 100kHz Frequency
- 0.25Ω Internal Power MOSFET Switch
- Stable with Low ESR Output Ceramic Capacitors
- 92% Efficiency @ 500mA (Vo=5V)
- Thermal Shutdown
- Cycle-by-Cycle Over Current Protection
- Available in a 16-Pin SOIC Package

APPLICATIONS

- 12V/24V Systems with High Input Surge
- Automotive Cigarette Lighter Adapters
- Power Supply for Linear Chargers
- Industrial Power Supplies
- Avionics

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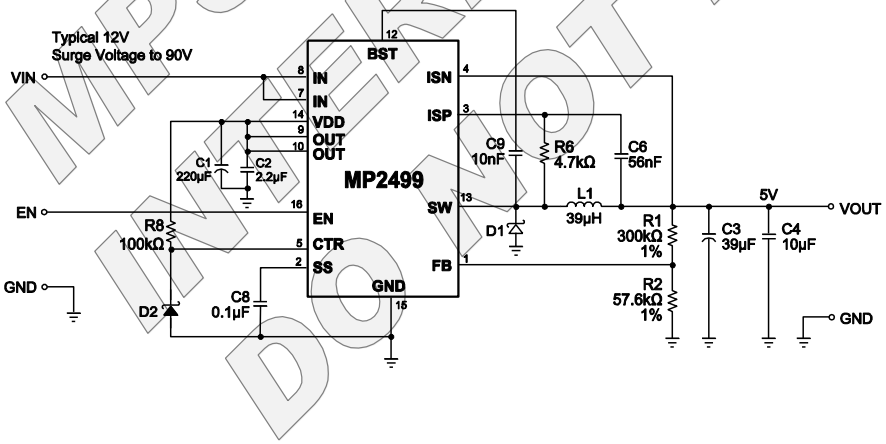
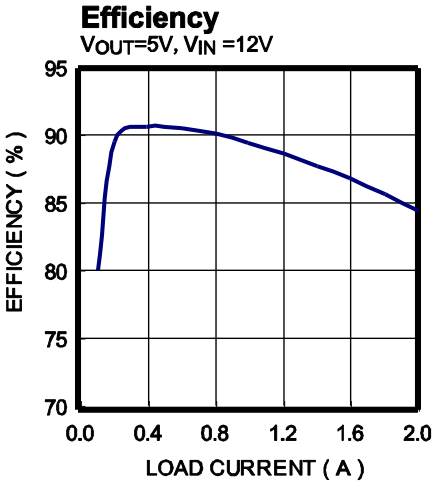
TYPICAL APPLICATION





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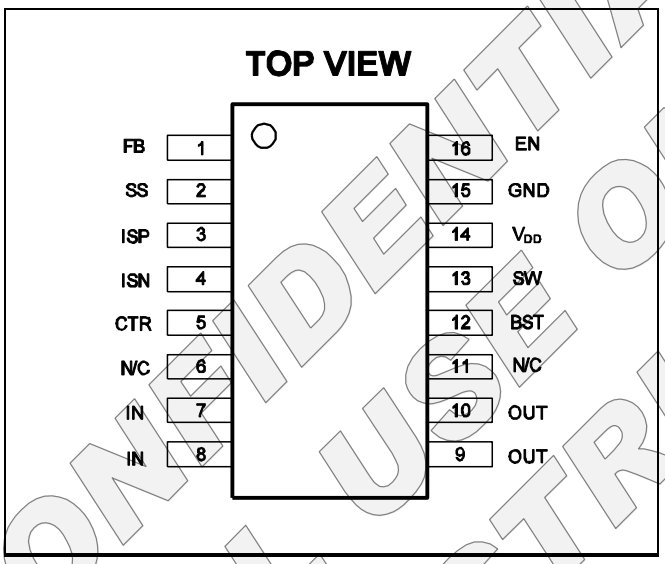
ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature (T_A)
MP2499DS	SOIC16	MP2499DS	–40°C to +85°C

* For Tape & Reel, add suffix –Z (e.g. MP2499DS–Z).

For RoHS compliant packaging, add suffix –LF (e.g. MP2499DS–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage IN 100V
IN to CTR..... -0.3V to 100V
OUT to CTR..... -0.3V to 45V
V_{DD} 58V
V_{SW} ..... –0.3V to V_{DD} + 0.3V
V_{BST} ..... V_{SW} + 6.5V
V_{ISN}, V_{ISP} 0V to15V
All Other Pins..... –0.3V to +6.5V
Continuous Power Dissipation (T_A = +25°C) (2) 1.6W
Junction Temperature..... 150°C
Lead Temperature ..... 260°C
Storage Temperature..... –65°C to +150°C

Recommended Operating Conditions (3)

Car Battery Input Voltage ..... 12V to 24V
Surge Voltage V_{IN} ..... 90V/200ms duration
V_{DD} 55V
Output Voltage V_{OUT} ..... 3.3V to 5V
Operating Junct. Temp (T_J)..... –40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}
SOIC16	80	30 ...°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Feedback Voltage	V_{FB}	4.5V ≤ V_{IN} ≤ 36V	0.78	0.8	0.82	V
Feedback Bias Current	$I_{BIAS(FB)}$	V_{FB} = 0.8V		10		nA
PWM Switch On Resistance	$R_{DS(ON)}$			0.25		Ω
OV Protection Switch On Resistance		V_{OUT} = V_{CTR}		0.3		Ω
Switch Leakage		V_{EN} = 0V, V_{SW} = 0V		0.1	10	μA
Current Limit				3.0		A
Oscillator Frequency	f_{SW}	V_{FB} = 0.6V	80	100	120	kHz
Boot-Strap Voltage	V_{BST} - V_{SW}			4.3		V
Minimum On Time	t_{ON}	V_{FB} = 1V		100		ns
Under Voltage Lockout Threshold Rising			3.0	3.3	3.6	V
Under Voltage Lockout Threshold Hysteresis				200		mV
EN Input Low Voltage (5)					0.4	V
En Input High Voltage (5)			1.8			V
EN Input Bias Current (5)		V_{EN} = 0-6V	–10	–2	10	μA
Supply Current (Shutdown)		V_{EN} = 0V		4	10	μA
Supply Current (Quiescent)		V_{EN} = 2V, V_{FB} = 1V		500	800	μA
Thermal Shutdown(5)				150		°C
Current Sense Voltage	V_{ISP} –V_{ISN}	V_{ISP}, V_{ISN} 0.4–15V	90	100	110	mV
Input Bias Current (ISN, ISP)	$I_{BIAS\ (ISN,ISP)}$	V_{ISP}, V_{ISN} 0.4–15V	–1	0.5	+1	μA

Note:

5) Guaranteed by design

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PIN FUNCTIONS

PIN #	Name	Description
1	FB	Feedback. An external resistor divider from the output to GND, tapped to the FB pin sets the output voltage. To prevent current limit run away during a short circuit fault condition the frequency-fold-back comparator lowers the oscillator frequency when the FB voltage is below 250mV.
2	SS	Connect to an external capacitor used for Soft-Start and compensation for current limiting loop.
3	ISP	Positive Current Sense
4	ISN	Negative Current Sense Input for load current limiting.
5	CTR	Control pin. Tie a zener diode from CTR to ground. The zener voltage should equal to normal output voltage.
6	N/C	No connection
7	IN	Input. Connect input power supply, which may have surge voltage to IN pin.
8	IN	Input. Connect input power supply, which may have surge voltage to IN pin.
9	OUT	Output Pin. Connect to VDD pin.
10	OUT	Output Pin. Connect to VDD pin.
11	N/C	No connection
12	BST	Bootstrap. This capacitor is needed to drive the power switch's gate above the supply voltage. It is connected between SW and BST pins to form a floating supply across the power switch driver. An on-chip regulator is used to charge up the external bootstrap capacitor. If the on-chip regulator is not strong enough, an optional diode can be connected from IN or OUT to charge the external bootstrap capacitor.
13	SW	Switch Output. It is the source of power device.
14	VDD	Supply Voltage Bypass pin. This pin is also the output of the OV protection switch. The MP2499 operates from a +5V to +36V unregulated input. CIN is needed to prevent large voltage spikes from appearing at the input. Put CIN as close to the IC as possible. It is the drain of the internal power device and power supply for the whole chip.
15	GND	Ground. This pin is the voltage reference for the regulated output voltage. For this reason care must be taken in its layout. This node should be placed outside of the D1 to CIN ground path to prevent switching current spikes from inducing voltage noise into the part.
16	EN	On/Off Control Input.

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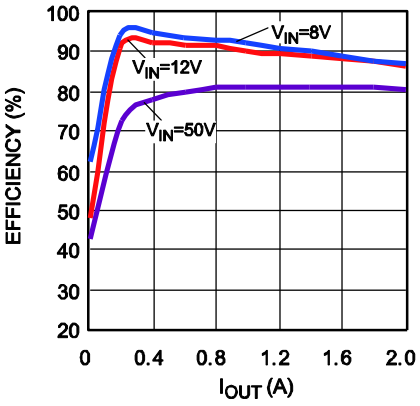
TYPICAL PERFORMANCE CHARACTERISTICS

C_1=220µF, C_2=2.2µF, C_3=39µF, C_4=22µF, L=39µH, V_{OUT}=5V, T_A=25°C, unless otherwise noted.

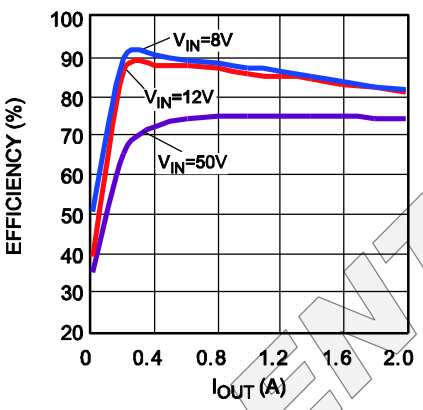
Efficiency vs. Load Current

V_{OUT}=5V



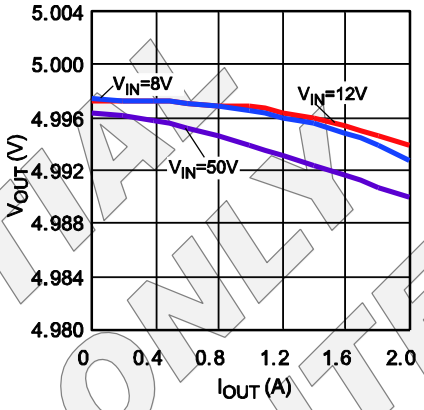
Efficiency vs. Load Current

V_{OUT}=3.3V

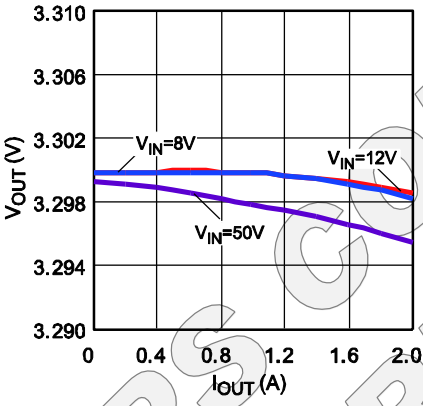


Load Regulation

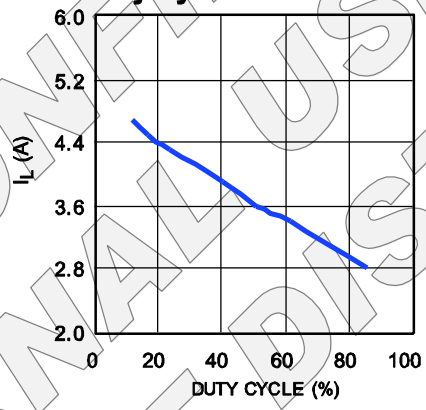
V_{OUT}=5V



Load Regulation

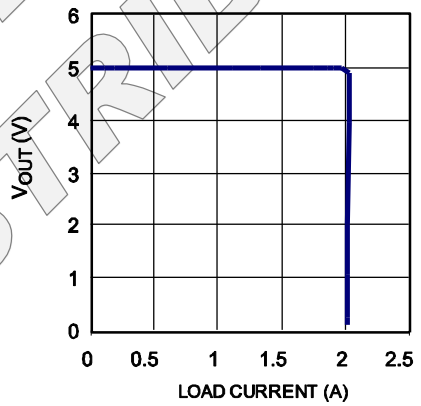


Peak Current Limit vs. Duty Cycle



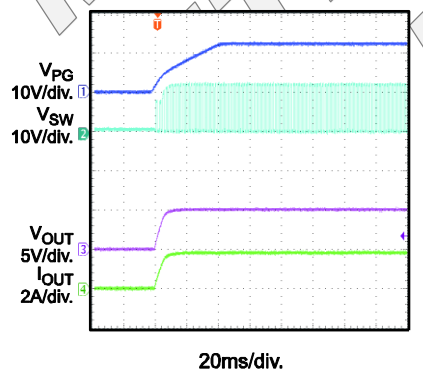
Current Regulation

Sense DCR



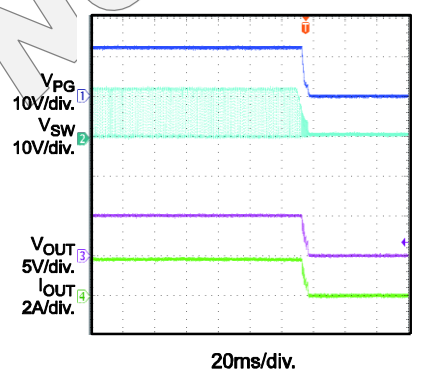
Power Ramp Up

V_{IN} =12V, I_{OUT}=2A, Resistor Load



Power Ramp Down

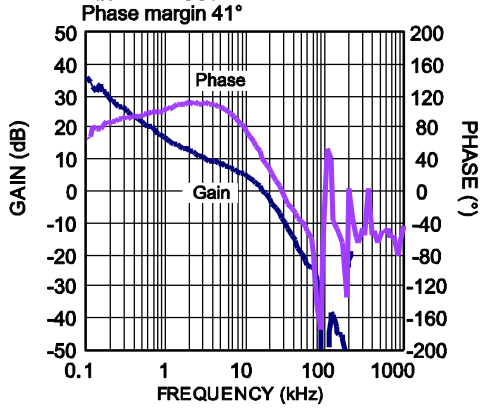
V_{IN} =12V, I_{OUT}=2A, Resistor Load



Loop Gain with Phase Margin

V_{IN} =12V, I_{OUT}=1.8A, 0dB Frequency 17kHz

Phase margin 41°



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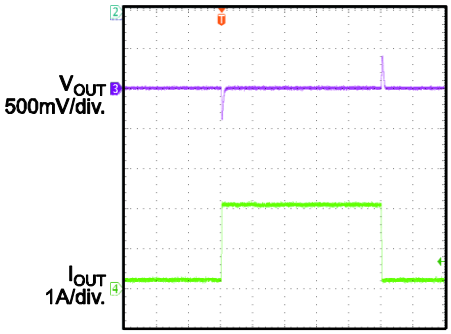
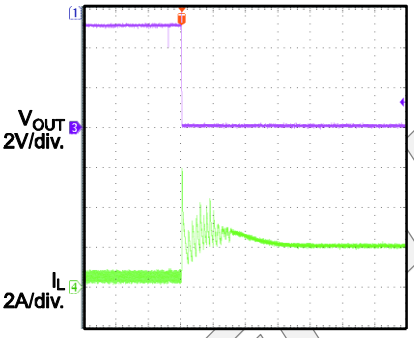
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

C_1=220µF, C_2=2.2µF, C_3=39µF, C_4=22µF, L=39µH, V_{OUT}=5V, T_A=25ºC, unless otherwise noted.

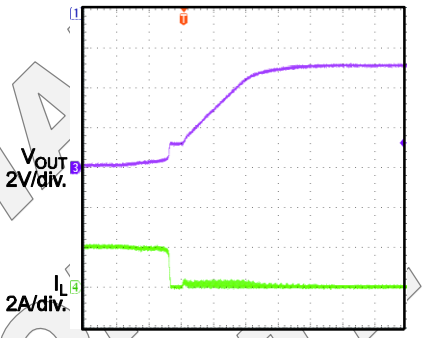
Load Transient Response
V_{IN}=12V, I_{OUT}=0.1A to 2A,
Electrical Load



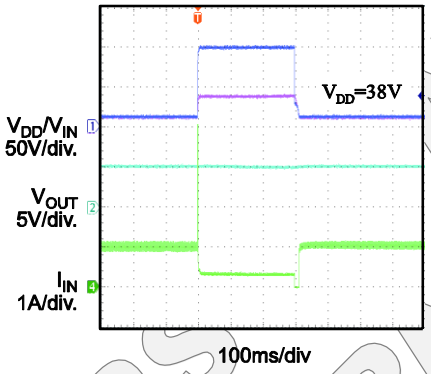
Short Circuit
V_{IN}=12V, I_{OUT}=0.5A



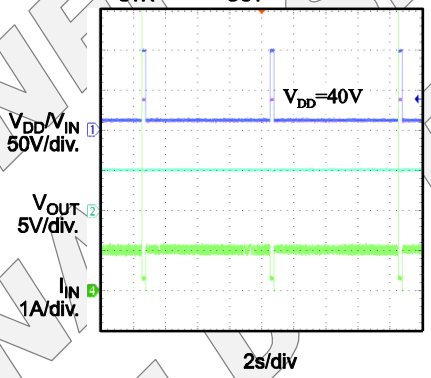
Short Circuit Recovery
V_{IN}=12V



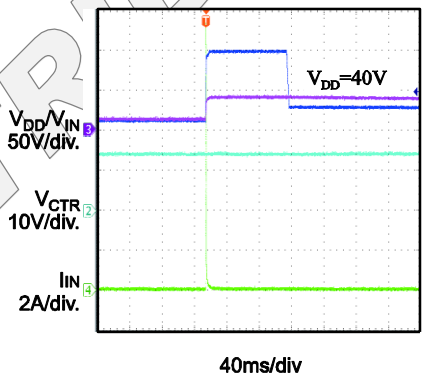
100V Input Single Pulse
V_{IN}=12V plus 100V/300ms pulse.
V_{CTR}=12V, I_{OUT}=2A Load



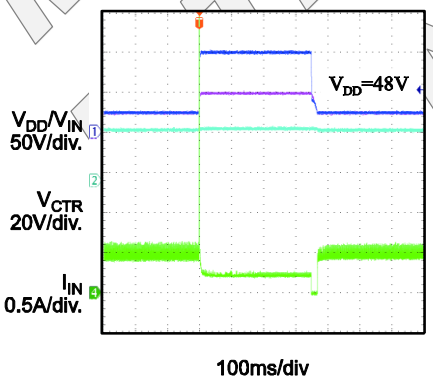
100V Continuous Input Pulse
V_{IN}=12V, D=0.2s, T=0.125s
Continuous pulse.
V_{CTR}=12V, I_{OUT}=2A Load



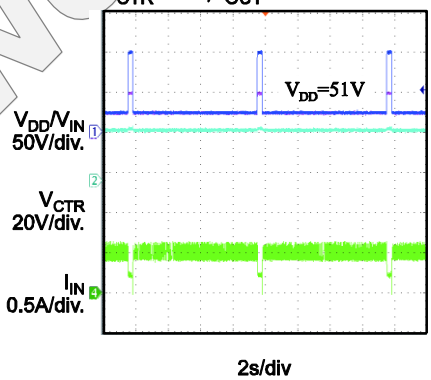
100V Input Single Pulse
V_{IN}=12V plus 100V/100ms pulse.
V_{CTR}=12V, No Load



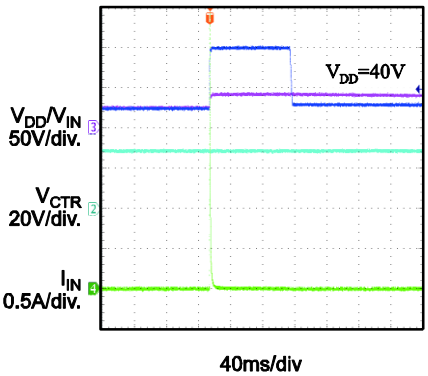
100V Input Single Pulse
V_{IN}=24V plus 100V/300ms pulse.
V_{CTR}=24V, I_{OUT}=2A Load



100V Continuous Input Pulse
V_{IN}=24V, D=0.3s, T=0.125s
Continuous pulse.
V_{CTR}=24V, I_{OUT}=2A Load



100V Input Single Pulse
V_{IN}=24V plus 100V/300ms pulse.
V_{CTR}=24V, No Load



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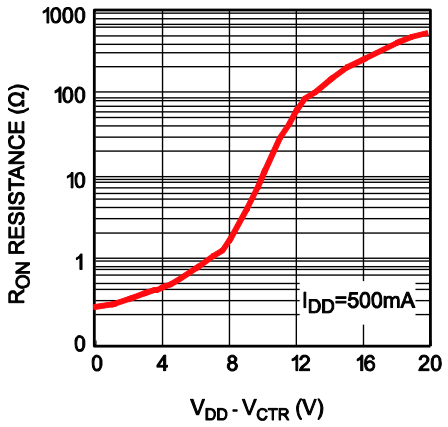
END OF LIFE

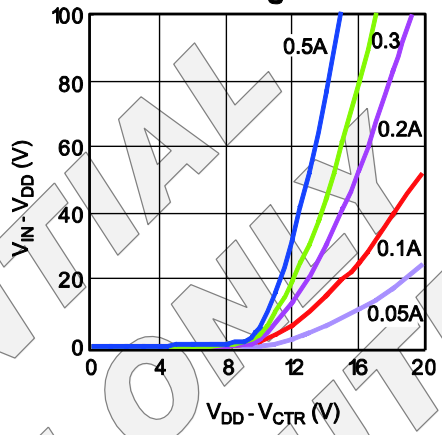
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

C_1=220µF, C_2=2.2µF, C_3=39µF, C_4=22µF, L=39µH, V_{OUT}=5V, T_A=25°C, unless otherwise noted.

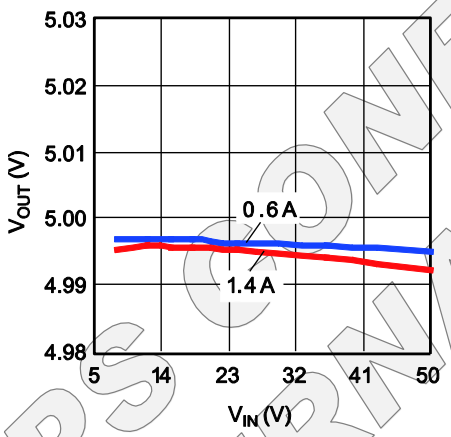
Protector On Resistance



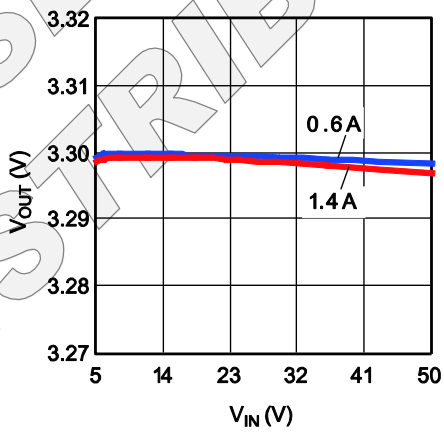
Clamp Voltage vs. Control Voltage



5V Line Regulation



3.3V Line Regulation



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OPERATION

Main Control Loop

The MP2499 is a current mode buck regulator. That is, the error amplifier (EA) output voltage is proportional to the peak inductor current.

At the beginning of a cycle, the integrated high side power switch M1 (Fig.1) is off; the EA output voltage is higher than the current sense amplifier output; and the current comparator's output is low. The rising edge of the 100kHz clock signal sets the RS Flip-Flop. Its output turns on M1 thus connecting the SW pin and inductor to the input supply.

The increasing inductor current is sensed and amplified by the Current Sense Amplifier. Ramp compensation is added to Current Sense Amplifier output and compared to the Error Amplifier output by the PWM Comparator. When the Current Sense Amplifier plus Slope Compensation signal exceeds the EA output voltage, the RS Flip-Flop is reset and the MP2499 reverts to its initial M1 off state.

If the Current Sense Amplifier plus Slope Compensation signal does not exceed the COMP voltage, then the falling edge of the CLK resets the Flip-Flop.

The output of the Error Amplifier integrates the voltage difference between the feedback and the 0.8V bandgap reference. The polarity is such that a FB pin voltage lower than 0.8V increases the EA output voltage. Since the EA output voltage is proportional to the peak inductor current, an increase in its voltage increases current delivered to the output. An external Schottky Diode (D1) carries the inductor current when M1 is off.

Load Current Limiting Loop

The output current information is sensed via the ISP and ISN pins. The regulation threshold is set at 100mV. If V_{SENSE}, the difference of V_{ISP} and V_{ISN}, is less than 100mV, the output voltage of the power supply will be set by the FB pin. If V_{SENSE} reaches 100mV, the current limit loop will pull down SS and regulate the output at a constant current determined by the external sense resistor. The external capacitor on SS pin is the dominant compensation capacitor for load current regulation loop. The capacitor has normal value of 100nF, which will put the bandwidth of load current regulation loop to be less than 1kHz. When V_{SENSE} is higher than 100mV, SS will not drop down to the final regulation level immediately. It will cause the load current to be higher than the programmed level for a short period. A fast comparator is added to shut down power switch when the average load current is higher than 120% of the programmed current limit level.

An inductor DC resistance (DCR) or accurate sense resistor can be used for load current sensing.

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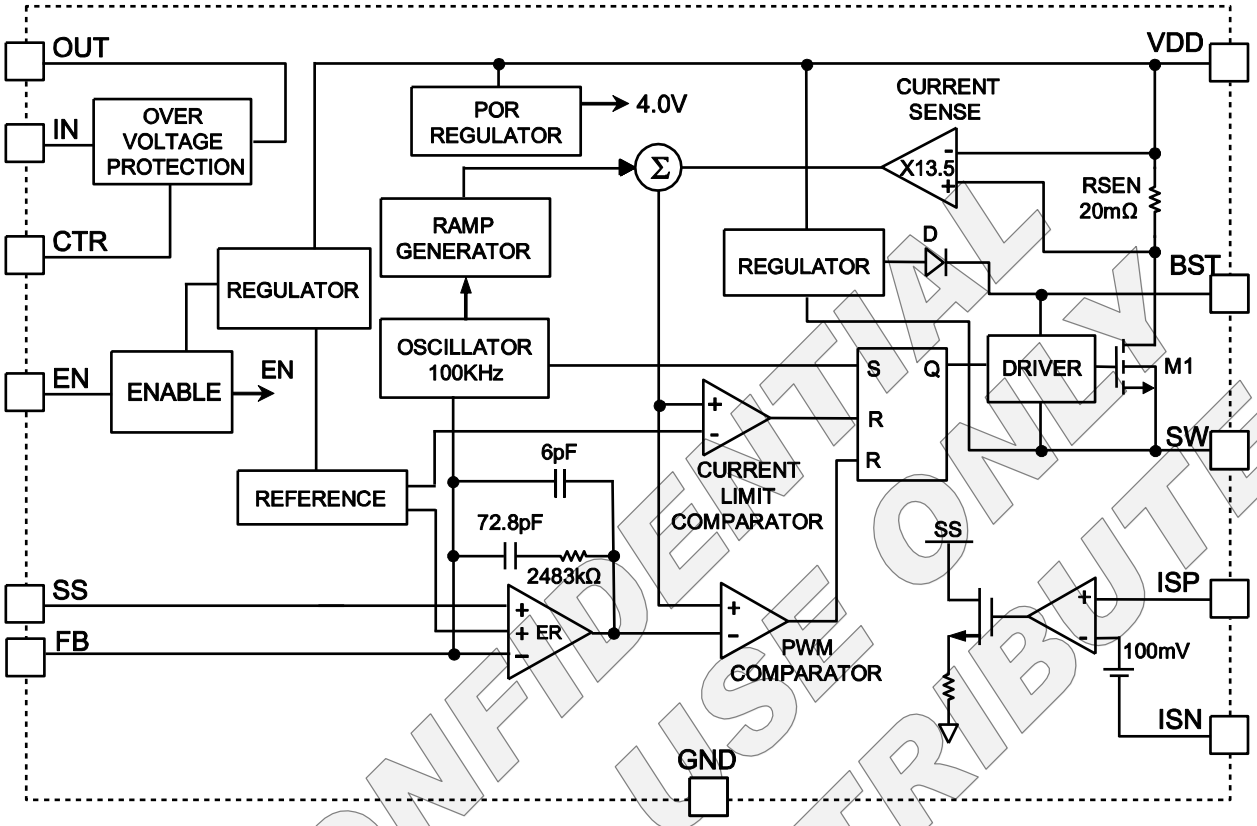

Figure 1—Function Block Diagram

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APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see the schematic on front page). The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor (see Figure 1). Choose R1 to be around 300kΩ for optimal transient response. R2 is then given by:

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.8V} - 1}$$

Table 1—Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.8	300 (1%)	240 (1%)
2.5	300 (1%)	141.1(1%)
3.3	300 (1%)	96 (1%)
5	300 (1%)	57.1 (1%)

Selecting the Inductor

A 33µH to 47µH inductor with a DC current rating of at least 25% percent higher than the maximum load current is recommended for most applications. For highest efficiency, the inductor DC resistance should be less than 200mΩ. For most designs, the inductance value can be derived from the following equation.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{SW}}$$

Where ΔI_L is the inductor ripple current.

Choose inductor current ripple to be approximately 30% of the maximum load current,. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency.

Selecting the Input Capacitor

The input capacitor reduces the surge current drawn from the input and also the switching noise from the device. The input capacitor impedance at the switching frequency should be less than the input source impedance to prevent high frequency switching current from pass to the input. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 220µF electrolytic capacitor is sufficient.

Selecting the Output Capacitor

The output capacitor keeps output voltage small and ensures regulation loop stability. The output capacitor impedance should be low at the switching frequency. Ceramic capacitors with X5R or X7R dielectrics are recommended.

Selecting D2 Diode

The D2 Zener diode voltage is a reference voltage to control the clamp voltage of the OVP protection during a surge condition to choose the Zener voltage to be the same as the input voltage to reduce any OVP protection losses.

Refer to the typical operation curve on page 6 titled “Clamp Voltage vs. VDD-VCTR” to make sure the VDD voltage doesn’t exceed the maximum input voltage, when a surge voltage is applied to the OVP protection.

Selecting Soft Start Capacitor

MP2499 has external soft start function. This external function reduces the start up current surge into the output capacitor. This allows the gradual built up of output voltage to its final set value. The soft start time is decided by following equation:

$$T_{SS} = \frac{0.7 \times C_{SS}}{39 \times 10^{-6}}$$

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Output Current Sensing

The output current can be sensed through the DC resistance (DCR) of the inductor, as shown in Figure 2a.

In Figure 2a, the output current limit is set as:

$$I_{OUT} = \frac{100mV}{DCR} \times \frac{R_a + R_b}{R_b}$$

Where DCR is the DC resistance of the inductor winding.

In Figure 2a, it is desirable to keep

$$\frac{R_a \cdot R_b}{R_a + R_b} \times C_S = \frac{L1}{DCR}$$

For more accurate sensing, use a more accurate (1% or less) sense resistor, as in Figure 2b, where the output current limit is set as:

$$I_{OUT} = \frac{100mV}{R_{SENSE}}$$

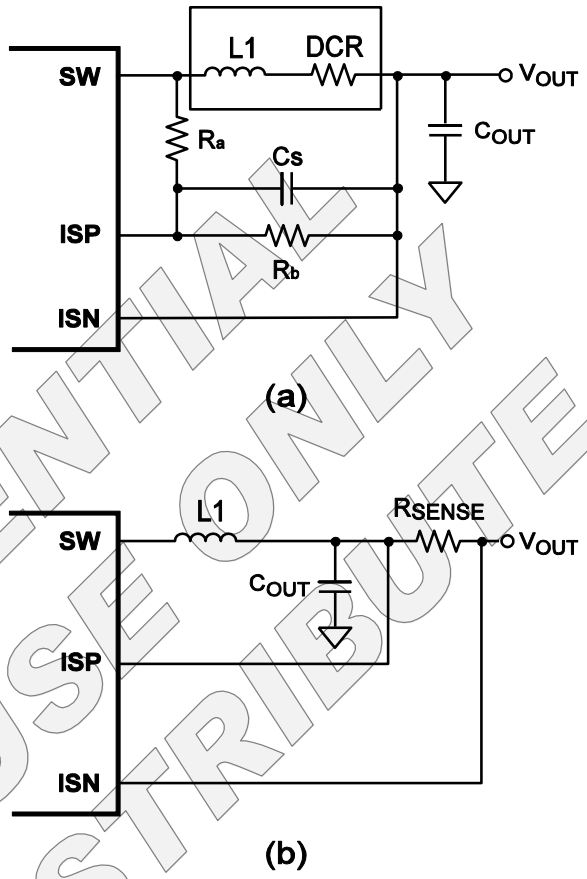

Figure 2—Current Sensing Methods

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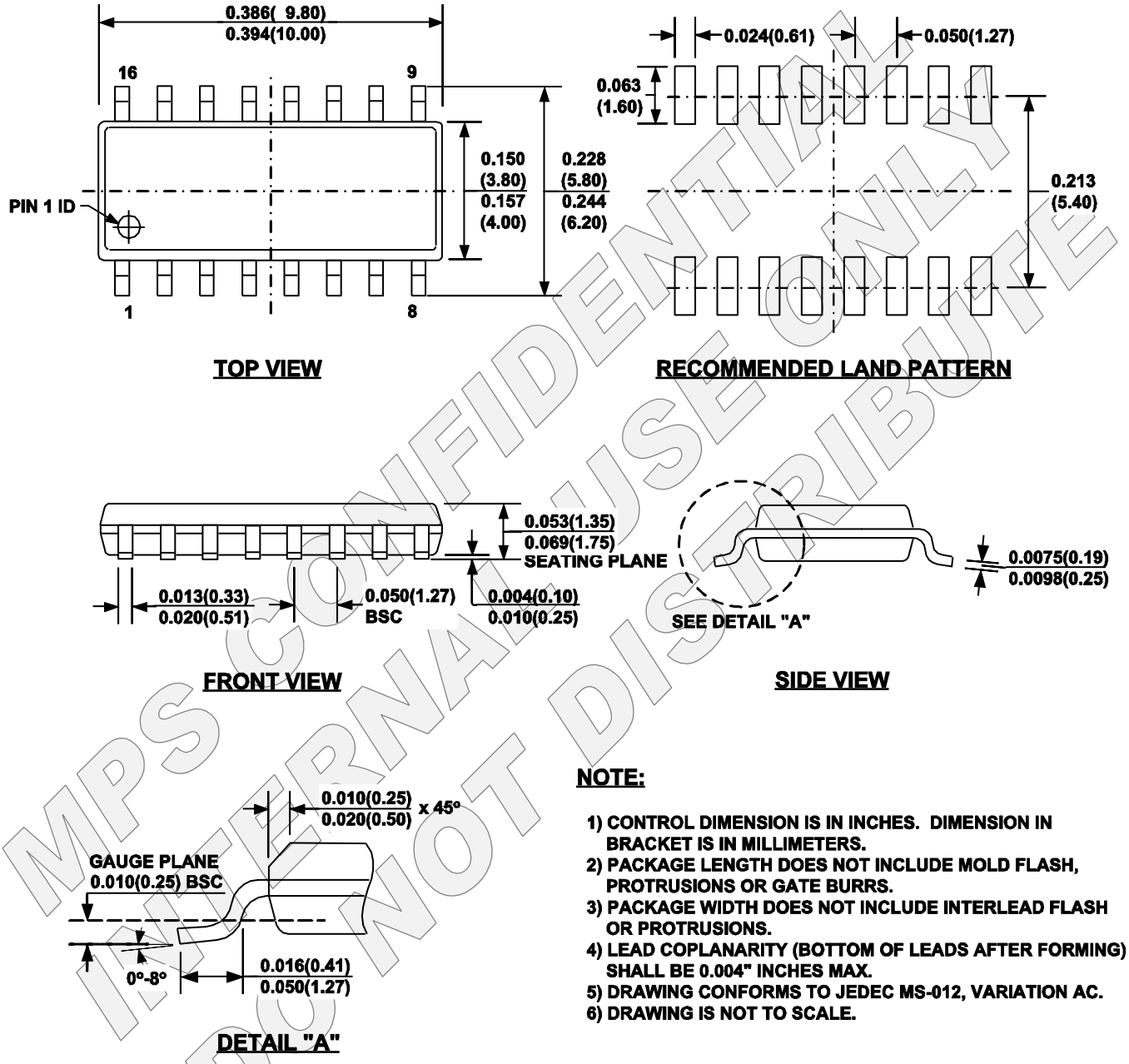
PACKAGE INFORMATION

SOIC16



NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AC.
6) DRAWING IS NOT TO SCALE.

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