MP2497-A

3A, 50V, 100kHz Step-Down Converter with Programmable Output OVP Threshold

The Future of Analog IC Technology

DESCRIPTION

The MP2497-A is a monolithic step-down switch mode converter with a programmable output current limit. The MP2497-A is the high efficiency version of MP2497. It has fast switching speed thus the switching loss is greatly reduced. It achieves 3A continuous output current over a wide input supply range with excellent load and line regulation. An internal 2-4ms soft start prevents inrush current at turning on. And it is capable of providing output line drop compensation.

Fault condition protection includes hiccup current limit and short circuit protection, programmable output over voltage protection and thermal shutdown.

The MP2497-A requires a minimum number of readily available standard external components. The MP2497-A is available in SOIC8E package.

FEATURES

- Wide 4.5V to 50V Operating Input Range
- Programmable Output Over Voltage Protection
- Output Adjustable from 0.8V to 25V
- 0.15Ω Internal Power MOSFET Switch
- Internal 4ms Soft Start
- Stable with Low ESR Output Ceramic Capacitors
- Fixed 100kHz Frequency
- Fast Switching Speed
- Thermal Shutdown
- Output Line Drop Compensation
- Hiccup Circuit Limit and Short Circuit Protection
- Available in SOIC8E Package

APPLICATIONS

- USB Power Supplies
- Automotive Cigarette Lighter Adapters
- Power Supply for Linear Chargers

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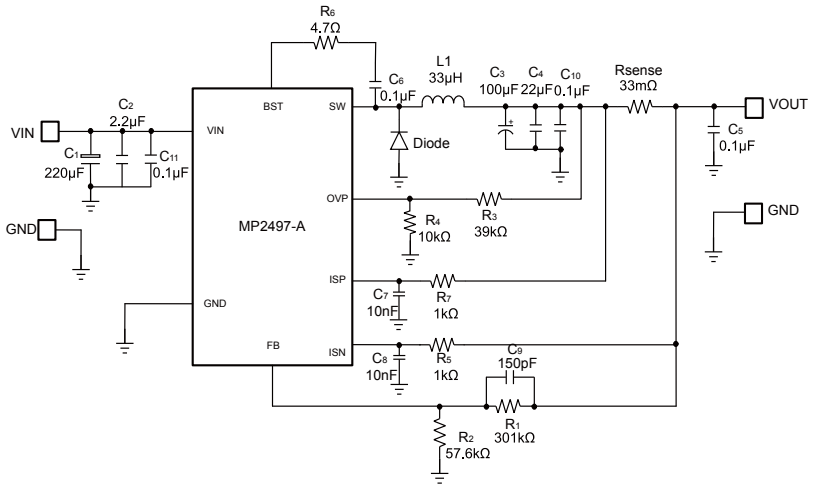
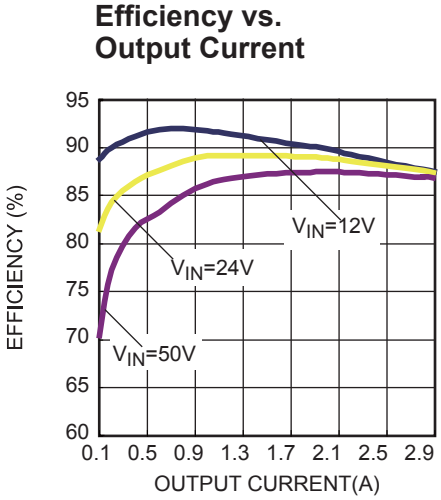
TYPICAL APPLICATION





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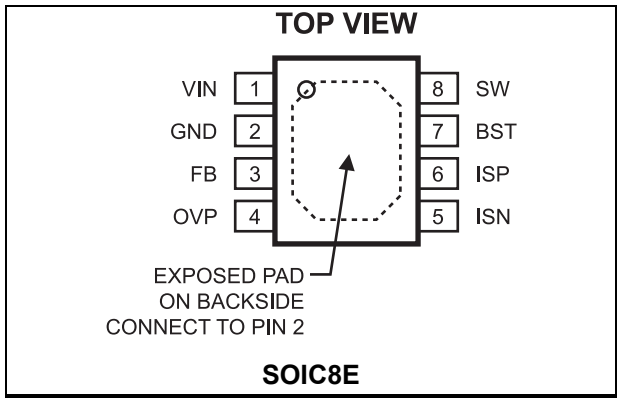
ORDERING INFORMATION

Part Number	Package	Top Marking
MP2497GN-A*	SOIC8E	MP2497-A

* For Tape & Reel, add suffix –Z (e.g. MP2497GN-A–Z);

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Input Voltage V_{IN} 60V
V_{ISN}, V_{ISP} ..... 0V to 25V
$|V_{ISN} - V_{ISP}|$ ..... 0V to 0.4V
V_{SW} ..... -0.3V to V_{IN} + 0.3V
V_{BST} ..... V_{SW} + 6.5V
All Other Pins ..... -0.3V to +6.5V
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... -65°C to +150°C
Continuous Power Dissipation (T_A = +25°C) (2)
SOIC8E 2.5W

Recommended Operating Conditions (3)

Input Voltage V_{IN} ..... 4.5V to 50V
Output Voltage V_{OUT} (V_{IN}>26.5V) ..... 0.8V to 25V
Output Voltage V_{OUT} (V_{IN}<=26.5V) .....
..... 0.8V to (V_{IN}–1.5)V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

SOIC8E ..... 50 ..... 10... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Feedback Voltage	V_{FB}	T_A=+25°C 4.5V ≤ V_{IN} ≤ 50V	0.78	0.8	0.82	V
		T_A=-40°C to +85°C 4.5V ≤ V_{IN} ≤ 50V	0.775	0.8	0.825	
Feedback Bias Current	$I_{BIAS(FB)}$	V_{FB} = 0.8V		10		nA
Output Over Voltage Reference	V_{OVREF}	T_A=-40°C to +85°C	1.10	1.23	1.36	V
Input Bias Current (OVP)	$I_{BIAS(OVP)}$	V_{OVP}=1.23V		0.1		µA
Switch On Resistance	$R_{DS(ON)}$			0.15		Ω
Current Limit(5)		Duty Cycle=10%		5		A
Oscillator Frequency	f_{SW}	V_{FB} = 0.6V	80	100	120	kHz
Boot-Strap Voltage	V_{BST} - V_{SW}			4.5		V
Minimum On Time(5)	t_{ON}			100		ns
SW Rising Edge(5)	t_{RISE}			3		ns
SW Falling Edge(5)	t_{FALL}			3		ns
Under Voltage Lockout Threshold Rising			2.9	3.4	3.9	V
Under Voltage Lockout Threshold Hysteresis				200		mV
Load Line Compensation Gain	G_{LLC}	V_{ISP}-V_{ISN}=100mV, check I_{FB}	15	20	25	µA/V
Current Sense Voltage	V_{ISP} –V_{ISN}	V_{ISP}, V_{ISN} 0.5–15V	90	100	110	mV
Input Bias Current (ISN, ISP)	$I_{BIAS (ISN,ISP)}$	V_{ISP}, V_{ISN} 0.5–15V	-1	-0.5	+1	µA
Supply Current (Quiescent)		V_{OVP} = 0V, V_{FB} = 1V		1.2	1.5	mA
Thermal Shutdown(5)				150		°C
Thermal Shutdown Hysteresis(5)				30		°C

Notes:

5) Guaranteed by design.

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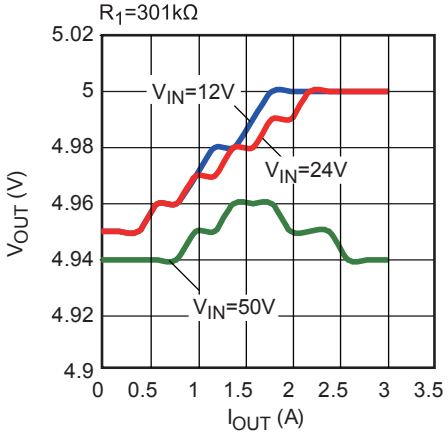
TYPICAL CHARACTERISTICS

C1=220µF, C2=2.2µF, C3=100µF, C4=22µF, L=33µH, R_{SENSE}=33mΩ, T_A=25ºC，unless otherwise noted.

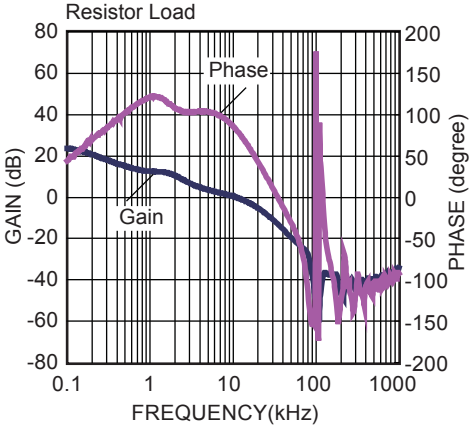
Output Line Drop Compensation

R_{SENSE}=25mΩ, R_{TRACE}=120mΩ
R_1=301kΩ

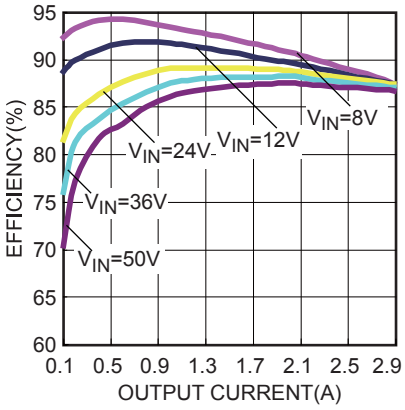


Loop Gain with Phase Margin

V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A
Resistor Load

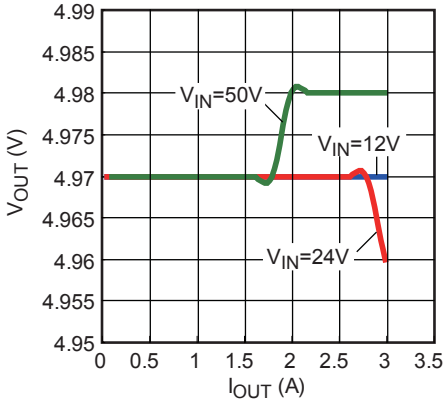


Efficiency vs. Output Current



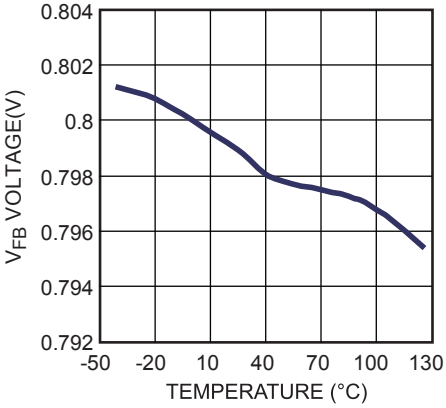
Load Regulation

Connect ISP, ISN to GND



V_{FB} vs. Temperature

V_{IN}=12V



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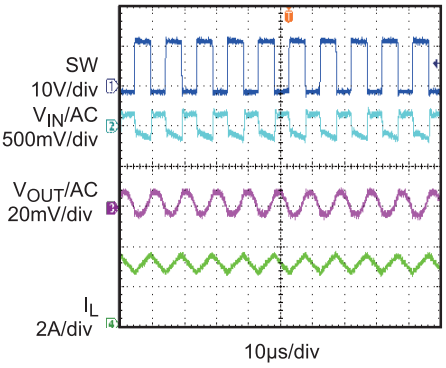
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

C1=220µF, C2=2.2µF, C3=100µF, C4=22µF, L=33µH, R_{SENSE}=33mΩ, T_A=25ºC，unless otherwise noted.

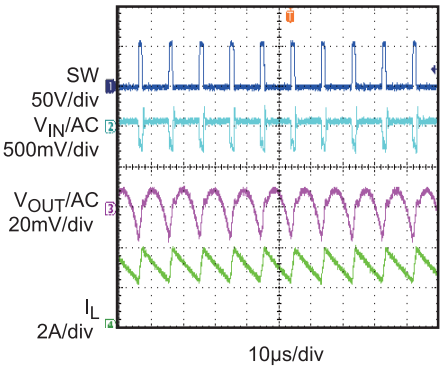
Steady State

V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A
E-Load



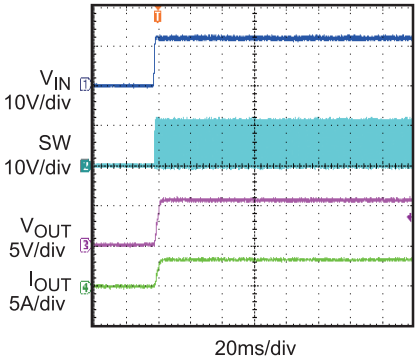
Steady State

V_{IN}=50V, V_{OUT}=5V, I_{OUT}=3A
E-Load



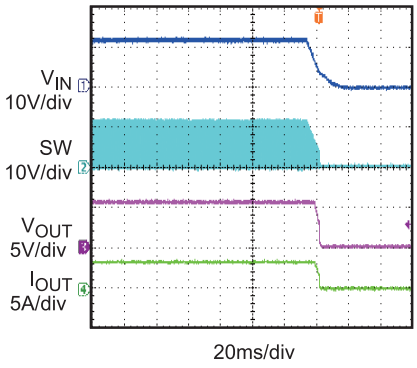
Power Ramp Up

V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A
Resistor Load



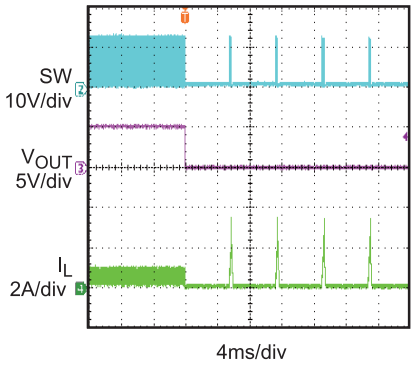
Power Ramp Down

V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A
Resistor Load



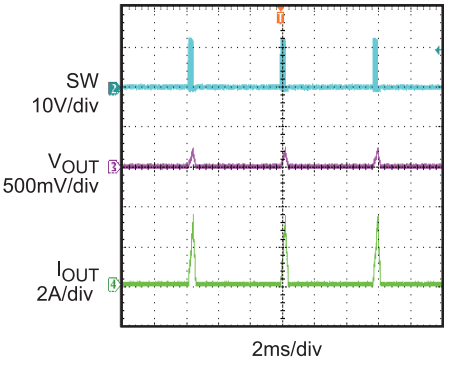
Short Circuit Enter

V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0.5A
E-Load



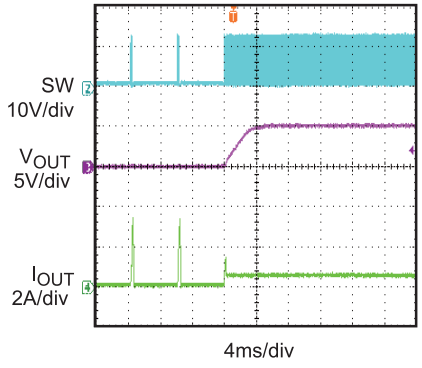
Short Circuit Steady

V_{IN}=12V, V_{OUT}=5V
E-Load



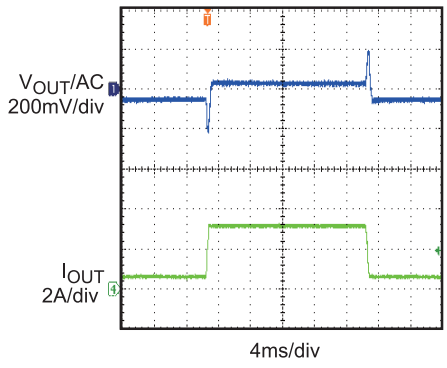
Short Circuit Recovery

V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0.5A
E-Load



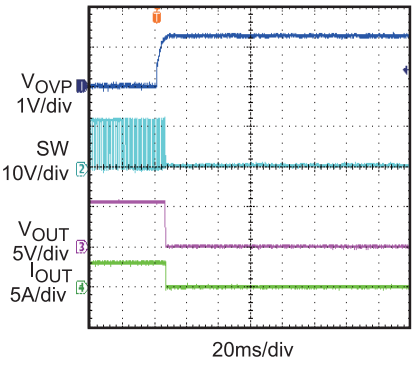
Load Transient Response

V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0.3A-3A
Slew Rate=6.4mA/µs



Over Voltage Protection

V_{IN}=12V, V_{OUT}=5V, I_{OUT}=3A
Add an External Power to OVP



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PIN FUNCTIONS

Package Pin #	Name	Description
1	VIN	Supply Voltage. The MP2497-A operates from a +4.5V to +50V unregulated input. C_{IN} is needed to prevent large voltage spikes from appearing at the input. Put C_{IN} as close to the IC as possible. It is the drain of the internal power device and power supply for the whole chip.
2	GND, Exposed Pad	Ground. This pin is the voltage reference for the regulated output voltage. For this reason care must be taken in its layout. This node should be placed outside of the D1 to C_{IN} ground path to prevent switching current spikes from inducing voltage noise into the part. Connect exposed pad to GND plane for optimal thermal performance.
3	FB	Feedback. An external resistor divider from the output to GND tapped to the FB pin sets the output voltage. To prevent current limit run away during a short circuit fault condition the frequency-fold-back comparator lowers the oscillator frequency when the FB voltage is below 250mV.
4	OVP	Output Over Voltage Protection. Connect OVP to the center point of an external resistor divider from output to GND. The OVP reference is 1.23V.
5	ISN	Negative Current Sense Input. It is used for load current limiting and output line drop compensation.
6	ISP	Positive Current Sense Input. It is used for load current limiting and output line drop compensation.
7	BST	Bootstrap. This capacitor is needed to drive the power switch's gate above the supply voltage. It is connected between SW and BST pins to form a floating supply across the power switch driver. An on-chip regulator is used to charge up the external boot-strap capacitor. If the on-chip regulator is not strong enough, one optional diode can be connected from IN or OUT to charge the external boot-strap capacitor.
8	SW	Switch Output. It is the source of power device.

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BLOCK DIAGRAM

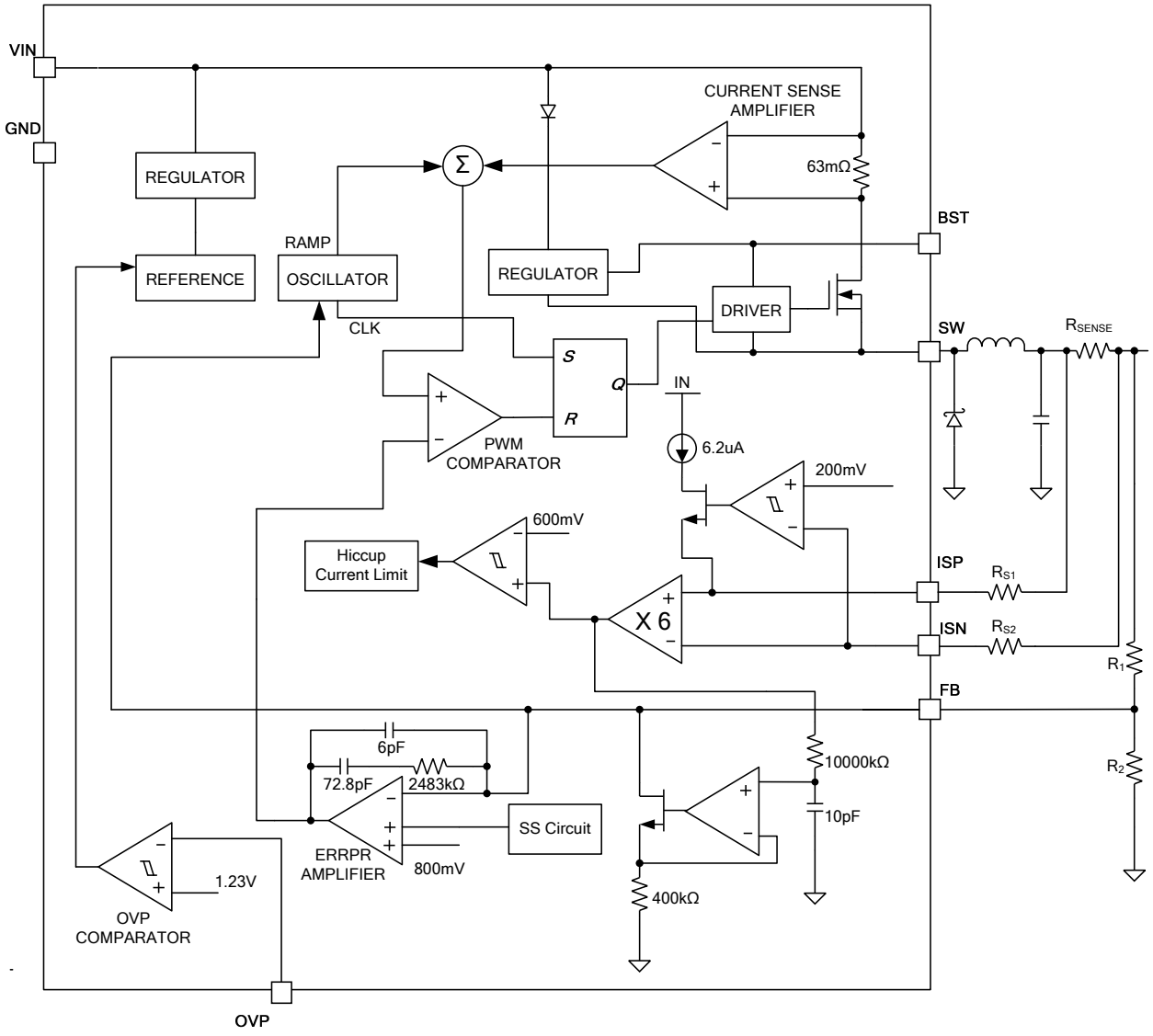

Figure 1—Functional Block Diagram

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OPERATION

Main Control Loop

The MP2497-A is a current mode buck regulator. That is, the EA output voltage is proportional to the peak inductor current.

At the beginning of a cycle SW is off; the Error Amplifier output voltage is higher than the Current Sense Amplifier output. The rising edge of the 100kHz CLK signal sets the RS Flip-Flop. Its output turns on SW thus connecting the SW pin and inductor to the input supply.

The increasing inductor current is sensed and amplified by the Current Sense Amplifier. Ramp Compensation is summed to Current Sense Amplifier output and compared to the Error Amplifier output by the PWM Comparator. When the Current Sense Amplifier plus Slope Compensation signal exceeds the Error Amplifier output voltage, the RS Flip-Flop is reset and the MP2497-A reverts to its initial SW off state.

If the Current Sense Amplifier plus Slope Compensation signal does not exceed the COMP voltage, then the falling edge of the CLK resets the Flip-Flop.

The output of the Error Amplifier integrates the voltage difference between the feedback and the reference. The polarity is such that an FB pin voltage is lower than 0.8V increases the EA output voltage. Since the EA output voltage is proportional to the peak inductor current, an increase in its voltage increases current delivered to the output. An external Schottky Diode (D1) carries the inductor current when SW is off.

Hiccup Mode Current Limit Protection

The output current information for current limit protection is sensed via the ISP and ISN pins. The sense voltage limit threshold is set at 100mV. MP2497-A has hiccup over current limit function. Once the V_{SENSE} exceeds the 100mV, the current limit loop will turn off high side switch immediately. Meanwhile, internal soft start circuit will be reset after FB is lower than 0.3V, and then the high side switch turns on and MP2497-A restarts with a full soft start. This hiccup process is repeated until the fault is removed. And, current limit value can be programmed to be lower by internal current source and external resistors connected to ISN and ISP pins, when output voltage is lower than 200mV. Then, the average short circuit current can be greatly reduced.

Output Over Voltage Protection

The MP2497-A has output over voltage protection. The OVP reference 1.23V is on the positive input of the OVP comparator. The output voltage is fed to OVP pin through an external resistor divider. If the voltage on OVP pin is higher than 1.23V, the high side switch will be turned off immediately and part will be lathed off after a timer delay.

Output Line Drop Compensation

If the trace from MP2497-A output terminator to the load is too long, there will be a voltage drop on the long trace which is variable with load current. MP2497-A is capable of compensating the output voltage drop to keep a constant voltage at load, whatever the load current is. The output voltage is compensated by feeding a current to the top feedback resistance R1. The load line compensation gain can be programmed according to R_{SENSE} and R_{TRACE} (Figure 2) values.

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APPLICATION INFORMATION

Setting the Output Line Drop Compensation

Figure 2 shows the block of output line drop compensation.

If the trace to the load is long, there is a voltage drop between V_{OUT} and V_{LOAD}. V_{OUT} (voltage at output terminator) is not equal to V_{LOAD}(voltage at load). The voltage drop can be described by:

$$V_{DROP} = I_{OUT} \times R_{TRACE} \quad (1)$$

Where, the R_{TRACE} is the resistance of the output line. ($R_{TRACE} = R_{TRACE1} + R_{TRACE2}$)

Then, the V_{LOAD} is:

$$V_{LOAD} = V_{OUT} - I_{OUT} \times R_{TRACE} \quad (2)$$

To keep an accurate and constant load voltage, the output line drop compensation is necessary.

MP2497-A offers a compensation method, by adjusting the FB voltage slightly according to the load current.

The relation between V_{OUT} and V_{FB} can be described by:

$$\frac{V_{OUT} - V_{FB}}{R1} = \frac{V_{FB}}{R2} + \frac{I_{OUT} \times R_{SENSE} \times 6}{400k\Omega} \quad (3)$$

Where, V_{FB} is 0.8V.

Then, the V_{OUT} can be calculated by:

$$V_{OUT} = (1 + \frac{R1}{R2}) \times 0.8V + \frac{I_{OUT} \times R_{SENSE} \times 6 \times R1}{400k\Omega} \quad (4)$$

The V_{LOAD} is determined by:

$$V_{LOAD} = (1 + \frac{R1}{R2}) \times 0.8V + \frac{I_{OUT} \times R_{SENSE} \times 6 \times R1}{400k\Omega} - I_{OUT} \times R_{TRACE} \quad (5)$$

To maintain the V_{LOAD} is not variable with load current. The equation below should be satisfied:

$$\frac{I_{OUT} \times R_{SENSE} \times 6 \times R1}{400k\Omega} = I_{OUT} \times R_{TRACE} \quad (6)$$

Simplify the formula above, we can get:

$$R1 = \frac{R_{TRACE} \times 400k\Omega}{6 \times R_{SENSE}} \quad (7)$$

In the formula above, R_{SENSE} is known. And R_{TRACE} can be tested or evaluated. So, we can select a proper top feedback resistor R1 according to the R_{TRACE} and R_{SENSE} to compensate the output line voltage drop.

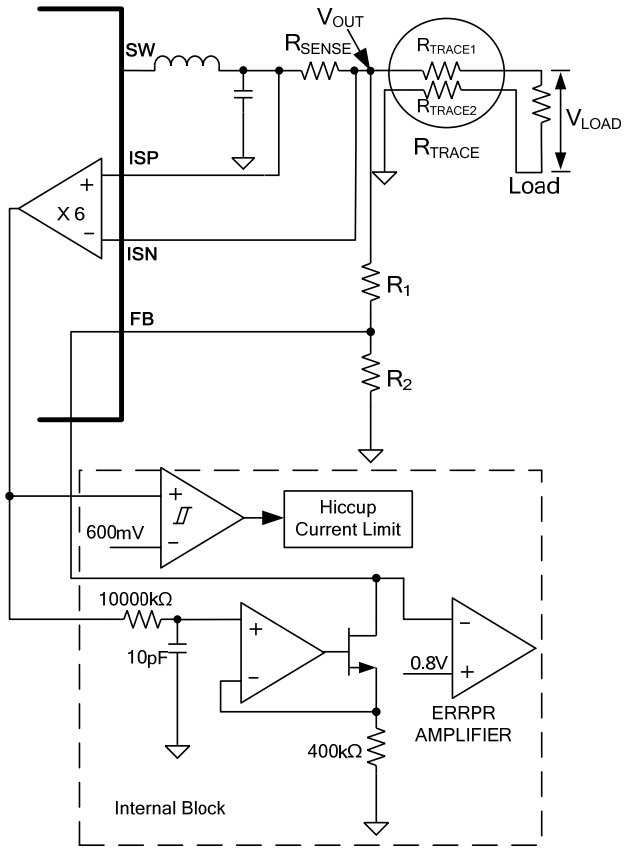

FIGURE 2—OUTPUT LINE DROP COMPENSATION

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see the typical application circuit on the front page). The feedback resistor R1 is decided by output line drop compensation. R2 is then given by:

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.8V} - 1} \quad (8)$$

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Selecting the Inductor

A 10μH to 47μH inductor with a DC current rating of at least 25% percent higher than the maximum load current is recommended for most applications. For highest efficiency, the inductor DC resistance should be less than 200mΩ. For most designs, the inductance value can be derived from the following equation.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (9)$$

Where ΔI_L is the inductor ripple current.

Choose inductor current ripple to be approximately 30% of the maximum load current, 3A. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (10)$$

Under light load conditions below 100mA, larger inductance is recommended for improving efficiency.

Selecting the Input Capacitor

The input capacitor reduces the surge current drawn from the input and also the switching noise from the device. The input capacitor impedance at the switching frequency should be less than the input source impedance to prevent high frequency switching current from passing to the input. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 4.7μF capacitor is sufficient.

Selecting the Output Capacitor

The output capacitor keeps output voltage small and ensures regulation loop stability. The output capacitor impedance should be low at the switching frequency. Ceramic capacitors with X5R or X7R dielectrics are recommended.

Setting the Output OVP Threshold

The output OVP threshold is set by connecting an external resistor divider (R3, R4 see the typical application circuit on the front page) at OVP pin. Choose R3 to be 39kΩ for lower power dissipation. Then, R4 is given by:

$$R4 = \frac{R3}{\frac{V_{OVP}}{V_{OVREF}} - 1} (k\Omega) \quad (11)$$

Where, V_{OVREF} is the OVP reference, 1.23V. V_{OVP} is over voltage protection threshold.

Setting the Current Limit

The hiccup current limit can be set by the DC resistance (DCR) of the inductor, as shown in Figure 3a.

For more accurate sensing, use a more accurate sense resistor.

In Figure 3a, the output current limit is set as:

$$I_{OUT_L} = \frac{100mV}{DCR} \quad (12)$$

Where, DCR is the DC resistance of the inductor winding. R_a and C_a is a low pass filter.

In Figure 3b, the output current limit is set as:

$$I_{OUT_L} = \frac{100mV}{R_{SENSE}} \quad (13)$$

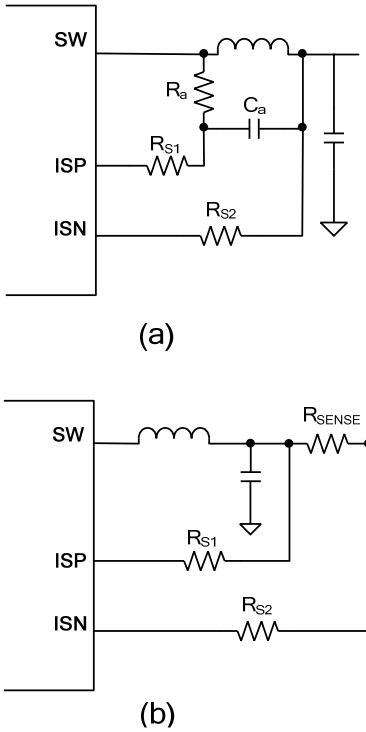

Figure 3—Current Sensing Methods

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Programming the Short Circuit Current Limit

The hiccup current limit at output short condition can be programmed to be lower by external resisters (R_{S1}, R_{S2}, R_{S1}=R_{S2}), as shown in figure 4.

When output voltage is lower than 200mV, the current limit is described by:

$$I_{OUT_SL} \times R_{SENSE} + 6.2\mu A \times R_{S1} = 100mV \quad (14)$$

The current limit at output short condition is:

$$I_{OUT_SL} = \frac{100mV - 6.2\mu A \times R_{S1}}{R_{SENSE}} \quad (15)$$

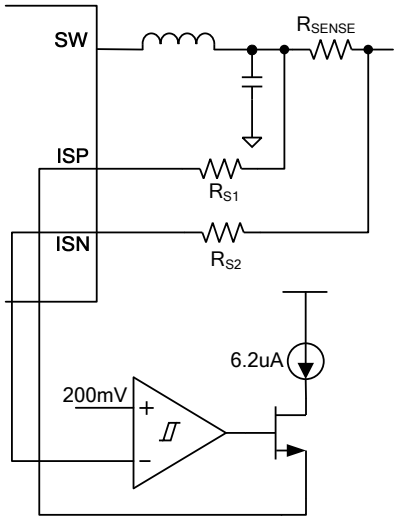


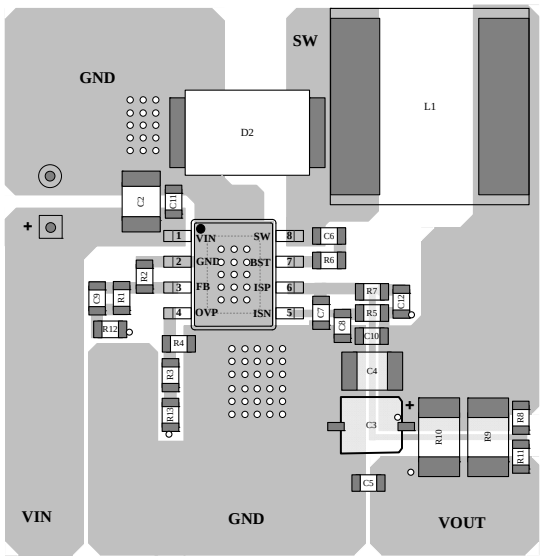
Figure 4—Short Circuit Current Limit

PCB Layout Guide

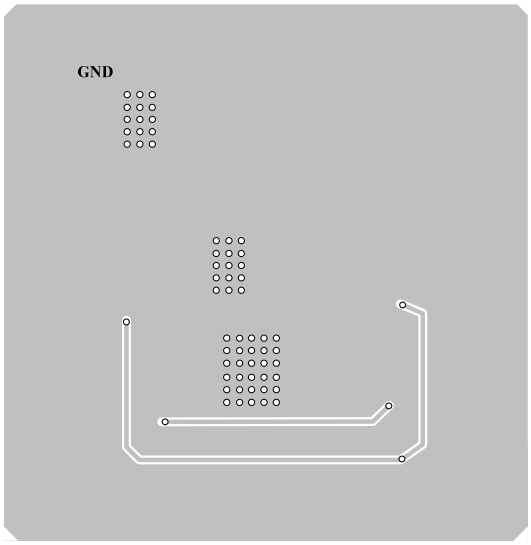
PCB layout is very important to achieve stable operation. It is highly recommended to duplicate EVB layout for optimum performance.

If change is necessary, please follow these guidelines and take Figure 5 for reference.

1) Keep the path of switching current short and minimize the loop area formed by Input cap, high-side MOSFET and external switching diode.
2) Bypass ceramic capacitors are suggested to be put close to the VIN Pin.
3) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
4) Route SW away from sensitive analog areas such as FB.
5) Connect IN, SW, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.



Top Layer



Bottom Layer

Figure 5—PCB Layout

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External Bootstrap Diode

It is recommended that an external bootstrap diode be added when the system has a 5V fixed input or the power supply generates a 5V output. This helps improve the efficiency of the regulator. The bootstrap diode can be a low cost one such as IN4148 or BAT54.

This diode is also recommended for high duty cycle operation (when $\frac{V_{OUT}}{V_{IN}}$ >65%) and high output voltage (V_{OUT}>12V) applications.

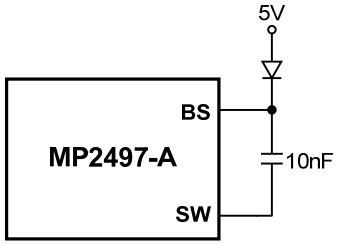

Figure 6—External Bootstrap Diode

Design Example

Below is a design example following the application guidelines for the specifications:

V_{IN}	8 to 50V
V_{OUT}	5V
V_{OVP}	6V
F_{SW}	100kHz
I_{OUT-L}	3A

The detailed application schematic is shown in Figure 7. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more possible applications of this device, please refer to related Evaluation Board Data Sheets.

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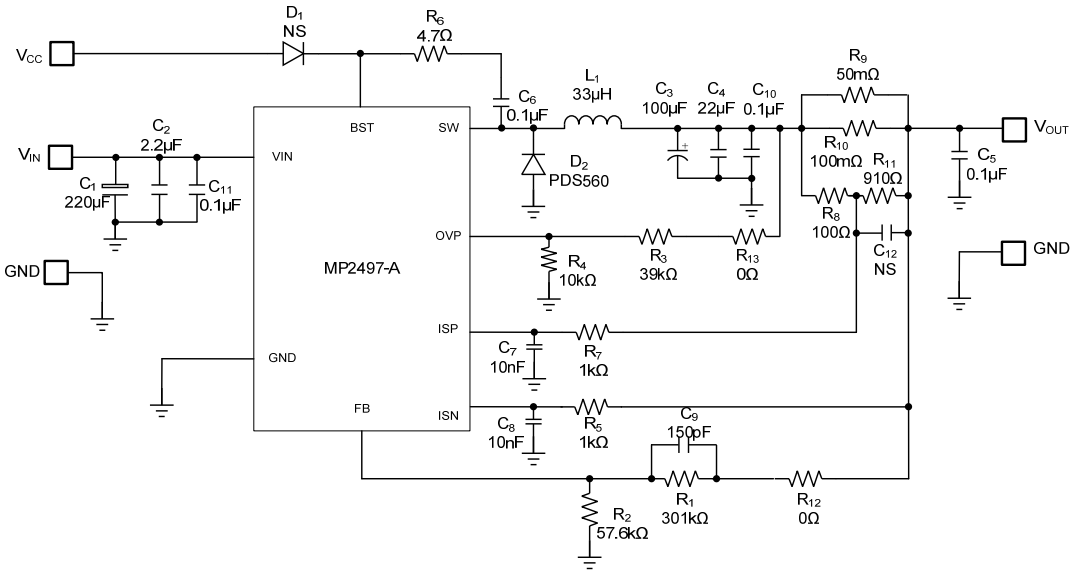

Figure 7—Detailed Application Schematic

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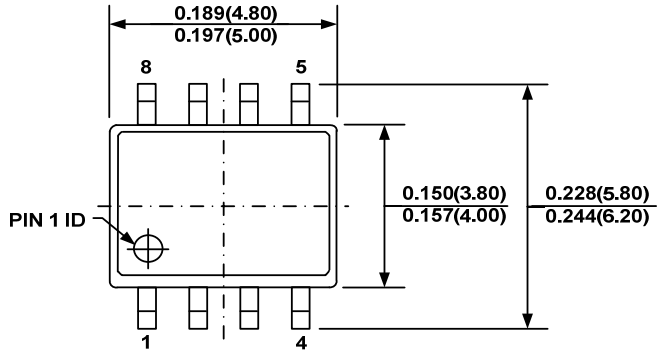
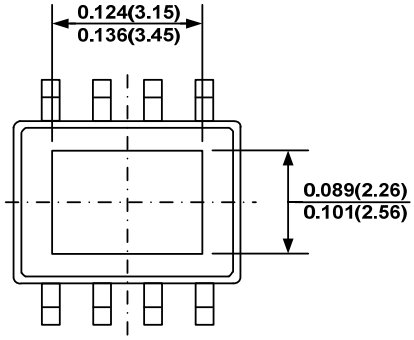
PACKAGE INFORMATION

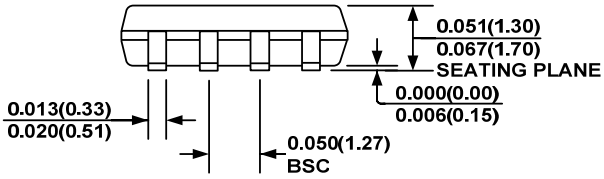
SOIC8E (EXPOSED PAD)



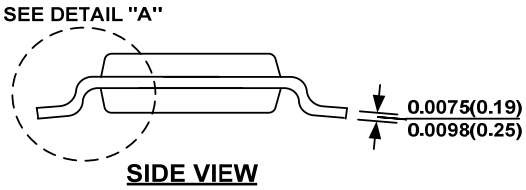
TOP VIEW



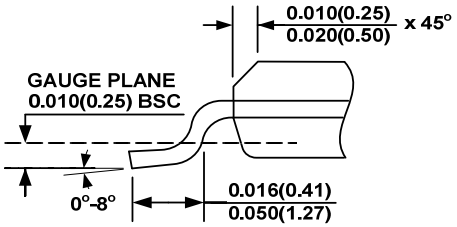
BOTTOM VIEW



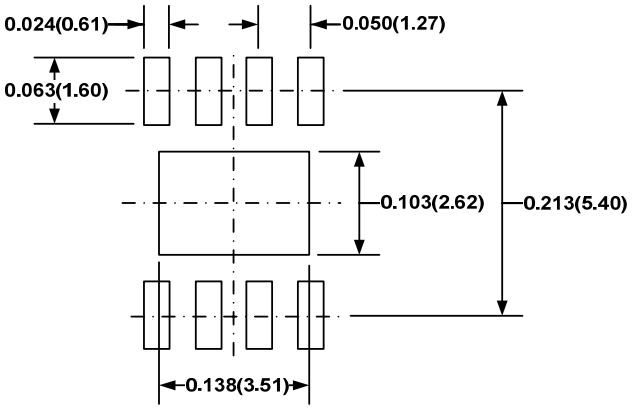
FRONT VIEW



SIDE VIEW



DETAIL "A"



RECOMMENDED LAND PATTERN

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6) DRAWING IS NOT TO SCALE.

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