MP2462

32V, 2A, 800kHz, Synchronous Step-Down Converter

DESCRIPTION

The MP2462 is a synchronous, step-down, switching regulator with integrated, internal, high-side and low-side power MOSFETs (HS-FETs and LS-FETs, respectively). It provides 2A of highly efficient output current (I_{OUT}) with current-mode control for fast loop response.

The wide 4.2V to 32V input voltage (V_{IN}) range accommodates a variety of step-down applications. A low shutdown-mode quiescent current allows the MP2462 to be used in battery-powered applications.

High power conversion efficiency across a wide load range is achieved by scaling down the switching frequency (f_{SW}) under light-load conditions to reduce switching and gate driving losses.

Frequency foldback helps prevent inductor current (I_L) runaway during start-up. Thermal shutdown provides reliable and fault-tolerant operation. A high duty cycle and low-dropout (LDO) mode are provided for battery-powered systems.

The MP2462 requires a minimal number of readily available, standard external components, and is available in a space-saving TSOT23-6 package.

FEATURES

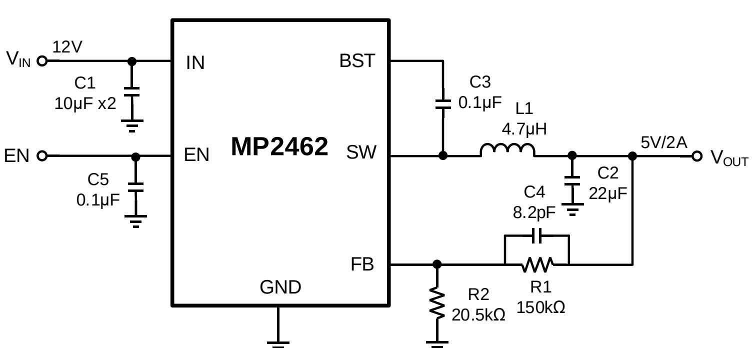
- Wide 4.2V to 32V Operating Input Voltage (V_{IN}) Range
- 2A Continuous Output Current (I_{OUT})
- 55μA Sleep-Mode Quiescent Current
- 160mΩ/80mΩ High-Side/Low-Side On Resistance ($R_{DS(ON)}$) for Internal Power MOSFETs
- High Feedback (FB) Accuracy: ±0.7% at T_J = 25°C, or ±1% at T_J = -40°C to +125°C
- Internal Soft Start (SS)
- Fixed 800kHz Switching Frequency (f_{SW})
- Low-Dropout (LDO) Mode
- Output Discharge
- Thermal Shutdown
- Over-Current Protection (OCP) with Hiccup Mode
- Available in a TSOT23-6 Package

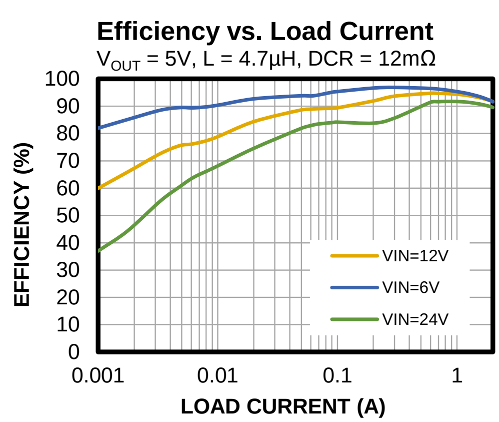
MPL Optimized Performance with MPS Inductor MPL-AL6060 Series

APPLICATIONS

- Battery-Powered Systems
- Smart Homes
- Wide Input Range Power Supplies
- Standby Power Supplies

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP2462GJ	TSOT23-6	*See Below*	1

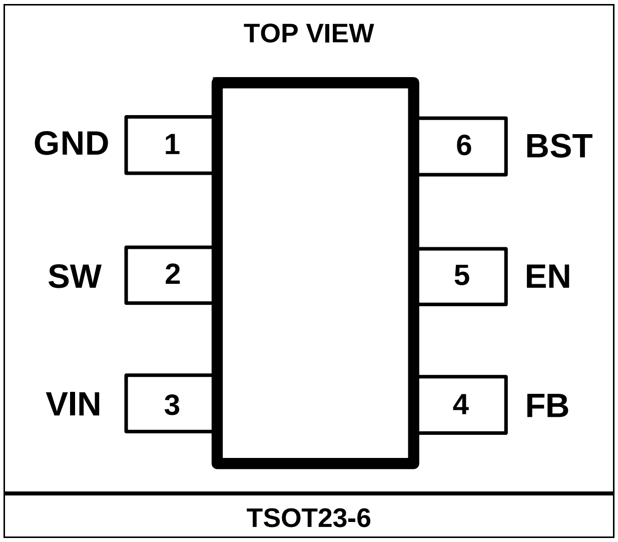
* For Tape & Reel, add suffix -Z (e.g. MP2462GJ-Z).

TOP MARKING

|BTDY

BTD: Product code of MP2462GJ
Y: Year code

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Description
1	GND	**System ground.** The GND pin is the reference ground of the regulated output voltage (V_{OUT}), and requires extra care during PCB layout. Make the GND pin connections using copper traces and vias.
2	SW	**Switch output.** Make the SW pin connections using a wide PCB trace.
3	VIN	**Supply voltage.** The MP2462 operates from a 4.2V to 32V input rail. The VIN pin must be connected to a capacitor using a wide PCB trace to decouple the input rail.
4	FB	**Feedback.** Connect the FB pin to the tap of an external resistor divider connected between the output and GND to set V_{OUT}. Place the resistor divider as close to FB as possible. Avoid vias on the FB traces and keep the trace far away from the SW node.
5	EN	**Enable**. The EN pin is a digital input that turns the buck regulator on or off. When the control circuit's power supply is ready, pull EN high to turn the buck regulator on; pull EN low to turn the regulator off. Connect EN to VIN via a voltage resistor divider for automatic start-up. Ensure that the EN pin voltage (V_{EN}) does not exceed 5.5V.
6	BST	**Bootstrap.** Connect a capacitor between the BST and SW pins to form a floating supply across the high-side MOSFET (HS-FET) driver. It is typically recommended to use a 0.1µF BST capacitor (C_{BST}).

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN}....................................-0.3V to +40V
V_{SW}........-0.3V (-5V for <10ns) to V_{IN_MAX} + 0.3V
V_{BST}....................................V_{SW_MAX} + 6V
All other pins ....-0.3V to 6V
Continuous power dissipation (T_A = 25°C) (2) (5)
....2.2W
Operating junction temperature (T_J)..........150°C
Lead temperature ....260°C
Storage temperature .... -65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ....4.2V to 32V
Output voltage (V_{OUT})..0.6V to V_{IN} x D_{MAX} or 30V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance

	θ_{JA}	θ_{JB}	
TSOT23-6			
JEDEC (4)	97.3	25	°C/W
EVL2462-J-00B (5)	57.3	......	°C/W
	θ_{JC_TOP}	θ_{JC_BOT}	
JEDEC (4)	45.5	8.5	°C/W
		Ψ_{JT}	
JEDEC (4)		7.7	°C/W
EVL2462-J-00B (5)		12.6	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can generate an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) The θ_{JA} value is only valid for comparison with other packages and cannot be used for design purposes. This value is based on a JEDEC51-7 board. They do not represent the performance obtained in an actual application.
5) Measured on a 2-layer, 2oz EVL2462-J-00B (5.1cmx5.1cm). The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature in the real system based on the following equation: $T_J = \psi_{JT} \times P_{LOSS} + T_{CASE\_TOP}$, where P_{LOSS} is the entire loss of the IC in real application, and T_{CASE_TOP} is the case top temperature.

ELECTRICAL CHARACTERISTICS

V_{IN} = 24V, V_{EN} = 2V, T_J = -40°C to +125°C (6), typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Power Supply						
Input voltage range	V_{IN}		4.2		32	V
V_{IN} under-voltage lockout (UVLO) rising threshold	V_{IN_UVLO}		3.55	3.85	4.15	V
V_{IN} UVLO threshold hysteresis	$V_{IN\_UVLO\_HYS}$			360		mV
Supply Current						
Quiescent supply current	I_Q	V_{FB} = 0.65V, no switching		55	100	µA
Shutdown supply current	I_{SD}	V_{EN} = 0V			3	µA
MOSFET						
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS}$	V_{BST} - V_{SW} = 5V		160		mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS}$			80		mΩ
Switch leakage current	I_{SW_LKG}				1	µA
Current Limit and Zero-Current Detection (ZCD)						
High-side (HS) switching peak current limit	I_{LIMIT_HS}	Duty cycle = 42%	2.1	2.8	3.6	A
Low-side (LS) switching valley-current limit	I_{LIMIT_LS}		1.85	2.4	2.95	A
Short hiccup duty cycle (7)	D_{HICCUP}			11.5		%
ZCD current	I_{ZCD}	V_{OUT} = 5V, L = 15µH		50		mA
Reference and Soft Start (SS)						
Feedback (FB) voltage	V_{FB}	T_J = 25°C	596	600	604	mV
		T_J = -40°C to +125°C	594	600	606	mV
FB current	I_{FB}	V_{FB} = 0.65V	-50	0	+50	nA
Internal SS time	t_{SS}	V_{OUT} = 0% to 100%		2.5		ms
Switching Frequency and Minimum On/Off Timer						
Switching frequency	f_{SW}		600	800	950	kHz
Minimum on time (7)	t_{ON_MIN}			110		ns
Minimum off time (7)	t_{OFF_MIN}			200		ns
Enable (EN) and Under-Voltage Lockout (UVLO)						
EN rising threshold	V_{EN_RISING}		1.14	1.22	1.3	V
EN hysteresis	V_{EN_HYS}			220		mV
EN pull-down resistor	R_{EN_PD}			1		MΩ
Protection						
Output under-voltage protection (UVP) threshold	V_{UVP}	Hiccup entry	35	40	45	% of V_{REF}

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 24V, V_{EN} = 2V, T_J = -40°C to +125°C (6), typical values are at T_J = 25°C, unless otherwise noted.

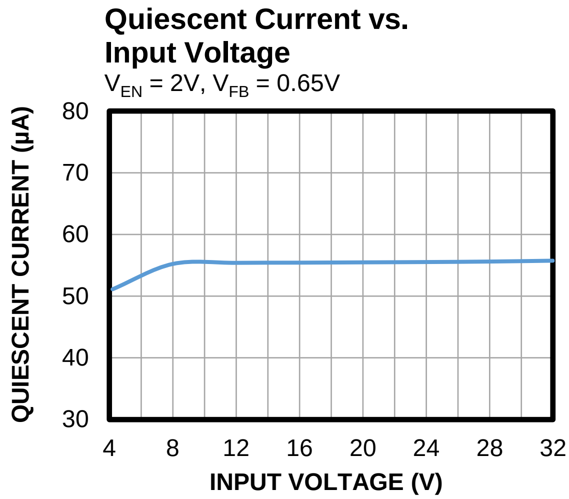
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output over-voltage protection (OVP) rising threshold	V_{OVP_R}		110	115	120	% of V_{REF}
Output OVP threshold hysteresis	V_{OVP_HYS}			10		% of V_{REF}
Output over-voltage (OV) delay	t_{OVP_DELAY}			2		µs
Discharge resistor	R_{DSC}	OVP or shutdown through EN discharges on SW		150		Ω
Thermal shutdown (7)	T_{SD}			150		°C
Thermal hysteresis (7)	T_{SD_HYS}			20		°C

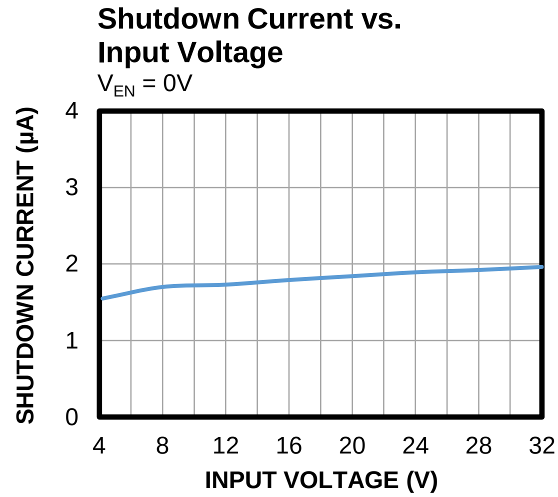
Notes:

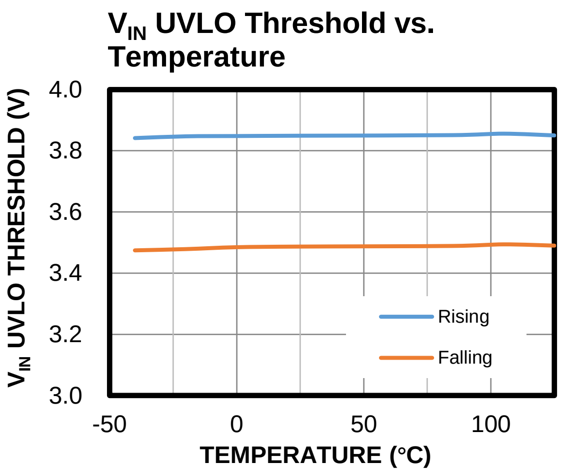
6) Not tested in production and derived by the over-temperature correlation.
7) Not tested in production and derived by sample characterization.

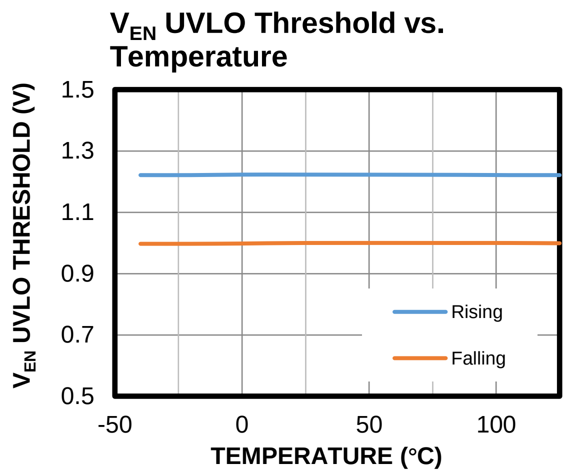
TYPICAL CHARACTERISTICS

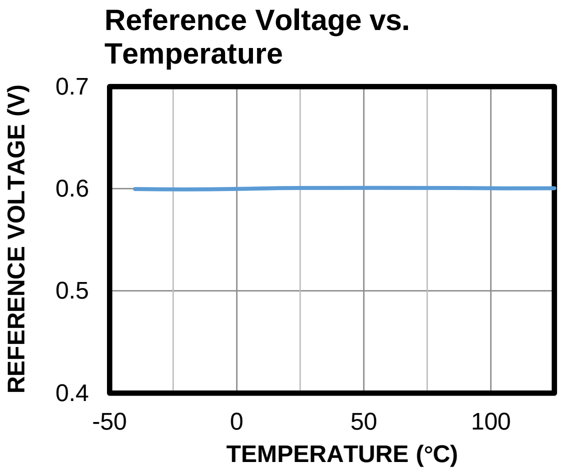
V_{IN} = 24V, T_A = 25°C, unless otherwise noted.

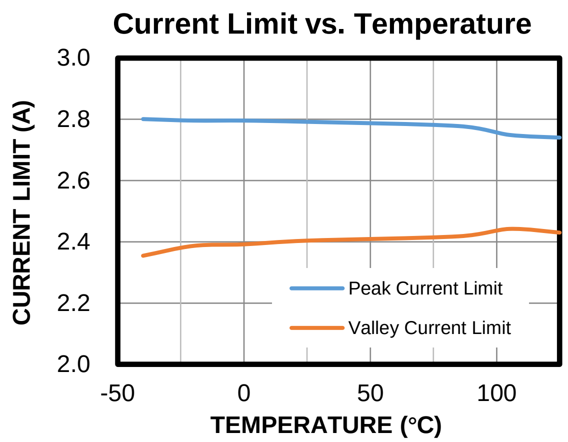






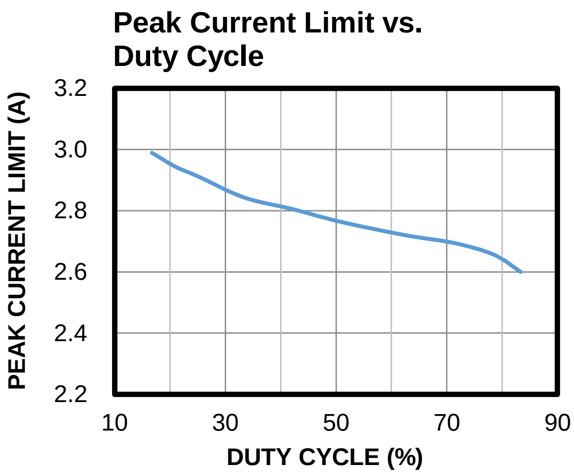






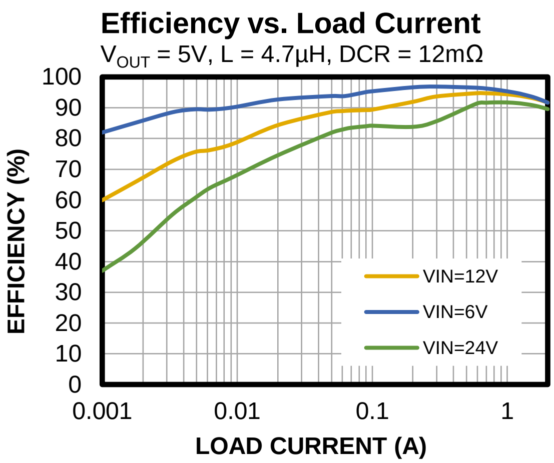
TYPICAL CHARACTERISTICS *(continued)*

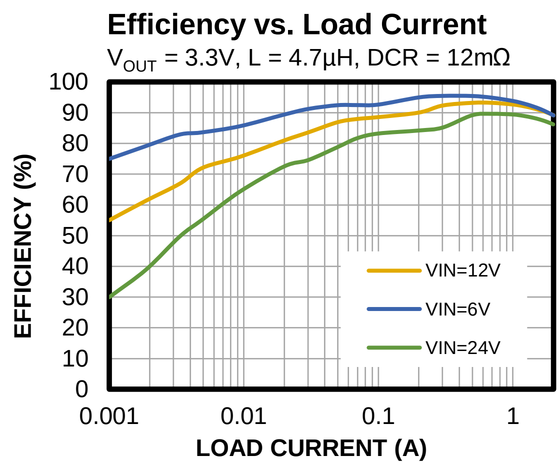
V_{IN} = 24V, T_A = 25°C, unless otherwise noted.

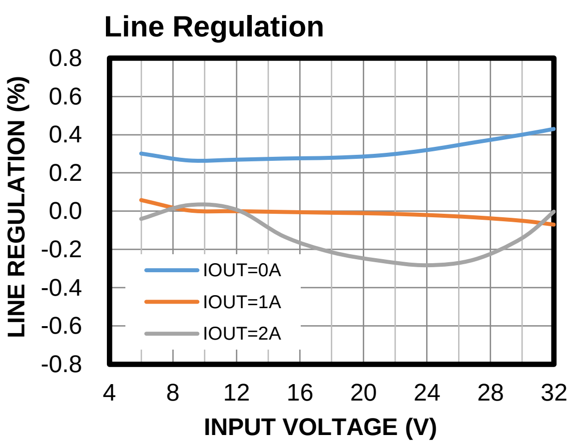


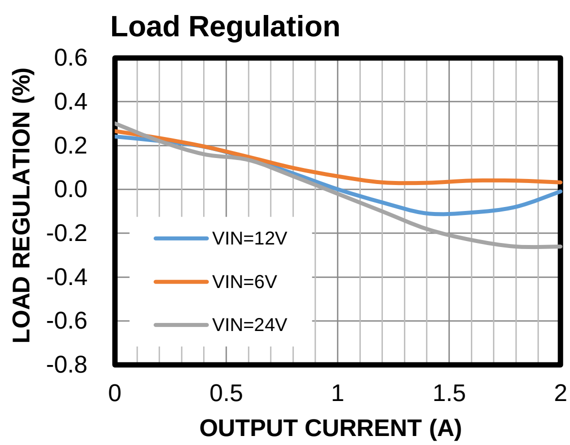
TYPICAL PERFORMANCE CHARACTERISTICS

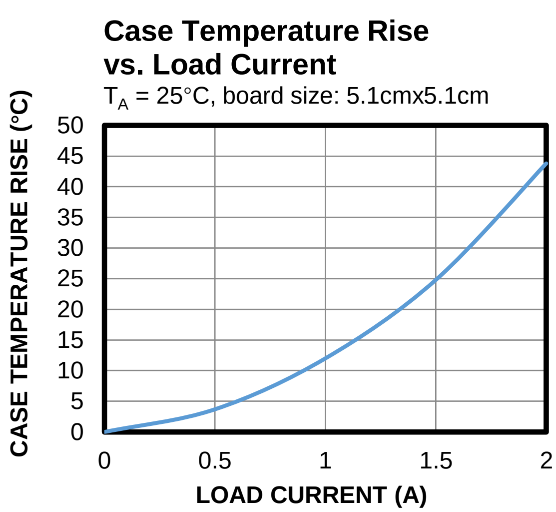
V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 800kHz, T_A = 25°C, unless otherwise noted.









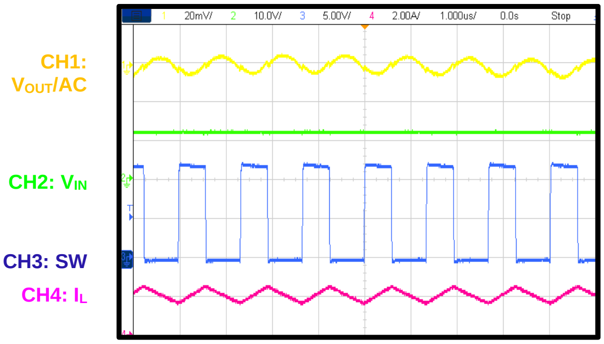


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 800kHz, T_A = 25°C, unless otherwise noted.

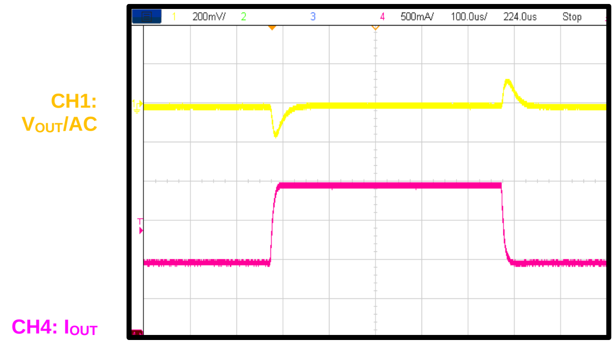
Output Ripple

I_{OUT} = 2A



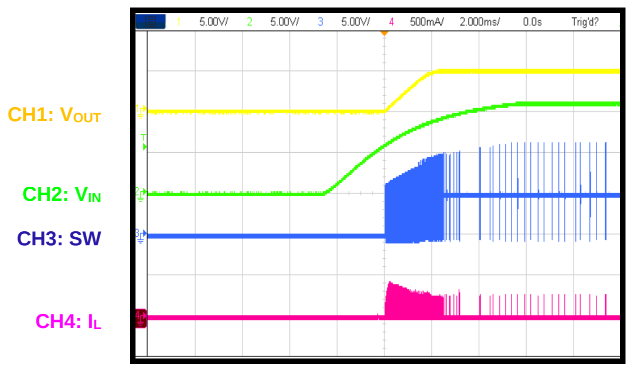
Load Transient Response

I_{OUT} = 1A to 2A, slew rate = 2.5A/µs with e-load



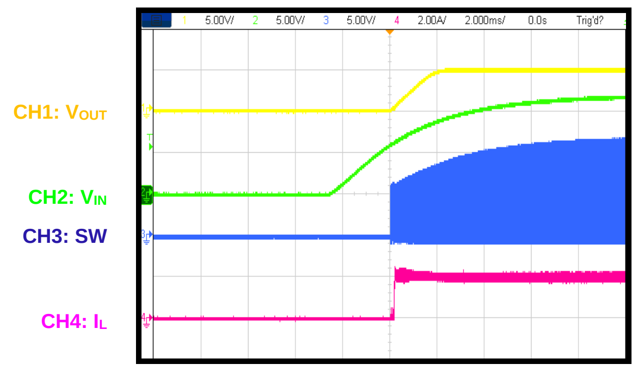
Start-Up through VIN

I_{OUT} = 0A



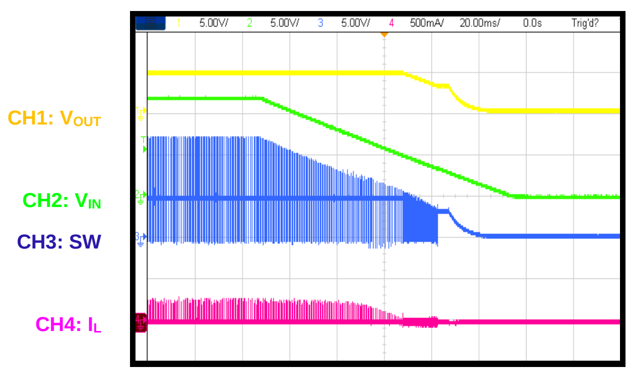
Start-Up through VIN

I_{OUT} = 2A



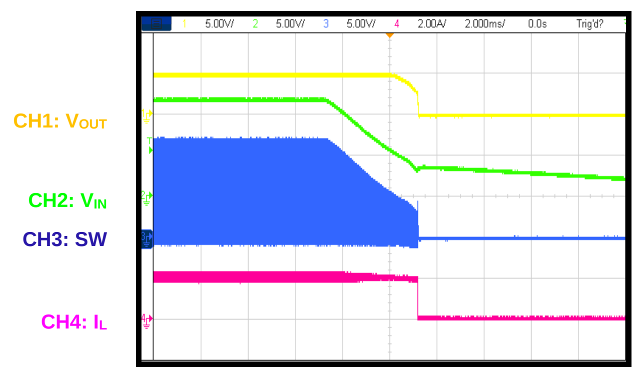
Shutdown through VIN

I_{OUT} = 0A



Shutdown through VIN

I_{OUT} = 2A

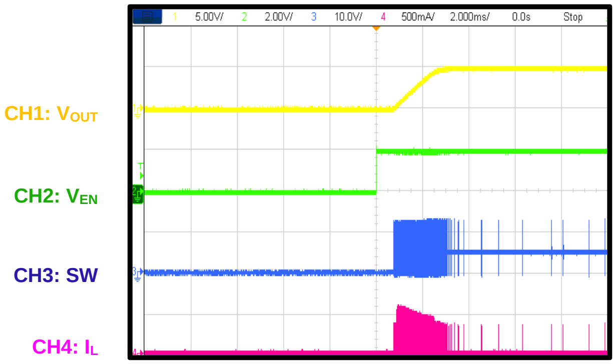


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 800kHz, T_A = 25°C, unless otherwise noted.

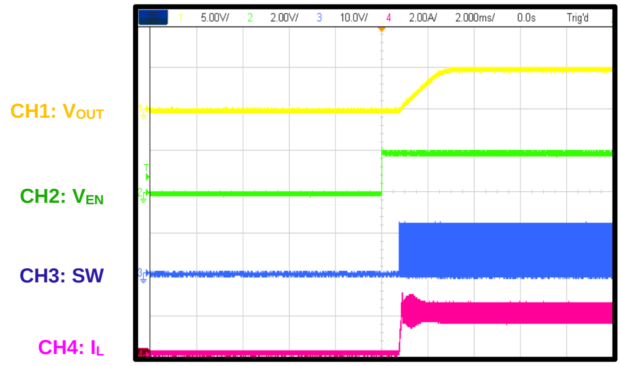
Start-Up through EN

I_{OUT} = 0A



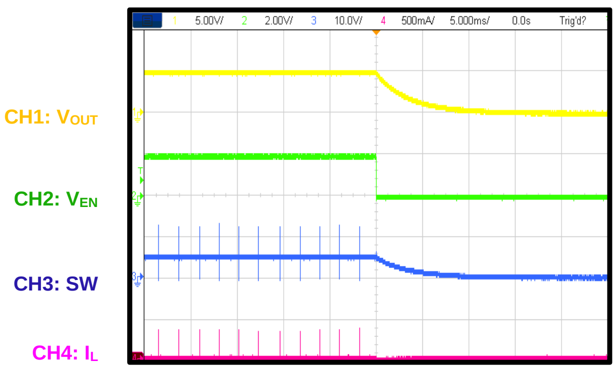
Start-Up through EN

I_{OUT} = 2A



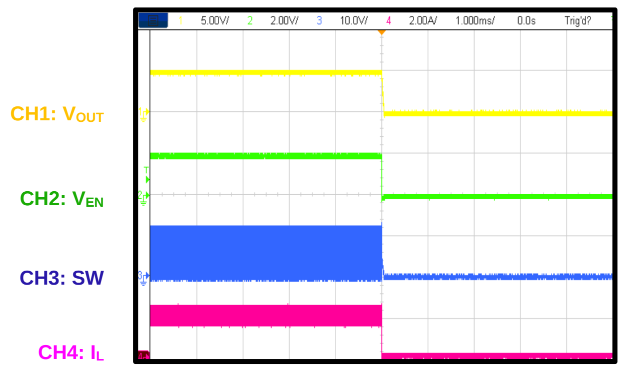
Shutdown through EN

I_{OUT} = 0A



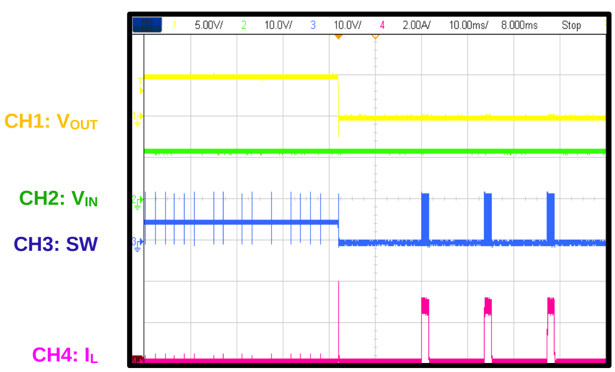
Shutdown through EN

I_{OUT} = 2A



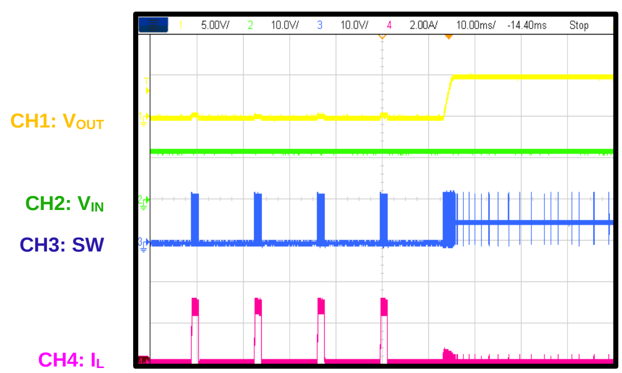
Short-Circuit Entry

I_{OUT} = 0A



Short-Circuit Recovery

I_{OUT} = 0A

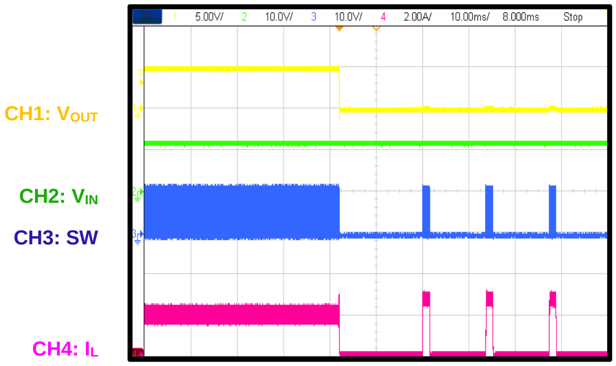


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 800kHz, T_A = 25°C, unless otherwise noted.

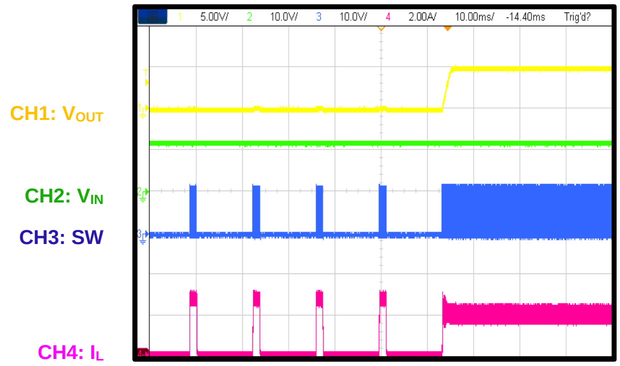
Short-Circuit Entry

I_{OUT} = 2A



Short-Circuit Recovery

I_{OUT} = 2A



FUNCTIONAL BLOCK DIAGRAM

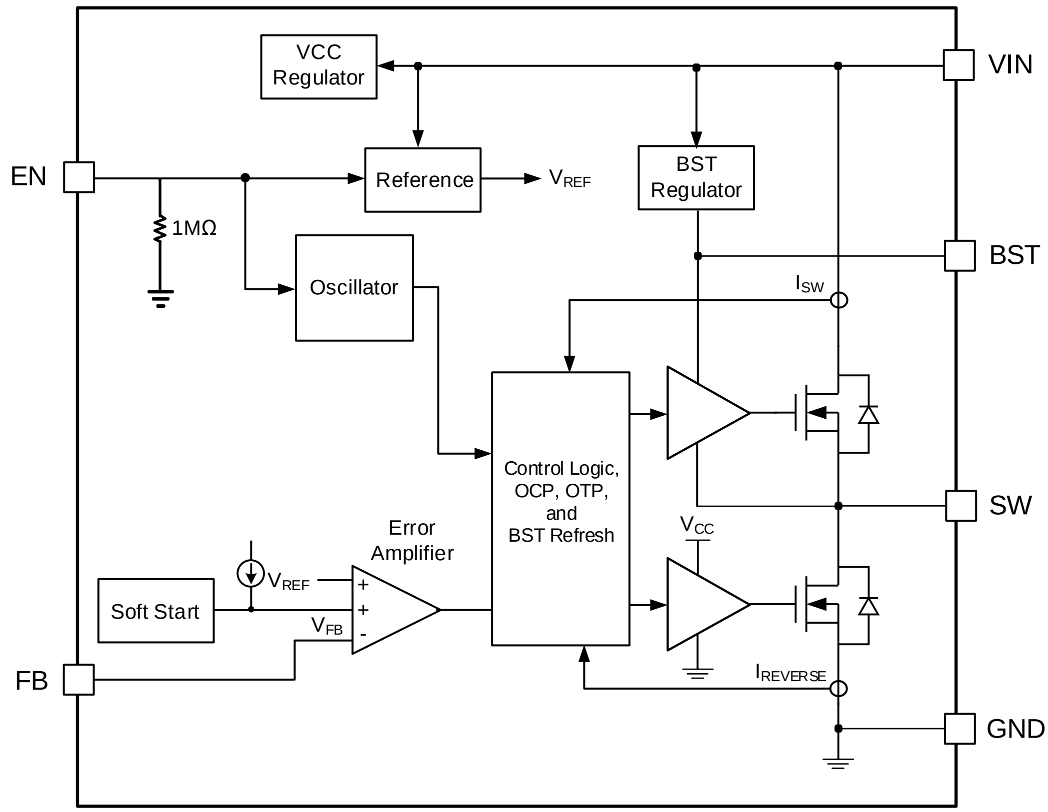


Figure 1: Functional Block Diagram

OPERATION

The MP2462 is a synchronous, step-down switching regulator with integrated, internal high-side and low-side power MOSFETs (HS-FETs and LS-FETs, respectively). It provides 2A of highly efficient output current (I_{OUT}) with current mode control. Its very low operational quiescent current (I_Q) makes the device well-suited for battery-powered applications.

Pulse-Width Modulation (PWM) Control

At moderate to high output currents, the MP2462 operates in a fixed-frequency, peak current control mode to regulate the output voltage (V_{OUT}). A pulse-width modulation (PWM) cycle is initiated by the internal clock. At the clock's rising edge, the HS-FET turns on until its current reaches the value set by the COMP voltage (V_{COMP}). When the HS-FET is off, the LS-FET turns on until the next cycle begins.

If the current in the HS-FET does not reach the current set via V_{COMP} within one PWM period, then the HS-FET remains on.

Advanced Asynchronous Modulation (AAM) Mode

The MP2462 employs advanced asynchronous modulation (AAM) mode to optimize efficiency during light-load or no-load conditions.

The device first enters asynchronous operation while the inductor current (I_L) approaches 0A at light loads. If the load further decreases or there is no load, then V_{COMP} drops below the AAM mode voltage (V_{AAM}), and the MP2462 enters AAM mode or sleep mode, which consumes very low I_Q and improves light-load efficiency.

In AAM mode, the internal clock is reset whenever V_{COMP} exceeds V_{AAM}, and the crossover time is taken as the benchmark for the next clock. If the load increases, and the V_{COMP} DC value exceeds V_{AAM}, then the device enters discontinuous conduction mode (DCM) or continuous conduction mode (CCM), which have a constant switching frequency (f_{SW}).

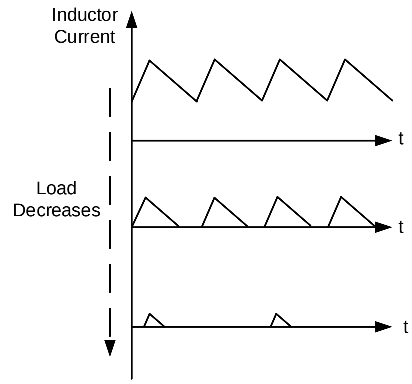


Figure 2: AAM Mode and PWM Mode

Error Amplifier (EA)

The error amplifier (EA) is comprised of an internal operation amplifier (op amp) with an RC feedback network connected between its output node (internal COMP node) and its negative input node (FB). If the FB voltage (V_{FB}) drops below the internal reference voltage (V_{REF}), then the op amp pulls the COMP output high, generating a higher switch peak current output and delivering more energy to the output. Conversely, if V_{FB} rises, then the switch peak current output drops.

Bootstrap (BST) Charging

The bootstrap (BST) capacitor (C_{BST}) is charged and regulated to about 5V via the dedicated internal BST regulator. When the HS-FET is on, the input voltage (V_{IN}) is about equal to the SW pin voltage (V_{SW}), meaning C_{BST} cannot be charged.

At higher duty cycle operation conditions, the time period available to BST charging is less. This means that C_{BST} may not be charged sufficiently. If the internal circuit does not have sufficient voltage or time to charge C_{BST}, then additional external circuitry can be used to ensure that the BST voltage (V_{BST}) is within the normal operation region.

Low-Dropout (LDO) Operation

To improve dropout, the MP2462 is designed to extend the on time (t_{ON}) when the minimum off time (t_{OFF_MIN}) is reached. When the HS-FET on time is extended, the frequency drops. The MP2462 can support a maximum 98% duty cycle with a 100kHz minimum frequency.

Enable (EN) Control

EN is a digital control pin that turns the regulator on and off. Pull EN high to turn on the regulator; pull the pin low to turn the regulator off. An internal 1MΩ resistor between EN and GND allows EN to be floated, which shuts down the chip. The MP2462 provides an accurate EN threshold, meaning a resistor divider between VIN and GND can configure V_{IN}, at which the MP2462 is enabled. This is highly recommended for applications where there is no dedicated EN logic signal.

The pull-up resistor (R_{UP}) and pull-down resistor (R_{DOWN}) should be selected to ensure that the EN pin voltage (V_{EN}) does not exceed 5.5V if V_{IN} reaches its maximum.

EN can also be connected to VIN directly via R_{UP}. To avoid excess sink current on the EN pin, R_{UP} is typically between 1MΩ and 2MΩ. A typical R_{UP} is 1MΩ.

If EN is connected directly to a voltage source without any R_{UP} requirements, then the voltage source amplitude must be limited to ≤5.5V.

To aviod noise on EN, place a 0.1µF ceramic capacitor as close to the EN and GND pins as possible.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The V_{IN} UVLO rising threshold is about 3.85V, while the V_{IN} UVLO falling threshold is about 3.49V.

Internal Soft Start (SS)

Soft start (SS) prevents the output voltage (V_{OUT}) from overshooting during start-up. When the chip starts up, the internal circuit generates a soft-start voltage (V_{SS}) that ramps up from 0V to 1V during the SS time (t_{SS}). If V_{SS} is below V_{REF}, then V_{SS} overrides V_{REF}, meaning the EA uses V_{SS} as the reference; if V_{SS} exceeds V_{REF}, then the EA continues using V_{REF} as its reference. t_{SS} is internally set to 2.5ms.

Pre-Biased Start-Up

The MP2462 is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, then V_{BST} is refreshed and charged. The voltage on the soft-start capacitor (C_{SS}) is charged as well. If V_{BST} exceeds its rising threshold, and the internal V_{SS} exceeds the sensed V_{OUT} at FB, then the device enters normal operation.

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from running away thermally. If the silicon die temperature exceeds its upper threshold, then the power MOSFETs shut down. If the temperature is below its lower threshold, then thermal shutdown is removed, and the chip is enabled again.

Output Discharge

The MP2462 discharges the output when the controller is turned off by the protection functions, including over-voltage protection (OVP) and shutdown through EN. The discharge resistor on the output is typically 150Ω.

Current Comparator and Current Limit

The power MOSFET current is sensed accurately via a current-sense MOSFET. The current is fed to the high-speed current comparator for current-mode control purposes. The current comparator uses this sensed current as one of its inputs. When the HS-FET turns on, the comparator is first blanked until the end of the turn-on transition to avoid noise. Then the comparator compares the power switch current with V_{COMP}. If the sensed current exceeds V_{COMP}, then the comparator outputs low to turn off the HS-FET.

The internal power MOSFET's maximum current is limited cycle-by-cycle internally.

Hiccup Protection

If the output is shorted to ground, causing V_{OUT} to drop below 40% of its nominal output, then the IC shuts down momentarily and begins discharging C_{SS}. The IC restarts with a full soft start once C_{SS} is fully discharged. This hiccup process is repeated until the fault is removed.

Start-Up and Shutdown

If both V_{IN} and V_{EN} exceed their respective thresholds, then the chip starts up. The reference block starts first, generating stable reference voltages and currents, then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

While the internal supply rail starts up, an internal timer holds the power MOSFET off to blank the start-up glitches. When the SS block is enabled, it first holds the SS output low to ensure that the remaining circuitries are ready, then slowly ramps up.

Three events can shut down the chip: V_{EN} going low, V_{IN} going low, and thermal shutdown.

APPLICATION INFORMATION

Setting the Output

The external resistor divider sets the output voltage (V_{OUT}). First, select a value for R2, where R2 should be chosen reasonably. A small R2 results in considerable quiescent current (I_Q) loss, while a too-large R2 makes the FB noise sensitive. Typically, set the current through R2 between 5µA and 100µA to achieve a good balance between system stability and no-load loss. Then R1 can be calculated with Equation (1):

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (1)$$

The feedback network is highly recommended (see Figure 3).

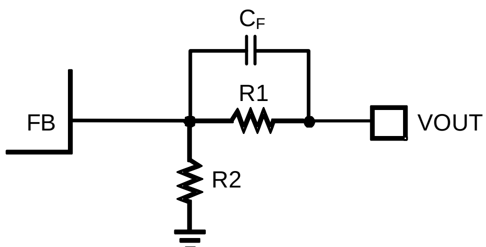


Figure 3: Feedback Network

Table 1 shows the recommended feedback network parameters for common output voltages. The minimum on time (t_{MIN_ON}) must not be triggered in application; otherwise, this leads to instability since frequency foldback only works during the start-up period.

Table 1: Recommended Parameters for Common Output Voltages (8)

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C_F (pF)	L (µH)
5	150	20.5	8.2	4.7
3.3	150	33.2	8.2	4.7

Note:

8) Based on V_{IN} = 12V, a different V_{IN}, output inductance, and output capacitance may affect the selection of R1, R2, and C_F. For additional component parameters, see the Typical Application Circuits section on page 19.

Selecting the Inductor

MPL Optimized Performance with MPS Inductor MPL-AL6060 Series

For most applications, use a inductor with a DC current rating at least 25% higher than the maximum load current (I_{LOAD_MAX}). For the highest efficiency, use an inductor with a DC resistance less than 15mΩ.

For most designs, the inductance (L) can be calculated with Equation (2):

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{SW}} \quad (2)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current at about 30% to 60% of I_{LOAD_MAX}. The maximum inductor peak current (I_{L_MAX}) can be calculated with Equation (3):

$$I_{L\_MAX} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (3)$$

MPS inductors are optimized and tested for use with our complete line of integrated circuits.

Table 2 shows the recommended power inductors, where the part number can be selected based on the design requirements.

Table 2: Power Inductor Selection

Part Number	Inductance	Manufacturer
MPL-AL6060-4R7	4.7µH	MPS

For more information, visit the Inductors pages on the MPS website.

Selecting the Input Capacitor

The step-down converter has a discontinuous input current (I_{IN}) and requires a capacitor to supply AC current while maintaining the DC input voltage. For optimal performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are recommended because of their low ESR and small temperature coefficients. For most applications, use two 10µF capacitors.

Since the input capacitor (C1, also called C_{IN}) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in C_{IN} (I_{C1}) can be estimated with Equation (4):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (4)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, which can be calculated with Equation (5):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (5)$$

For simplification, choose C1 with an RMS current rating that is greater than half of I_{LOAD_MAX}.

C1 can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, a small, high-quality ceramic capacitor (e.g. 0.1μF) should be placed as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input.

The input voltage ripple (ΔV_{IN}) caused by the capacitance can be estimated with Equation (6):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

Selecting the Output Capacitor

The output capacitor (C2, also called C_{OUT}) maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For the best results, use low-ESR capacitors to maintain a low output voltage ripple. The output voltage ripple (ΔV_{OUT}) can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (7)$$

Where R_{ESR} is the C2 equivalent series resistance (ESR).

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency (f_{SW}), and the capacitance causes the majority of ΔV_{OUT}. For simplification, ΔV_{OUT} can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}{}^2 \times L \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (9)$$

The C2 characteristics affect the stability of the regulation system. The MP2462 can be optimized for a wide range of capacitances and ESR values.

Design Example

Table 3 shows a design example where ceramic capacitors are applied.

Table 3: Design Example

V_{IN}	V_{OUT}	I_{OUT}
12V	5V	2A

Figure 5 and Figure 6 on page 19 show the detailed application schematics. See the Typical Characteristics section on page 6 for the typical performance and waveforms. For more device applications, refer to the EVL2462-J-00B datasheet.

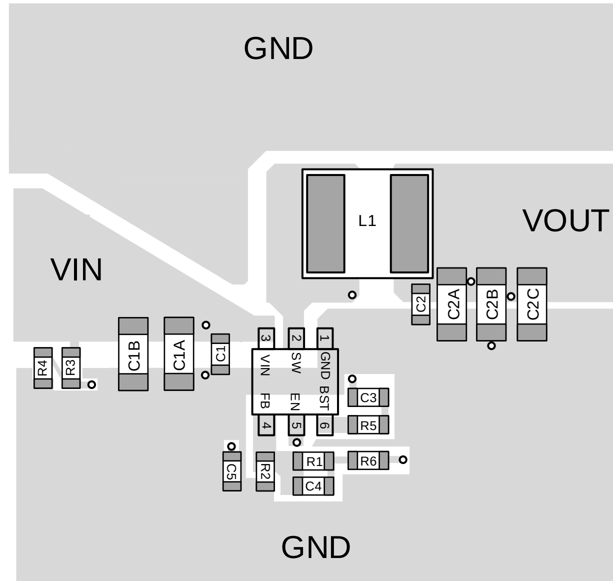
PCB Layout Guidelines [9]

Proper layout, especially of the switching power supplies, is critical for stable operation. Poor layout design can result in poor line or load regulation and stability issues. For the best results, refer to Figure 4 and follow the guidelines below:

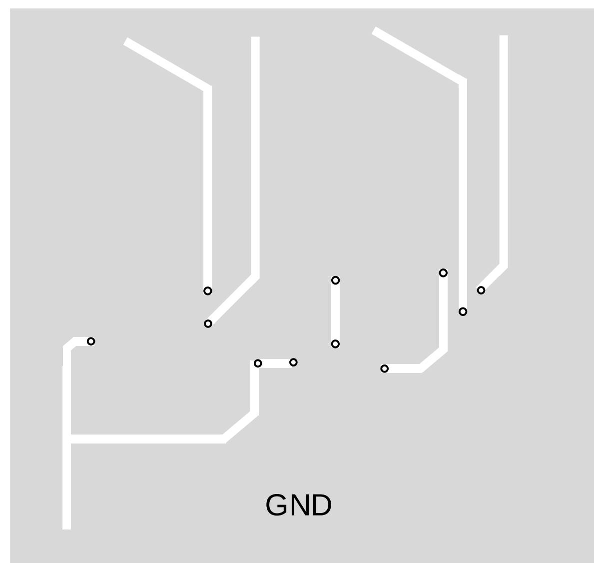
1. Keep the connection between the input ground and GND as short and wide as possible.
2. Keep the connection between C1 and VIN as short and wide as possible.
3. Ensure all feedback connections are short and direct.
4. Place the feedback resistors and compensation components as close to the chip as possible.
5. Route SW away from sensitive analog areas such as FB.
6. Place the BST capacitor (C_{BST}) as close to the BST and SW pins as possible.

Note:

9) The recommended layout is based on the Typical Application Circuits section on page 19.



Top Layer



Bottom Layer

Figure 4: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

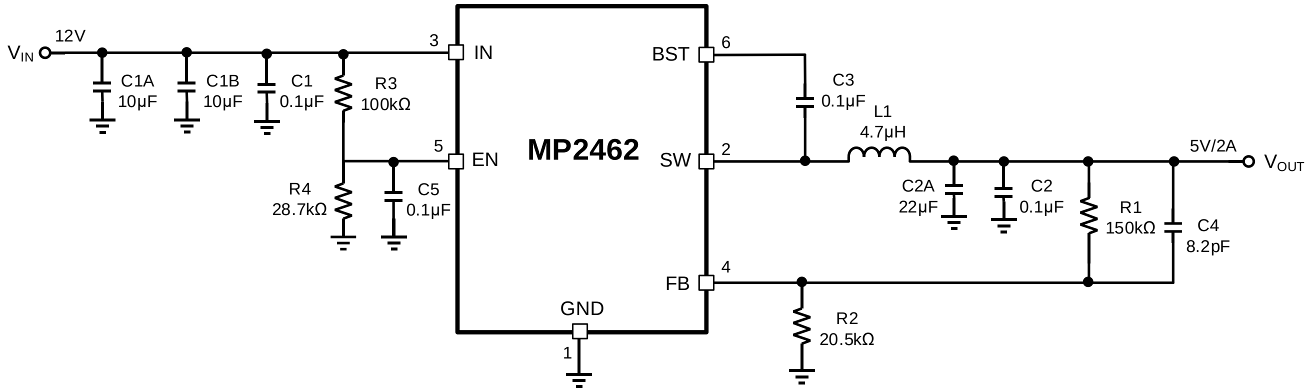


Figure 5: Typical Application Circuit (5V Output)

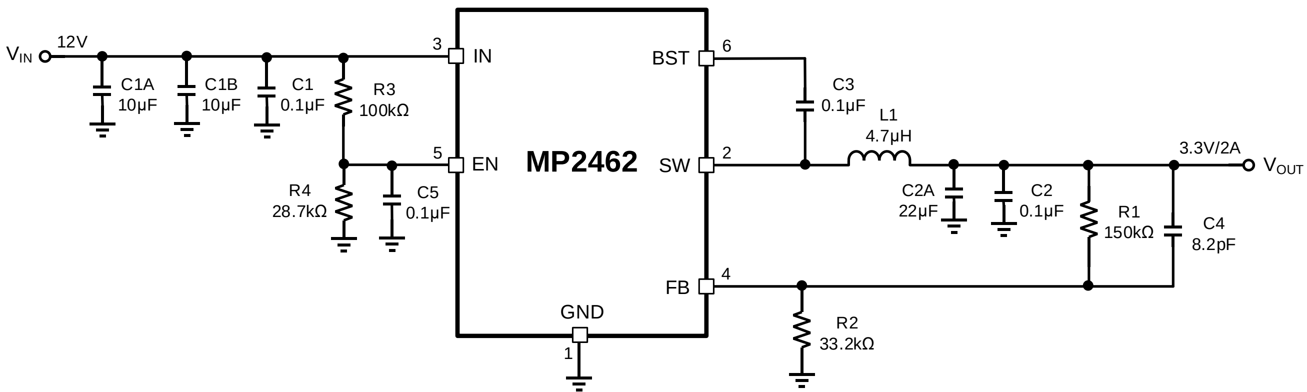
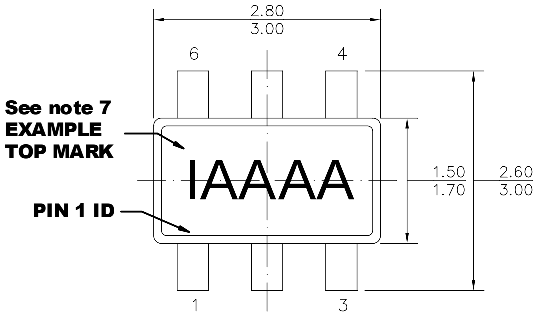


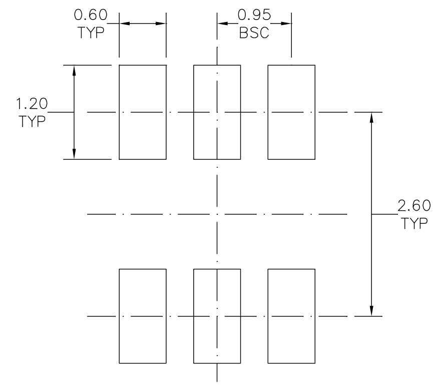
Figure 6: Typical Application Circuit (3.3V Output)

PACKAGE INFORMATION

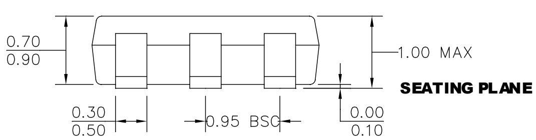
TSOT23-6



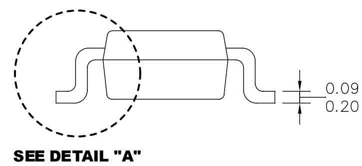
TOP VIEW



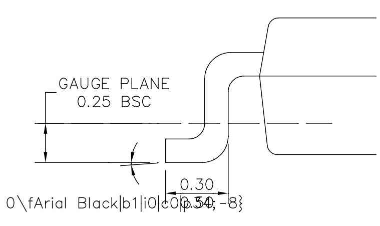
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

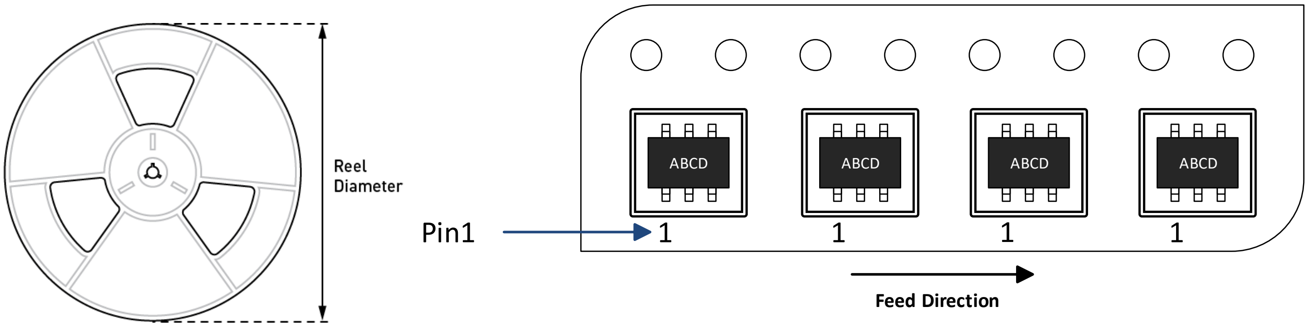


DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2462GJ-Z	TSOT23-6	3000	N/A	N/A	7in	8mm	4mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	9/24/2025	Initial Release	-