MP2307

3A, 23V, 340KHz Synchronous Rectified Step-Down Converter

The Future of Analog IC Technology

DESCRIPTION

The MP2307 is a monolithic synchronous buck regulator. The device integrates 100mΩ MOSFETS that provide 3A of continuous load current over a wide operating input voltage of 4.75V to 23V. Current mode control provides fast transient response and cycle-by-cycle current limit.

An adjustable soft-start prevents inrush current at turn-on and in shutdown mode, the supply current drops below 1μA.

This device, available in an 8-pin SOIC package, provides a very compact system solution with minimal reliance on external components.

EVALUATION BOARD REFERENCE

Board Number	Dimensions
EV2307DN-00A	2.0"X x 1.5"Y x 0.5"Z

FEATURES

- 3A Continuous Output Current
  4A Peak Output Current
- Wide 4.75V to 23V Operating Input Range
- Integrated 100mΩ Power MOSFET Switches
- Output Adjustable from 0.925V to 20V
- Up to 95% Efficiency
- Programmable Soft-Start
- Stable with Low ESR Ceramic Output Capacitors
- Fixed 340KHz Frequency
- Cycle-by-Cycle Over Current Protection
- Input Under Voltage Lockout
- Thermally Enhanced 8-Pin SOIC Package

APPLICATIONS

- Distributed Power Systems
- Networking Systems
- FPGA, DSP, ASIC Power Supplies
- Green Electronics/Appliances
- Notebook Computers

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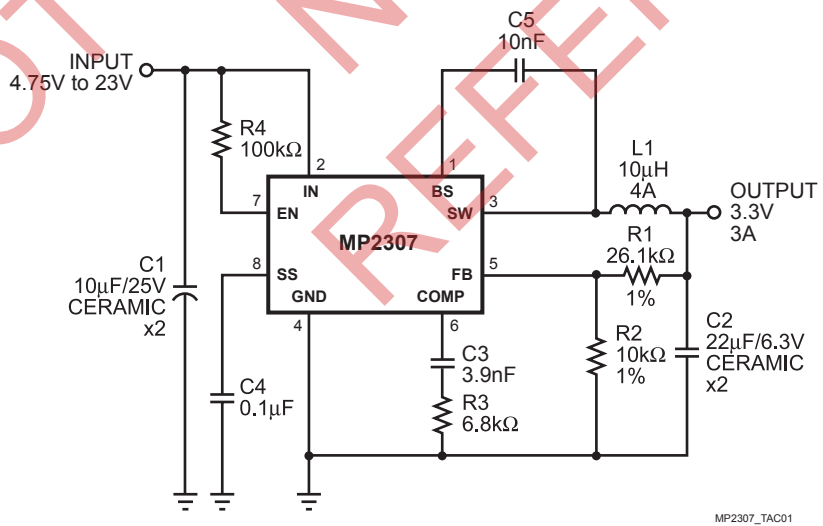
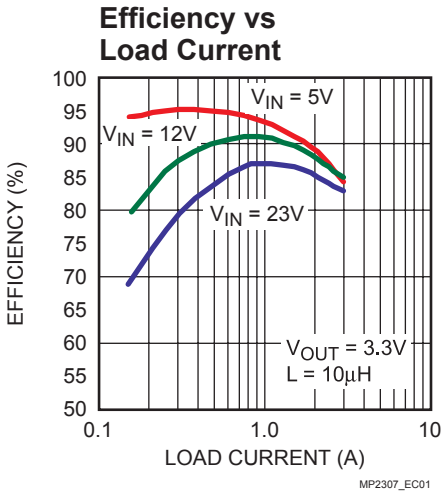
TYPICAL APPLICATION



MP2307_TAC01



MP2307_EC01

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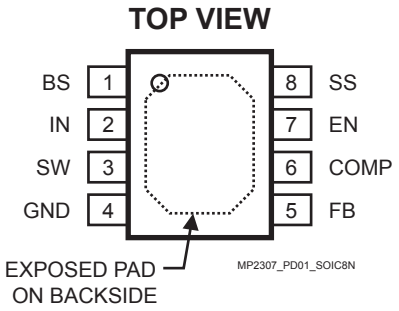
PACKAGE REFERENCE



Part Number*	Package	Temperature
MP2307DN	SOIC8N (Exposed Pad)	–40° to +85°C

* For Tape & Reel, add suffix –Z (eg. MP2307DN–Z)
For Lead Free, add suffix –LF (eg. MP2307DN–LF–Z)

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} ..... –0.3V to +26V
Switch Voltage V_{SW} ..... –1V to V_{IN} + 0.3V
Boost Voltage V_{BS} ..... V_{SW} – 0.3V to V_{SW} + 6V
All Other Pins ..... –0.3V to +6V
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... –65°C to +150°C

Recommended Operating Conditions (2)

Input Voltage V_{IN} ..... 4.75V to 23V
Output Voltage V_{OUT} ..... 0.925V to 20V
Ambient Operating Temp ..... –40°C to +85°C

Thermal Resistance (3)

	θ_{JA}	θ_{JC}	
SOIC8N	50	10	°C/W

Maximum Power Dissipation Operating

(*TA=25°C*)
SOIC8N(4), P_{OUT} 2W

Notes:
1) Exceeding these ratings may damage the device.
2) The device is not guaranteed to function outside of its operating conditions.
3) Measured on approximately 1" square of 1 oz copper.
4) Derating 20mW/°C at TA > 25°C

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Shutdown Supply Current		V_{EN} = 0V		0.3	3.0	µA
Supply Current		V_{EN} = 2.0V, V_{FB} = 1.0V		1.3	1.5	mA
Feedback Voltage	V_{FB}	4.75V ≤ V_{IN} ≤ 23V	0.900	0.925	0.950	V
Feedback Overvoltage Threshold				1.1		V
Error Amplifier Voltage Gain (5)	A_{EA}			400		V/V
Error Amplifier Transconductance	G_{EA}	ΔI_C = ±10µA		820		µA/V
High-Side Switch On-Resistance (5)	$R_{DS(ON)1}$			100		mΩ
Low-Side Switch On-Resistance (5)	$R_{DS(ON)2}$			100		mΩ
High-Side Switch Leakage Current		V_{EN} = 0V, V_{SW} = 0V		0	10	µA
Upper Switch Current Limit		Minimum Duty Cycle	4.0	5.8		A
Lower Switch Current Limit		From Drain to Source		0.9		A
COMP to Current Sense Transconductance	G_{CS}			5.2		A/V
Oscillation Frequency	F_{osc1}		300	340	380	KHz
Short Circuit Oscillation Frequency	F_{osc2}	V_{FB} = 0V		110		KHz
Maximum Duty Cycle	D_{MAX}	V_{FB} = 1.0V		90		%
Minimum On Time (5)	T_{ON}			220		ns
EN Shutdown Threshold Voltage		V_{EN} Rising	1.1	1.5	2.0	V
EN Shutdown Threshold Voltage Hysterisis				220		mV

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
EN Lockout Threshold Voltage			2.2	2.5	2.7	V
EN Lockout Hysterisis				210		mV
Input Under Voltage Lockout Threshold		V_{IN} Rising	3.80	4.05	4.40	V
Input Under Voltage Lockout Threshold Hysteresis				210		mV
Soft-Start Current		V_{SS} = 0V		6		µA
Soft-Start Period		C_{SS} = 0.1µF		15		ms
Thermal Shutdown (5)				160		°C

Note:

5) Guaranteed by design, not tested.

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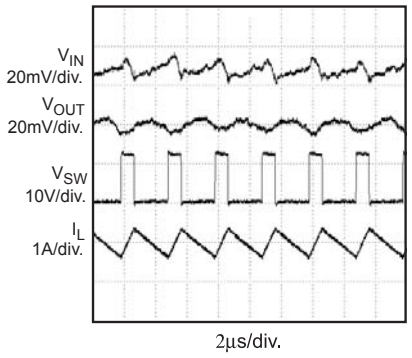
TYPICAL PERFORMANCE CHARACTERISTICS

C1 = 2 x 10µF, C2 = 2 x 22µF, L= 10µH, C_{SS}= 0.1µF, T_A = +25°C, unless otherwise noted.

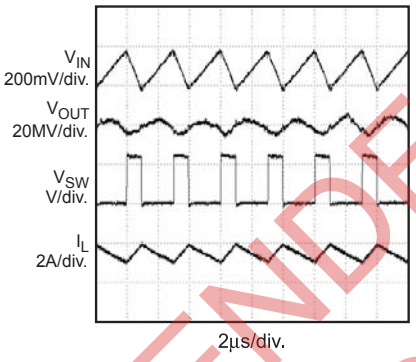
Steady State Test Waveforms

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A



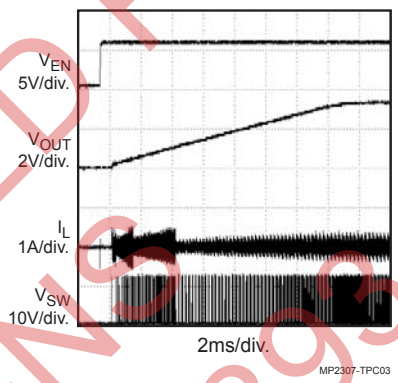
Steady State Test Waveforms

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 3A



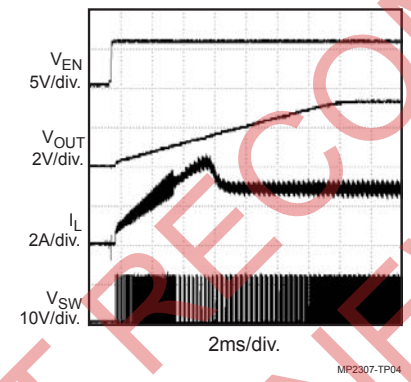
Startup through Enable Waveforms

V_{IN} = 12V, V_{OUT} = 3.3V, No Load



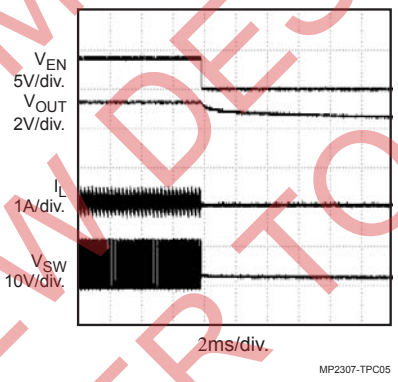
Startup Through Enable Waveforms

V_{IN} = 12V, V_{OUT} = 3.3V,
I_{OUT} = 3A (Resistance Load)



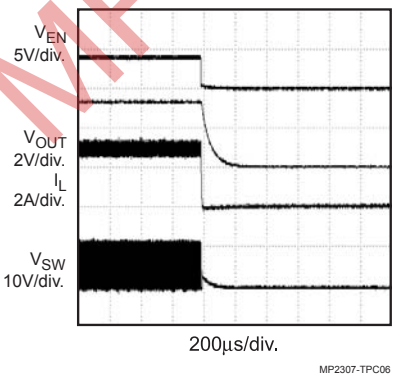
Shutdown Through Enable Waveforms

V_{IN} = 12V, V_{OUT} = 3.3V, No Load



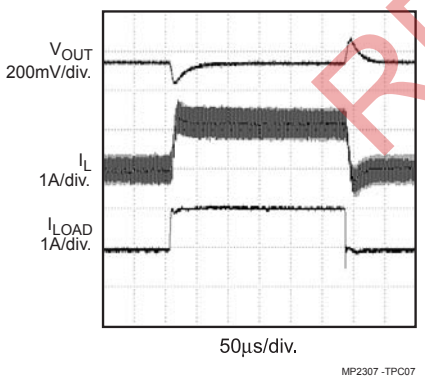
Shutdown Through Enable Waveforms

V_{IN} = 12V, V_{OUT} = 3.3V,
I_{OUT} = 3A (Resistance Load)



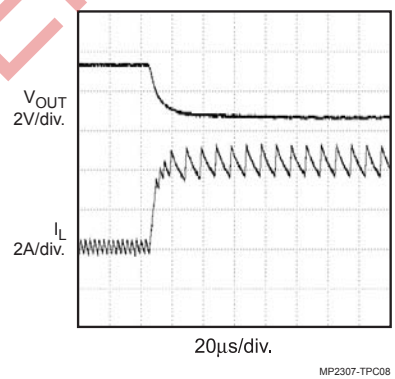
Load Transient Test Waveforms

V_{IN} = 12V, V_{OUT} = 3.3V,
I_{OUT} = 1A to 2A step



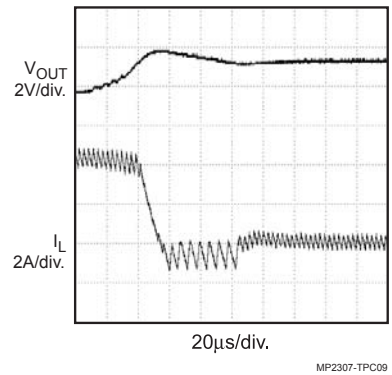
Short Circuit Test Waveforms

V_{IN} = 12V, V_{OUT} = 3.3V



Short Circuit Recovery Waveforms

V_{IN} = 12V, V_{OUT} = 3.3V



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PIN FUNCTIONS

Pin #	Name	Description
1	BS	High-Side Gate Drive Boost Input. BS supplies the drive for the high-side N-Channel MOSFET switch. Connect a 0.01µF or greater capacitor from SW to BS to power the high side switch.
2	IN	Power Input. IN supplies the power to the IC, as well as the step-down converter switches. Drive IN with a 4.75V to 23V power source. Bypass IN to GND with a suitably large capacitor to eliminate noise on the input to the IC. See *Input Capacitor*.
3	SW	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BS to power the high-side switch.
4	GND	Ground (Connect the exposed pad to Pin 4).
5	FB	Feedback Input. FB senses the output voltage and regulates it. Drive FB with a resistive voltage divider connected to it from the output voltage. The feedback threshold is 0.925V. See *Setting the Output Voltage*.
6	COMP	Compensation Node. COMP is used to compensate the regulation control loop. Connect a series RC network from COMP to GND. In some cases, an additional capacitor from COMP to GND is required. See *Compensation Components.*
7	EN	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator; low to turn it off. Attach to IN with a 100kΩ pull up resistor for automatic startup.
8	SS	Soft-Start Control Input. SS controls the soft-start period. Connect a capacitor from SS to GND to set the soft-start period. A 0.1µF capacitor sets the soft-start period to 15ms. To disable the soft-start feature, leave SS unconnected.

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OPERATION

FUNCTIONAL DESCRIPTION

The MP2307 regulates input voltages from 4.75V to 23V down to an output voltage as low as 0.925V, and supplies up to 3A of load current.

The MP2307 uses current-mode control to regulate the output voltage. The output voltage is measured at FB through a resistive voltage divider and amplified through the internal transconductance error amplifier. The voltage at the COMP pin is compared to the switch current (measured internally) to control the output voltage.

The converter uses internal N-Channel MOSFET switches to step-down the input voltage to the regulated output voltage. Since the high side MOSFET requires a gate voltage greater than the input voltage, a boost capacitor connected between SW and BS is needed to drive the high side gate. The boost capacitor is charged from the internal 5V rail when SW is low.

When the FB pin voltage exceeds 20% of the nominal regulation value of 0.925V, the over voltage comparator is tripped and the COMP pin and the SS pin are discharged to GND, forcing the high-side switch off.

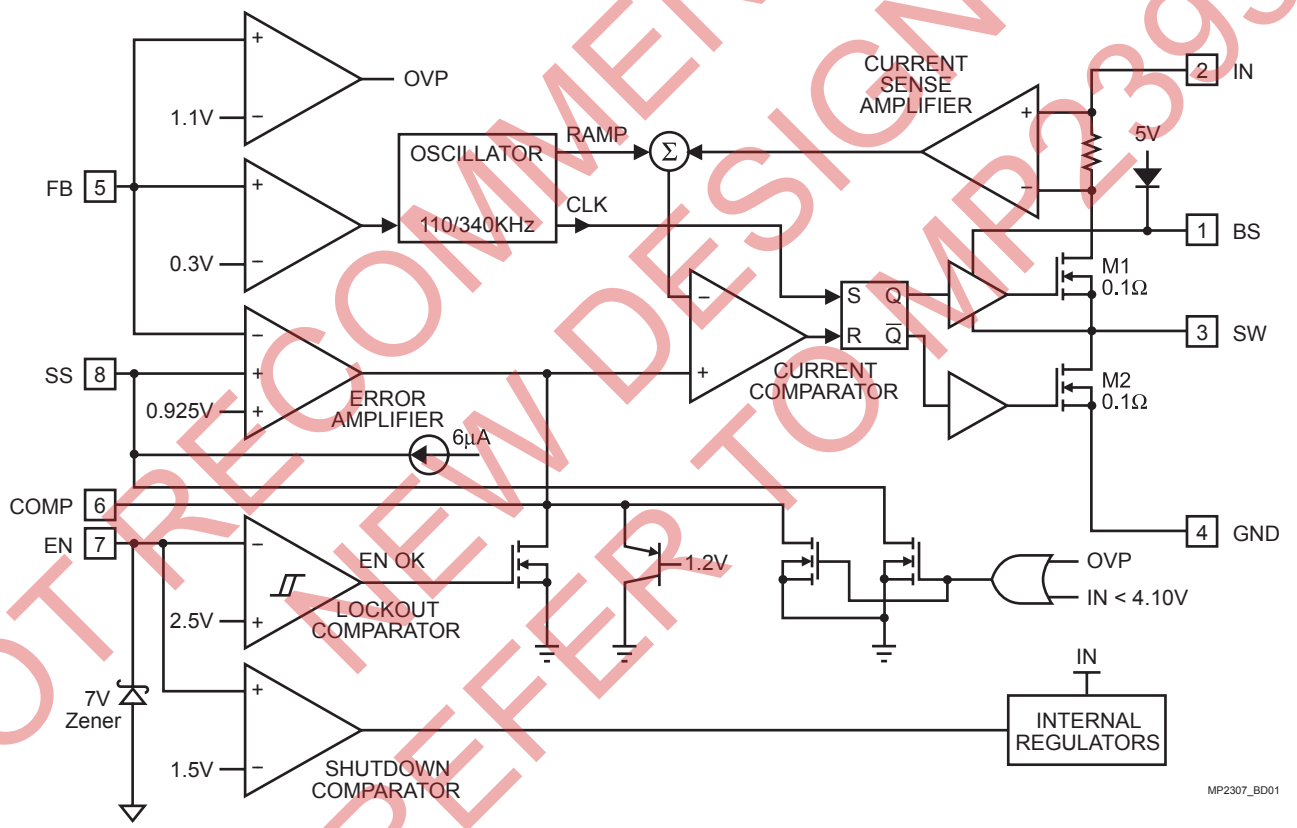

Figure 1—Functional Block Diagram

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APPLICATIONS INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

The output voltage is set using a resistive voltage divider connected from the output voltage to FB. The voltage divider divides the output voltage down to the feedback voltage by the ratio:

$$V_{FB} = V_{OUT} \frac{R2}{R1+R2}$$

Thus the output voltage is:

$$V_{OUT} = 0.925 \times \frac{R1+R2}{R2}$$

R2 can be as high as 100kΩ, but a typical value is 10kΩ. Using the typical value for R2, R1 is determined by:

$$R1 = 10.81 \times (V_{OUT} - 0.925) \ (k\Omega)$$

For example, for a 3.3V output voltage, R2 is 10kΩ, and R1 is 26.1kΩ. Table 1 lists recommended resistance values of R1 and R2 for standard output voltages.

Table 1—Recommended Resistance Values

VOUT	R1	R2
1.8V	9.53kΩ	10kΩ
2.5V	16.9kΩ	10kΩ
3.3V	26.1kΩ	10kΩ
5V	44.2kΩ	10kΩ
12V	121kΩ	10kΩ

Inductor

The inductor is required to supply constant current to the load while being driven by the switched input voltage. A larger value inductor will result in less ripple current that will in turn result in lower output ripple voltage. However, the larger value inductor will have a larger physical size, higher series resistance, and/or lower saturation current. A good rule for determining inductance is to allow the peak-to-peak ripple current to be approximately 30% of the maximum switch current limit. Also, make sure that the peak inductor current is below the maximum switch current limit.

The inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_S \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, f_S is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current, calculated by:

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2 \times f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where I_{LOAD} is the load current.

The choice of which style inductor to use mainly depends on the price vs. size requirements and any EMI constraints.

Optional Schottky Diode

During the transition between the high-side switch and low-side switch, the body diode of the low-side power MOSFET conducts the inductor current. The forward voltage of this body diode is high. An optional Schottky diode may be paralleled between the SW pin and GND pin to improve overall efficiency. Table 2 lists example Schottky diodes and their Manufacturers.

Table 2—Diode Selection Guide

Part Number	Voltage/Current Rating	Vendor
B130	30V, 1A	Diodes, Inc.
SK13	30V, 1A	Diodes, Inc.
MBRS130	30V, 1A	International Rectifier

Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors will also suffice. Choose X5R or X7R dielectrics when using ceramic capacitors.

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Since the input capacitor (C1) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where $I_{C1} = I_{LOAD}/2$. For simplification, use an input capacitor with a RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small, high quality ceramic capacitor, i.e. 0.1µF, should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple for low ESR capacitors can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{C1 \times f_S} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where C1 is the input capacitance value.

Output Capacitor

The output capacitor (C2) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right)$$

Where C2 is the output capacitance value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

When using ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance which is the main cause for the output voltage ripple. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^{\,2} \times L \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

When using tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP2307 can be optimized for a wide range of capacitance and ESR values.

Compensation Components

MP2307 employs current mode control for easy compensation and fast transient response. The system stability and transient response are controlled through the COMP pin. COMP is the output of the internal transconductance error amplifier. A series capacitor-resistor combination sets a pole-zero combination to govern the characteristics of the control system.

The DC gain of the voltage feedback loop is given by:

$$A_{VDC} = R_{LOAD} \times G_{CS} \times A_{EA} \times \frac{V_{FB}}{V_{OUT}}$$

Where V_{FB} is the feedback voltage (0.925V), A_{VEA} is the error amplifier voltage gain, G_{CS} is the current sense transconductance and R_{LOAD} is the load resistor value.

The system has two poles of importance. One is due to the compensation capacitor (C3) and the output resistor of the error amplifier, and the other is due to the output capacitor and the load resistor. These poles are located at:

$$f_{P1} = \frac{G_{EA}}{2\pi \times C3 \times A_{VEA}}$$

$$f_{P2} = \frac{1}{2\pi \times C2 \times R_{LOAD}}$$

Where G_{EA} is the error amplifier transconductance.

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The system has one zero of importance, due to the compensation capacitor (C3) and the compensation resistor (R3). This zero is located at:

$$f_{Z1} = \frac{1}{2\pi \times C3 \times R3}$$

The system may have another zero of importance, if the output capacitor has a large capacitance and/or a high ESR value. The zero, due to the ESR and capacitance of the output capacitor, is located at:

$$f_{ESR} = \frac{1}{2\pi \times C2 \times R_{ESR}}$$

In this case, a third pole set by the compensation capacitor (C6) and the compensation resistor (R3) is used to compensate the effect of the ESR zero on the loop gain. This pole is located at:

$$f_{P3} = \frac{1}{2\pi \times C6 \times R3}$$

The goal of compensation design is to shape the converter transfer function to get a desired loop gain. The system crossover frequency where the feedback loop has the unity gain is important. Lower crossover frequencies result in slower line and load transient responses, while higher crossover frequencies could cause system instability. A good standard is to set the crossover frequency below one-tenth of the switching frequency.

To optimize the compensation components, the following procedure can be used.

1. Choose the compensation resistor (R3) to set the desired crossover frequency.

Determine R3 by the following equation:

$$R3 = \frac{2\pi \times C2 \times f_C}{G_{EA} \times G_{CS}} \times \frac{V_{OUT}}{V_{FB}} < \frac{2\pi \times C2 \times 0.1 \times f_S}{G_{EA} \times G_{CS}} \times \frac{V_{OUT}}{V_{FB}}$$

Where f_C is the desired crossover frequency which is typically below one tenth of the switching frequency.

2. Choose the compensation capacitor (C3) to achieve the desired phase margin. For applications with typical inductor values, setting the compensation zero (f_{Z1}) below one-forth of the crossover frequency provides sufficient phase margin.

Determine C3 by the following equation:

$$C3 > \frac{4}{2\pi \times R3 \times f_C}$$

Where R3 is the compensation resistor.

3. Determine if the second compensation capacitor (C6) is required. It is required if the ESR zero of the output capacitor is located at less than half of the switching frequency, or the following relationship is valid:

$$\frac{1}{2\pi \times C2 \times R_{ESR}} < \frac{f_S}{2}$$

If this is the case, then add the second compensation capacitor (C6) to set the pole f_{P3} at the location of the ESR zero. Determine C6 by the equation:

$$C6 = \frac{C2 \times R_{ESR}}{R3}$$

PCB Layout Guide

PCB layout is very important to achieve stable operation. It is highly recommended to duplicate EVB layout for optimum performance.

If change is necessary, please follow these guidelines and take Figure2 for reference.

1) Keep the path of switching current short and minimize the loop area formed by Input cap., high-side MOSFET and low-side MOSFET.
2) Bypass ceramic capacitors are suggested to be put close to the Vin Pin.
3) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
4) R_{OUT} SW away from sensitive analog areas such as FB.

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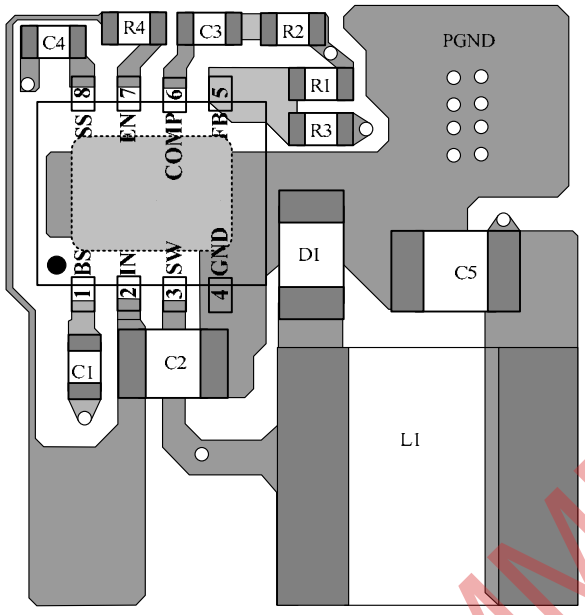
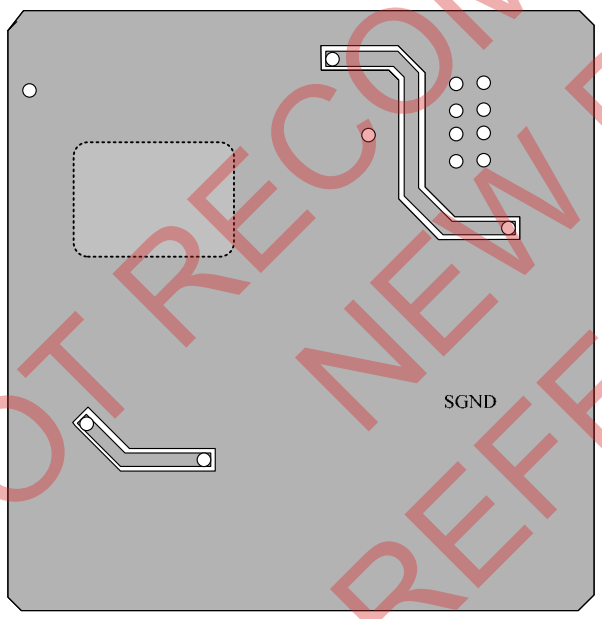
5) Connect IN, SW, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.



TOP Layer



Bottom Layer

Figure 2—PCB Layout (Double Layer)

External Bootstrap Diode

An external bootstrap diode may enhance the efficiency of the regulator, the applicable conditions of external BS diode are:

- V_{OUT} is 5V or 3.3V; and
- Duty cycle is high: $D=\frac{V_{OUT}}{V_{IN}}$ >65%

In these cases, an external BS diode is recommended from the output of the voltage regulator to BS pin, as shown in Figure3

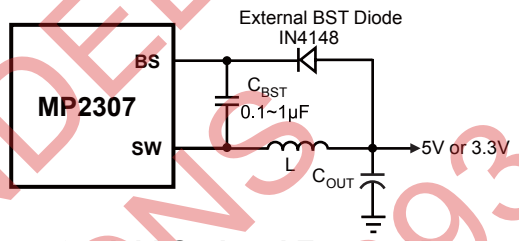


Figure 3—Add Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BS diode is IN4148, and the BS cap is 0.1~1μF.

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TYPICAL APPLICATION CIRCUIT

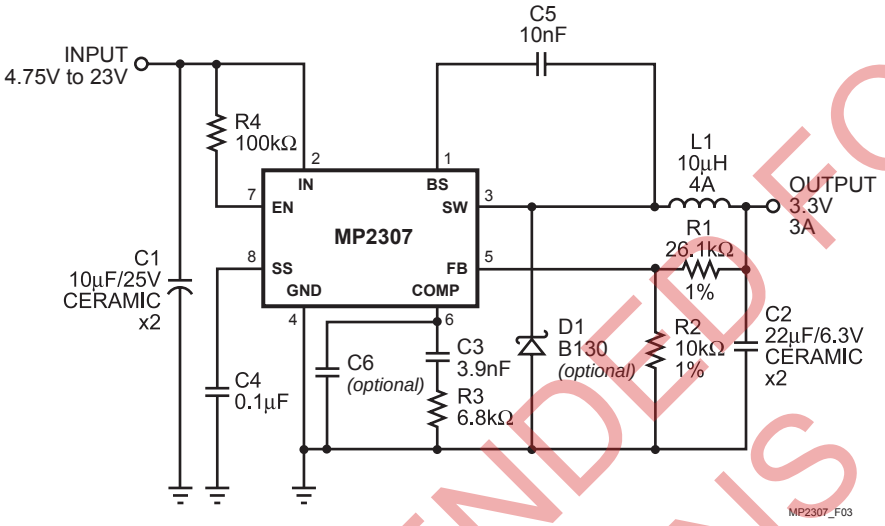

Figure 4—MP2307 with 3.3V Output, 22uF/6.3V Ceramic Output Capacitor

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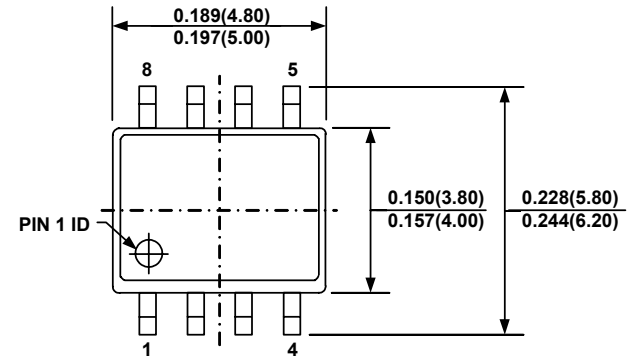
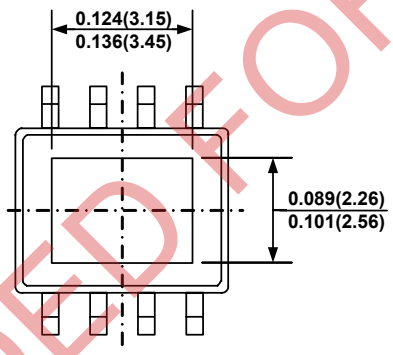
PACKAGE INFORMATION

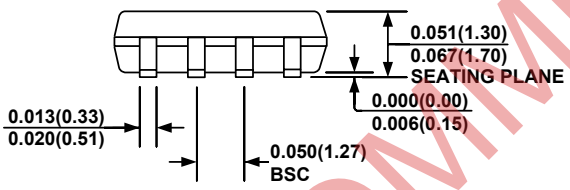
SOIC8N (EXPOSED PAD)



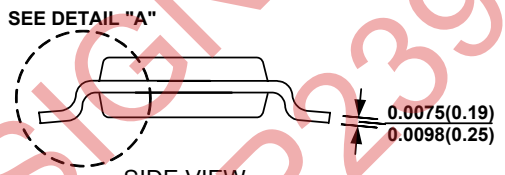
TOP VIEW



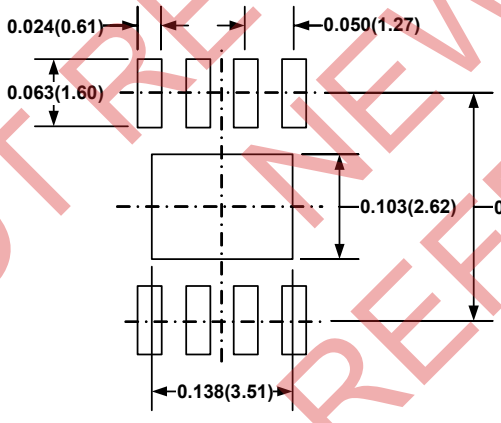
BOTTOM VIEW



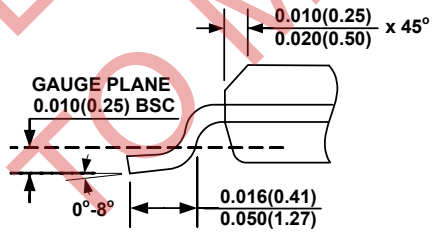
FRONT VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6) DRAWING IS NOT TO SCALE.

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