MP2127

2.7-6V Input, 2A, 1.2MHz Synchronous Step-Down Converter

The Future of Analog IC Technology

DESCRIPTION

The MP2127 is a fully integrated, internally compensated 1.2MHz fixed frequency PWM step-down converter. It is ideal for powering portable equipment that runs from a single cell Lithium-Ion (Li+) Battery, with an input range from 2.7V to 6V. The MP2127 can provide up to 2A of load current with output voltage as low as 0.8V. It can also operate at 100% duty cycle for low dropout applications. With peak current mode control and internal compensation, the MP2127 is stable with ceramic capacitors and small inductors. Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown.

MP2127 is available in the small 6-pin 3mmx3mm QFN package.

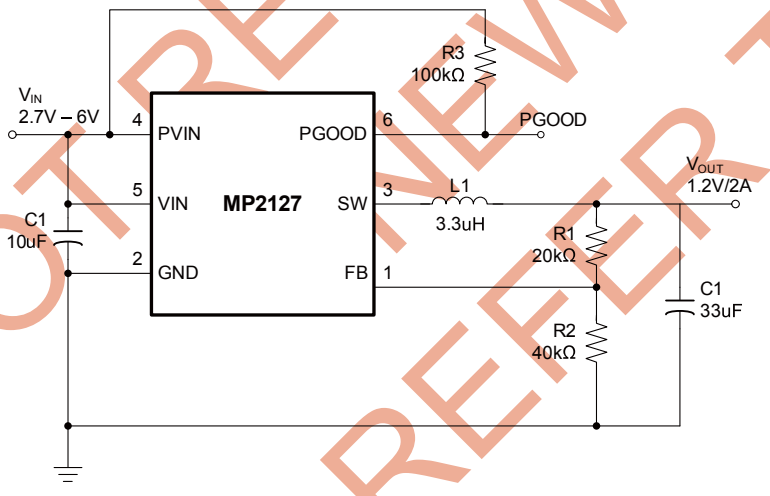
FEATURES

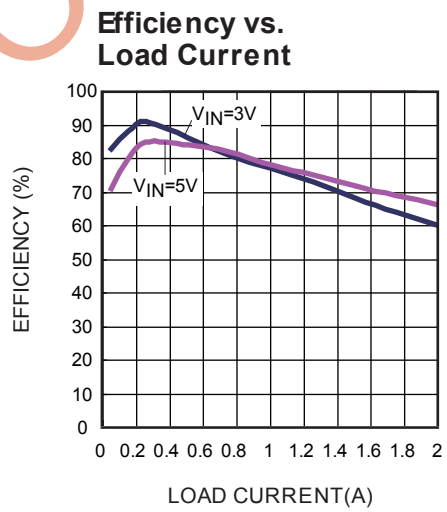
- Output Adjustable from 0.8V to VIN
- Up to 95% Efficiency
- 100% Duty Cycle for Low Dropout Applications
- Power Good Indicator Output
- 1.2MHz Fixed Switching Frequency
- Stable with Low ESR Output Ceramic Capacitors
- Thermal Shutdown
- Cycle-by-Cycle Over Current Protection
- Short circuit protection
- 2.7V-6V Input Operation Range
- Available in 6-pin 3x3mm QFN

APPLICATIONS

- Smart Phones, PDA's
- DVD+/-RW Drives
- Digital Cameras
- Portable Instruments

TYPICAL APPLICATION



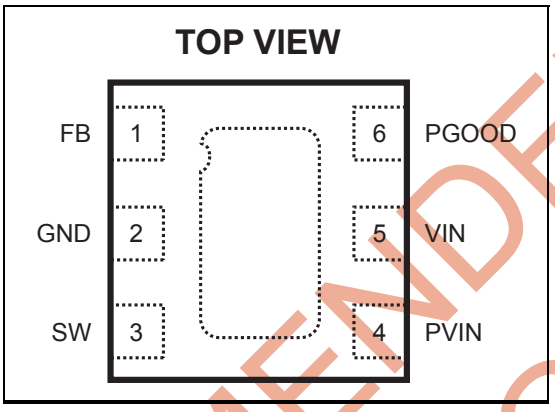


ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature (T_A)
MP2127DQ	QFN6 (3mm x 3mm)	8G	–40°C to +85°C

* For Tape & Reel, add suffix –Z (e.g. MP2127DQ–Z).
For RoHS compliant packaging, add suffix –LF (e.g. MP2127DQ–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

PVIN, VIN to GND.....–0.3V to + 7.0V
SW to GND .....–0.3V to V_{IN} + 0.3V
PGOOD, FB to GND .....–0.3V to +6.5V
Operating Temperature..... –40°C to +85°C
Continuous Power Dissipation…(T_A = +25°C) (2)
……..2.5W
Junction Temperature .....150°C
Lead Temperature .....260°C
Storage Temperature ..... –65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} .....2.7V to 6V
Operating Junct. Temp (T_J).....-40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN6 (3mm x 3mm) .....50 ..... 12 ... °C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS (5)

V_{IN} = 3.6V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current	I_{IN}	V_{FB} = 0.9V		500	750	μA
Thermal Shutdown Trip Threshold	T_{SD}	Hysteresis = 20°C		150		°C
IN Undervoltage Lockout Threshold	$INUV_{VTH}$	Rising Edge	2.15	2.40	2.65	V
IN Undervoltage Lockout Hysteresis	$INUV_{HYS}$			160		mV
Regulated FB Voltage	V_{FB}	T_A = +25°C	0.784	0.800	0.816	V
		-40°C≤ T_A≤ +85°C	0.776	0.800	0.824	
FB Input Bias Current	I_{FB}	V_{FB} = 0.9V	-50	-2	+50	nA
SW PFET On Resistance	HS_{RDS-ON}	I_{SW} = 100mA	0.19	0.23	0.27	Ω
SW NFET On Resistance	LS_{RDS-ON}	I_{SW} = -100mA	0.16	0.2	0.24	Ω
SW PFET Peak Current Limit	I_{LIMIT}	Duty Cycle=100%	2.2	3.0	3.8	A
		Duty Cycle=50% (6)	2.5	3.5	4.5	
Switching Frequency	F_{SW}		1.0	1.2	1.4	MHz
OVP threshold (PGOOD Output High)	$V_{FB\ OVP-}$	V_{FB} ramps up from V_{FB} nominal operating point	103%			V_{FB}
OVP threshold (Fault Detected)	$V_{FB\ OVP+}$	V_{FB} ramps up from V_{FB} nominal operating point			111%	V_{FB}
OVP Hysteresis				25		mV
PGOOD, Output High	$V_{FB\ OVP+}$	Ramp up V_{FB}, starting at V_{FB}≤700mV	94%		98.5%	V_{FB}
PGOOD, Output Low	$V_{FB\ OVP-}$	Ramp down V_{FB},starting at V_{FB}= $V_{FB\ nom}$			95%	V_{FB}
PGOOD output low voltage		ISINK = 6mA			0.4	V
PGOOD Deglitch Time				160		μs
Line Regulation		4.5V≤V_{IN}≤5.5V, I_{OUT}=100mA		0.1		%
Load Regulation		0A ≤I_{OUT}≤ 2A		0.1		%

Notes:

5) Production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.

6) Guaranteed by design

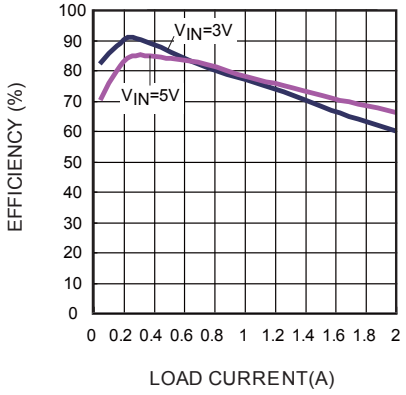
PIN FUNCTIONS

Pin #	Name	Description
1	FB	Feedback input. An external resistor divider from the output to GND, tapped to the FB pin sets the output voltage.
2	GND	Ground pin. This pin is the reference ground of the regulated output voltage. For this reason care must be taken in PCB layout. Suggested to be connected to GND with copper and vias. Connect exposed pad to ground plane for proper thermal performance.
3	SW	Switch node to the inductor
4	PVIN	Input supply pin for power FET
5	VIN	Input Supply pin for controller
6	PGOOD	Power-good indicator output. “Low” output indicates output is outside the window of regulation level. PGOOD is pulled down in shutdown. PGOOD output has 160us deglitch timer to avoid false trigger during transient response.

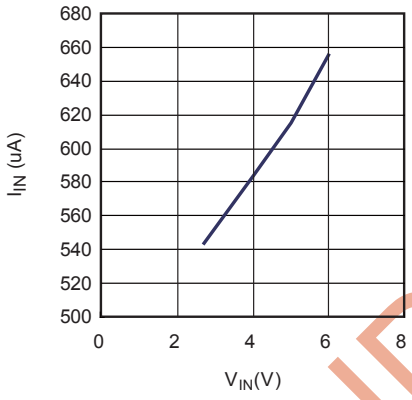
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 1.2V, T_A = +25°C, unless otherwise noted.

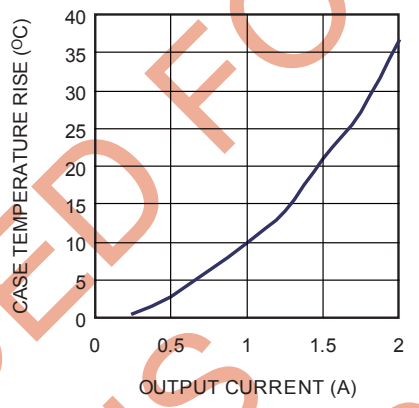
Efficiency vs. Load Current



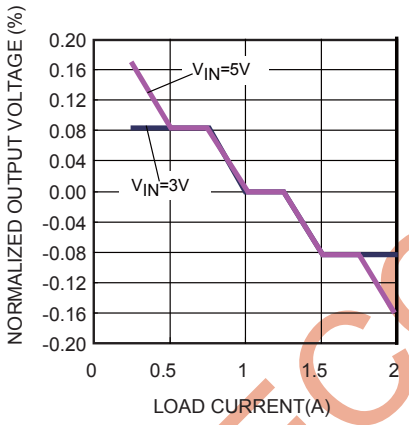
Enabled Supply Current vs. Input Voltage



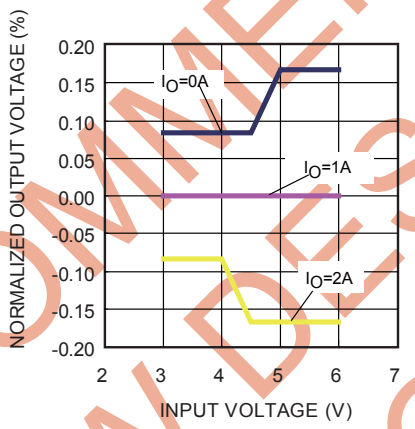
Case Temperature Rise vs. Output Current



Load Regulation



Line Regulation

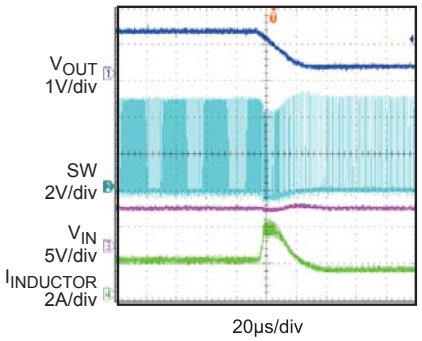


Ipeak vs. Duty

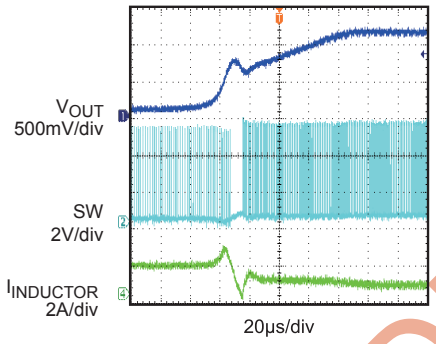
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, T_A = +25°C, unless otherwise noted.

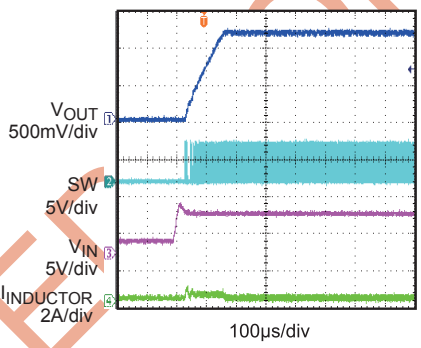
Short Entry
Full Load



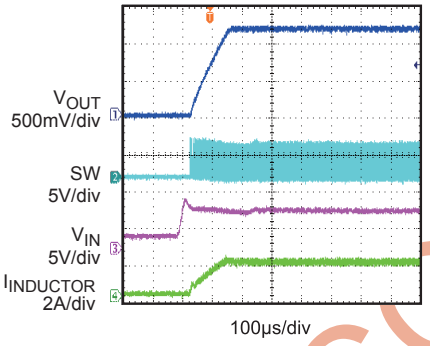
Short Recovery
Full Load



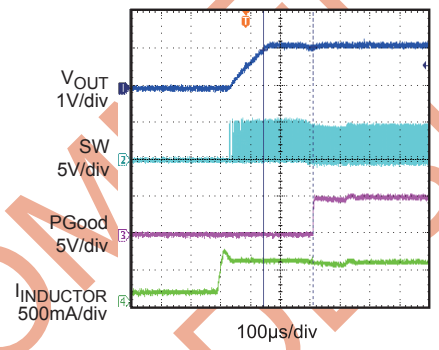
Power Up without Load



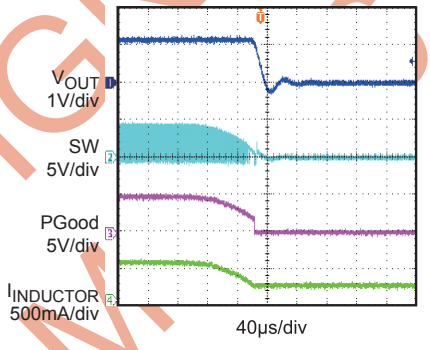
Power Up with 2A Load



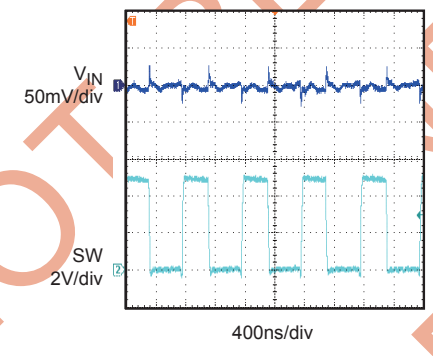
Power Good



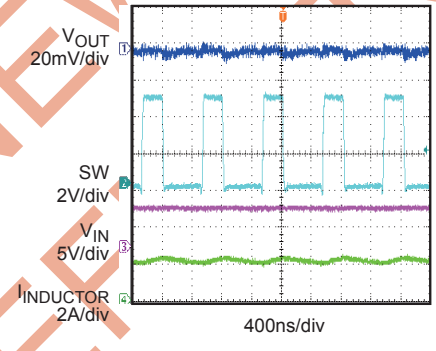
Power Good



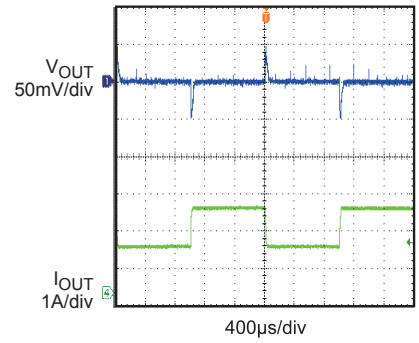
Input Ripple Voltage
Full Load



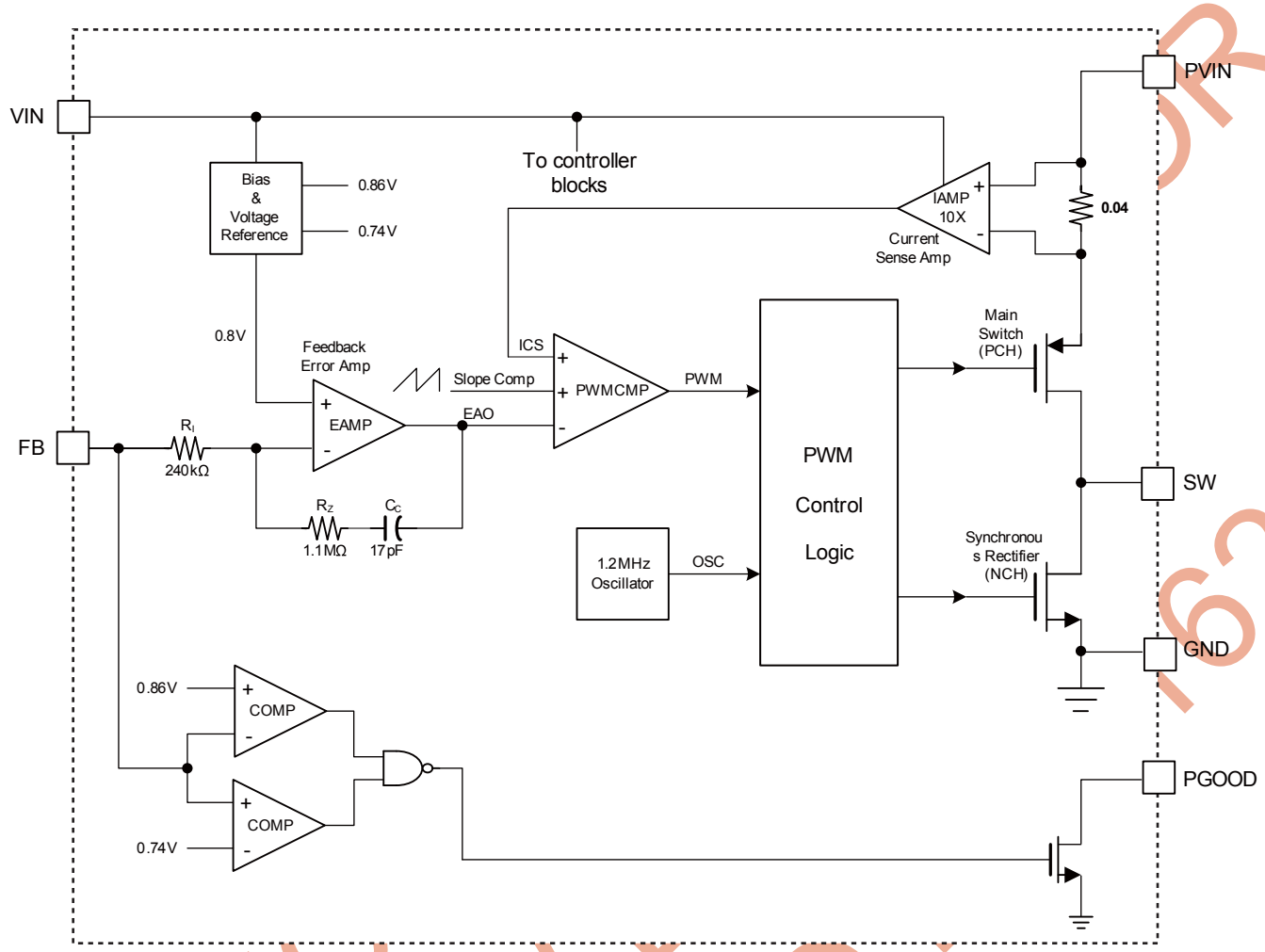
Output Ripple Voltage
I_{OUT}=2A



Load Transient Response
I_{OUT}=1A-2A



FUNCTIONAL BLOCK DIAGRAM



OPERATION

The MP2127 is a fixed frequency 1.2MHz current mode 2A step-down converter, optimized for low voltage, Li-Ion battery powered applications where high efficiency and small size are critical. MP2127 integrates a high side PFET main switch and a low side synchronous rectifier. It always operates in continuous conduction mode, simplifies the control scheme and eliminates the random spectrum noise due to discontinuous conduction mode.

The steady state duty cycle D for this mode can be calculated as:

$$D = T_{ON} \times f_{OSC} \times 100\% \approx \frac{V_{OUT}}{V_{IN}} \times 100\%$$

Where T_{ON} is the main switch on time and f_{OSC} is the oscillator frequency (1.2MHz typ.).

Current Mode PWM Control

Slope compensated current mode PWM control provides stable switching and cycle-by-cycle current limiting for superior load and line response as well as protection of the internal main switch and synchronous rectifier. The MP2127 switches at a constant frequency (1.2MHz) and modulates the inductor peak current to regulate the output voltage. Specifically, for each cycle the PWM controller forces the inductor peak current to an internal reference level derived from the feedback error voltage. At normal operation, the main switch is turned on at each rise edge of the internal oscillator, and remains on for a certain period of time to ramp up the inductor current. As soon as the inductor current reaches the reference level, the main switch is turned off and immediately the synchronous rectifier will be turned on to provide the inductor current. In forced PWM mode, the synchronous rectifier will stay on until the next oscillator cycle.

Dropout Operation

The MP2127 allows the main switch to remain on for more than one switching cycle to increase the duty cycle when the input voltage is dropping close to the output voltage. When the duty cycle reaches 100%, the main switch is held on continuously to deliver current to the output up to the PFET current limit. In this case, the output voltage becomes the input voltage minus the voltage drop across the main switch and the inductor.

Maximum Load Current

The MP2127 can operate down to 2.7V input voltage; however the maximum load current decreases at lower input due to a large IR drop on the main switch and synchronous rectifier. The slope compensation signal reduces the peak inductor current as a function of the duty cycle to prevent sub-harmonic oscillations at duty cycles greater than 50%. Conversely, the current limit increases as the duty cycle decreases.

Short Circuit Protection

When the output is shorted to ground, the oscillator frequency is reduced to prevent the inductor current from increasing beyond the PFET current limit. The PFET current limit is also reduced to lower the short circuit current. The frequency and current limit will return to the normal values once the short circuit condition is removed and the feedback voltage approaches 0.8V.

PGOOD Indicator

MP2127 provides an open-drain PGOOD output that becomes high-impedance (open circuit) after output level reaches regulation after startup. PGOOD is pulled low if the output goes out of regulation level for more than the de-glitch time of 160us, or when device enters shutdown.

APPLICATION INFORMATION

Output Voltage Setting

The output voltage is set by the external resistor divider:

$$V_{OUT} = 0.8 \cdot (1 + \frac{R_1}{R_2})$$

The divider ratio also affects the loop bandwidth of the step-down converter. The approximate relationship between them is given below:

$$BW \propto \frac{1}{R_1 + 240k \cdot (1 + \frac{R_1}{R_2})}$$

To minimize the impact of R1 to loop bandwidth, one should choose R1 much smaller than 240k. Some recommended value for common output voltage is listed below:

Table 1—Resistor Selection vs. Output Voltage Setting

V_{OUT}	R1	R2
1.2V	20kΩ (1%)	40.2kΩ (1%)
1.8V	49.9kΩ (1%)	40.2kΩ (1%)
2.5V	84.5kΩ (1%)	40.2kΩ (1%)

Inductor Selection

A 1μH to 10μH inductor with DC current rating at least 25% higher than the maximum load current is recommended for most applications. For best efficiency, the inductor DC resistance shall be <200mΩ. See Table 2 for recommended inductors and manufacturers. For most designs, the inductance value can be derived from the following equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is inductor ripple current. Choose inductor ripple current approximately 30% of the maximum load current, 2A.

The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Table 2—Suggested Inductors

Manufacturer	Part Number	Inductance (μH)	Dimensions LxWxH (mm^3)
TOKO	B1015AS-3R0N	3	8.4X8.3X4
TDK	RLF7030T-3R3M4R1	3.3	7.3X6.8X3.2

Input Capacitor C_{IN} Selection

The input capacitor reduces the surge current drawn from the input and switching noise from the device. The input capacitor impedance at the switching frequency shall be less than input source impedance to prevent high frequency switching current passing to the input

Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 10μF capacitor is sufficient.

Output Capacitor COUT Selection

The output capacitor keeps output voltage ripple small and ensures regulation loop stable. The output capacitor impedance shall be low at the switching frequency. Ceramic capacitors with X5R or X7R dielectrics are recommended. For forced PWM mode operation, the output ripple ΔV_{OUT} is approximately:

$$\Delta V_{OUT} = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{V_{IN} \cdot f_{OSC} \cdot L} (R_{ESR} + \frac{1}{8} \cdot \frac{1}{f_{OSC} \cdot C_{OUT}})$$ F

or most applications, a 33μF capacitor is sufficient.

Thermal Dissipation

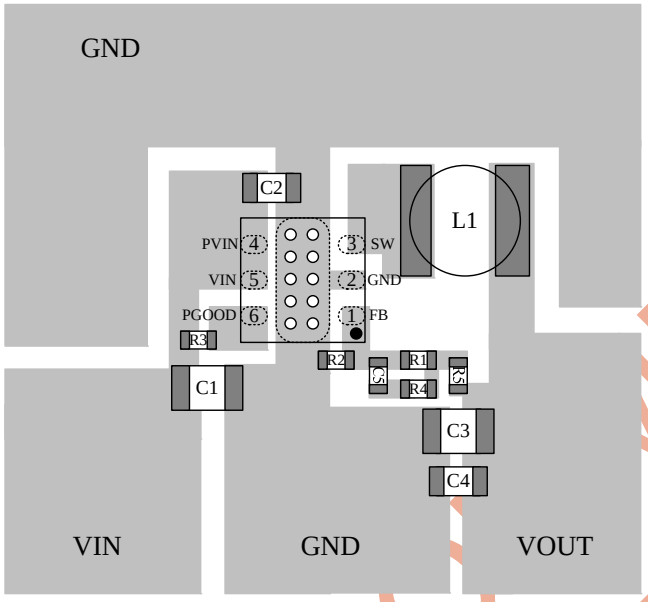
Power dissipation shall be considered when operates MP2127 at maximum 2A output current. If the junction temperature rises above 150°C, MP2127 will be shut down by internal thermal protection circuitry.

The junction-to-ambient thermal resistance of the 6-pin QFN (3mm x 3mm) $R_{\Theta JA}$ is 50°C/W. The maximum allowable power dissipation is about1.6W when MP2127 is operating in a 70°C ambient temperature environment:

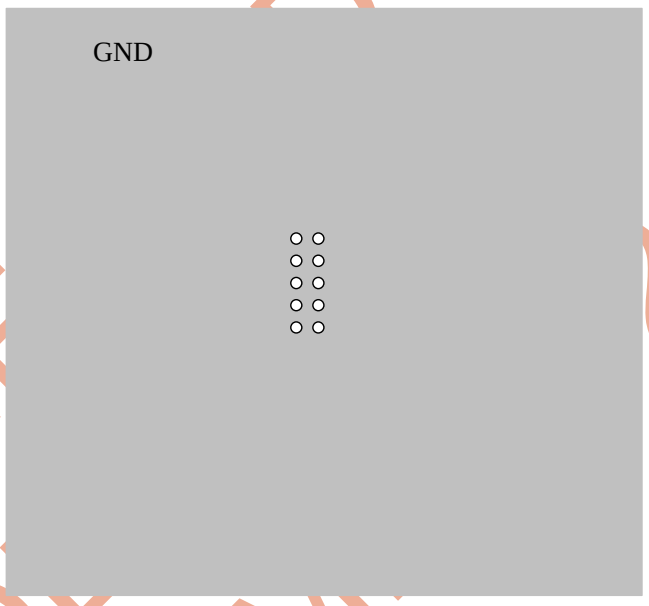
$$PD_{MAX} = \frac{150^{\circ}C - 70^{\circ}C}{50^{\circ}C/W} = 1.6W$$

PC Board Layout

The high current paths (GND, IN and SW) should be placed very close to the device with short, direct and wide traces. Input capacitors should be placed as close as possible to the respective IN and GND pins. The external feedback resistors shall be placed next to the FB pins. Keep the switching nodes SW short and away from the feedback network.



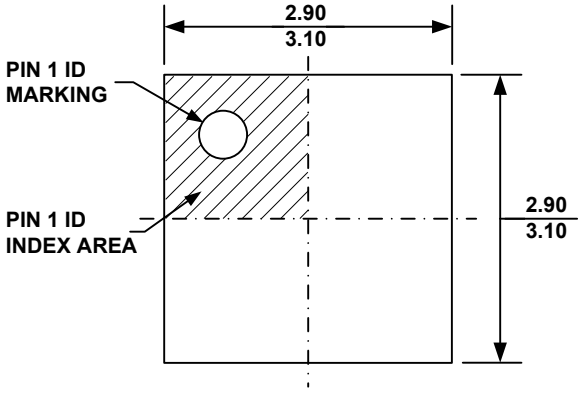
Top Layer



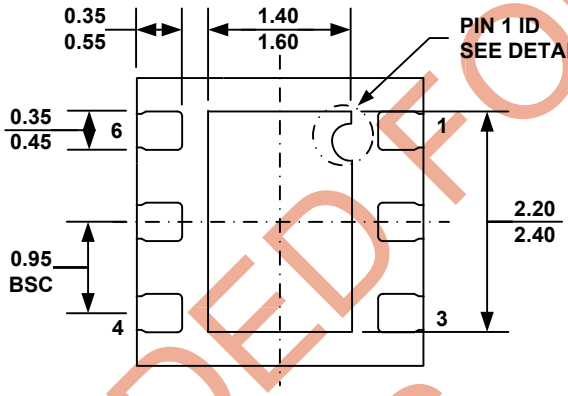
Bottom Layer

PACKAGE INFORMATION

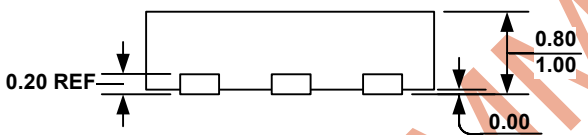
QFN6 (3mmx3mm)



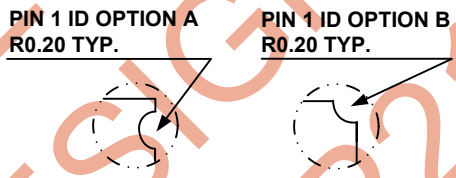
TOP VIEW



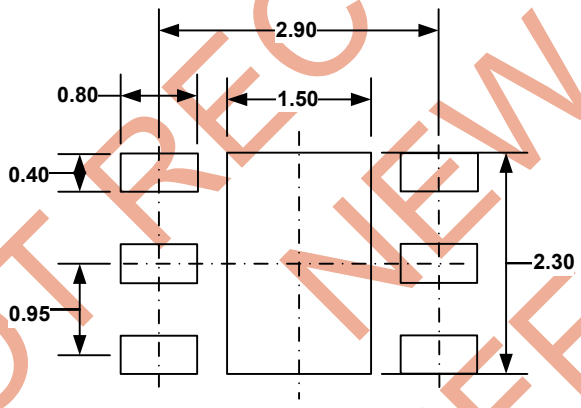
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) JEDEC REFERENCE IS MO-229, VARIATION VEEA-2.
5) DRAWING IS NOT TO SCALE.