MP2122

6V, 2A, Low Quiescent Current Dual, SYNC Buck Regulator

The Future of Analog IC Technology

DESCRIPTION

The MP2122 is an internally-compensated, 1MHz fixed-frequency, dual PWM, synchronous, step-down regulator. The MP2122 operates from a 2.7V-to-6V input, generates an output voltage as low as 0.608V, and has a 45μA quiescent current that makes it ideal for powering portable equipment that runs on a single cell lithium-ion (Li+) battery.

The MP2122 integrates dual 80mΩ high-side switches and 35mΩ synchronous rectifiers for high efficiency without an external Schottky diode. Peak-current mode control and internal compensation limits the minimum number of readily-available external components.

Fault-condition protections include cycle-by-cycle current limiting and thermal shutdown.

The MP2122 is available in an 8-pin TSOT23-8 package.

FEATURES

- Dual 2A-Output Current
- >93% Peak Efficiency
- >80% Light-Load Efficiency
- Wide 2.7V-to-6V Operating Input Range
- 80mΩ and 35mΩ Internal Power MOSFET
- 1MHz Fixed Switching Frequency
- Adjustable Output from 0.608V to VIN
- 180° Phase-Shifted Operation
- 100% Duty-Cycle Operation
- 45μA Quiescent Current
- Cycle-by-Cycle Over-Current Protection
- Short-Circuit Protection with Hiccup Mode
- Thermal Shutdown
- Available in an 8-pin TSOT23-8 Package

APPLICATIONS

- Small/Handhold Devices
- DVD Drivers
- Portable Instruments
- Smartphones and Feature Phones
- Battery-Powered Devices

All MPS parts are lead-free and adhere to the RoHS directive. For MPS green status, please visit MPS website under Quality Assurance.

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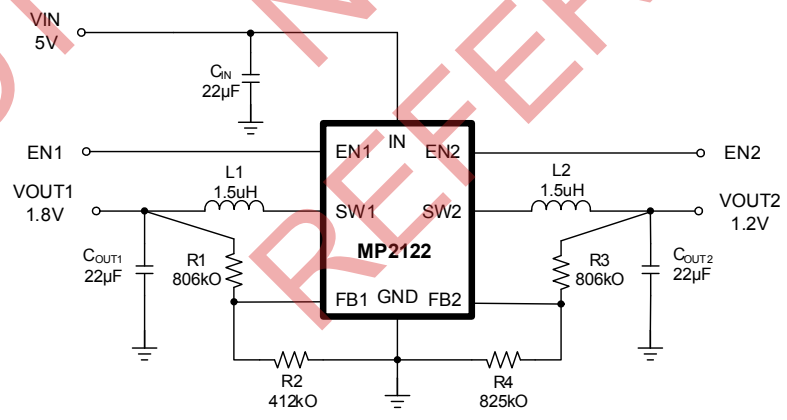
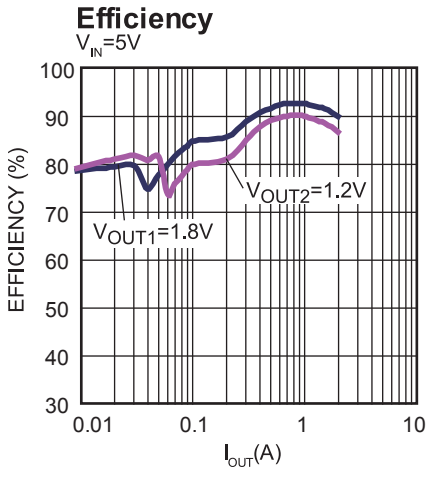
TYPICAL APPLICATION





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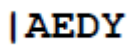
ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2122GJ	TSOT23-8	*See Below*

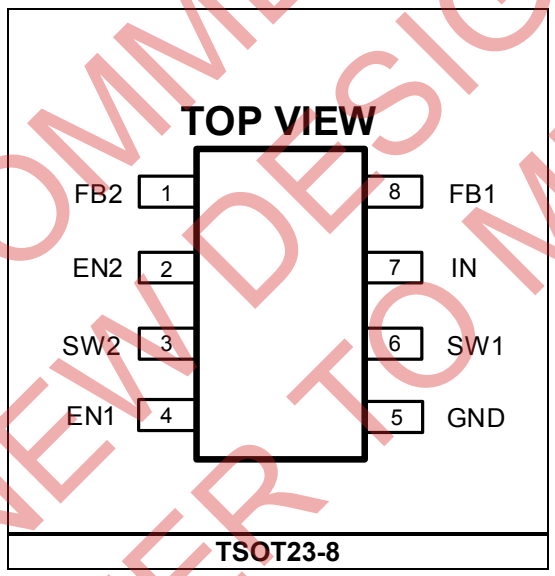
* For Tape & Reel, add suffix –Z (e.g. MP2122GJ–Z);

TOP MARKING



AED: product code of MP2122GJ
Y: year code

PACKAGE REFERENCE



TSOT23-8

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage VIN 6.5V
V_{SW} –0.3V (-3V for<10ns) to 6.5V (7.5V for<10ns)
All Other Pins ..... –0.3V to +6.5 V
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Continuous Power Dissipation (T_A = +25°C) (2)
..... 1.25W
Storage Temperature ..... –65°C to +150°C

Recommended Operating Conditions

Supply Voltage V_{IN} ..... 2.7V to 6V
Output Voltage V_{OUT} ..... 0.608V to 5.5V
Operating Junction Temp. ..... -40°C to +125°C

Thermal Resistance (3)

	θ_{JA}	θ_{JC}
TSOT23-8	100	..... 55 °C/W

Notes:

1) Absolute maximum ratings are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS (4)

VIN = V_{EN} = 3.6V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current (Quiescent)	I_Q	VIN=3.6V, V_{EN}=2V, V_{FB} = 0.65V	35	45	55	µA
Shutdown Current		V_{EN} = 0V		0	1	µA
IN Under-Voltage Lockout Threshold		Rising edge	2.4	2.5	2.6	V
IN Under-Voltage Lockout Hysteresis				300		mV
Regulated FB Voltage	V_{FB}	T_A = +25°C	0.596	0.608	0.620	V
FB Input Current		V_{FB} = 0.608V		±10	50	nA
EN, HIGH Threshold		–40°C ≤ T_A ≤ +85°C	1.2			V
EN, LOW Threshold		–40°C ≤ T_A ≤ +85°C			0.4	V
Internal Soft-Start Time	τ_{SS}			0.5		ms
High-Side Switch, ON-Resistance	R_{DSON_P}	VIN=5V		80		mΩ
Low-Side Switch, ON-Resistance	R_{DSON_N}	VIN=5V		35		mΩ
SW Leakage Current		V_{EN} = 0V; VIN = 6V V_{SW} = 0V and 6V	–1	0	1	µA
High-Side Switch, Current Limit		Sourcing, D=40%	2.8	3.5	4.5	A
Oscillator Frequency		Both channels work in CCM	0.8	1	1.2	MHz
Phase Shift				180		degree
Minimum ON Time(5)	τ_{ON_MIN}			90		ns
Minimum OFF Time	τ_{OFF_MIN}			100		ns
Maximum Duty Cycle				100		%
Thermal Shutdown Threshold(5)		Hysteresis = 30°C		160		°C

Notes:

4) Production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.

5) Guarantee by design

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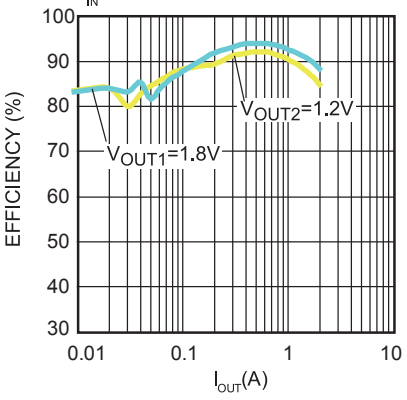
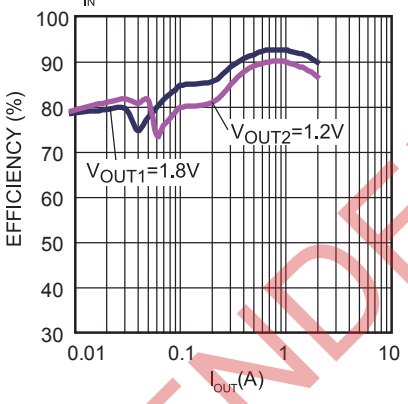
TYPICAL PERFORMANCE CHARACTERISTICS

VIN = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L = 1.5µH, C_{OUT1}=C_{OUT2}=22µF, T_A = 25°C, unless otherwise noted.

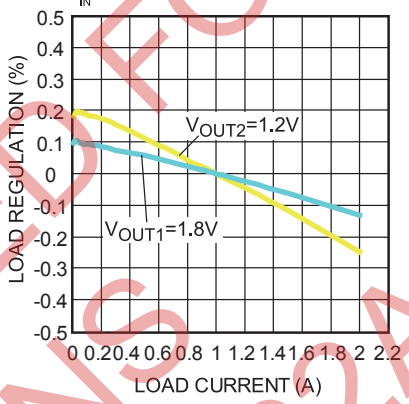
Efficiency
V_{IN}=3.6V



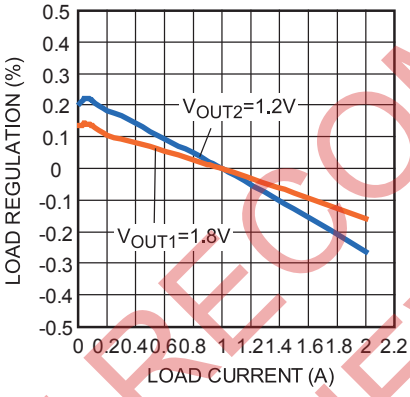
Efficiency
V_{IN}=5V



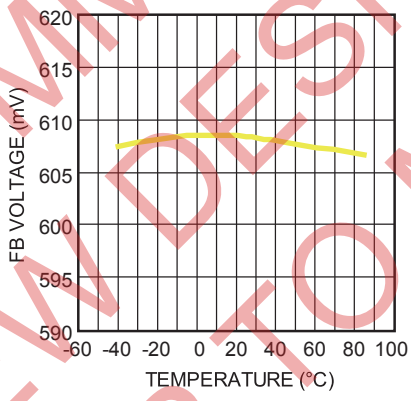
Load Regulation
V_{IN}=3.6V



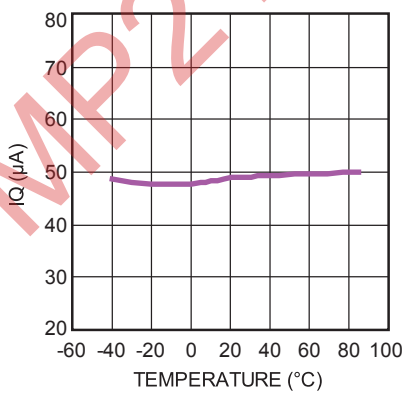
Load Regulation
V_{IN}=5V



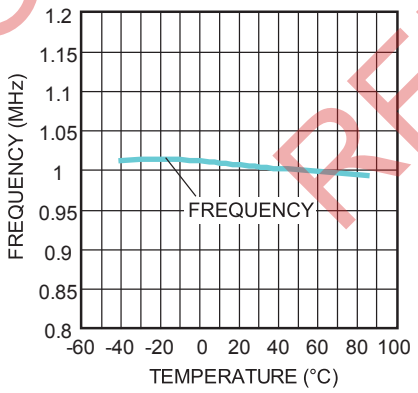
FB Votage vs. Temperature



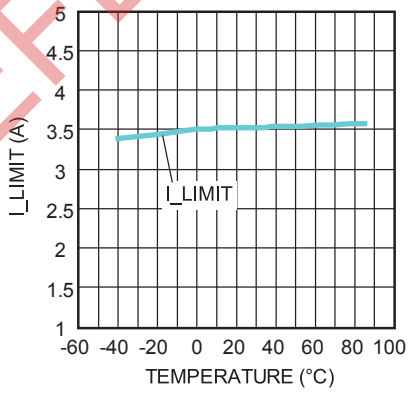
Quiescent Current vs. Temperature



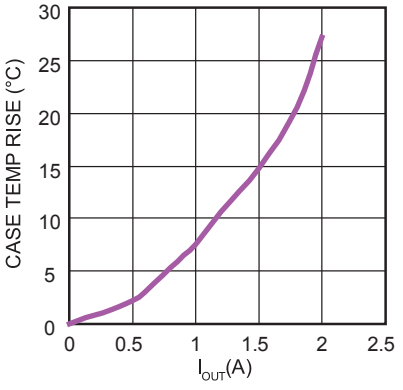
Frequency vs. Temperature
Both channel on



I_Limit vs. Temperature



Case Temp Rise
Both channel on



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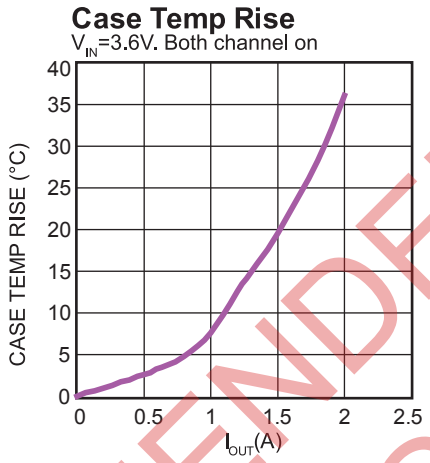
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L = 1.5µH, C_{OUT1}=C_{OUT2}=22µF, T_A = 25°C, unless otherwise noted.



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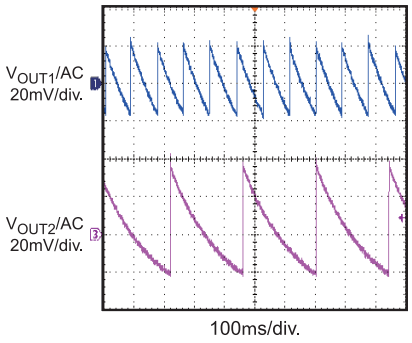
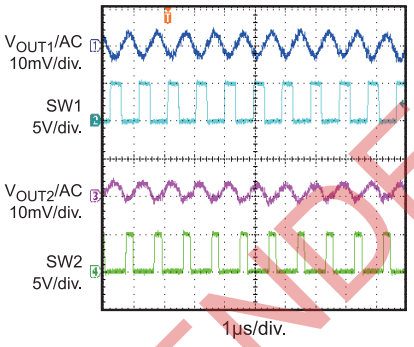
VIN = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L = 1.5µH, C_{OUT1}=C_{OUT2}=22µF, T_A = 25°C, unless otherwise noted.

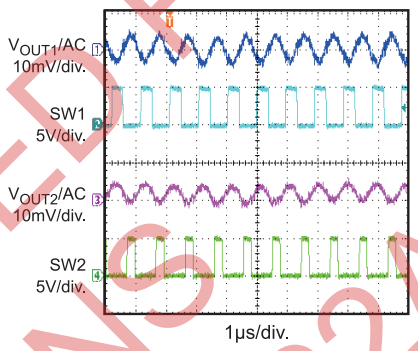
Output ripple
I_{OUT1} = I_{OUT2}= 0A



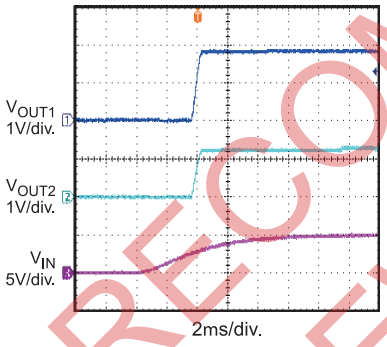
Output ripple
I_{OUT1} = I_{OUT2}= 1A



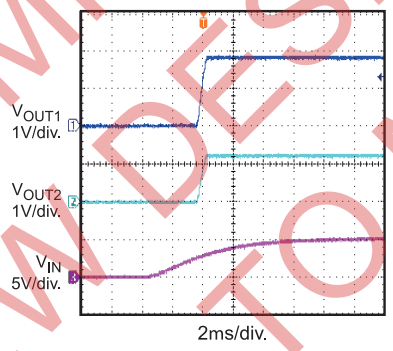
Output ripple
I_{OUT1} = I_{OUT2}= 2A



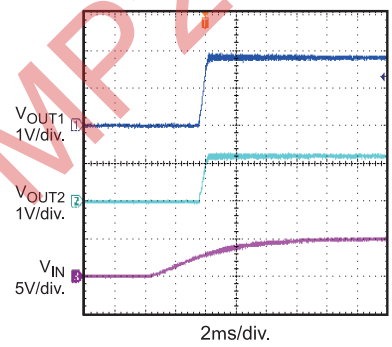
Vin power up without load
I_{OUT1} = I_{OUT2}= 0A



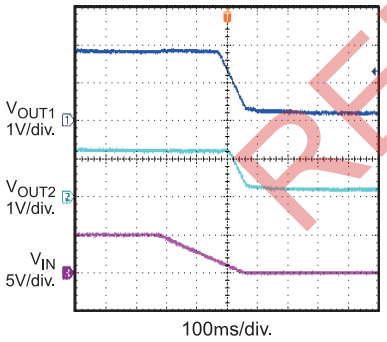
Vin power up half oad
I_{OUT1} = I_{OUT2}= 1A



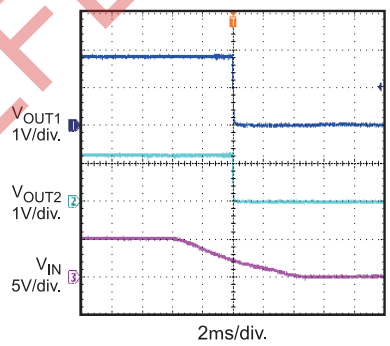
Vin power up full load
I_{OUT1} = I_{OUT2}= 2A



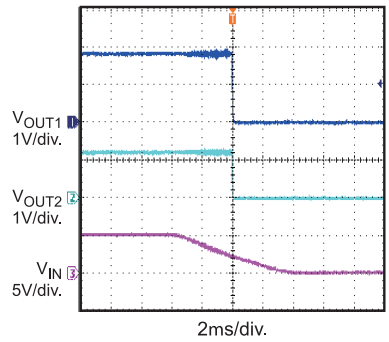
Vin power down without load
I_{OUT1} = I_{OUT2}= 0A



Vin power down half load
I_{OUT1} = I_{OUT2}= 1A



Vin power down full load
I_{OUT1} = I_{OUT2}= 2A



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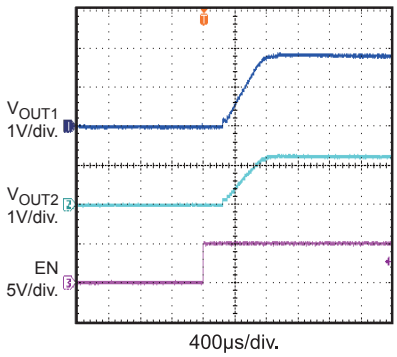
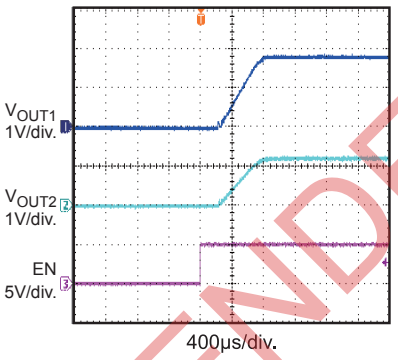
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L = 1.5µH, C_{OUT1}=C_{OUT2}=22µF, T_A = 25°C, unless otherwise noted.

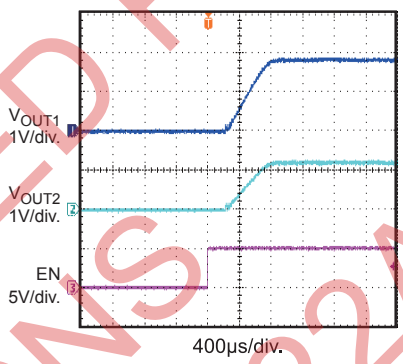
EN on without load
I_{OUT1} = I_{OUT2}= 0A



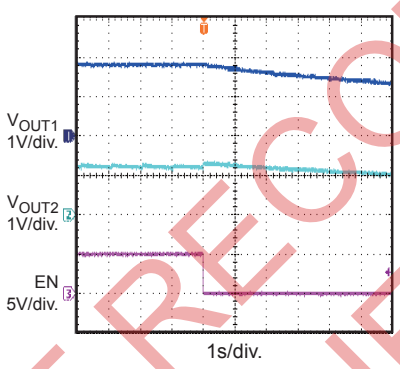
EN on with half load
I_{OUT1} = I_{OUT2}= 1A



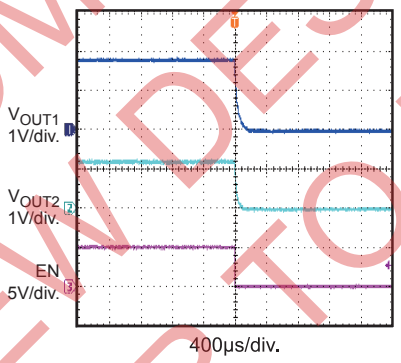
EN on with full load
I_{OUT1} = I_{OUT2}= 2A



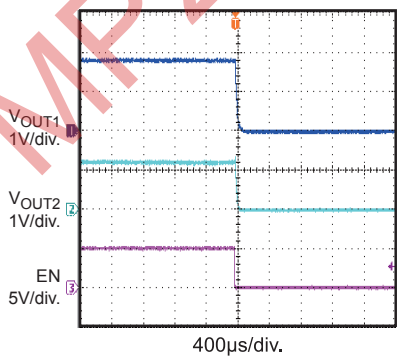
EN down without load
I_{OUT1} = I_{OUT2}= 0A



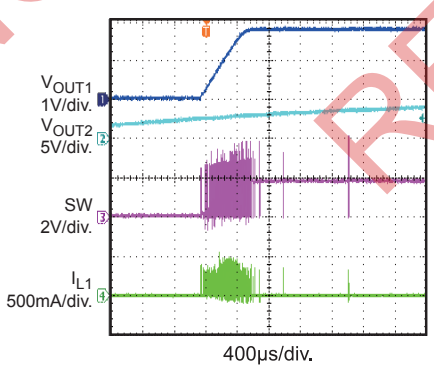
EN down with half load
I_{OUT1} = I_{OUT2}= 1A



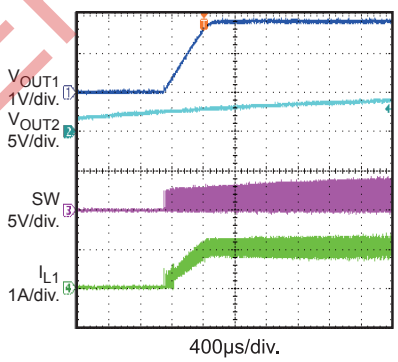
EN down with full load
I_{OUT1} = I_{OUT2}= 2A



Vin Power On without load
I_{OUT1} = I_{OUT2}= 0A



Vin Power On
I_{OUT1} =1A, I_{OUT2}= 0A



Vin Power On
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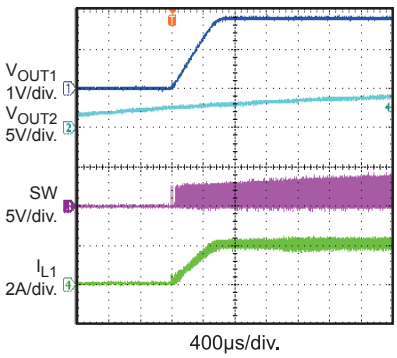

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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

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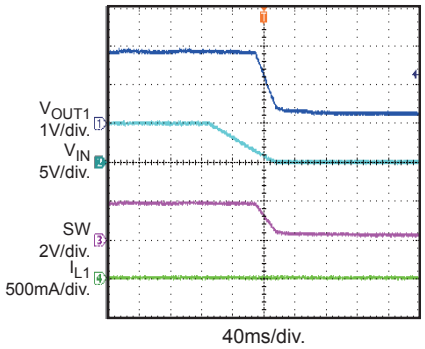
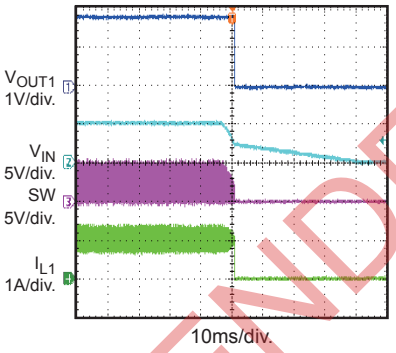
Vin Power down
I_{OUT1} = I_{OUT2}= 0A



Vin Power down
I_{OUT1} = 1A, I_{OUT2}= 0A



Vin Power down
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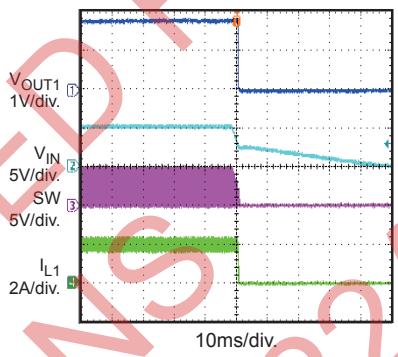

Enable on
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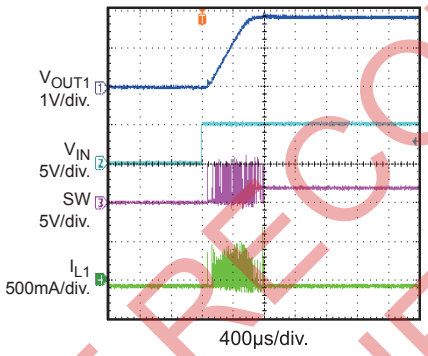
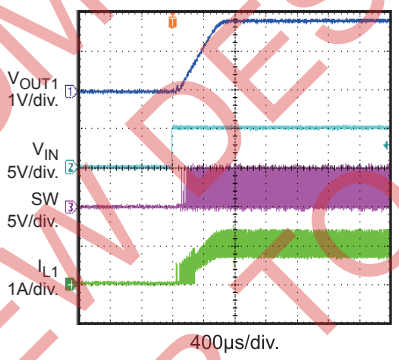
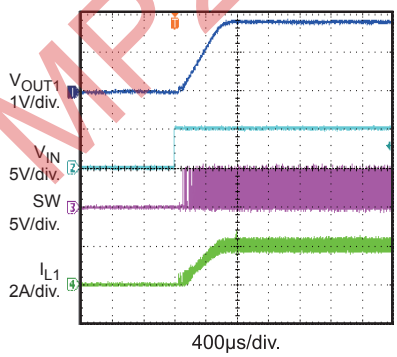


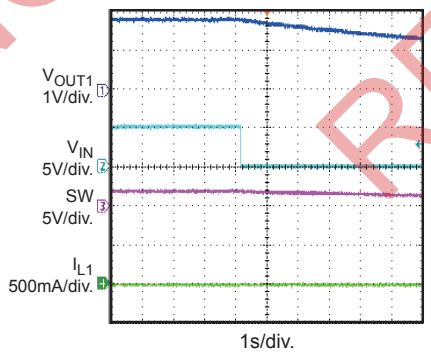
Enable on
I_{OUT1} = 1A, I_{OUT2}= 0A



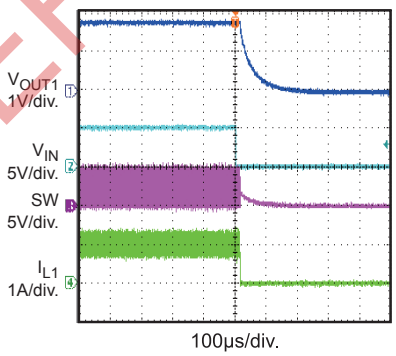
Enable on
I_{OUT1} = 2A, I_{OUT2}= 0A



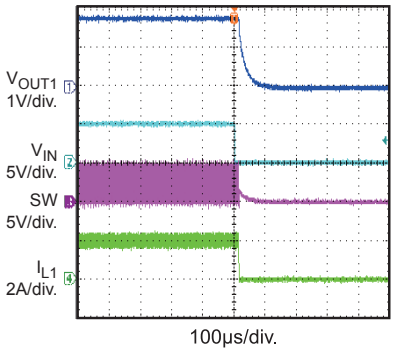
Enable down
I_{OUT1} = I_{OUT2}= 0A



Enable down
I_{OUT1} =1A, I_{OUT2}= 0A



Enable down
I_{OUT1} = 2A, I_{OUT2}= 0A



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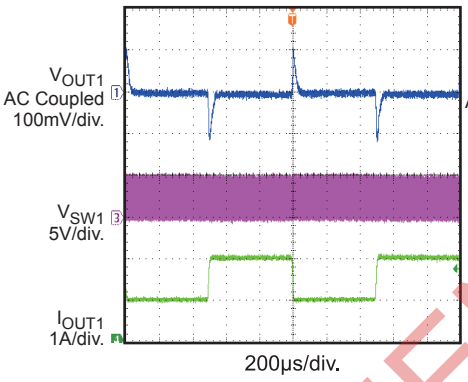
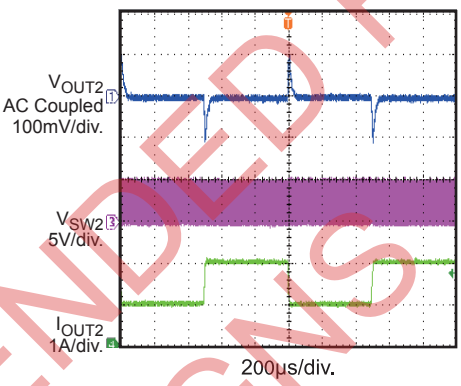
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L = 1.5µH, C_{OUT1}=C_{OUT2}=22µF, T_A = 25°C, unless otherwise noted.

Load Transient
1A Transient to 2A, 2.5A/µS speed



Load Transient
1A Transient to 2A, 2.5A/µS speed



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PIN FUNCTIONS

Package Pin #	Name	Description
1	FB2	Feedback 2. Error amplifier input. Connect to the tap of an external resistor divider between the output and GND. Sets the regulation voltage.
2	EN2	Channel 2 Enable. Buck.
3	SW2	Switch Node Connects to the channel 2 internal high-side and low-side power MOSFETs..Connects to the inductor.
4	EN1	Channel 1 Enable. Buck.
5	GND	Ground.
6	SW1	Switch Node Connects to the channel 1 internal high-side and low-side power MOSFETs..Connects to the inductor.
7	IN	Input Supply. Requires a decoupling capacitor to ground to reduce switching spikes.
8	FB1	Feedback 1. Error amplifier input. Connect to the tap of an external resistor divider between the output and GND. Sets the regulation voltage.

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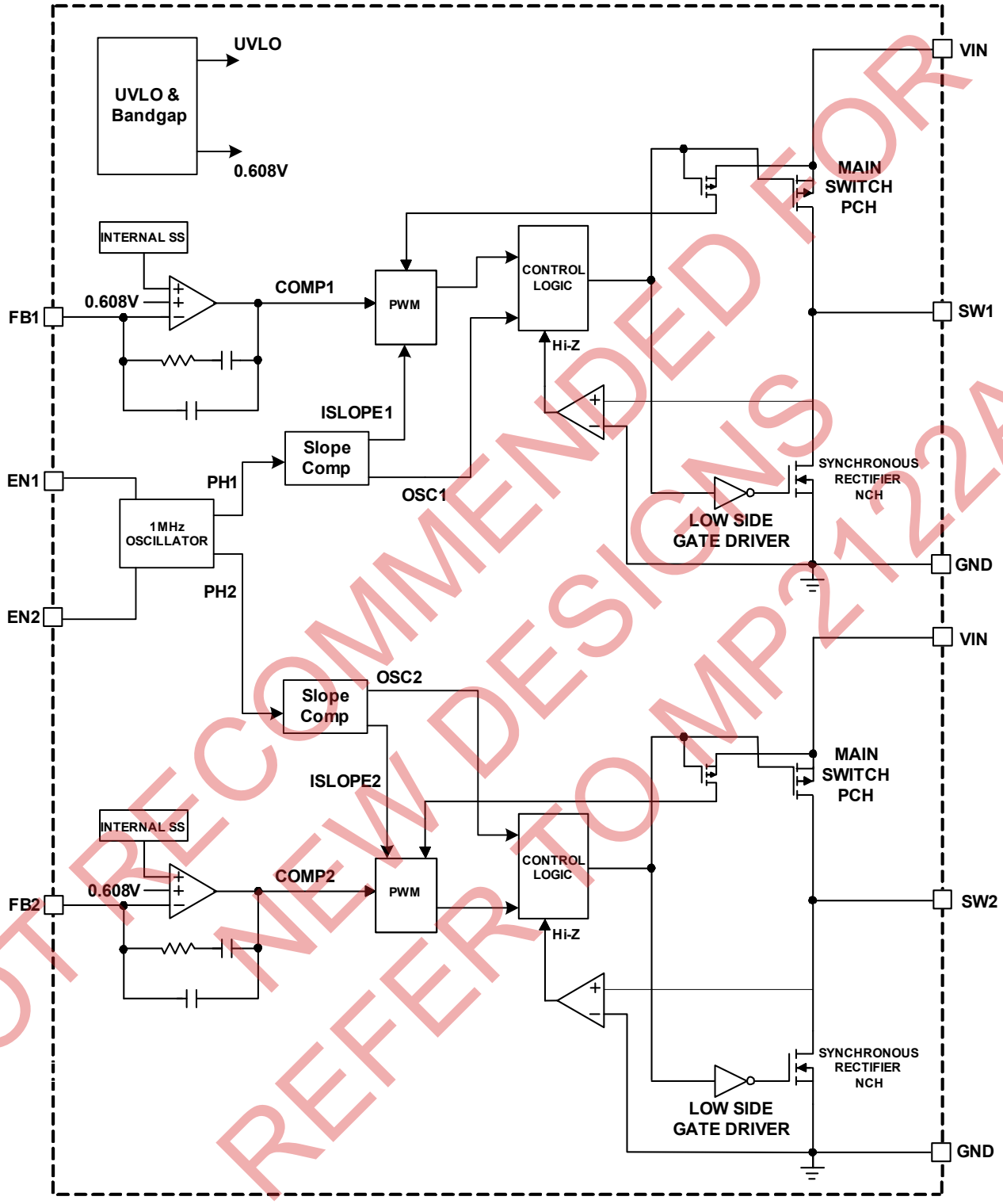

Figure 1: Functional Block Diagram

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OPERATION

MP2122 is a fully-integrated, dual-channel, synchronous, step-down converter. Both channels have peak-current modes with internal compensation for faster transient responses and cycle-by-cycle current limits.

MP2122 is optimized for low-voltage, portable applications where efficiency and small size are critical.

180° Phase-Shift

By default, the MP2122's two channels operate at a 180° phase-shift to reduce input current ripple: The smaller current ripple allows for a smaller input bypass capacitor. In CCM, two internal clocks control the switching: The high-side MOSFET turns on at the corresponding CLK's rising edge.

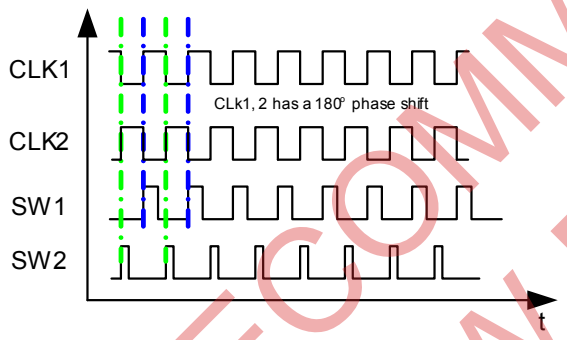

Figure 2: Clock/Switching Timing

However, the switching frequency for each channel falls when operating at low dropout, so the MP2122 operates at a default switching frequency of 1MHz with a fixed OFF time. After the input voltage recovers, switching for PWM mode resumes normally and synchronizes with the master oscillator for phase-shifted operation.

Light-Load Operation

In light loads, the MP2122 uses a proprietary control scheme to save power and improve efficiency. The MP2122 will turn off the low side switch when inductor current starts to reverse. Then MP2122 works in discontinuous conduction mode (DCM) operation.

When either channel enters DCM or low-dropout operation, this channel will not be controlled by the internal 1MHz oscillator.

	Condition		Mode	
	CH1	CH2	CH1	CH2
1	Heavy Load		1MHz CCM	1MHz CCM,0° Phase
2	Light Load		DCM	DCM
3	Low Dropout		Fixed OFF Time	Fixed OFF Time
4	Heavy Load	Light Load	0.95MHz CCM	DCM
5	Light Load	Heavy Load	DCM	0.95MHz CCM
6	Heavy Load	Low Dropout	0.95MHz CCM	Fixed OFF Time
7	Low Dropout	Heavy Load	Fixed OFF Time	0.95MHz CCM
8	Light Load	Low Dropout	DCM	Fixed OFF Time
9	Low Dropout	Light Load	Fixed OFF Time	DCM

Soft Start

MP2122 has a built-in soft start that ramps up the output voltage at a controlled slew rate to start-up overshoot. The soft-start time is ~0.5ms.

Current Limit and Short-Circuit Recovery

Each channel's high-side switch has a 3.5A (typ.) current limit. The MP2122 treats any current-limit condition that remains for 400us as a short and enter hiccup mode.

The MP2122 disables its output power stage in hiccup mode, and then slowly discharges the soft-start capacitor before initiating soft-start. If the short-circuit condition remains, the MP2122 repeats this operation till the short circuit disappears and output returns to the regulation level.

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APPLICATION INFORMATION

COMPONENT SELECTION

Output Voltage

External resistor dividers connected to the FB pins set the output voltages. The feedback resistor connected to FB1 (R1) also sets the feedback loop bandwidth (f_C).

f_C does not exceed $0.1 \times f_{SW}$. When using a ceramic output capacitor (C_O), set the range to 50kHz and 100kHz for optimal transient performance and good phase margin. When using an electrolytic capacitor, set the loop bandwidth no higher than 1/4 the ESR zero frequency (f_{ESR}). f_{ESR} is:

$$f_{ESR} = \frac{1}{2\pi \cdot R_{ESR} \cdot C_O}$$

We suggest using a 600k to 800k resistor for R1 when C_O=22µF. R2 is then:

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.608V} - 1}$$

Table 1: Resistor Values vs. Output Voltage

V_{OUT}	R1	R2	L	C_{OUT} (Ceramic)
1.2V	806kΩ	825kΩ	0.47µH-2.2µH	22µF
1.5V	806kΩ	549kΩ	0.47µH-2.2µH	22µF
1.8V	806kΩ	412kΩ	0.47µH-2.2µH	22µF
2.5V	806kΩ	261kΩ	1µH-4.7µH	22µF
3.3V	806kΩ	182kΩ	1µH-4.7µH	22µF

Inductor Selection

Use a 1.5µH-to-2.2µH inductor with a DC current rating of at least 1.25 times the maximum load current for most applications. For best efficiency, select an inductor with a DC resistance <20mΩ. See Table 2 for recommended inductors. For most designs, estimate the inductance value using the following equation:

$$L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \cdot \Delta I_L \cdot f_{OSC}}$$

Where ΔI_L is the inductor ripple current. Select an inductor ripple current equal to approximately 30% of the maximum load current, 2A.

The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Table 2: Suggested Surface-Mount Inductors

Vendor	Part Number	L (µH)	DCR (mΩ)	SC (A)	L x W x H (mm^3)
WURTH					
	744777002	2.2	13	6	7.3×7.3×4.5
	744310200	2	14.2	6.5	7×6.9×3
TDK					
	RLF7030T-1R5N6R1-T	1.5	8	6.5	7.8×6.8×3.2

Input Capacitor

The input capacitor reduces the surge current drawn from the input and the switching noise from the device. Select an input capacitor with a switching-frequency impedance that is less than the input source impedance to prevent high-frequency-switching current from passing to the input source. Use low-ESR ceramic capacitors with X5R or X7R dielectrics with small temperature coefficients. For most applications, a 22µF capacitor is sufficient.

Output Capacitor

The output capacitor limits the output voltage ripple and ensures a stable regulation loop. Select an output capacitor with low impedance at the switching frequency. Use ceramic capacitors with X5R or X7R dielectrics. Using an electrolytic capacitor may result in additional output voltage ripple, thermal issues, and requires additional care in selecting the feedback resistor (R1) due to the large ESR. The output ripple (ΔV_{OUT}) is approximately:

$$\Delta V_{OUT} = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \cdot f_{OSC} \cdot L} \cdot \left(ESR + \frac{1}{8 \cdot f_{OSC} \cdot C_O} \right)$$

Power Dissipation

IC power dissipation plays an important role in circuit design—not only because of efficiency concerns, but also because of the chip's thermal requirements. Several parameters influence power dissipation, such as:

- Conduction Loss (Cond)
- Dead Time (DT)

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- Switching Loss (SW)
- MOSFET Driver Current (DR)
- Supply Current (S)

Based on these parameters, we can estimate the power loss as:

$$P_{LOSS} = P_{Cond} + P_{DT} + P_{SW} + P_{DR} + P_S$$

Thermal Regulation

As previously discussed, changes in IC temperature change the electrical characteristics, especially when the temperature exceeds the IC's recommended operating range. Managing the IC's temperature requires additional considerations to ensure that the IC runs below the maximum-allowable temperature. While operating the IC within recommended electrical limits is a major component to maintaining proper thermal regulation, specific layout designs can improve the thermal profile while limiting costs to either efficiency or operating range.

For the MP2122, connect the ground pin on the package to a GND plane on top of the PCB to use this plane as a heat sink. Connect this GND plane to GND planes beneath the IC using vias to further improve heat dissipation. However, given that these GND planes can introduce unwanted EMI noise and occupy valuable PCB space, design the size and shape of these planes to match the thermal resistance requirement:

$$\theta_{SA} = \theta_{JA} - \theta_{JC}$$

However, connecting the GND pin to a heat sink can not guarantee that the IC will not exceed its recommended temperature limits; for instance, if the ambient temperature exceeds the IC's temperature limits. If the ambient air temperature approaches the IC's temperature limit, options such as derating the IC so it operates using less power can help prevent thermal damage and unwanted electrical characteristics.

PCB Layout

Proper layout of the switching power supplies is very important, and sometimes critical for proper function: poor layout design can result in poor line or load regulation and stability issues.

Place the high-current paths (GND, IN and SW) very close to the device with short, direct, and wide traces. Place the input capacitor as close as possible to the IN and GND pins. Place the external feedback resistors next to the FB pin. Keep the switching node SW short and away from the feedback network. The circuit of below PCB layout is shown in Figure 4.

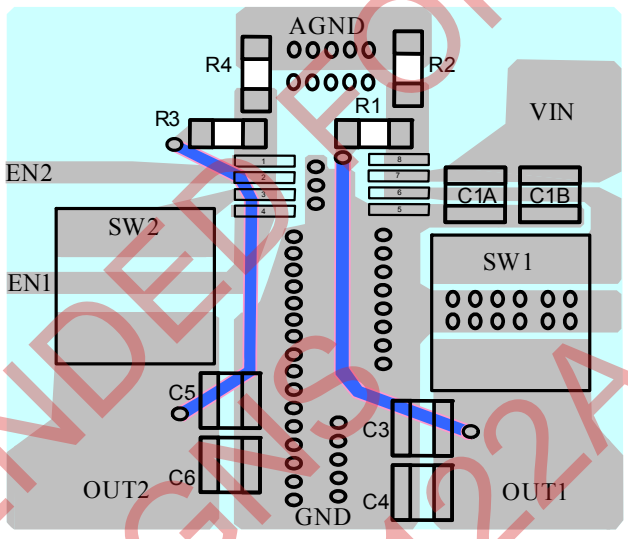

Figure 3: Suggested PCB Layout

Design Example

Below is a design example following the application guidelines for the specifications:

Table 3: Design Example

VIN	5V
VOUT1	1.8V
VOUT2	1.2V

The detailed application schematic is shown in Figure 4. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more device applications, please refer to the related Evaluation Board Datasheets.

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TYPICAL APPLICATION CIRCUITS

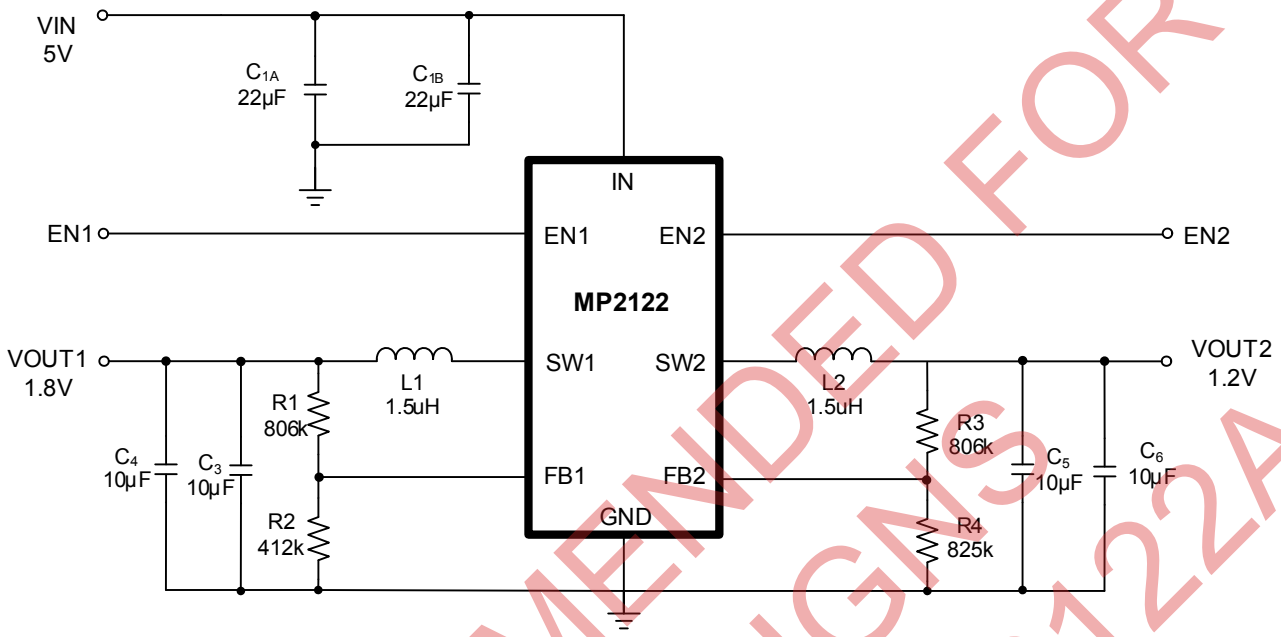

Figure 4: Typical Application Circuit

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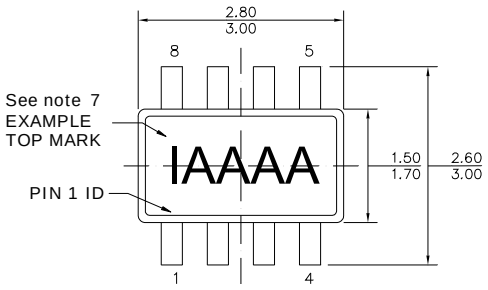
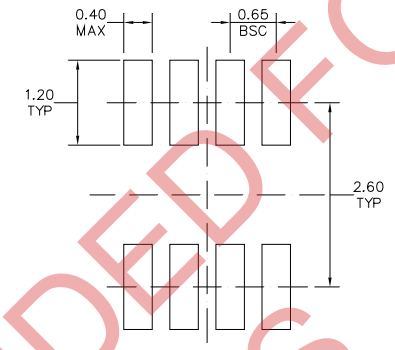
PACKAGE INFORMATION

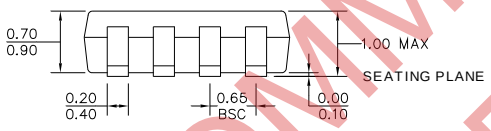
TSOT23-8



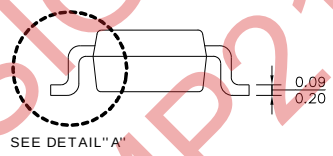
TOP VIEW



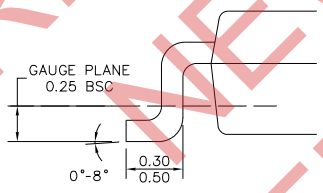
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION
4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO193, VARIATION BA
6) DRAWING IS NOT TO SCALE
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

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