MP20045

Low Noise, 1A Linear Regulator

The Future of Analog IC Technology

DESCRIPTION

The MP20045 is a low-dropout linear regulator supplies up to 1A current with 140mV dropout voltage. The output voltage is set externally which ranges from 1.5V to 5V by operating from +2.5V to +5.5V input or can be preset internally from 1.5V to 5V.

An internal PMOS pass element is used to allow a low 110μA ground current, making the MP20045 suitable for battery-power devices. Other features include low-power shutdown, short-circuit and thermal protection. The MP20045 is available in 8-pin QFN (3mm x 3mm) and SOIC8E packages.

FEATURES

- Up to 1A Output Current
- Low 140mV Dropout at 1A
- Low 110μA Ground Current
- Fixed Output Versions Ranging from 1.5V to 5V and Adjustable Versions
- Open Drain Power-Good Status Output
- 13μV_{RMS} Low Noise Output
- 56dB PSRR at 1kHz
- Current Limiting and Thermal Protection
- 3mm×3mm QFN8 and SOIC8E Packages

APPLICATIONS

- Notebook Computers
- Cordless Telephones
- Cellular Phones
- Modems
- Hand-Held Instruments
- PDA and Palmtop Computers

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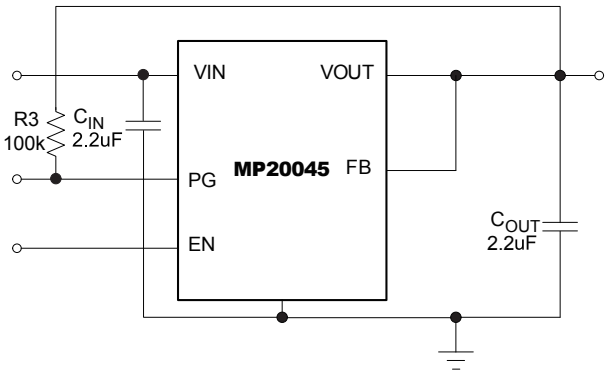
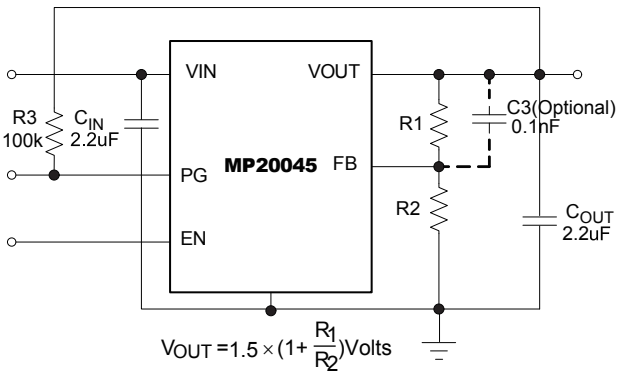
TYPICAL APPLICATION



Fixed Version



Adjustable Version

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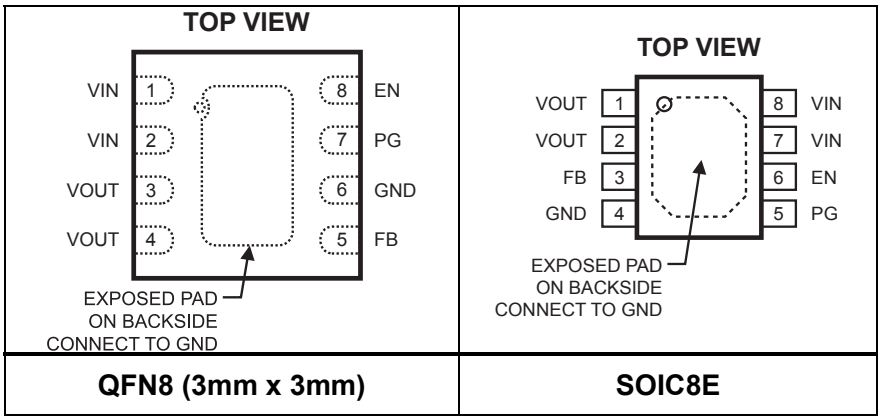
ORDERING INFORMATION

Part Number*	Output Voltage	Package	Top Marking	Free Air Temperature (T_A)
MP20045DQ**	Adjustable	QFN8 (3mm x 3mm)	8K	-40°C to +85°C
MP20045DQ-18**	1.8V	QFN8 (3mm x 3mm)	3V	
MP20045DQ-25**	2.5V	QFN8 (3mm x 3mm)	9Z	
MP20045DN**	Adjustable	SOIC8E	M20045DN	
MP20045DN-18**	1.8V	SOIC8E	20045-18	

* For fixed output voltage versions between 1.5V and 5V. Contact factory for availability.

** For Tape & Reel, add suffix –Z (e.g. MP20045DQ–Z, MP20045DN–Z);
For RoHS compliant packaging, add suffix –LF (e.g. MP20045DQ–LF–Z, MP20045DN–LF–Z).

PACKAGE REFERENCE



QFN8 (3mm x 3mm) | **SOIC8E**

ABSOLUTE MAXIMUM RATINGS (1)

VIN, EN, PG, FB to GND ..... -0.3V to +6V
OUT to GND..... -0.5V to V_{IN} + 0.5V
Continuous Power Dissipation (T_A=+25°C) (2)
QFN8 (3x3) 2.0W
SOIC8E.....2.0W
Free Air Temperature (T_A).....-40°C to 85°C
Storage Temperature Range.....-65°C to 150°C
Lead Temperature (Soldering, 10sec).....260°C

ESD Susceptibility

HBM (Human Body Mode)..... 2kV
MM (Machine Mode)..... 200V

Recommended Operating Conditions (3)

Supply Input Voltage..... 2.5V to 5.5V
Enable Input Voltage ..... 0V to 5.5V
Operating Junct. Temp (T_J) .....-40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN8 (3x3).....50 ..... 12... °C/W
SOIC8E.....50 ..... 10... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/ θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7 4-layer board.

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ELECTRICAL CHARACTERISTICS

V_{IN}=V_{OUT}+0.5V or V_{IN}=2.5V, EN=V_{IN}, Typical values are at T_A=+25°C, unless otherwise specified

Parameter		Condition		Min	Typ	Max	Units
Input Voltage				2.5		5.5	V
Input Under voltage Lockout		V_{IN} rising		2.0		2.3	V
Hysteresis of UVLO					160		mV
FB Accuracy	Adjustable	I_{OUT}=1mA		-2.5		2.5	%
Output Voltage Accuracy	1.5V	I_{OUT}=1mA, 2.5V<V_{IN}<5.5V		-2.5		2.5	
	1.8V	I_{OUT}=1mA, 2.5V<V_{IN}<5.5V		-2.5		2.5	
	2.5V	I_{OUT}=1mA, 3V<V_{IN}<5.5V		-2.5		2.5	
Maximum Output Current		Continuous, V_{IN}>=3V		1			A
Short-Circuit Current Limit		V_{OUT}=0, V_{IN}>=3V			1.6		A
In-Regulation Current Limit		V_{OUT} within 4% of normal output voltage V_{IN}=5.5V		1.4	2.2	3.0	A
Ground Current		I_{OUT}=100μA			110		μA
Dropout Voltage(5)		I_{OUT}=1A			140	280	mV
Line Regulation(6)		V_{IN} from V_{OUT}+0.5V to 5.5V, I_{OUT}=5mA		-0.15		0.15	%/V
Load Regulation(7)		I_{OUT} from 1mA to 1A			-0.3		%
Output Voltage Noise		V_{IN}=3.3V, V_{OUT}=2.8V, C_{OUT}=2.2μF, I_{OUT}=100mA, f ranges from 10Hz to 100kHz			13		μV_{RMS}
PSRR		At 1kHz, I_{OUT}=250mA			56		dB
Shutdown Supply Current		V_{IN}=+5.5V			5	16	μA
EN PIN Threshold		EN Logic High		1.5			V
		EN Logic Low				0.4	
EN pin PULL-UP resistor				550k	1.1M		Ω
Thermal Shutdown Temperature		Typical thermal hysteresis =20°C			150		°C
PG	Minimum input voltage	$I_{OUT(PG)}$=300μA			1.1	1.3	V
	Trip threshold voltage	V_{OUT} decreasing	MP20045 MP20045-15 MP20045-18 MP20045-25	80		86	$\%V_{OUT}$
	Hysteresis voltage	Measured at V_{OUT}			6		$\%V_{OUT}$
	Output low voltage	$I_{OUT(PG)}$=1mA			0.15	0.4	V
	Leakage current	$V_{(PG)}$=5.5V				1	μA

Notes:

5) Dropout Voltage is defined as the input to output differential when the output voltage drops 100mV below its nominal value.

6) Line Regulation= $\frac{\left|V_{OUT[V_{IN(MAX)}]} - V_{OUT[V_{IN(MIN)}]}\right|}{\left[V_{IN(MAX)} - V_{IN(MIN)}\right] \times V_{OUT(NOM)}} \times 100(\%/V)$

7) Load Regulation= $\frac{\left|V_{OUT[I_{OUT(MAX)}]} - V_{OUT[I_{OUT(MIN)}]}\right|}{V_{OUT(NOM)}} \times 100(\%)$

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PIN DESCRIPTION

QFN8 (3X3) Pin #	SOIC8E Pin #	Name	Description
1, 2	7, 8	VIN	Regulator Input. Supply voltage ranges from +2.5V to 5.5V. Bypass with 2.2μF capacitor. These pins must be externally connected for proper operation even if they are internally connected.
3, 4	1, 2	VOUT	Regulator output. Bypass with a 2.2μF low-ESR capacitor to GND. Connect all the pin together externally.
5	3	FB	Feedback Input. For the adjustable output version, connect FB to the center point of the external resistor divider. The feedback threshold voltage is 1.5V. For the fixed output version, connect FB to the output directly.
6	4	GND Exposed pad	Ground. Connect exposed pad to GND plane for optimal thermal performance.
7	5	PG	Open-drain power-good (PG) output.
8	6	EN	Positive polarity enable (EN) input. Regulator Enable Control Input. Drive EN above 1.5V to turn on the MP20045. Drive EN below 0.4V to turn it off. Do not float the EN pin.

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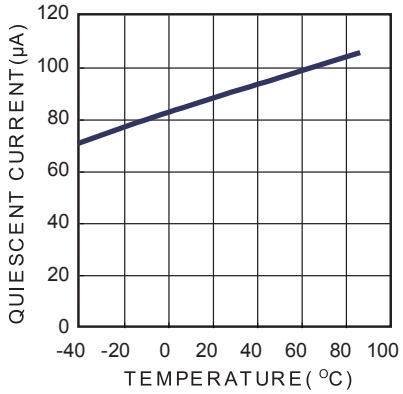
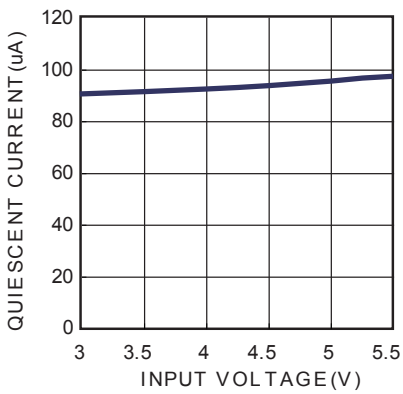
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=3.3V, V_{OUT}=2.8V, C_{IN}=C_{OUT}=2.2µF, T_A=25°C, unless otherwise noted

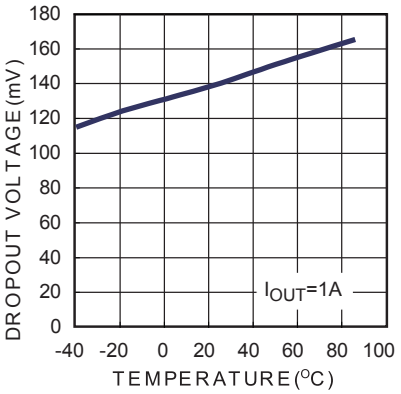
Quiescent Current vs. Temperature



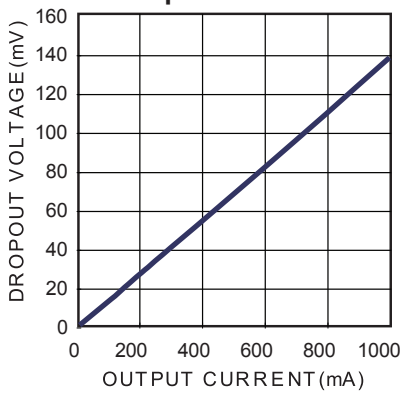
Quiescent Current vs. Input Voltage



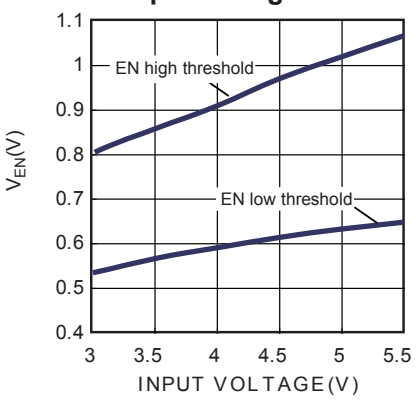
Dropout Voltage vs. Temperature



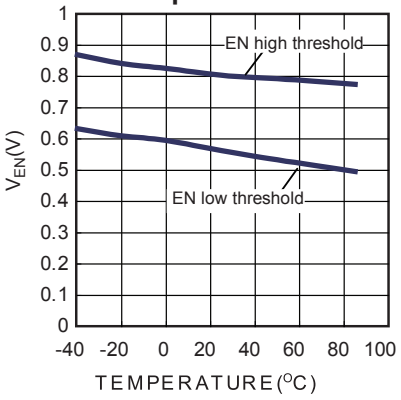
Dropout Voltage vs. Output Current



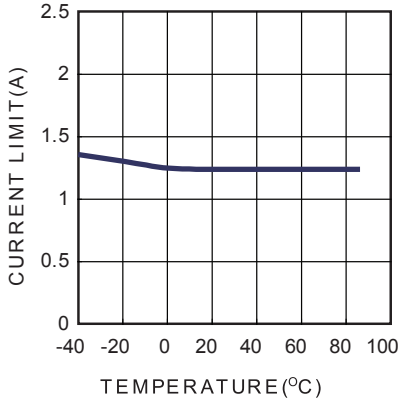
EN threshold vs. Input Voltage



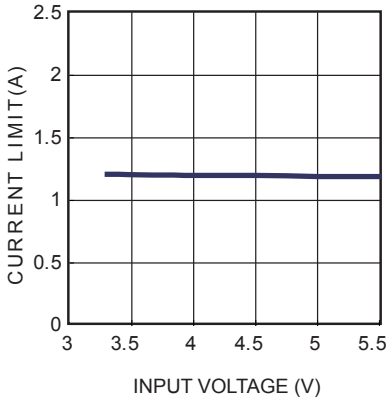
EN threshold vs. Temperature



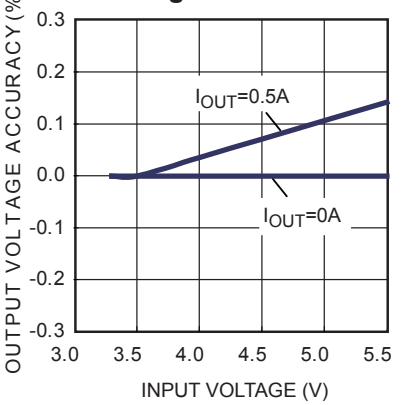
Current Limit vs. Temperature



Current Limit vs. Input Voltage



Line Regulation



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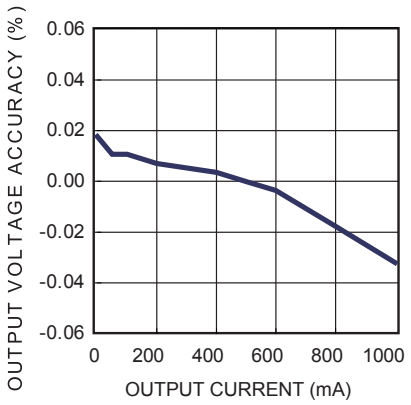
TYPICAL PERFORMANCE CHARACTERISTICS (*continued*)

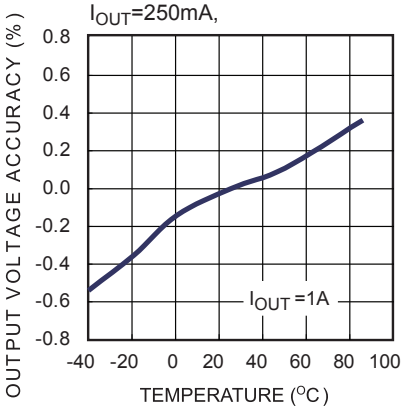
V_{IN}=3.3V, V_{OUT}=2.8V, C_{IN}=C_{OUT}=2.2µF, T_A=25°C, unless otherwise noted

Load Regulation



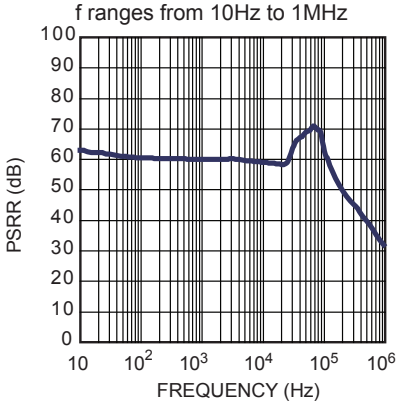
Output Voltage Accuracy vs. Temperature

I_{OUT}=250mA,

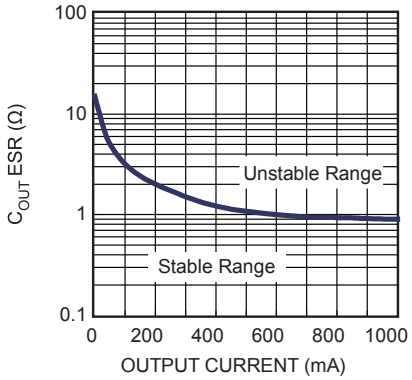


PSRR Vs. Frequency

I_{OUT}=800mA,
f ranges from 10Hz to 1MHz



Region of Stable C_{OUT} ESR vs. Output Current



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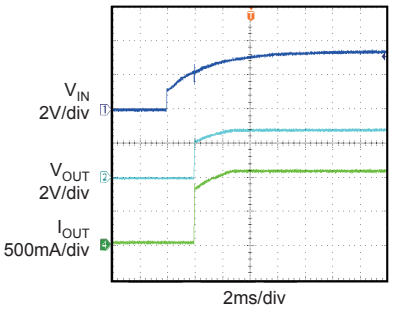
TYPICAL PERFORMANCE CHARACTERISTICS (*continued*)

V_{IN}=3.3V, V_{OUT}=2.8V, C_{IN}=C_{OUT}=2.2µF, T_A=25°C, unless otherwise noted

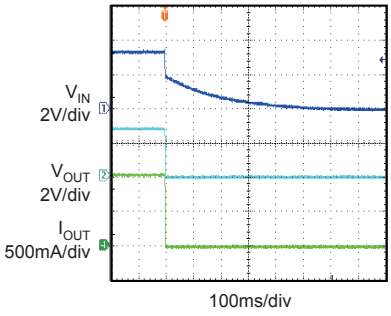
Input Power Start Up

I_{OUT}=1A, with Resistor Load



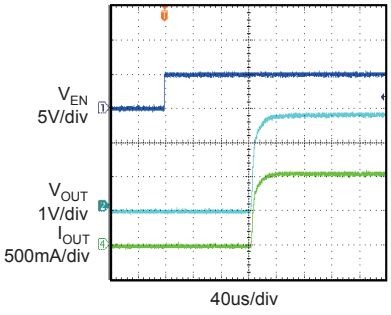
Input Power Shutdown

I_{OUT}=1A, with Resistor Load



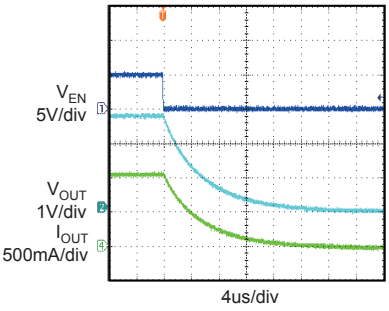
EN Start Up

I_{OUT}=1A, with Resistor Load



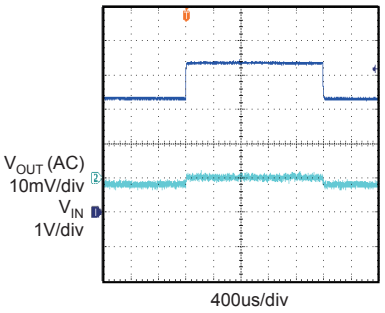
EN Shutdown

I_{OUT}=1A, with Resistor Load



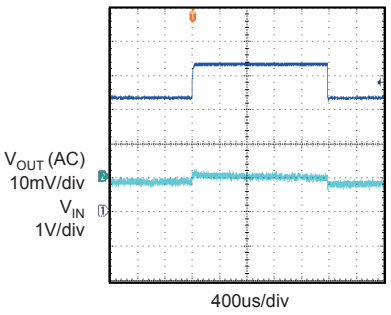
Line Transient

V_{IN}=3.3V to 4.3V, I_{OUT}=100mA, with Resistor Load



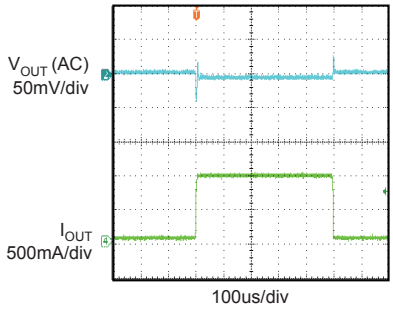
Line Transient

V_{IN}=3.3V to 4.3V, I_{OUT}=1A, with Resistor Load

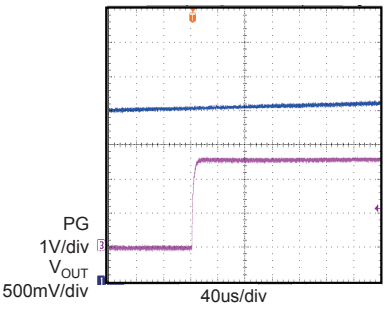


Load Transient

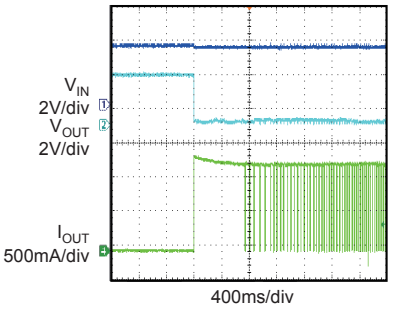
I_{OUT}=50mA to 1A, with Resistor Load



Power Good Status



Over Current Protection Entry



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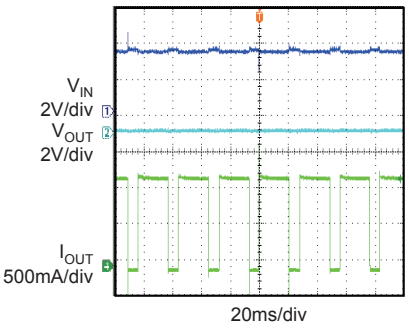
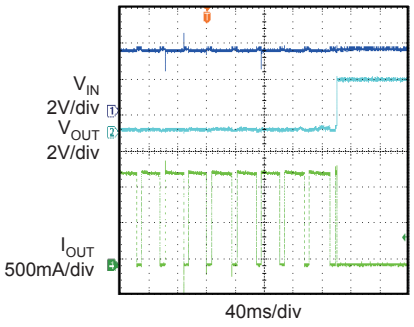
TYPICAL PERFORMANCE CHARACTERISTICS (*continued*)

V_{IN}=3.3V, V_{OUT}=2.8V, C_{IN}=C_{OUT}=2.2µF, T_A=25°C, unless otherwise noted

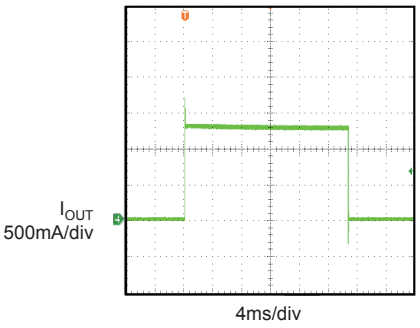
Over Current Protection Steady State
No Load



Over Current Protection Recovery
No Load



Current Limit



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BLOCK DIAGRA

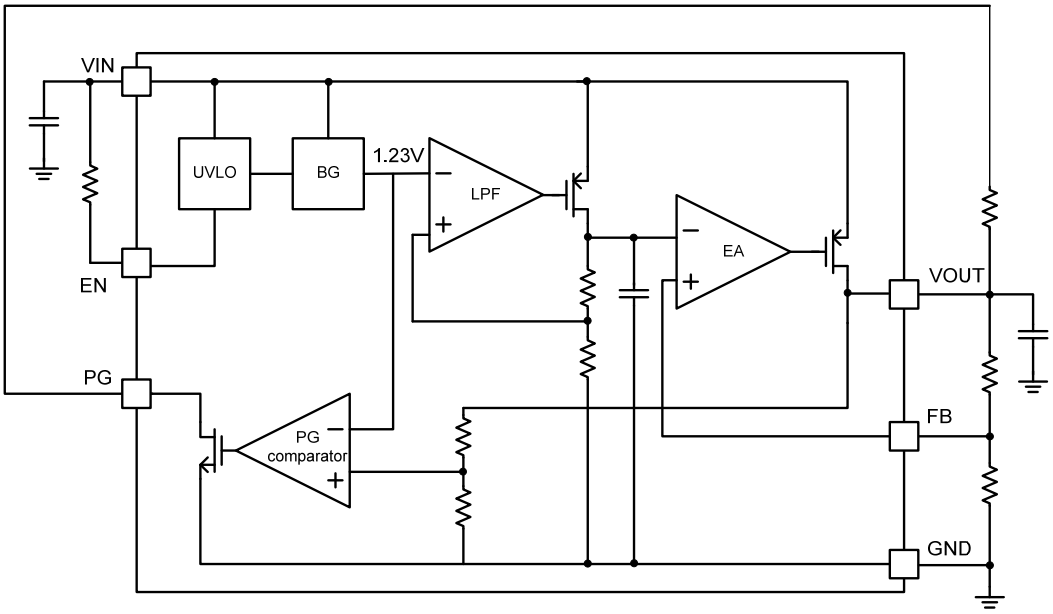

Figure 1—Block Diagram of Super Low Dropout Regulation

OPERATION

The MP20045 is a low-dropout linear regulator supplies up to 1A current. It is intended for use in devices that require very low voltage, low quiescent, low noise and high PSRR such as wireless LAN, battery powered equipment and hand-held equipment.

The MP20045 uses an internal PMOS as the pass element and features internal thermal shutdown and internal current limit circuit.

Dropout Voltage

Dropout voltage is the minimum input to output differential voltage required for the regulator to maintain an output voltage within 100mV of its nominal value. Because the PMOS pass element behaves as a low-value resistor, the dropout voltage of MP20045 is very low.

Shutdown

The MP20045 can be switched ON or OFF by a logic input at the EN pin. A high voltage at this pin will turn the device on. When the EN pin is low, the regulator output is off. The EN pin should be tied to VIN to keep the regulator output always on if the application does not require the shutdown feature. Do not float the EN pin.

Current Limit

The MP20045 includes a current limit structures which monitor and control PMOS's gate voltage limiting the guaranteed maximum output current to 1.2A.

Thermal Protection

Thermal protection turns off the PMOS when the junction temperature exceeds +150ºC, allowing the IC to cool. When the IC's junction temperature drops by 20ºC, the PMOS will be turned on again. Thermal protection limits total power dissipation in the MP20045. For reliable operation, junction temperature should be limited to 125 ºC maximum.

Load-Transient Considerations

The output response of load-transient consists of a DC shift and transient response. Because of the excellent load regulation of MP20045, the DC shift is very small. The output voltage transient depends on the output capacitor's value and the ESR. Increasing the capacitance and decreasing the ESR will improve the transient response.

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APPLICATION INFORMATION

Setting the Output Voltage

The output voltage of MP20045 can be set externally which ranges from 1.5V to 5V by operating from +2.5V to +5.5V input or preset internally at 1.5V, 1.8V, 2.5V, 5V. For the adjustable version, the output voltage is set by using a resistive voltage divider from the output voltage to FB pin. The voltage divider divides the output voltage down to the feedback voltage by the ratio:

$$V_{FB} = V_{OUT} \frac{R2}{R1+R2}$$

Where V_{FB} is the feedback threshold voltage (V_{FB} = 1.5V), and V_{OUT} is the output voltage. Thus the output voltage is:

$$V_{OUT} = 1.5 \times \frac{R1+R2}{R2}$$

R2 can be as high as 100kΩ, but a typical value is 10kΩ. Using that value, R1 is determined by:

$$R1 = R2 \times \left(\frac{V_{OUT} - V_{FB}}{V_{FB}} \right)$$

For example, for a 2.8V output voltage, R2 is 10kΩ, and R1 is 8.66kΩ. You can select a standard 8.66kΩ (±1%) resistor for R1.

Power Dissipation

The power dissipation for any package depends on the thermal resistance of the case and circuit board, the temperature difference between the junction and ambient air, and the rate of air flow. The power dissipation across the device can be represented by the equation:

$$P = (V_{IN} - V_{OUT}) \times I_{OUT}$$

The allowable power dissipation can be calculated using the following equation:

$$P_{(MAX)} = (T_{Junction} - T_{Ambient}) / \theta_{JA}$$

Where ($T_{Junction}$ − $T_{Ambient}$) is the temperature difference between the junction and the surrounding environment, θ_{JA} is the thermal resistance from the junction to the ambient environment. Connecting the GND pin of MP20045 to ground using a large pad or ground plane helps to channel heat away.

Output Capacitor Selection

The MP20045 is designed specifically to work with very low ESR ceramic output capacitor in space-saving and performance consideration. A 2.2μF ceramic capacitor with ESR lower than 0.9Ω is suitable for the MP20045 application circuit. Output capacitor of larger values will help to improve load transient response and reduce noise with the drawback of increased size.

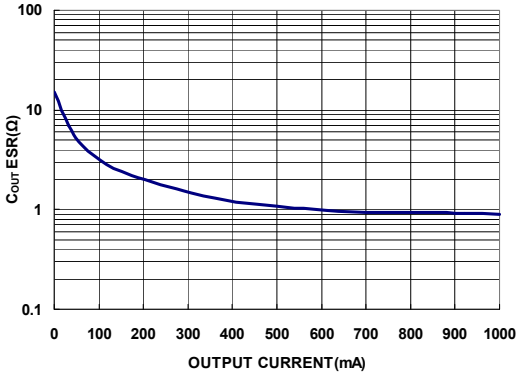

Figure 2—Relationship between ESR and LDO Stability

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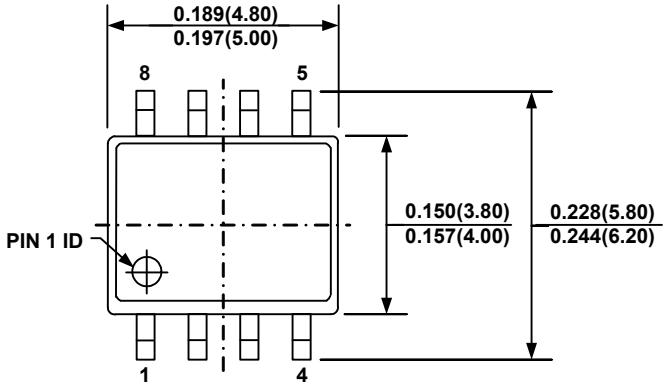
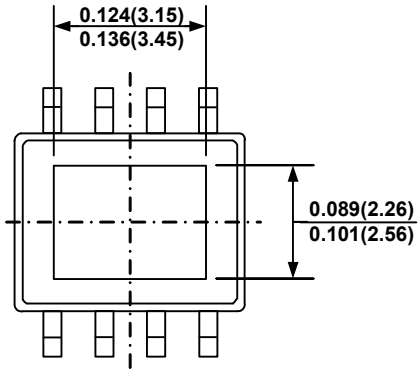
PACKAGE INFORMATION

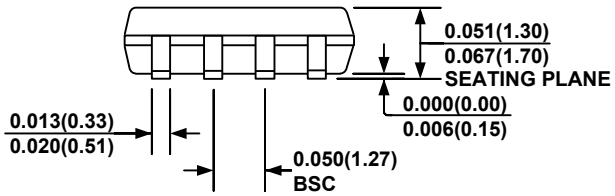
SOIC8E



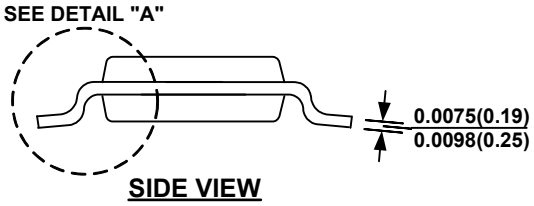
TOP VIEW



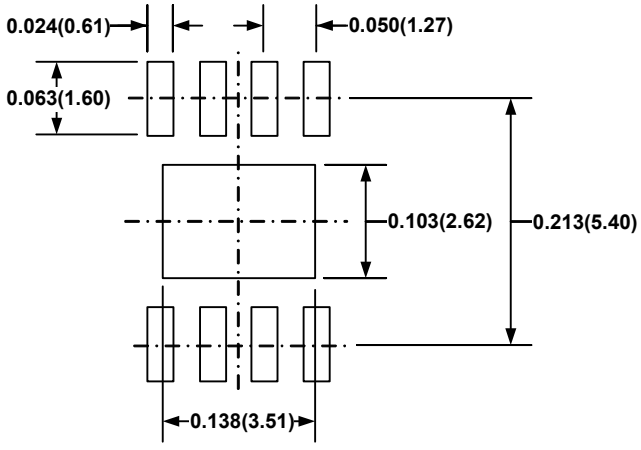
BOTTOM VIEW



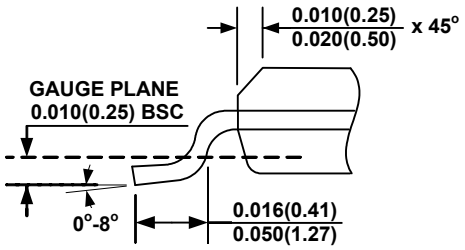
FRONT VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6) DRAWING IS NOT TO SCALE.

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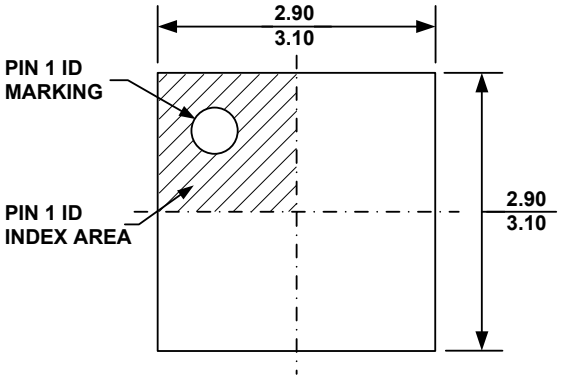
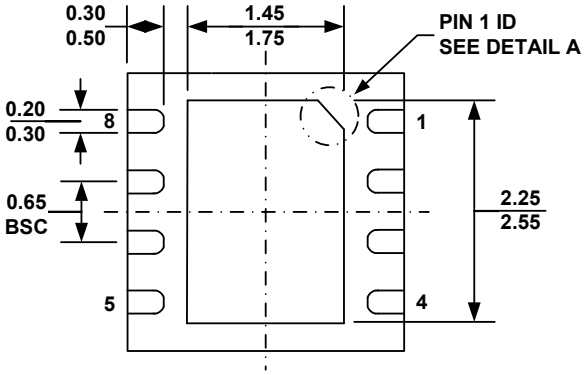
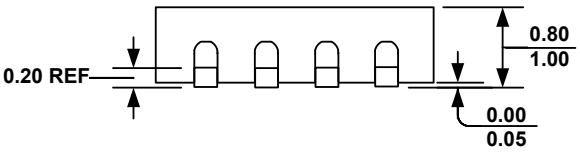
QFN8 (3mm×3mm)



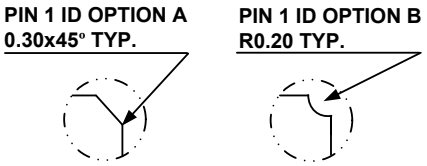
TOP VIEW



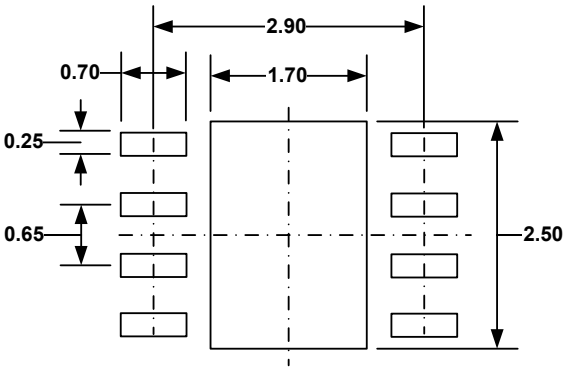
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEEC-2.
5) DRAWING IS NOT TO SCALE.

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