MP1653F

16V, 3A, 1.1MHz, High-Efficiency, Synchronous Step-Down Converter with FCCM in an SOT563 Package

DESCRIPTION

The MP1653F is a fully integrated, high-frequency, synchronous, rectified, step-down switch-mode converter with internal power MOSFETs. The MP1653F offers a very compact solution that achieves 3A of continuous output current (I_{OUT}) with excellent load and line regulation across a wide input voltage (V_{IN}) range. The MP1653F is well-suited to support applications with a tight output voltage (V_{OUT}) ripple.

Constant-on-time (COT) control operation provides very fast transient response, easy loop design, and very tight output regulation.

Full protection features include short-circuit protection (SCP), over-current protection (OCP), under-voltage protection (UVP), and thermal shutdown.

The MP1653F requires a minimal number of readily available, standard external components, and is available in a space-saving SOT563 package.

FEATURES

- Forced Continuous Conduction Mode (FCCM)
- 1.1MHz Fixed Switching Frequency (f_{SW})
- Wide 4.5V to 16V Operating Input Voltage (V_{IN}) Range
- 3A of Output Current (I_{OUT})
- 58mΩ/32mΩ Low On Resistance ($R_{DS(ON)}$) Internal Power MOSFETs
- 0.6V to 8V Output Voltage (V_{OUT}) Range
- ±1% Feedback (FB) Accuracy at Room Temperature
- ±1.5% FB Accuracy Across Full Temperature Raneg
- Excellent Load Transient Performance
- Pre-Biased Start-Up
- Enable (EN) Power Sequencing
- Over-Current Protection (OCP) and Hiccup Mode
- V_{IN} Over-Voltage Protection (OVP)Thermal Shutdown
- Available in an SOT563 (1.6mmx1.6mm) Package

MPL Optimized Performance with MPS Inductor MPL-AL Series

APPLICATIONS

- Flat-Panel Televisions and Monitors
- Digital Set-Top Boxes
- Security Cameras
- General-Purpose Power Supplies

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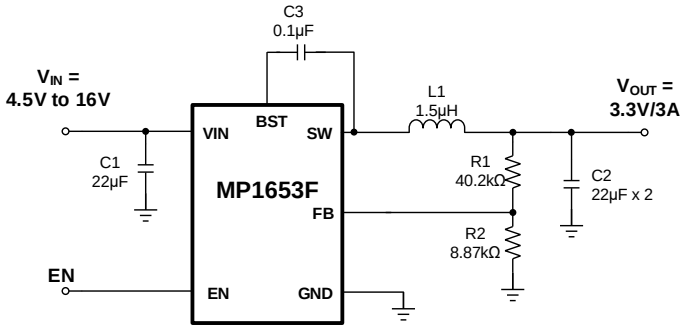
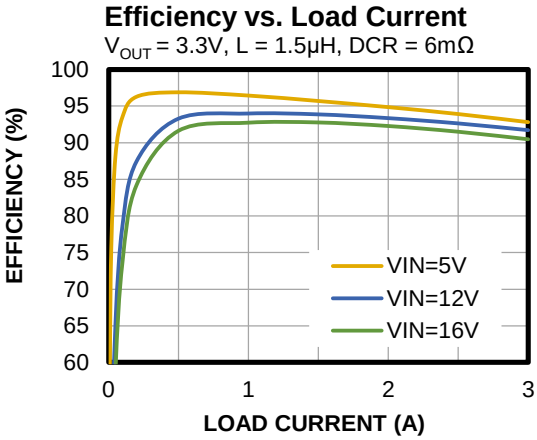
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP1653FGTF	SOT563 (1.6mmx1.6mm)	*See Below*	1

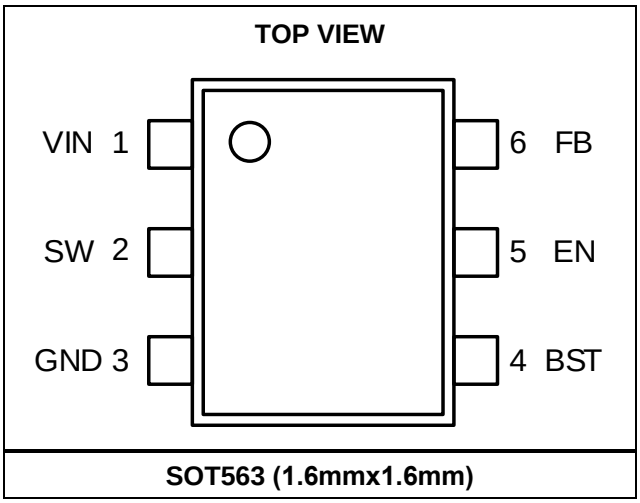
* For Tape & Reel, add suffix -Z (e.g. MP1653FGTF-Z).

TOP MARKING

CFEY
LLL

CFE: Product code of MP1653FGTF
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



SOT563 (1.6mmx1.6mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	VIN	**Supply voltage.** A capacitor is required to decouple the input rail. Make the VIN connection using a wide PCB trace.
2	SW	**Switch output.** Make the SW pin connection using a wide PCB trace
3	GND	**System ground.** The GND pin is the reference ground of the regulated output voltage, and requires extra care during the PCB layout. Connect GND with copper traces and vias
4	BST	**Bootstrap.** Connect a 0.1µF to 1µF BST capacitor, as well as a resistor, between SW and BST to form a floating supply across the high-side switch driver.
5	EN	**Enable.** Drive EN high to enable the chip. For automatic start-up, connect EN to VIN via a 100kΩ resistor.
6	FB	**Feedback.** Connect FB to the tap of an external resistor divider from the output to GND to set the output voltage (V_{OUT}).

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) .....-0.3V to +18V
V_{SW}.....-0.3V (-4V for <10ns) to V_{IN} + 0.3V (+22V for <10ns)
V_{BST} ..... V_{SW} + 4V
V_{EN}.....-0.3V to +18V
All other pins .....-0.3V to +4V
Continuous power dissipation (T_A = 25°C) (2) (5)
SOT563 ..... 2W
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....4.5V to 16V
Output voltage (V_{OUT}).....
..... 0.6V to V_{IN} x D_{MAX} or 8V max
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance

	θ_{JA}	θ_{JB}	
SOT563 (1.6mmx1.6mm)			
JEDEC (4)	130	33.5	°C/W
EVL1653F-TF-00A(5)	60		°C/W

	θ_{JC_TOP}	θ_{JC_BOT}	
JEDEC (4)	65	17.4	°C/W

	Ψ_{JT}	
JEDEC (4)	3.9	°C/W
EVL1653F-TF-00A (5)	4	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) The value of θ_{JA} is only valid for comparison with other packages and cannot be used for design purposes. This value is based on a JEDEC51-7 board. They do not represent the performance obtained in an actual application.
5) Measured on the EVL1653F-TF-00A, 5.0cmx5.0cm, 2 layers with 2oz.
   The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature in the real system, based on equation $T_J = \psi_{JT} \times P_{LOSS} + T_{CASE_TOP}$, where P_{LOSS} is the entire loss of the IC in real applications, T_{CASE_TOP} is the case top temperature.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C (6), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Current						
Supply current (shutdown)	I_{SD}	V_{EN} = 0V			10	μA
Supply current (quiescent)	I_Q	V_{EN} = 2V, V_{FB} = 0.65V, no switching		130	200	μA
MOSFET						
High-side MOSFET (HS-FET) switch on resistance	$R_{DS(ON)_HS}$	V_{BST-SW} = 3.3V		58		mΩ
Low-side MOSFET (LS-FET) switch on resistance	$R_{DS(ON)_LS}$	V_{CC} = 3.3V		32		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 16V			10	μA
Current Limit and NCL						
Valley current limit	I_{LIMIT_VY}		3.3	4.5	5.7	A
Short hiccup duty cycle (7)	D_{HICCUP}			12.5		%
Negative current limit	I_{LIMIT_NCL}		-3	-2.5	-2	A
Switching Frequency and Minimum On/Off Timer						
Switching frequency	f_{SW}	V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 1.5A, T_A = 25°C	1000	1100	1210	kHz
Minimum on time (7)	t_{ON_MIN}			45		ns
Minimum off time	t_{OFF_MIN}		80	115	150	ns
Reference and Soft Start (SS)						
Feedback voltage	V_{FB}	T_J = 25°C°	594	600	606	mV
		T_J = -40°C to +125°C (6)	591	600	609	mV
Soft-start time	t_{SS}	V_{OUT} from 10% to 90%	0.5	1	1.6	ms
Enable and Under-Voltage Lockout (UVLO)						
EN rising threshold	V_{EN_RISING}		1.15	1.2	1.35	V
EN falling threshold	$V_{EN_FALLING}$		0.9	1	1.1	V
EN hysteresis	V_{EN_HYS}			200		mV
EN pin pull-down resistor	R_{EN}			1		MΩ
EN turn-on delay	$t_{ENONDLY}$	From EN rising to the first switching		150		μs
Input voltage (V_{IN}) UVLO rising threshold	$V_{IN_UVRISING}$		4	4.25	4.5	V
V_{IN} UVLO falling threshold	$V_{IN_UVFALLING}$		3.7	4	4.3	V
V_{IN} UVLO hysteresis	V_{IN_UVHYS}			250		mV
Input Over-Voltage Protection (OVP)						
V_{IN} OVP rising threshold		Turn off both HS and LS	16.5	17.5	18.5	V
V_{IN} OVP falling threshold			15.4	16.4	17.4	V

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C (6), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Thermal Protection						
Thermal shutdown (7)	T_{SD}			155		°C
Thermal hysteresis (7)	T_{SDHYS}			20		°C

Note:

6) Over-temperature limits are guaranteed by design, characterization, and correlation. Not tested in production.
7) Derived by sample characterization; not tested in production.

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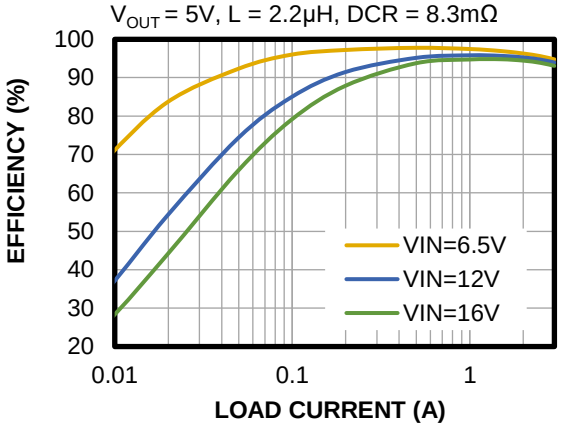
TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

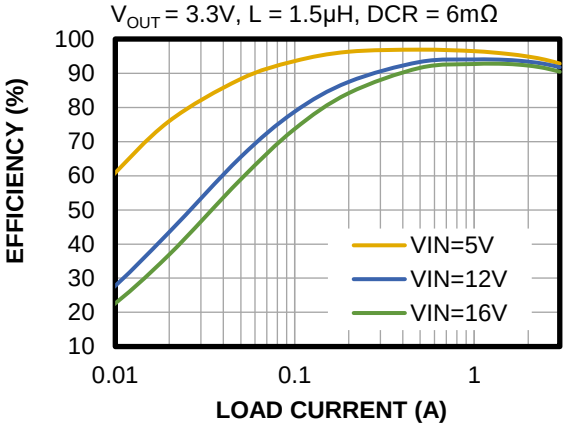
Efficiency vs. Load Current

V_{OUT} = 5V, L = 2.2µH, DCR = 8.3mΩ



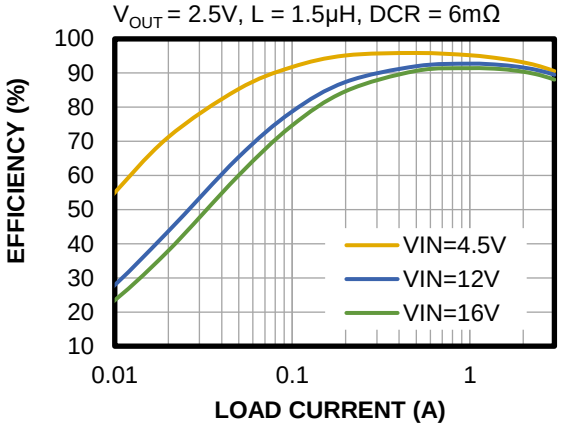
Efficiency vs. Load Current

V_{OUT} = 3.3V, L = 1.5µH, DCR = 6mΩ



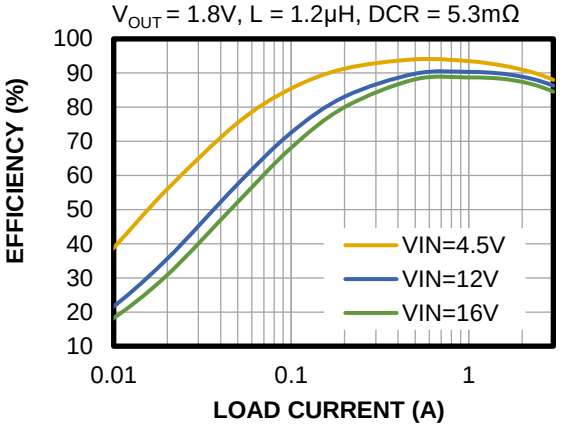
Efficiency vs. Load Current

V_{OUT} = 2.5V, L = 1.5µH, DCR = 6mΩ



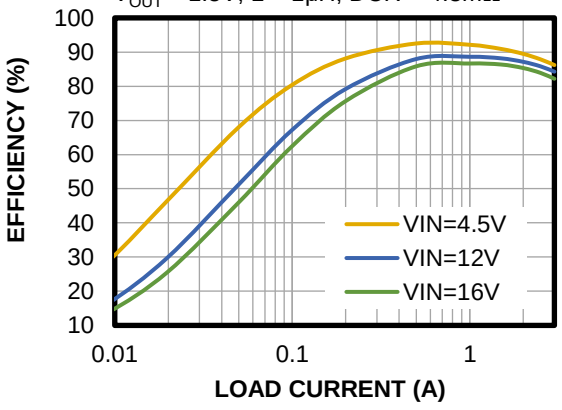
Efficiency vs. Load Current

V_{OUT} = 1.8V, L = 1.2µH, DCR = 5.3mΩ



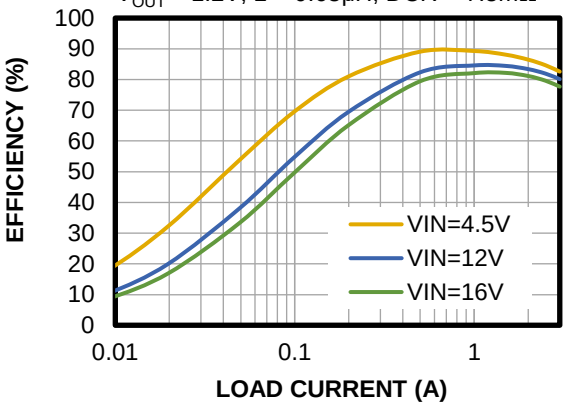
Efficiency vs. Load Current

V_{OUT} = 1.5V, L = 1µH, DCR = 4.3mΩ



Efficiency vs. Load Current

V_{OUT} = 1.2V, L = 0.68µH, DCR = 7.5mΩ



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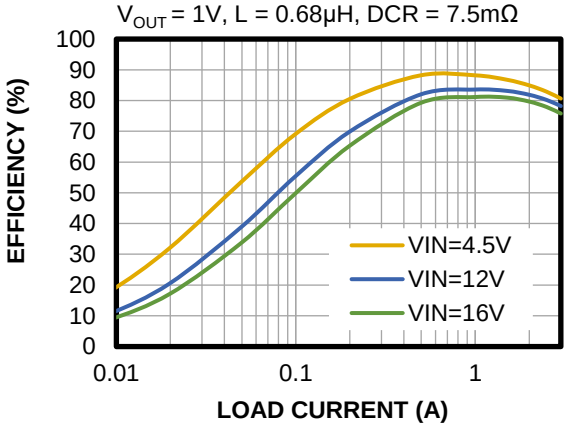
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

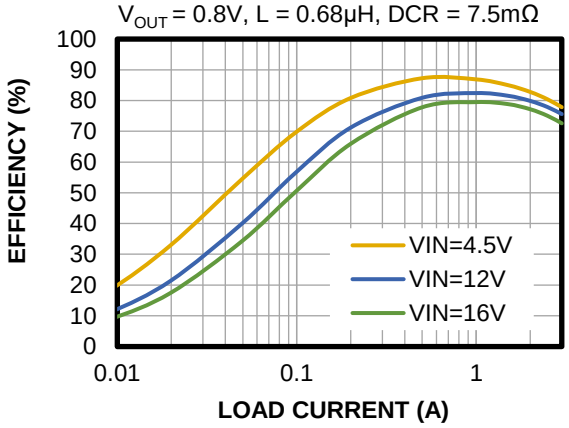
Efficiency vs. Load Current

V_{OUT} = 1V, L = 0.68µH, DCR = 7.5mΩ

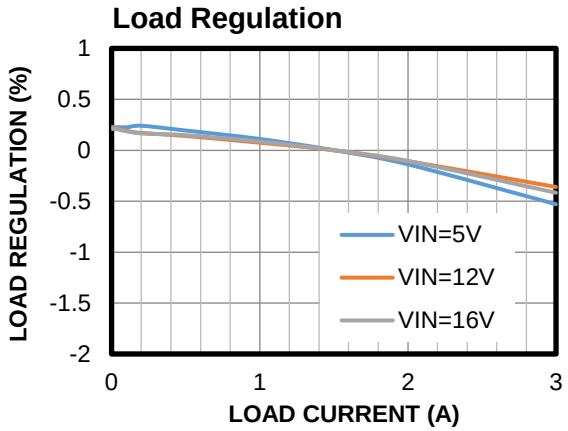


Efficiency vs. Load Current

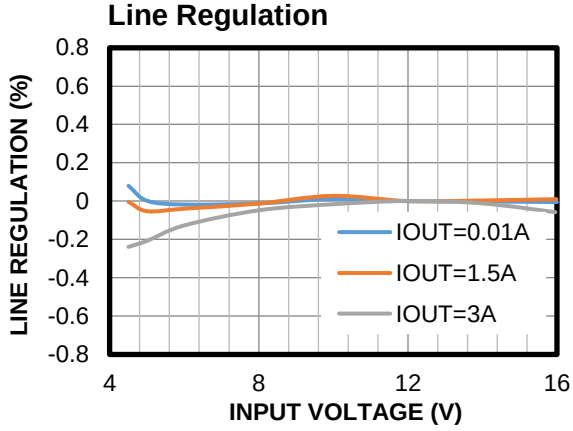
V_{OUT} = 0.8V, L = 0.68µH, DCR = 7.5mΩ



Load Regulation



Line Regulation



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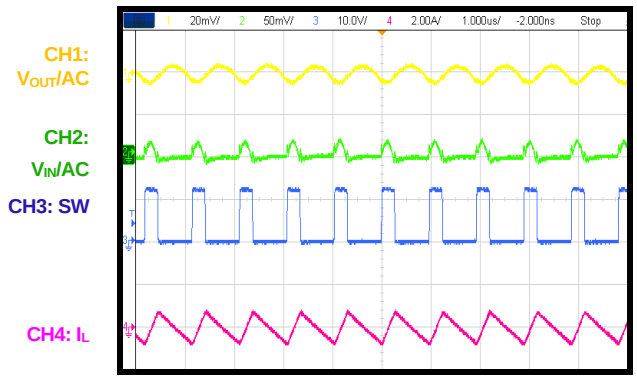
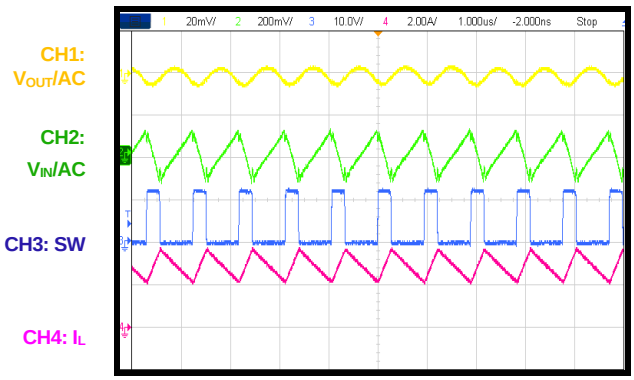
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

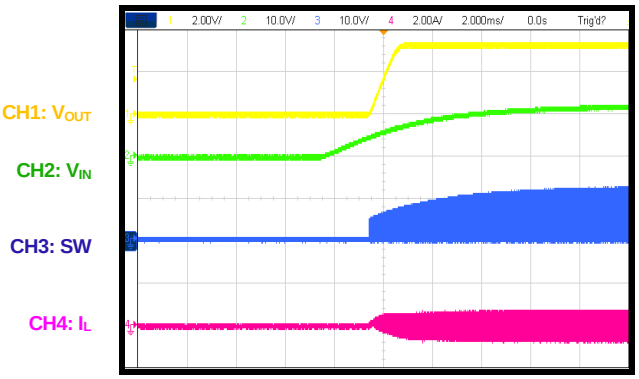
Input and Output Voltage Ripple
I_{OUT} = 0A



Input and Output Voltage Ripple
I_{OUT} = 3A



Start-Up through Input Voltage
I_{OUT} = 0A



Start-Up through Input Voltage
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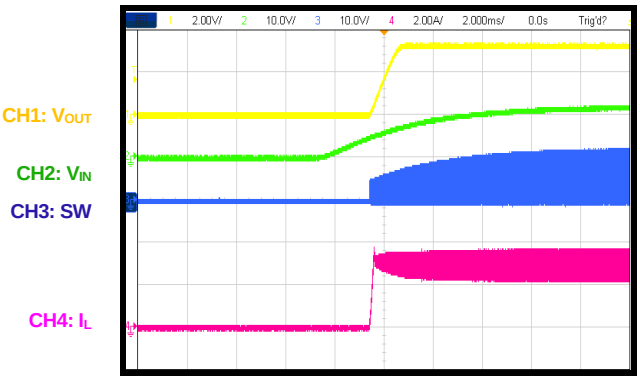

Shutdown through Input Voltage
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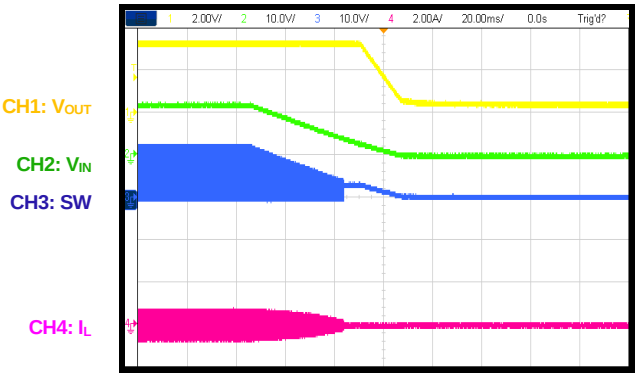
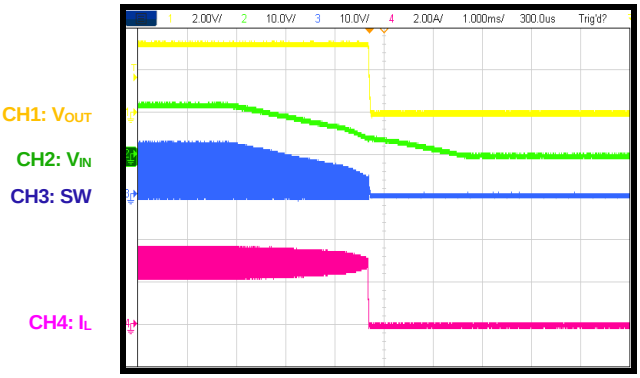


Shutdown through Input Voltage
I_{OUT} = 3A



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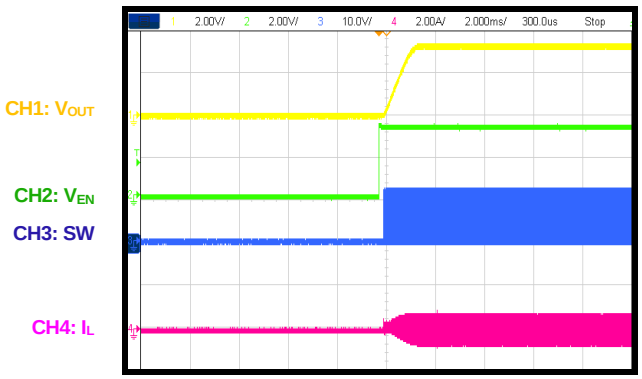
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

Start-Up through EN

I_{OUT} = 0A



Start-Up through EN

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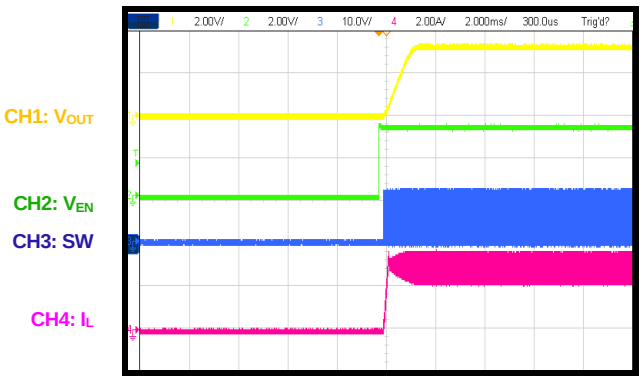
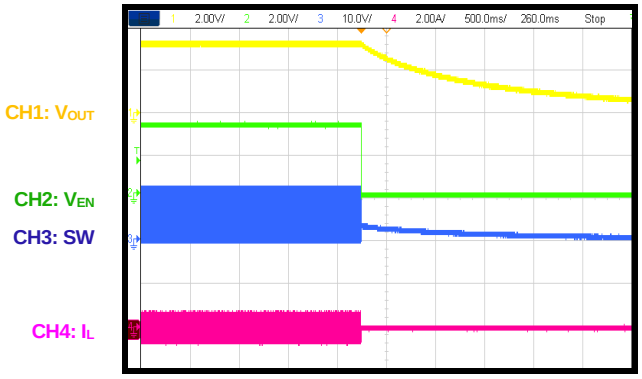


Shutdown through EN

I_{OUT} = 0A



Shutdown through EN

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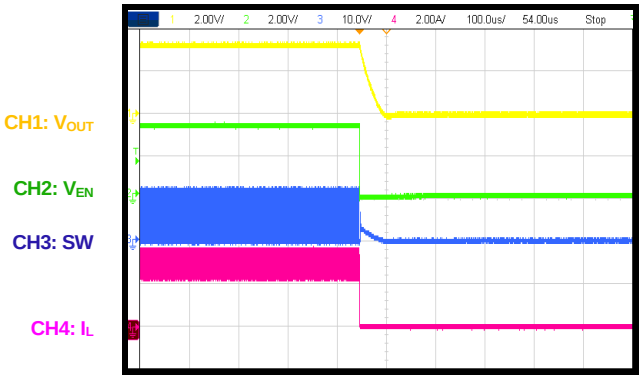
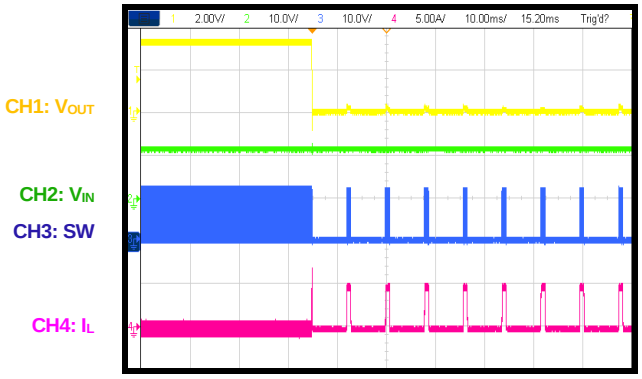


Short-Circuit Protection Entry

I_{OUT} = 0A



Short-Circuit Protection Entry

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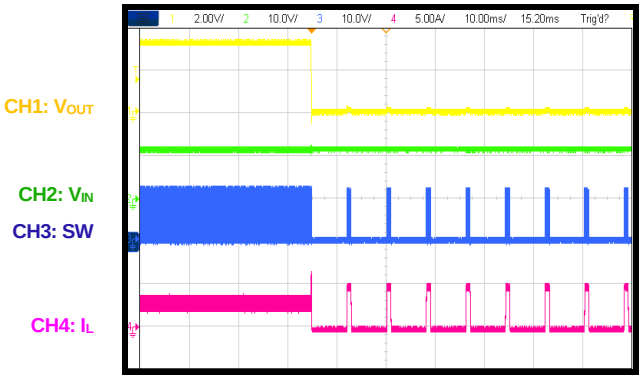

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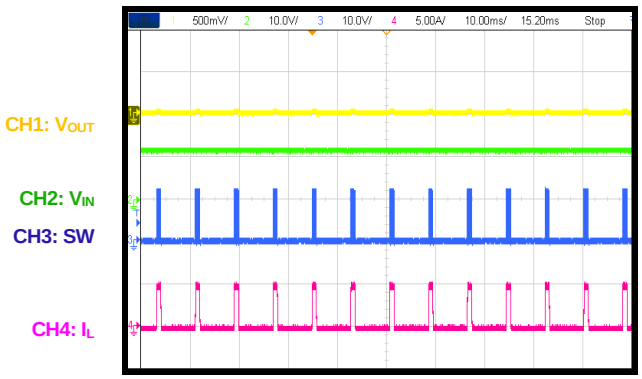
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

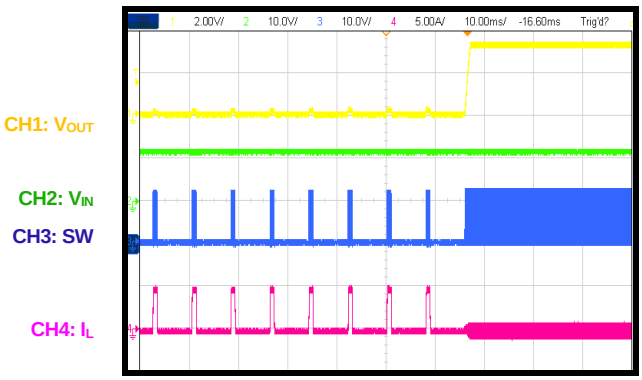
V_{IN} = 12V, V_{OUT} = 3.3V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

Short-Circuit Protection Steady State



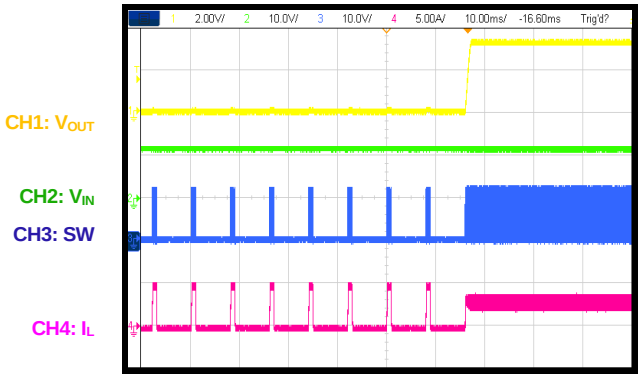
Short-Circuit Protection Recovery

I_{OUT} = 0A



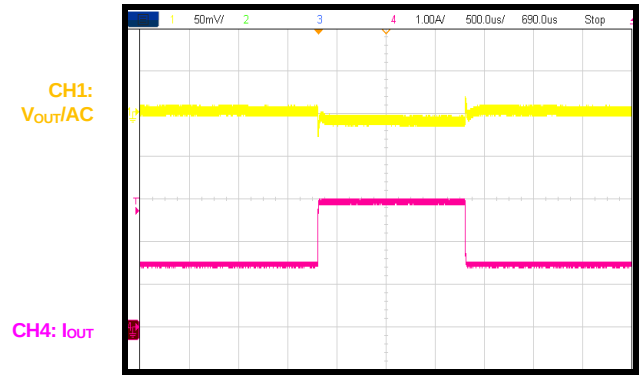
Short-Circuit Protection Recovery

I_{OUT} = 3A



Load Transient Response

I_{OUT} = 1.5A to 3A, 2.5A/µs by e-load



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FUNCTIONAL BLOCK DIAGRAM

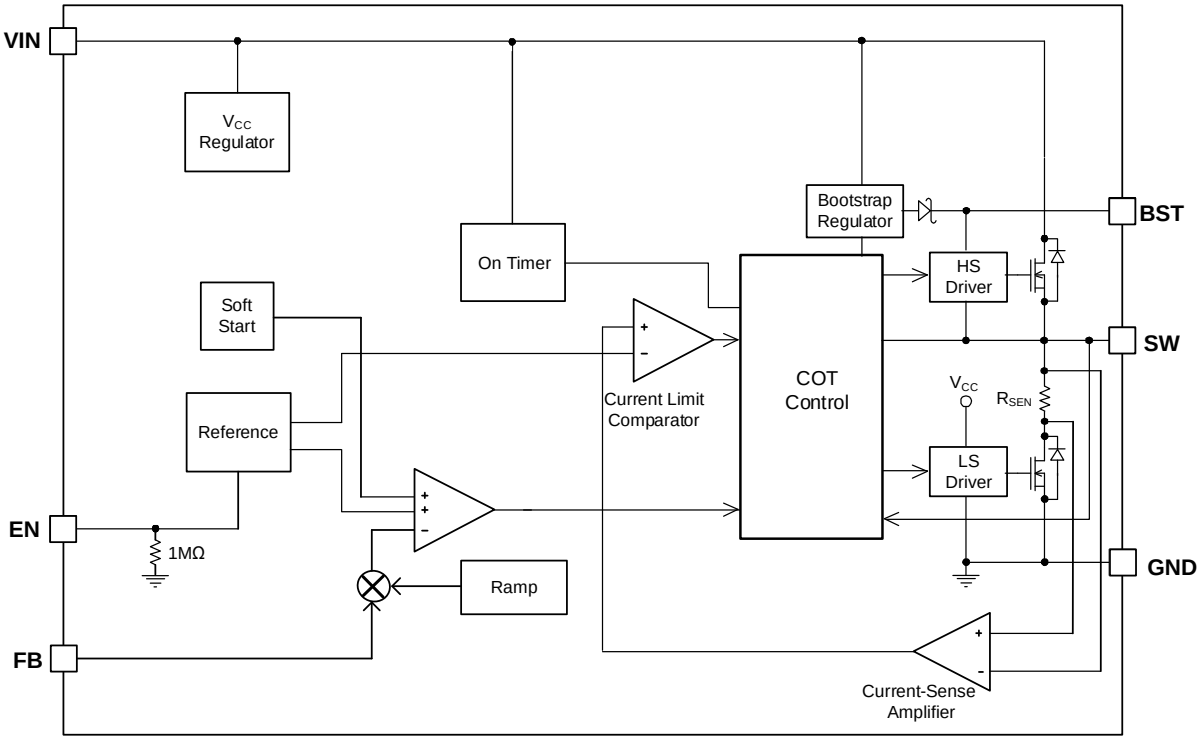

Figure 1: Functional Block Diagram

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OPERATION

Constant-On-Time (COT) Control

The MP1653F employs constant-on-time (COT) control to achieve a fast load transient response. Figure 2 shows the MP1653F's detailed control stage.

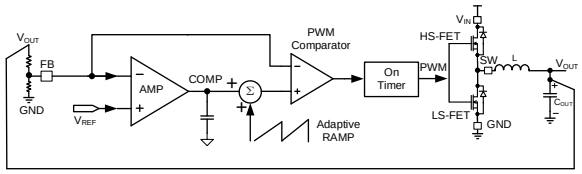

Figure 2: COT Control

The operational amplifier (AMP) corrects any error voltage between the FB pin and the reference voltage (V_{REF}). The MP1653F can use AMP to provide excellent load regulation across the entire load range.

The MP1653F has internal RAMP compensation to support a low-ESR MLCC output capacitor solution. The adaptive internal RAMP is optimized so that the MP1653F is stable across the entire operating input voltage (V_{IN}) and output voltage (V_{OUT}) ranges with a properly designed output LC filter.

The MP1653F operates in forced continuous conduction mode (FCCM). The low-side MOSFET (LS-FET) is turned on when the HS-FET is in its off state to minimize conduction loss. There is a dead short between the input and GND if both the HS-FET and LS-FET are turned on at the same time. This is called shoot-through. To avoid shoot-through, a dead time is generated internally between the HS-FET off and LS-FET on period or the LS-FET off and HS-FET on period.

Enable (EN) Control

EN is a digital control pin that turns the regulator on and off. Drive EN above EN rising threshold to turn on the regulator. Drive EN below EN falling threshold to turn off the regulator. When floating, EN is pulled down to GND by an internal 1MΩ resistor. EN can be connected to the VIN pin via 100kΩ resistor.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MP1653F's UVLO comparator monitors the internal regulator's output voltage (V_{CC}). The UVLO rising threshold is about 4.25V, while its falling threshold remains consistent at 4V.

Internal Soft Start (SS)

Soft start prevents the converter's V_{OUT} from overshooting during start-up. When the chip starts, the internal circuitry generates a soft-start voltage (V_{SS}) that ramps up from 0V to 1.2V. When V_{SS} is below V_{REF}, V_{SS} overrides V_{REF}, so the error amplifier uses V_{SS} as the reference. When V_{SS} exceeds V_{REF}, the error amplifier uses V_{REF} as the reference.

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

The MP1653F has valley-limit control. The LS-FET monitors the current flow through the LS-FET. The HS-FET waits until the valley current limit is removed before turning on again. Meanwhile, V_{OUT} drops until the feedback voltage (V_{FB}) is below the under-voltage (UV) threshold (typically 40% of V_{REF}). Once the UV condition is triggered, the MP1653F enters hiccup mode to restart the part periodically.

During over-current protection (OCP), the device attempts to recover from the OC fault with hiccup mode. This means that the chip disables the output power stage, discharges the soft-start circuit, and attempts to soft-start again automatically. If the OC condition still remains after soft start ends, the device repeats this operation cycle until the OC condition disappears, and then V_{OUT} rises back to the regulation level.

Pre-Biased Start-Up

The MP1653F is designed for monotonic start-up into pre-biased loads. If V_{OUT} is pre-biased to a certain voltage during start-up, the IC disables switching for the HS-FET and LS-FET until V_{SS} exceeds the sensed V_{FB}. If the BST voltage (V_{BST}) is below its UVLO threshold during start-up, the LS-FET turns on to allow V_{BST} to be charged through VIN. The LS-FET turns on for very narrow pulses, so the drop in the pre-biased level is negligible. After V_{SS} reaches the pre-biased voltage at the FB pin, the MP1653F begins to work normally.

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Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. If the silicon die temperature exceeds 155°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 135°C), the chip is enabled again.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. V_{IN} regulates the bootstrap capacitor voltage internally through D1, M1, R4, C4, L_{OUT}, and C_{OUT} (see Figure 3). If V_{IN} - V_{SW} exceeds 3.3V, U2 regulates M1 to maintain a 3.3V BST voltage across C4. The BST resistor (R4) is recommended to be below 4.7Ω.

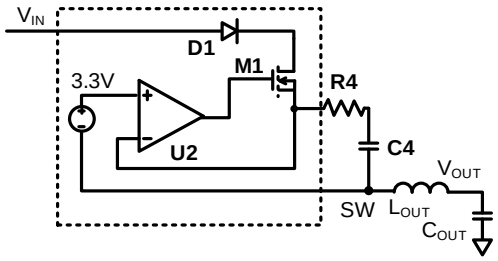

Figure 3: Internal Bootstrap Charger

Start-Up and Shutdown Circuit

If both V_{IN} and EN exceed their respective thresholds, the chip starts up. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuits.

Three events can shut down the chip: EN going low, V_{IN} going low, and thermal shutdown. The shutdown procedure starts by initially blocking the signaling path to avoid any fault triggering. The internal supply rail is then pulled down.

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APPLICATION INFORMATION

Setting the Output Voltage (V_{OUT})

The external resistor divider is used to set V_{OUT}. First, choose a value for R2. R2 should be chosen reasonably, since a small R2 leads to considerable quiescent current (I_Q) loss, while a larger-value R2 makes FB noise-sensitive. R2 is recommended be between 5kΩ and 100kΩ. Typically, set the current through R2 to be below 150μA for a good balance between system stability and no-load loss. R1 can be calculated with Equation (1):

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (1)$$

Figure 4 shows the feedback circuit.

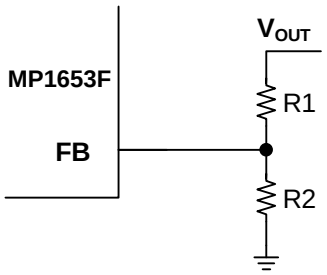

Figure 4: Feedback Network

Table 1 lists the recommended parameters for common output voltages.

Table 1: Parameter Selection for Common Output Voltages, C_{OUT} = 22μF x 2 (8)

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L (μH)
5	40.2	5.49	2.2
3.3	40.2	8.87	1.5
2.5	40.2	12.7	1.5
1.8	40.2	20	1.2
1.5	40.2	26.7	1
1.2	40.2	40.2	0.68
1	20.5	30.9	0.68
0.8	20.5	60.4	0.68

Note:

8) For the detailed design circuit, see the Typical Application Circuits section on page 18.

Selecting the Inductor

MPL **Optimized Performance with MPS Inductor MPL-AL Series**

An inductor is necessary to supply constant current to the output load while being driven by the switched input voltage. A larger-value inductor results in less ripple current and a lower output ripple voltage but also has a larger physical footprint, higher series resistance, and lower saturation current. A good rule to determine the inductance is to design the inductor's peak-to-peak ripple current to be between 30% and 60% of the maximum output current. The inductance can be estimated with Equation (2):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (2)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum inductor peak current. The peak inductor current can be calculated with Equation (3):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2 \times f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (3)$$

MPS inductors are optimized and tested for use with our complete line of integrated circuits.

Table 2 lists our power inductor recommendations. Select a part number based on your design requirements.

Table 2: Power Inductor Selection

Part Number	Inductor Value	Manufacturer
MPL-AL	0.68μH to 2.2μH	MPS
MPL-AL-4020-R68	0.68μH	MPS
MPL-AL-6050-1R0	1μH	MPS
MPL-AL-6050-1R2	1.2μH	MPS
MPL-AL6050-1R5	1.5μH	MPS
MPL-AL6050-2R2	2.2μH	MPS

Visit MonolithicPower.com under Products > Inductors for more information.

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. For the best results, use ceramic capacitors placed as close to VIN as possible. Capacitors with X5R and X7R ceramic

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dielectrics are recommended because they are fairly stable with temperature fluctuations.

The capacitors must also have a ripple current rating greater than the converter's maximum input ripple current. The input ripple current can be estimated with Equation (4):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (4)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, calculated with Equation (5):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (5)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance determines the converter's input voltage ripple. If there is an input voltage ripple requirement in the system, choose an input capacitor that meets the specification.

The input voltage ripple can be estimated with Equation (6):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (6)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, calculated with Equation (7):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (7)$$

Selecting the Output Capacitor

An output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (8)$$

With ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple.

For simplification, the output voltage ripple can be calculated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (9)$$

The output voltage ripple caused by the equivalent series resistance (ESR) is very small.

With POSCAP capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (10)$$

A larger-value output capacitor can improve load transient response, but consider the maximum output capacitor limit in the design application. If the output capacitance is too high, V_{OUT} cannot reach the design value during the soft-start time and fails to regulate. The maximum output capacitance (C_{O_MAX}) can be calculated with Equation (11):

$$C_{O_MAX} = (I_{LIM_AVG} - I_{OUT}) \times t_{SS} / V_{OUT} \quad (11)$$

Where I_{LIM_AVG} is the average start-up current during the soft-start period, and t_{SS} is the soft-start time.

Design Example

Table 3 shows a design example when ceramic capacitors are applied.

Table 3: Design Example

V_{IN}	12V
V_{OUT}	3.3V
I_{OUT}	3A

Figure 7 on page 18 shows the detailed application schematic. The typical performance and waveforms are shown in the Typical Performance Characteristics section starting on page 9. For more device applications, refer to the related evaluation board datasheet.

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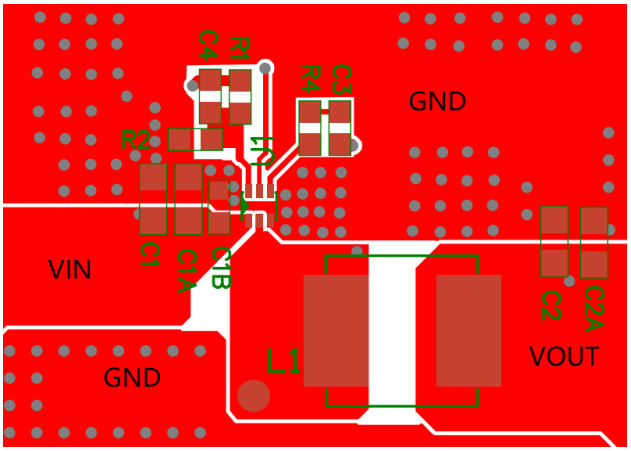
PCB Layout Guidelines

Efficient layout of the switching power supplies is critical for stable operation. A poor layout design can result in poor line or load regulation and stability issues. For the best results, refer to Figure 5 and follow the guidelines below.

1. Place the high-current paths (GND, VIN, and SW) very close to the device with short, direct, and wide traces.
2. Place the input capacitor as close to VIN and GND as possible.
3. Place the external feedback resistors next to FB.
4. Keep the switching node SW short, and route it away from the feedback network.
5. Place the BST capacitor as close to BST and SW as possible.



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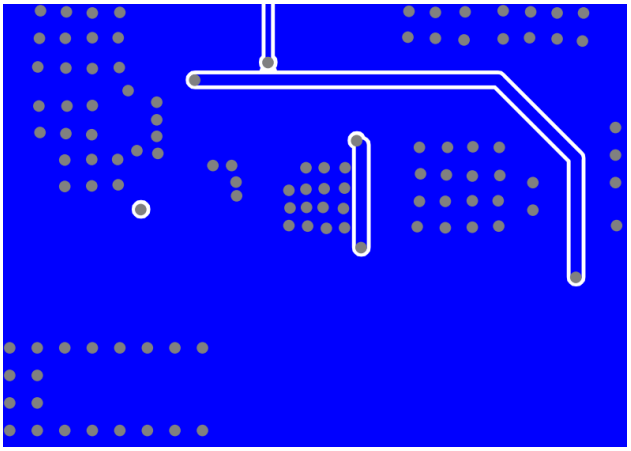

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Figure 5: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS

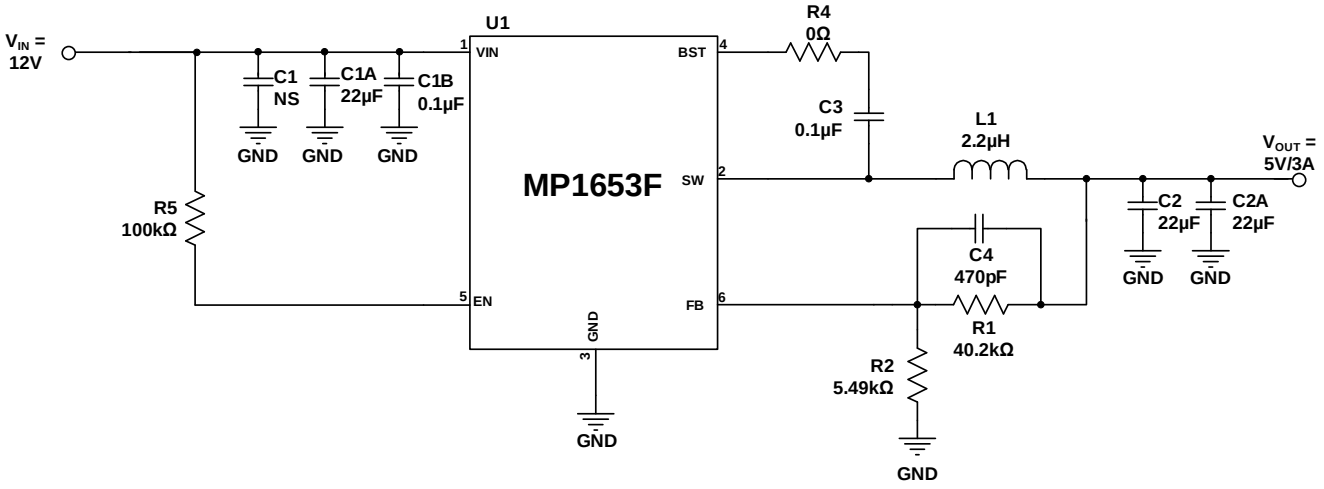

Figure 6: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 5V/3A)

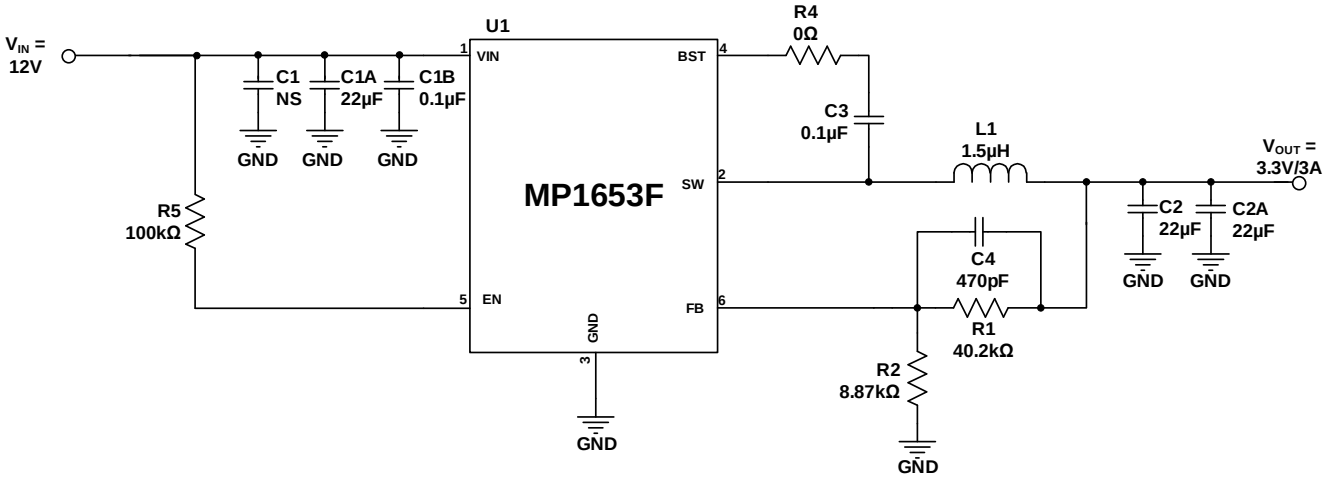

Figure 7: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 3.3V/3A)

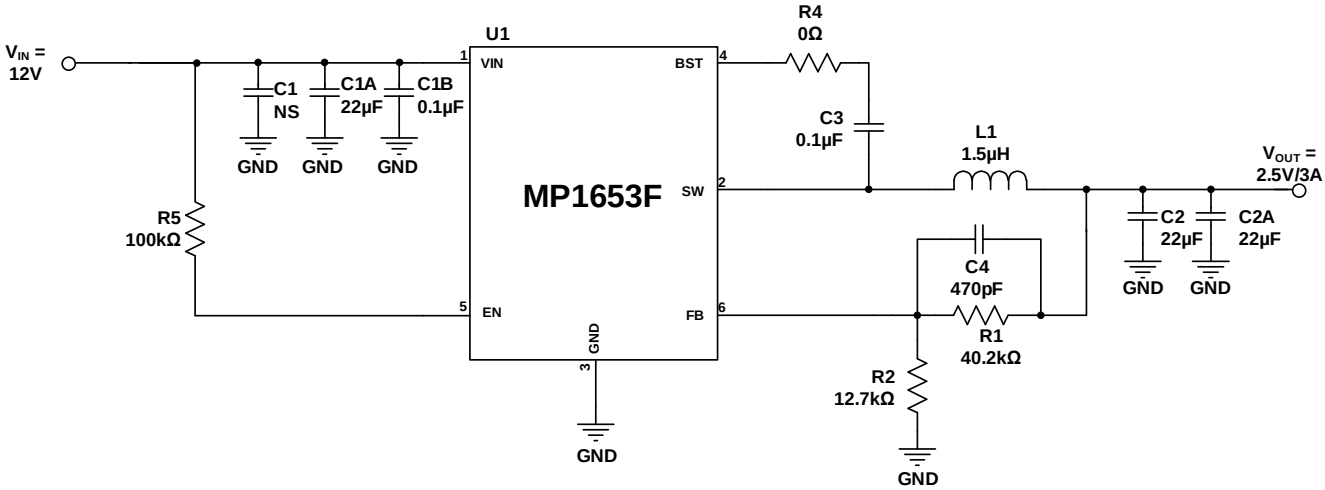

Figure 8: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 2.5V/3A)

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TYPICAL APPLICATION CIRCUITS *(continued)*

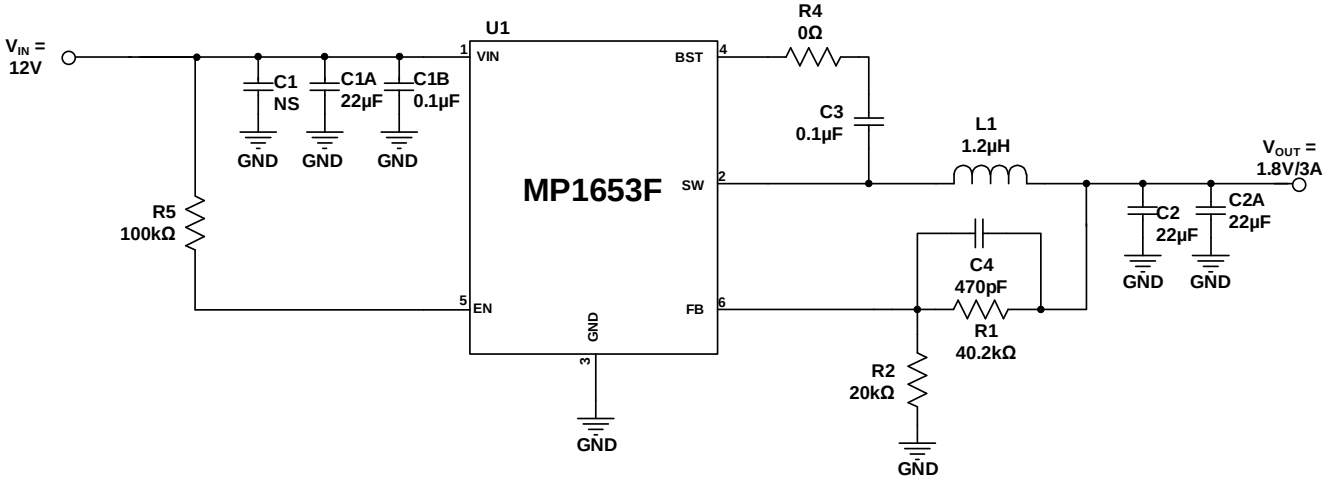

Figure 9: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 1.8V/3A)

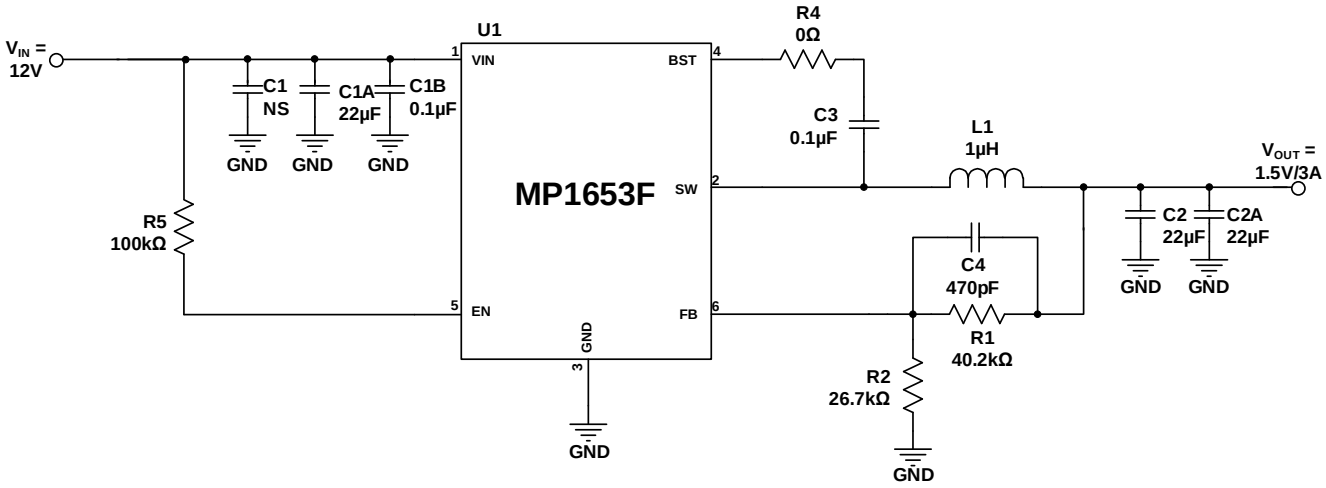

Figure 10: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 1.5V/3A)

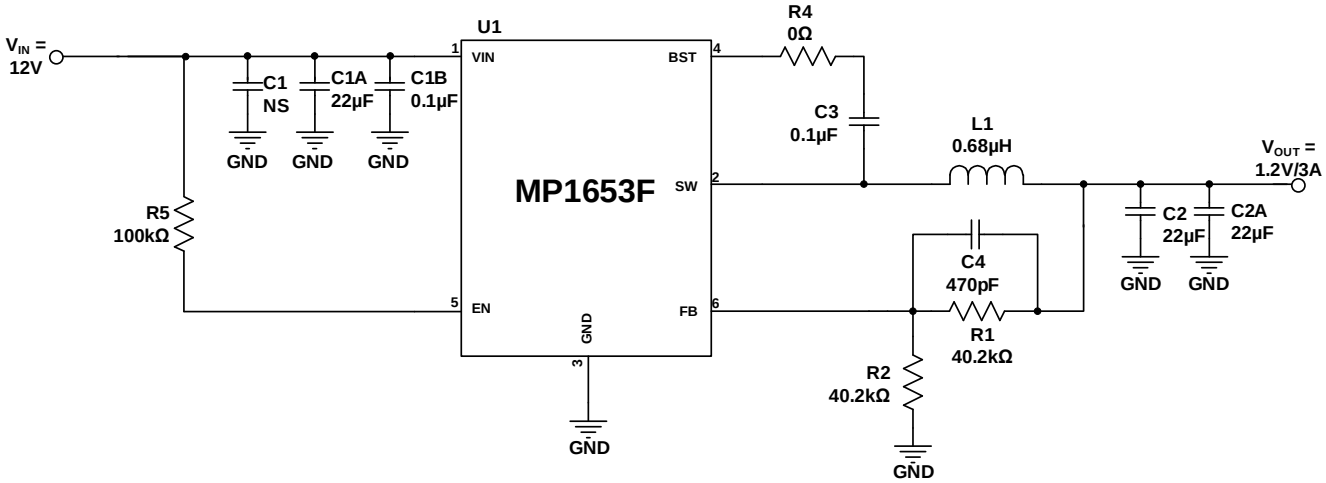

Figure 11: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 1.2V/3A)

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TYPICAL APPLICATION CIRCUITS *(continued)*

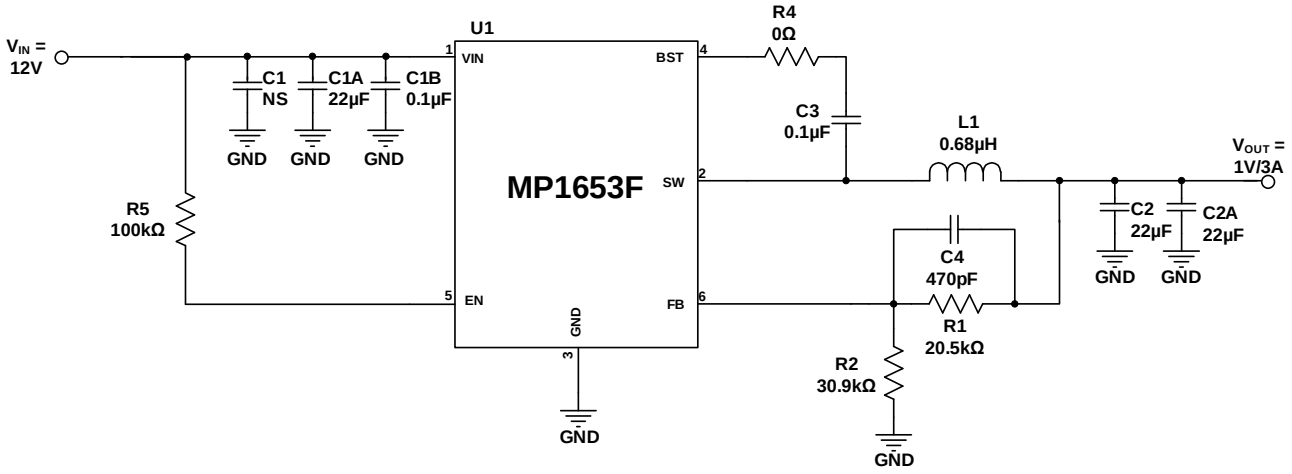

Figure 12: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 1V/3A)

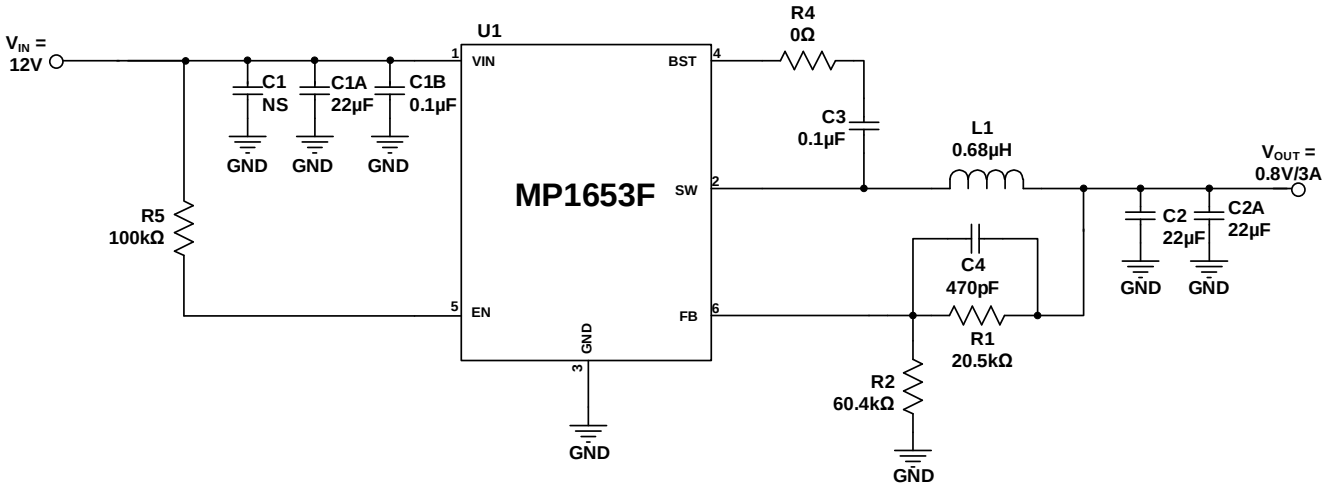

Figure 13: Typical Application Circuit (**V_{IN} = 12V, V_{OUT} = 0.8V/3A**)

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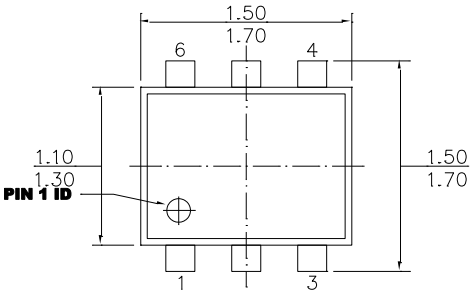
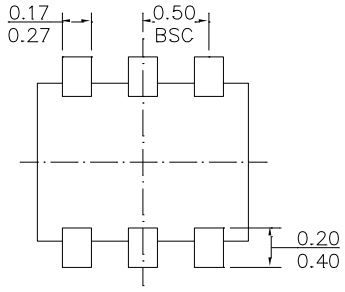
PACKAGE INFORMATION

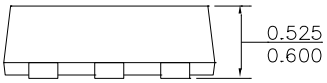
SOT563 (1.6mmx1.6mm)



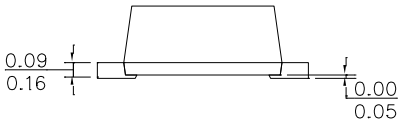
TOP VIEW



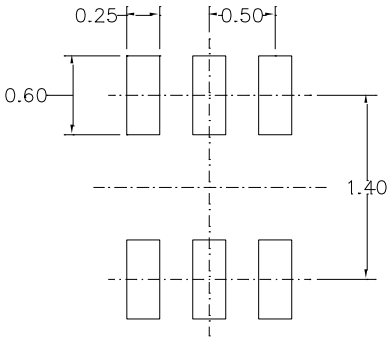
BOTTOM VIEW



FRONT VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING IS NOT TO SCALE.

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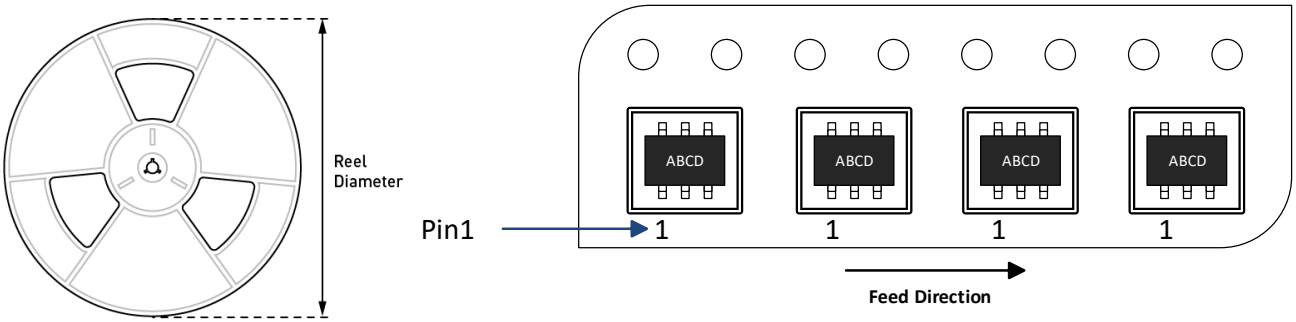
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP1653FGTF-Z	SOT563 (1.6mmx1.6mm)	5000	N/A	N/A	7in	8mm	4mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	12/10/2025	Initial Release	-

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