MID06W0505A

0.6W, 1.5kV$_{DC}$/3kV$_{DC}$, Regulated Isolated DC/DC Converter

DESCRIPTION

The MID06W0505A is a regulated, isolated DC/DC converter that can support 4.5V to 5.5V input voltage (V_{IN}) applications across a -40°C to +125°C operating temperature range. It has excellent load regulation, line regulation, and supports up to 0.6W of output power (P_{OUT}).

The device integrates a power MOSFET, transformer, and feedback (FB) circuit all in one chip. The MID06W0505A is a small solution that provides high reliability compared to traditional isolated power modules.

Full protection features include short-circuit protection (SCP), over-current protection (OCP), and OTP protection.

The MID06W0505A requires a minimal number of readily available, standard external components. It is available in a low-profile, wide body SOICW-16 package.

FEATURES

- 4.5V to 5.5V Operating Input Voltage (V_{IN}) Range
- 1.5KV$_{DC}$ or 3kV$_{DC}$ Isolation Voltage
- Up to 0.6W Output Power (P_{OUT})
- Max 53% Efficiency at Full Loads
- 0.2% Load Regulation
- 0.1% Line Regulation
- Excellent Transient Response
- Continuous Short-Circuit Protection (SCP) with Hiccup Mode
- Over-Temperature Protection (OTP)
- Meets CISPR32 Class B Emissions
- UL1577 Certified
- CB Certified per IEC62368-1 3rd Edition
- -40°C to +125°C Operating Temperature Range
- Available in an SOICW-16 Package

APPLICATIONS

- Industrial Automation Systems
- Isolated Bias Power for Digital Isolators
- Isolated Bias Power for RS-485, RS-422, and CAN Interfaces
- Isolated Sensor Power Supplies
- Telecom and Network Devices (e.g. 5G RRUs, Industrial CPE, and Network Gateways)

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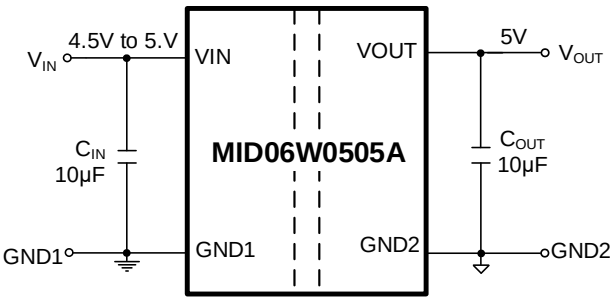
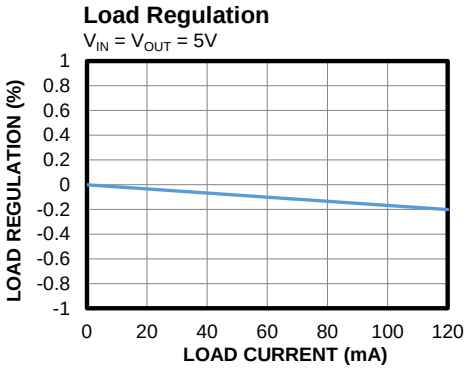
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number	Isolation Voltage	Package	Top Marking	MSL Rating
MID06W0505AGY-2R*	1.5kV$_{DC}$	SOICW-16	*See Below*	3
MID06W0505AGY-3R**	3kV$_{DC}$			

* For Tape & Reel, add suffix -Z (e.g. MID06W0505AGY-2R-Z).

** For Tape & Reel, add suffix -Z (e.g. MID06W0505AGY-3R-Z).

TOP MARKING (MID06W0505AGY-2R)

MPS YYWW
06W0505A2
LLLLLLLLL

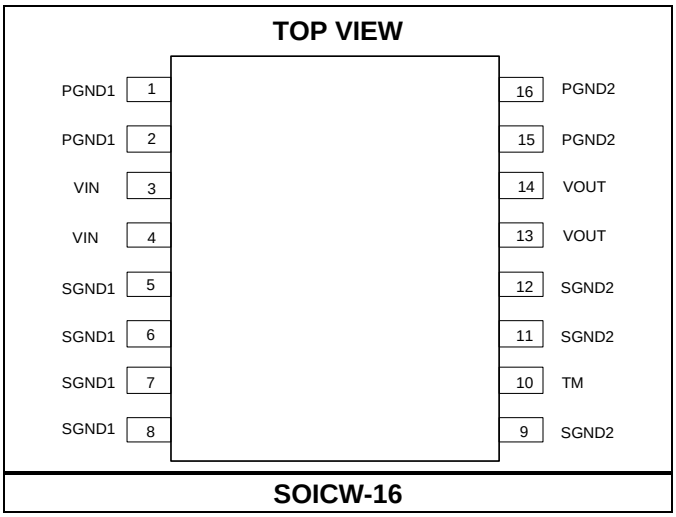
MPS: MPS prefix
YY: Year code
WW: Week code
06W0505A2: First nine digits of the part number
LLLLLLLLL: Lot number

TOP MARKING (MID06W0505AGY-3R)

MPS YYWW
06W0505A3
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
06W0505A3: First nine digits of the part number
LLLLLLLLL: Lot number

PACKAGE REFERENCE



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PIN FUNCTIONS

Pin #	Name	Description
1, 2	PGND1	**Power ground side 1.** Connect the PGND1 pin using large copper traces and multiple vias to improve thermal performance.
3, 4	VIN	**Power input pin.** Connect the VIN pin to a 4.5V to 5.5V power supply. Connect a 10μF capacitor and a 0.1μF capacitor between the VIN and PGND1 pins to stabilize the IC.
5, 6, 7, 8	SGND1	**Signal ground side 1.** Connect the SGND1 and PGND1 pins using large copper traces to improve thermal performance.
9, 11, 12	SGND2	**Signal ground side 2.** Connect the SGND2 and PGND2 pins using a thin trace. Do not connect SGND2 using large copper traces, as this can increase EMI.
10	TM	**Test mode.** Factory use only. Float this pin in application.
13, 14	VOUT	**Power output.** Connect a 10μF capacitor and a 0.1μF capacitor between the VOUT and PGND2 pins to decrease the output voltage (V_{OUT}) ripple and noise.
15, 16	PGND2	**Power ground side 2.** Do not connect the PGND2 pin using large copper traces, as this can increase EMI.

ABSOLUTE MAXIMUM RATINGS (1)

VIN to PGND1 or SGND1 .....-0.3V to +6V
VOUT to PGND2 or SGND2 .....-0.3V to +6V
Continuous power dissipation (T_A = 25°C) (2) (4)
..... 2.65W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) 6000V
Charged device model (CDM).....2000V

Recommended Operating Conditions (3)

Input voltage (V_{IN}) .....4.5V to 5.5V
Output voltage (V_{OUT})..... 5V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

EV06W0505A-Y-00B (4).....47.....11... °C/W
SOICW-16 (5).....48.....23… °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the converter to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on EV06W0505A-Y-00B (51mmx51mm), 1oz, 2-layer PCB.
5) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

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ELECTRICAL CHARACTERISTICS

V_{IN} = V_{OUT} = 5V, T_J = -40°C to +125°C (6), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Under-voltage lockout (UVLO) rising threshold	V_{UVLO_RISING}	Rising	2.4	2.61	2.8	V
UVLO hysteresis	V_{UVLO_HYS}			190		mV
Input current	I_{IN}	Load = 0A		7		mA
		Load = 0.12A		225		mA
Output voltage (V_{OUT}) accuracy	V_{OUT_ACC}	V_{IN} = 4.5V to 5.5V, load = 0A, T_J = 25°C	4.925	5	5.075	V
		V_{IN} = 4.5V to 5.5V, load = 0A, T_J = -40°C to +125°C	4.9	5	5.1	V
Load regulation		Load = 0A to 0.12A		0.2	1.5	%
Line regulation		Load = 0.12A, V_{IN} = 4.5V to 5.5V		0.1	1.5	%
Efficiency		Load = 0.12A		53		%
Ripple		Load = 0A to 0.12A, T_A = 25°C		50	100	mV
Capacitive load		With 40Ω resistance load	330			µF
Isolation voltage (MID06W0505AGY-2S)	V_{ISO_2S}	V_{TEST} = V_{ISO} for 60s (qualification), V_{TEST} = 1.2 x V_{ISO} for 1s (100% production)	1.5			kV_{DC}
Isolation voltage (MID06W0505AGY-3S)	V_{ISO_2S}	V_{TEST} = V_{ISO} for 60s (qualification), V_{TEST} = 1.2 x V_{ISO} for 1s (100% production)	3			kV_{DC}
Thermal shutdown (7)	T_{SD}			160		°C
Thermal shutdown hysteresis (7)	T_{SD_HYS}			20		°C

PACKAGE PARAMETERS

Parameter	Symbol	Condition	Min	Typ	Max	Units
Minimum external air gap (clearance)	L_{IO1}			8		mm
Minimum external tracking (creepage)	L_{IO2}			8		mm
Input to output capacitance (7)	C_{I-O}	Measure as a 2-terminal device, pin 1 to pin 8 are shorted together, pin 9 to pin 16 are shorted together, f_{SW} = 1MHz		7		pF
Input to output resistance (7)	R_{I-O}	Measure as a 2-terminal device, pin 1 to pin 8 are shorted together, pin 9 to pin 16 are shorted together, V_{TEST} = 500V_{DC}	50			GΩ

Notes:

6) Guaranteed by over-temperature correlation. Not tested in production.
7) Guaranteed by sample characterization. Not tested in production.

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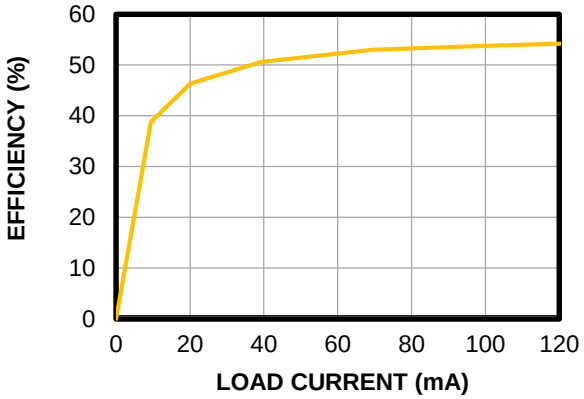
TYPICAL CHARACTERISTICS

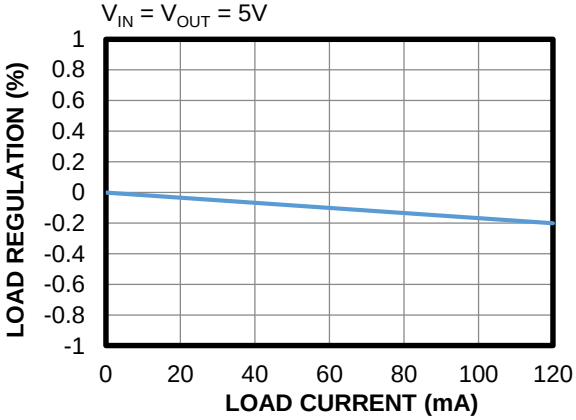
V_{IN} = 5V, V_{OUT} = 5V, C_{IN} = C_{OUT} = 10µF, T_A = 25°C, unless otherwise noted.

Efficiency vs. Load Current



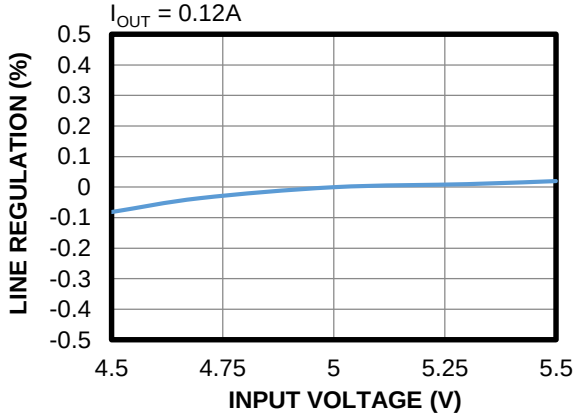
Load Regulation

V_{IN} = V_{OUT} = 5V

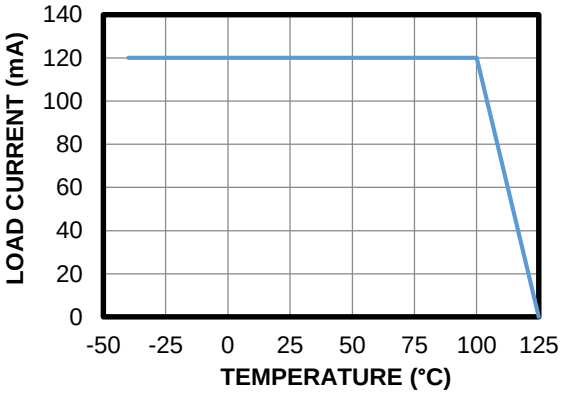


Line Regulation

I_{OUT} = 0.12A

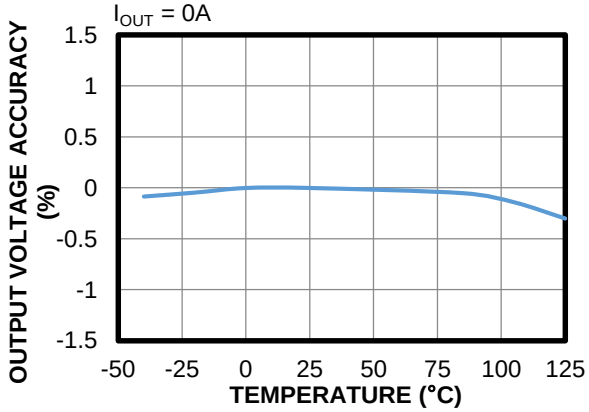


Load Current vs. Temperature



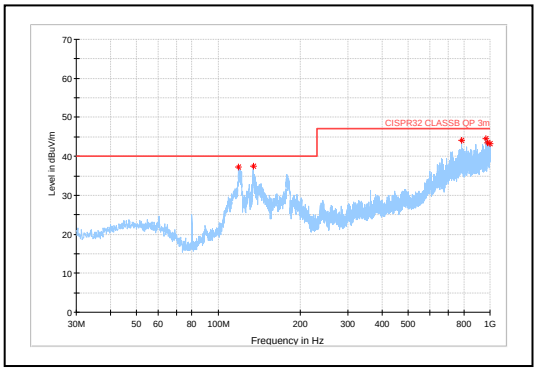
Output Voltage Accuracy vs. Temperature

I_{OUT} = 0A



Radiated Emissions

30MHz to 1GHz, CISPR32 Class B (8)



Note:

8) See Figure 2 on page 9 and Figure 3 on page 10 for details on the EMI circuit and PCB layout.

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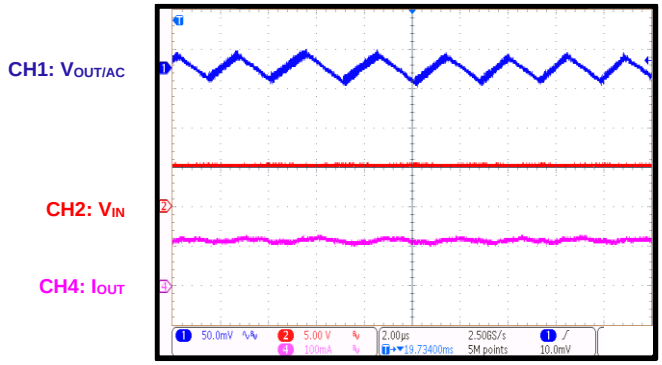
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 5V, C_{IN} = C_{OUT} = 10µF, T_A = 25°C, unless otherwise noted.

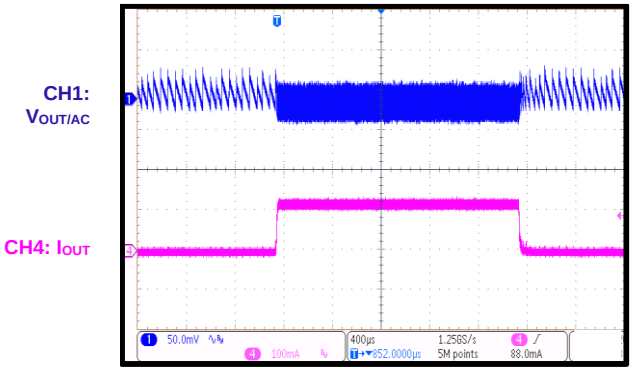
V_{OUT} Ripple

I_{OUT} = 0.12A



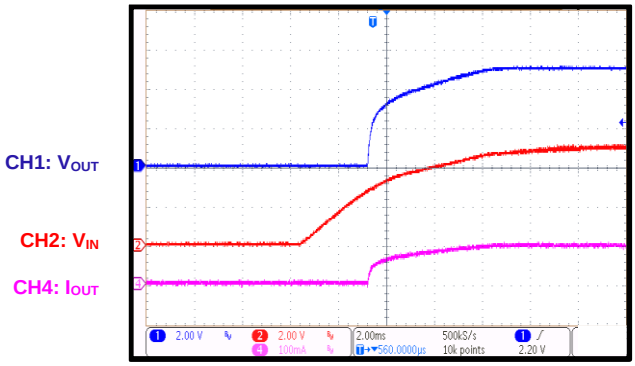
Load Transient

I_{OUT} = 0A to 0.12A



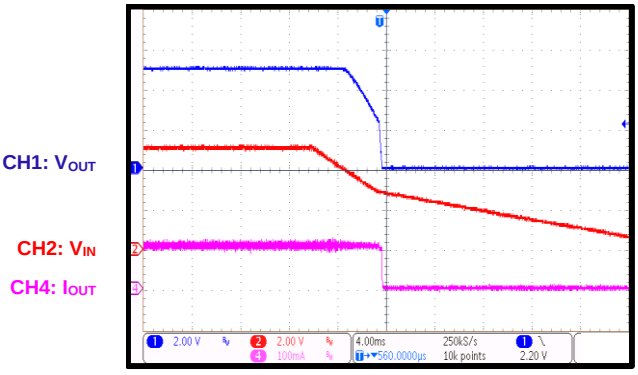
Start-Up through VIN

I_{OUT} = 0.1A

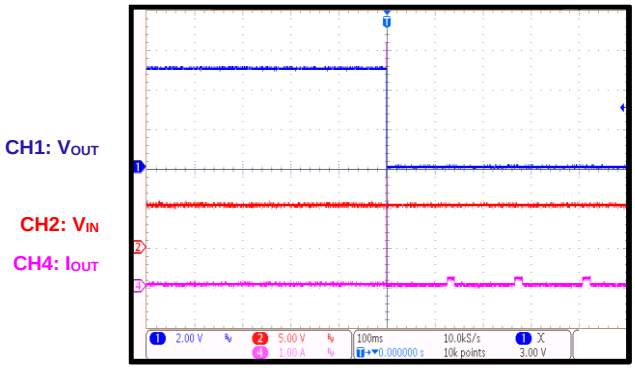


Shutdown through VIN

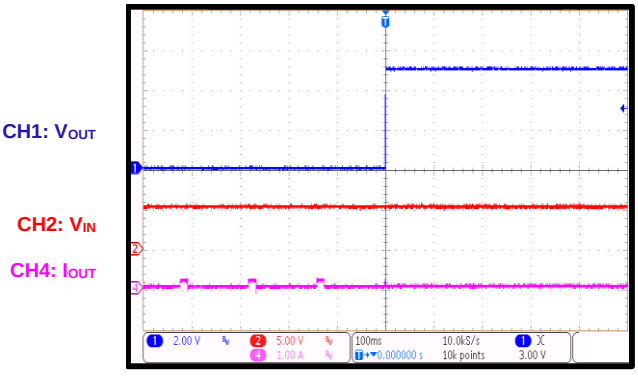
I_{OUT} = 0.1A



SCP Entry



SCP Recovery



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FUNCTIONAL BLOCK DIAGRAM

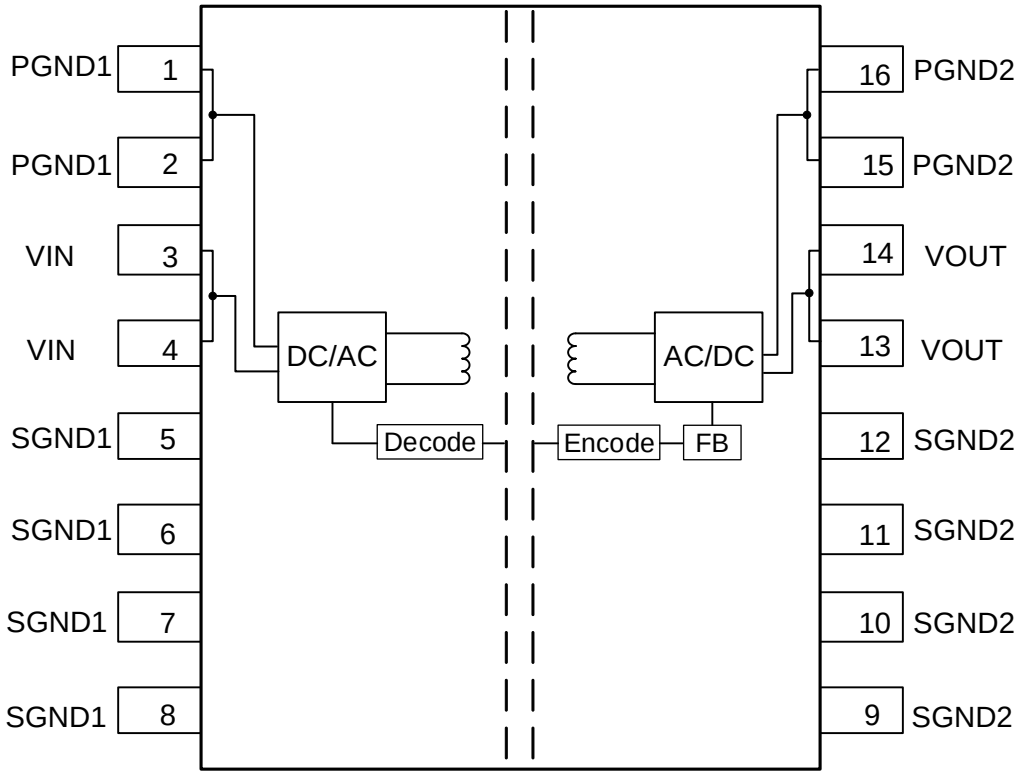

Figure 1: Functional Block Diagram

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OPERATION

The MID06W0505A is a regulated, isolated DC/DC converter that can support 4.5V to 5.5V input voltage (V_{IN}) applications across a -40°C to +125°C operating temperature range. It has excellent load regulation, line regulation, and supports up to 0.6W of output power (P_{OUT}).

Under-Voltage Lockout (UVLO) Protection

The MID06W0505A has input under-voltage lockout (UVLO) protection to ensure reliable P_{OUT}. The MID06W0505A starts up once V_{IN} exceeds the UVLO rising threshold. The device shuts down when V_{IN} drops below the UVLO falling threshold. This function prevents the device from operating at an insufficient voltage. UVLO is a non-latch protection.

Isolation Power Conversion

The MID06W0505A integrates a power MOSFET, transformer, and feedback (FB) circuit all in one chip, making it a high-performance, small-sized solution.

If V_{OUT} is below the target voltage, the IC starts switching to deliver power from V_{IN} to V_{OUT}. If V_{OUT} exceeds the target voltage, the device stops switching.

Power Converter Soft Start (SS) and Short-Circuit Protection (SCP)

To avoid overshoot and inrush current during start-up, the MID06W0505A has built-in internal soft start (SS) that gradually ramps up the output current (I_{OUT}).

The soft-start time (t_{SS}) is internally set to about 15ms. If V_{OUT} does not exceed 2.61V after t_{SS} due to a short circuit or large capacitive load, the MID06W0505A enters hiccup mode. The hiccup off time (t_{OFF}) is about 150ms. After the hiccup mode t_{OFF}, the MID06W0505A initiates another SS. If the short circuit is removed, then the MID06W0505A resumes normal operation.

Thermal Protection

The MID06W0505A monitors the IC temperature internally. If the die temperature exceeds 160°C, the driver outputs are disabled. Once the junction temperature (T_J) drops to 140°C, the driver outputs are enabled again and the device resumes normal operation.

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APPLICATION INFORMATION

Selecting the Input and Output Capacitors

For stable operation, connect a decoupling capacitor between the VIN and PGND1 pins at the input side, and one between the VOUT and PGND2 pins at the output side. Place these decoupling capacitors as close to VIN and VOUT as possible.

EMI Optimization

The first technique to reduce EMI is to build a low-ESL Y-capacitor using a 4-layer PCB layout to filter high-frequency noise on the secondary side. The Y-capacitor is formed with the two overlapping middle layers. Mid-layer 1 is the PGND1 copper plane, which forms the Y-capacitor's top plate. Mid-layer 2 is the ground after the ferrite bead (GND2), which forms the Y-capacitor's bottom plate. More overlap in these layers provides a larger Y-capacitor value, which further reduces EMI. The second technique to reduce EMI is to use stitching vias on the GND planes to suppress electromagnetic transmissions.

Aside from the two PCB layout techniques described above, a pair of ferrite beads are required to form a CLC structure filter (see Figure 2). Place this filter as close to VOUT and PGND2 as possible. The capacitor closest to the IC (C2B) should be ≥4.7µF to ensure a stable output. Do not place large copper areas on the secondary side pins, as this can increase switching noise and EMI. Connect SGND2 and PGND2 using a thin trace.

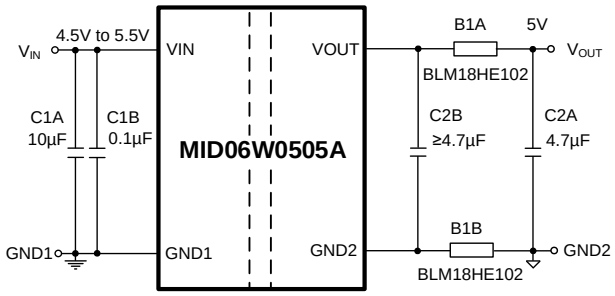

Figure 2: Recommended EMI Schematic

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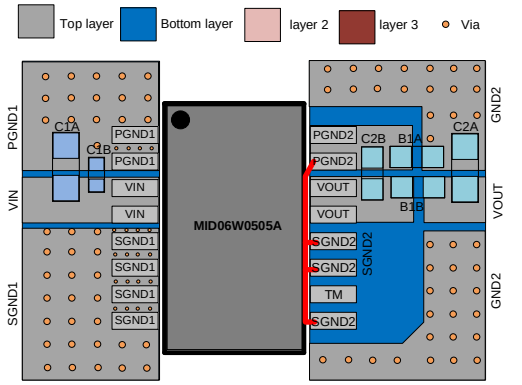
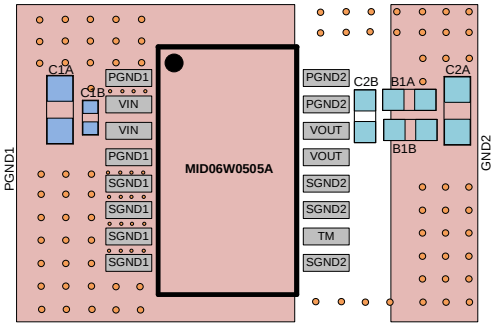
PCB Layout

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 3 and follow the guidelines below:

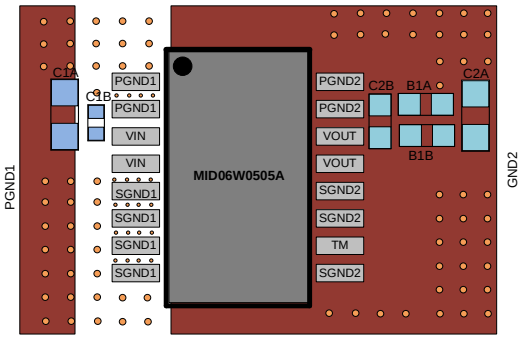
1. For safety, the primary side and secondary side should be physically separated. Ensure that the creepage/clearance meets the standards for the specified application.
2. To reduce output noise, minimize the loop area between VIN, the input capacitor, and PGND1, as well as VOUT, the output capacitor, and PGND2.
3. Place enough copper and vias around the IC's primary pin output to improve thermal performance.
4. Connect SGND1 and PGND1 using large copper traces and multiple vias to improve thermal dissipation.
5. Connect SGND2 and PGND2 using a thin trace (below the red trace in Figure 3) to reduce radiation.



Top Layer and Bottom Layer



Mid-Layer 1



Mid-Layer 2

Figure 3: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUIT

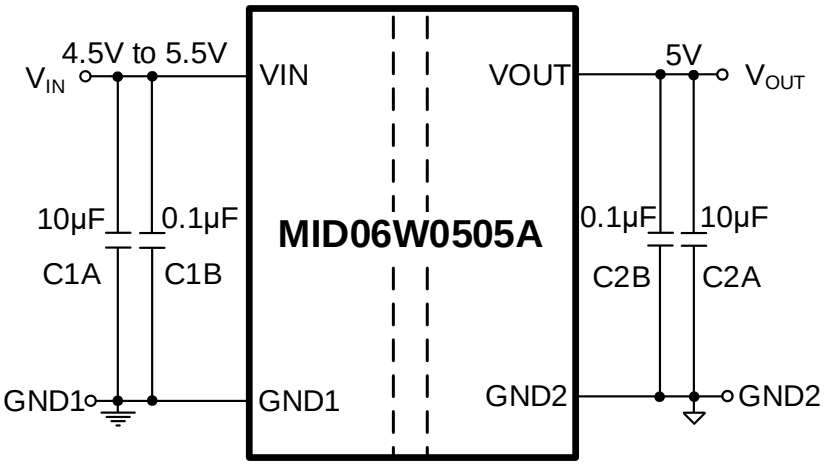

Figure 4: Typical Application Circuit

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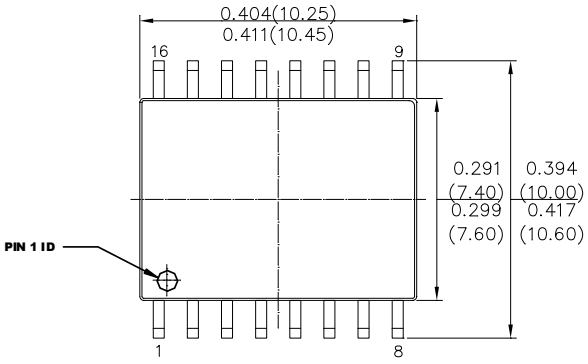
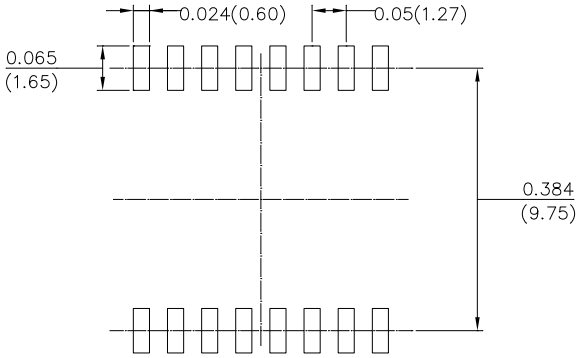
PACKAGE INFORMATION

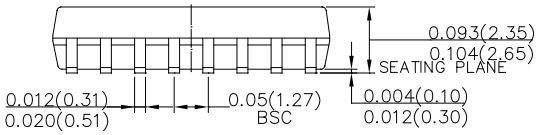
SOICW-16



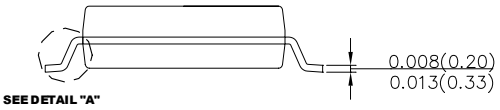
TOP VIEW



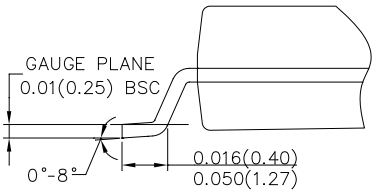
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-013, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

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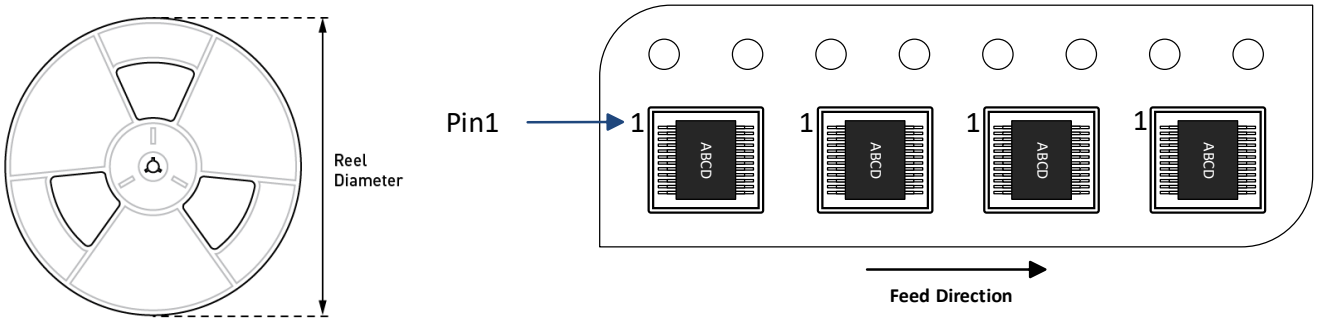
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MID06W0505AGY-2R-Z	SOICW-16	1000	44	N/A	13in	24mm	12mm
MID06W0505AGY-3R-Z							

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	2/8/2023	Initial Release	-

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