HR1213

Multi-Mode PFC and Current Mode LLC Combo Controller Supporting both AC and DC Inputs with Configurable Bias Options

DESCRIPTION

The HR1213 is a multi-mode PFC and current mode LLC combo controller that can be configured via the UART interface. Power-saving technology helps the device optimize efficiency across the full operating range.

The PFC controller employs a patented, digital average current control scheme to achieve hybrid continuous conduction mode (CCM) and discontinuous conduction mode (DCM) operation. Under heavy loads, CCM reduces the peak MOSFET current so the controller can be used across a wider load range. Under light loads, DCM reduces the switching frequency for better efficiency. Burst mode has configurable, digital soft switching to improve both light-load efficiency and audible noise.

Current mode control is implemented in the LLC stage to achieve good stability and fast response. Three operation modes are implemented based on the different load conditions: steady state, skip, and burst mode. This allows different load conditions to be independently optimized for efficiency. At light loads, digital, frequency-controlled burst mode is applied to reduce both switching power loss and audible noise. Adaptive dead-time adjustment (ADTA) and capacitive mode protection (CMP) is also applied to guarantee zero-voltage switching (ZVS) without capacitive mode operation.

The HR1213 has an internal, high-voltage (HV) current source for start-up, meaning that a traditional start-up resistor or external circuit is not required. An external DC source can provide a supply for VCC.

Protections include thermal shutdown (TSD), PFC open-loop protection (OLP), over-voltage protection (OVP), over-current limit (OCL) and LLC over-current protection (OCP), SO pin protection, and over-power protection (OPP).

The HR1213 is available in SOIC-20 and TSSOP-20 packages.

FEATURES

- **General System Features:**
  - High-Voltage Current Source for Start-Up
  - UART Interface for Configurations
  - User-Friendly GUI
  - Available in SOIC-20 and TSSOP-20 Packages
- **PFC Controller:**
  - CCM/DCM Multi-Mode PFC Control with High Efficiency across All Loads
  - Operating Frequency Up to 250kHz
  - High PF due to Input Capacitor Current Compensation
  - Configurable Frequency Jittering
  - Configurable Soft Start and Burst On
  - Configurable AC Input Brown-In/Out
  - Cycle-by-Cycle Current Limiting
  - OLP, OVP
- **LLC Controller:**
  - 600V HS Gate Driver with Bootstrap Diode and High dV/dt Immunity
  - Current Mode Control
  - Up to 500kHz in Steady State
  - Adaptive Dead-Time Adjustment with Minimum and Maximum Limit
  - Burst/Skip Mode Switching under Light Loads
  - Configurable Burst Frequency with Low Audible Noise
  - Configurable Soft Start
  - Configurable DC Input Brown-In/Out
  - Capacitive Mode Protection
  - OCP and OPP with Auto-Restart or Latch-Off Mode
  - Configurable Protections on the SO Pin

APPLICATIONS

- Desktop PCs and ATX Power Supplies
- All-in-One and Gaming Power Supplies
- Notebook Adapters
- TV Power Supplies
- Power Tools Power Supplies
- LED Drivers

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TYPICAL APPLICATIONS

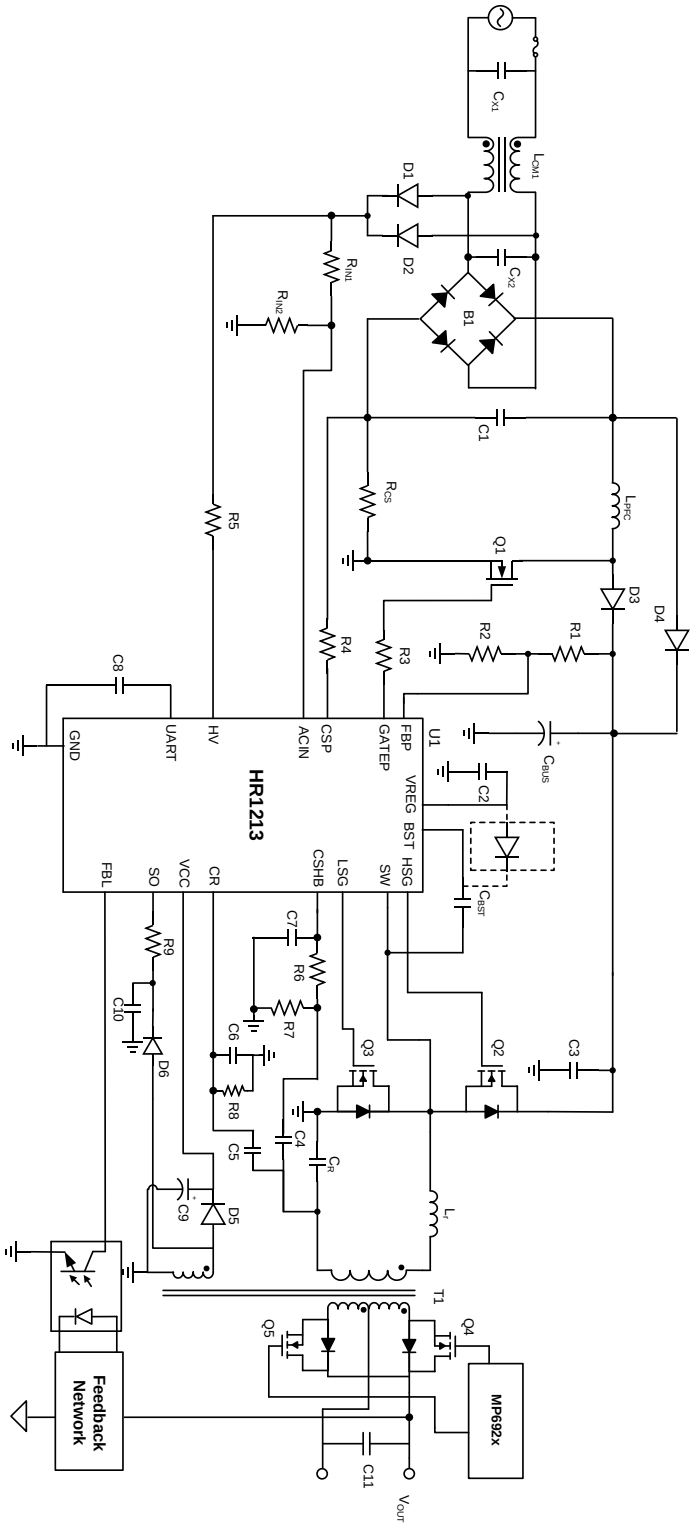

Figure 1: Typical Application Circuit (VCC Supplied by Auxiliary Winding)

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TYPICAL APPLICATIONS *(continued)*

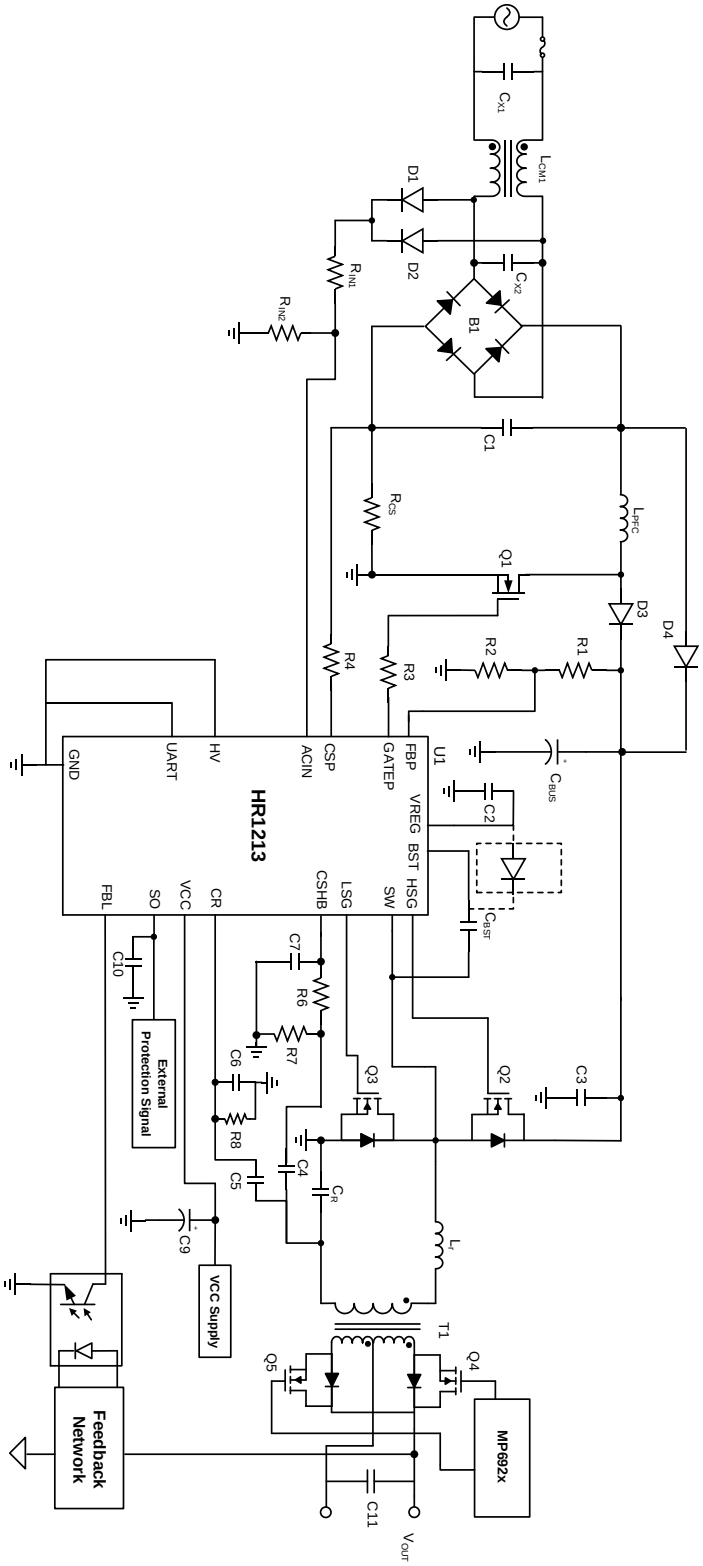

Figure 2: Typical Application Circuit (VCC Supplied by External DC Source)

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TYPICAL APPLICATIONS *(continued)*

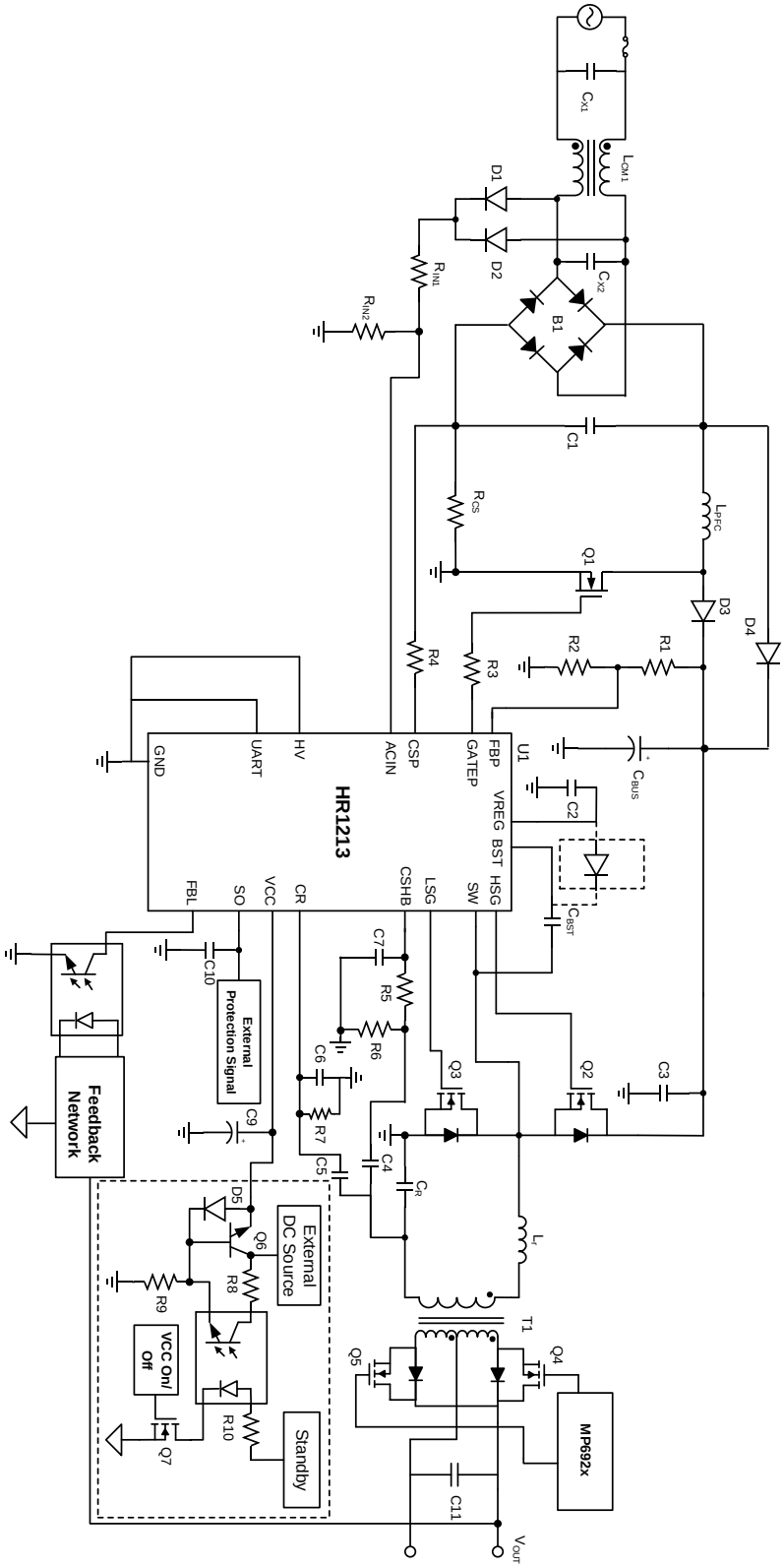

Figure 3: Typical Application Circuit (VCC Supplied by External DC Source with On/Off Control)

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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
HR1213GM-xxxx**	TSSOP-20	*See Below*	2
HR1213GY-xxxx	SOIC-20	*See Below*	3

* For Tape & Reel, add suffix -Z (e.g. HR1213GM-xxxx-Z).

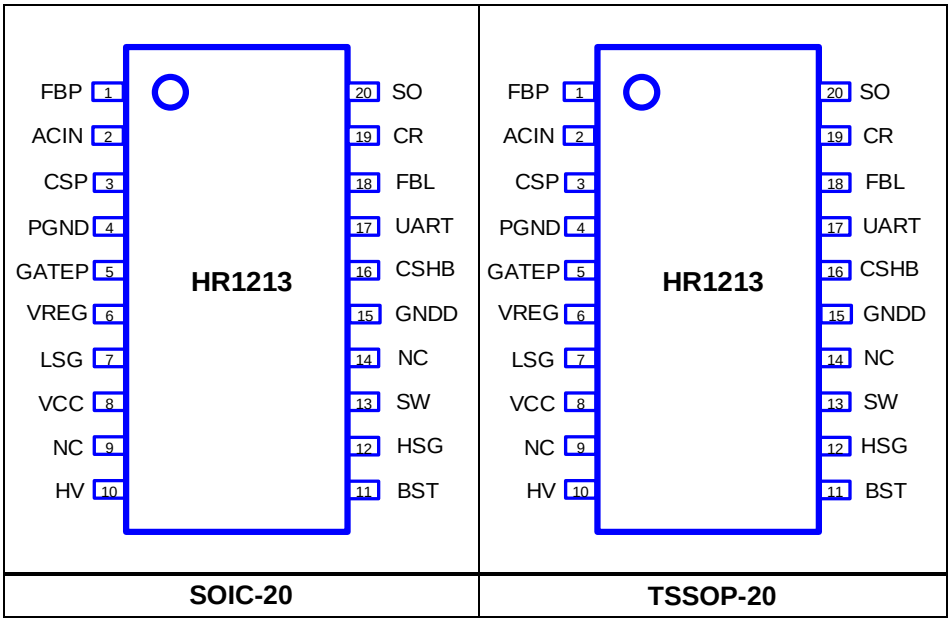
** "-xxxx" is for internal code version control. For custom projects, MPS assigns a unique 4-digit number.

TOP MARKING

MPSYYWW
HR1213
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
HR1213: Part number
LLLLLLLLL: Lot number

PACKAGE REFERENCE



SOIC-20	TSSOP-20

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PIN FUNCTIONS

Pin #	Name	Description
1	FBP	**PFC output voltage sense.** The FBP pin senses the PFC output voltage to calculate the PFC switch on time, monitor for over-voltage protection (OVP) and open-load protection (OLP), and calculate the digital current reference ($I_{REF(N)}$) that determines the PFC switching frequency. A 3.3MΩ pull-down resistor is connected to FBP internally. It is recommended to connect a capacitor (about 4.7nF) to FBP for noise immunity.
2	ACIN	**AC input voltage sense.** The ACIN pin senses the AC input voltage to calculate the PFC switch on time calculation, monitor for brown-in/out protection, and calculate the digital current reference ($I_{REF(N)}$) that determines the PFC switching frequency. It is recommended to connect a capacitor (about 2.2nF) to ACIN for noise immunity.
3	CSP	**PFC switching current sense.** CSP defines the PFC switch on time, switching frequency, and cycle-by-cycle current limit protection. Connect a 500Ω resistor in series between the current-sense resistor and the CSP pin via the internal ESD clamping capability. This resistor prevents the CSP pin from overstress under AC plug-in or surge conditions. Another solution is to add an external clamping component to CSP.
4	PGND	**Ground reference for the PFC and LLC low-side gates.**
5	GATEP	**PFC gate driver output.**
6	VREG	**Provides a regulated voltage for the PFC and LLC gate drivers and internal circuits.**
7	LSG	**LLC low-side gate driver output.**
8	VCC	**IC supply power.** VCC can be charged by an internal current source through HV or an external power supply.
9	NC	**No connection.**
10	HV	**High-voltage supply input for internal HV start-up source.**
11	BST	**Voltage bootstrap.** An internal bootstrap diode is connected between the BST and VCC pins. Connect an external capacitor between the BST and SW pins to drive the high-side MOSFET of the half-bridge LLC.
12	HSG	**LLC high-side gate driver output.**
13	SW	**High-side switch source.** SW is the current return for the high-side gate driver current. SW requires additional layout considerations to avoid creating large spikes below ground.
14	NC	**No connection.**
15	GNDD	**Ground reference for the digital PFC core.**
16	CSHB	**Half-bridge current sense.** Use a sense resistor or a capacitive divider to sense the primary current. The CSHB pin has the following functions: • Over-current protection (OCP): If the current continues to rise despite the increasing frequency and $V_{CSHB} > V_{CS-OCP}$, OCP is triggered. The IC initiates its configured protection mode (auto-retry or latch-off mode). • Capacitive mode protection (CMP): The voltage on CSHB is compared to V_{CSNR} and V_{CSPR} to determine whether the LLC current is in a positive or negative polarity. The IC terminates the high-side gate driver (HSG) if the current goes into negative polarity ($V_{CSHB} < V_{CSPR}$). The IC terminates the low-side gate driver (LSG) if the current goes into positive polarity ($V_{CSHB} > V_{CSNR}$).

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PIN FUNCTIONS *(continued)*

Pin #	Name	Description
17	UART	**Half-duplex communication I/O interface.** UART provides a half-duplex communication I/O interface. UART is internally pulled up to 3.3V with a 1.6kΩ resistor (R_{UART}). It is not recommended to rely on real-time communication in application. Do not pull UART high when V_{CC} drops below V_{CCUVP2}. When VCC supplied by an external power supply, short UART to GND.
18	FBL	**LLC output voltage feedback input.** FBL is internally pulled up by a voltage source with an internal resistor. FBL defines the LLC switching frequency according to the load condition. The voltage on FBL activates LLC skip mode, burst mode, and over-power protection (OPP).
19	CR	**LLC capacitor voltage-sense input.** CR senses the divided resonant capacitor voltage to determine the LLC switching frequency.
20	SO	**External protection input.** If the sensed SO voltage exceeds V_{SO_OVP}, a protection is triggered and the IC initiates its configured mode (auto-retry or latch-off mode). To achieve external thermal shutdown (TSD), attach an external NTC to this pin (see Figure 39).

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ABSOLUTE MAXIMUM RATINGS (1)

HV to PGND ..... -0.3V to +700V
BST to PGND ..... -0.3V to +618V
SW to PGND ..... -3V (6) to +618V
HSG to PGND 618V
LSG to PGND ..... -0.3V to +14V
BST to SW ..... -0.3V to +14V
HSG to SW ..... -0.3V to +14V
SW to PGND maximum slew rate 50V/ns
VCC to PGND ..... -0.3V to +38V
VREG to PGND ..... -0.3V to +14V
GATEP to PGND ..... -0.3V to +14V
CR, CSHB to GNDD ..... -3.3V (6) to +3.6V
CSP to GNDD ..... -5V to +3.6V
PGND to GNDD ..... -0.3V to +0.3V
All other pins to GNDD ..... -0.3V to +3.6V
VREG supply current 40mA
BST internal diode average forward current (5) 0.2A
CSP input current limit at negative voltage overstress (clamped by internal ESD device) (6)
2ms single pulse ..... -0.15A
100µs single pulse ..... -0.17A
20µs single pulse ..... -0.20A
Continuous power dissipation (T_A = 25°C) (3)
SOIC-20 ..... 1.92W
TSSOP-20 ..... 1.38W
Storage temperature ..... -55°C to +150°C
Junction temperature ..... -40°C to +150°C
Lead temperature ..... 260°C

ESD Ratings (1)

Human body model (HBM) 2000V
Charged device model (CDM) 1500V

Recommended Operating Conditions (2)

Supply voltage (V_{CC}) ..... 12V to 35V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
SOIC-20	65	30	°C/W
TSSOP-20	90	40	°C/W

Notes:

1) The device is not guaranteed to function outside of its operating conditions.
2) Exceeding these ratings may damage the device.
3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) Measured on JESD51-7, 4-layer PCB.
5) Guaranteed by design.
6) Guaranteed by characterization.

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ELECTRICAL CHARACTERISTICS

V_{CC} = 25V, T_J = -40°C to +125°C, min and max values are guaranteed by characterization, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
High-Voltage Start-Up Current Source (HV Pin)						
Breakdown voltage	V_{HVBR}		700			V
Normal charge current	I_{HVNOR}	V_{CCSCP} < V_{CC} < 15V, T_J = 25°C	7.9	10	12.5	mA
Extra charge current from the VCC pin	I_{VCCON_OUT}	V_{CC} = $V_{CCON(HV)}$ - 0.1V, T_J = 25°C	2.5			mA
Supply current when a fault occurs	$I_{HVLIMIT}$	V_{CC} < V_{CCSCP}	1.5	2.2	3.3	mA
Leakage current at off state	I_{HVOFF}	V_{HV} = 400V, V_{CC} = 24V		4.5	10	µA
IC Power Supply (VCC Pin)						
IC turn-on threshold voltage with HV detected	$V_{CCON(HV)}$	V_{HV} > V_{HVON}	20	21.5	23	V
IC turn-on threshold (at external supply mode and V3.3 enabled)	$V_{CCON(EX)}$		10.9	11.8	12.7	V
Internal V3.3 supply enable	$V_{3V3ENABLE}$		11.6	12.5	13.4	V
UV protection threshold 1	V_{CCUVP1}		10	10.8	11.5	V
UV protection threshold 2	V_{CCUVP2}		13.5	14.4	15.2	V
IC release threshold	V_{CCRST}		8	8.8	9.3	V
X-capacitor discharge regulation voltage (7)	V_{CCXCD}			17		V
Short-circuit protection	V_{CCSCP}		0.76	0.94	1.4	V
Normal operating current	$I_{CC(NOR)}$	C_{GATEP} = 1nF, f_{PFC} = 100kHz, C_{HSG} = 1nF, C_{LSG} = 1nF, f_{LLC} = 200kHz		15		mA
		No switch, T_J = 25°C		8	10	
Start-up current	$I_{CC-START1}$	V_{CC} = 20V		2.1	3	mA
Burst-mode current	$I_{CC-BURST}$	During burst off, T_J = 25°C		2	2.7	mA
PFC Gate Driver (GATEP Pin)						
Minimum gate high voltage	V_{OH}	C_{GATEP} = 1nF, source 20mA, V_{REG} = 11.5V	11.3			V
Maximum gate low voltage	V_{OL}	C_{GATEP} = 1nF, sink 20mA, V_{REG} = 11.5V			0.1	V
Gate on resistance	$R_{ON(H)}$	Source 20mA		4.5	7.5	Ω
	$R_{ON(L)}$	Sink 20mA		2.5	5	Ω
Voltage falling time	t_F	C_{GATEP} = 1nF		20	40	ns
Voltage rising time	t_R	C_{GATEP} = 1nF		20	40	ns
Sourcing capacity (7)	I_{GATE_SR}			650		mA
Sinking capacity (7)	I_{GATE_SK}			800		mA

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{CC} = 25V, T_J = -40°C to +125°C, min and max values are guaranteed by characterization, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Regulated Power Supply (VREG Pin)						
Regulated output voltage	V_{REG}	I_{REG} = 0mA	11	12	13	V
		I_{REG} = 20mA	10.9	11.9	12.8	V
Turn-on threshold	V_{REGON}		9	10	10.9	V
UVP	V_{REGUVP}		6.5	7.3	8.1	V
System Clock						
Clock frequencies	f_{OSC_LLC}	Normal operation	180	200	223	MHz
	f_{OSC_PFC}	Normal operation	16.6	17.5	18.7	
	f_{OSC_NOPWM} (7)	During burst off or if a fault occurs		1		
AC Input Sensing (ACIN Pin)						
Voltage range			0		1.6	V
PFC Feedback (FBP Pin)						
Voltage range			0		1.6	V
Current Sense (CSP Pin)						
Voltage range			-1.4		0	V
Internal biased voltage	V_{BIAS_CSP}	V_{CSP} = 0V	0.19	0.2	0.21	V
UART Interface (UART Pin)						
Internal pull-up voltage				3.3		V
Internal pull-up resistor				1.6		kΩ
ADC for CSP						
ADC voltage reference			1.585	1.6	1.61	V
		T_J = 25°C	1.595	1.6	1.605	V
ADC resolution (8)				12		bits
Acquisition time (7)				300		ns
INL (integral non-linearity) (8)				±4		LSB
DNL (differential non-linearity) (8)				±4.5		LSB
Offset error (8)				±0.5		LSB
Gain error (8)				±1.5		LSB
ADC for ACIN, FBP, FBL						
ADC voltage reference			1.585	1.6	1.61	V
		T_J = 25°C	1.595	1.6	1.605	V
ADC resolution (8)				10		bits
Acquisition time (7)				300		ns
INL(Integral non-linearity) (8)				±4		LSB
DNL (differential non-linearity) (8)				±4.5		LSB
Offset error (8)				±0.5		LSB
Gain error (8)				±1.5		LSB

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{CC} = 25V, T_J = -40°C to +125°C, min and max values are guaranteed by characterization, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
DAC for OVP OCL, BI/BO of PFC; OPP, ADOFF of LLC						
DAC voltage reference			1.585	1.6	1.61	V
		T_J = 25°C	1.595	1.6	1.605	V
Resolution (8)				8		bits
PFC BI/BO DAC Output				0.4		V
Offset error (8)				±0.2		LSB
Gain error (8)				±1.5		LSB
DAC for PFC Set Signal						
DAC voltage reference			1.585	1.6	1.61	V
		T_J = 25°C	1.595	1.6	1.605	V
Resolution (8)				10		bits
Offset error (8)				±0.5		LSB
Gain error (8)				±1.5		LSB
DAC for LLC Set Signal						
DAC voltage reference			1.77	1.8	1.825	V
		T_J = 25°C	1.788	1.8	1.812	V
Resolution (8)				10		bits
Offset error (8)				±0.5		LSB
Gain error (8)				±1.5		LSB
High-Side Floating Gate Driver Supply (BST and SW Pins)						
BST pin leakage current	I_{LKBST}	V_{BST} = 600V			10	µA
SW pin leakage current	I_{LKSW}	V_{SW} = 582V			10	µA
Half-Bridge Current Sense (CSHB Pin)						
OCP threshold	V_{CS-OCP}		1.475	1.5	1.52	V
Current polarity comparator reference when HSG is on	V_{CSPR}	T_J = 25°C		80		mV
Current polarity comparator reference when LSG is on	V_{CSNR}	T_J = 25°C		-80		mV
Output Voltage Sense (SO Pin)						
Over-voltage protection (OVP) on SO	V_{SO-OVP}		1.475	1.5	1.52	V
ADTA (SW Pin)						
Minimum voltage slew rate that can be detected (7)	dV_{MIN}/dt			85		V/µs
Turn-on delay (7)	t_D	Slope finished to turn-on delay		150		ns

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{CC} = 25V, T_J = -40°C to +125°C, min and max values are guaranteed by characterization, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Feedback Section (FBL Pin)						
Internal pull-up resistor on FBL	R_{FBL_LOW}	T_J = 25°C	7	8	9.6	kΩ
Internal pull-up resistor on FBL in power-save mode	R_{FBL_HIGH}		38	47	56	kΩ
Internal voltage reference	V_{FBL_SOURCE}	T_J = 25°C	2.46	2.53	2.6	V
V_{COMP} offset voltage from the FBL voltage	V_{FBL_OFFSET}		0.995	1	1.005	V
Current-Sense Input Section (CR Pin)						
Slope compensation amplitude per LSB	V_{CR_SLOPE}	T_J = 25°C	1.54	2.35	3.16	mV/µs
Zero-voltage detection threshold	V_{CR_ZERO}		15	20	25	mV
On-time comparator delay to HG driver off (7)	t_{D_CR}			150		ns
Current-sense input leakage current	$I_{CR_LEAKAGE}$	V_{CR} = 2V			±1	µA
Leading-edge blanking time (7)	t_{LEB}			300		ns
Low-Side Gate Driver (LSG Pin)						
Peak source current (7)	$I_{SOURCEPK}$			0.75		A
Peak sink current (7)	I_{SINKPK}			0.87		A
Source resistor	R_{SOURCE}			5	8	Ω
Sink resistor	R_{SINK}			2.5	5	Ω
Falling time	t_F			20	40	ns
Rising time	t_R			20	40	ns
High-Side Gate Driver (HSG Pin, Referenced to the SW Pin)						
Peak source current (7)	$I_{SOURCEPK}$			0.74		A
Peak sink current (7)	I_{SINKPK}			0.87		A
Source resistor	R_{SOURCE}			5	8	Ω
Sink resistor	R_{SINK}			2.5	5	Ω
Falling time	t_F			20	40	ns
Rising time	t_R			20	40	ns
Thermal Shutdown						
Thermal shutdown threshold (7)				145		°C
Thermal shutdown recovery threshold (7)				120		°C

Notes:

7) Guaranteed by design.
8) Guaranteed by characterization.

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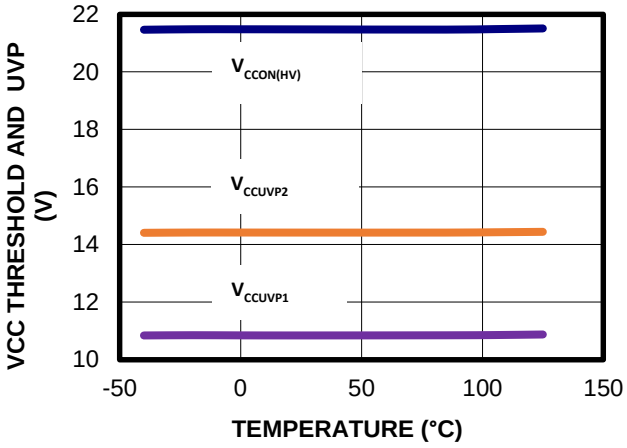
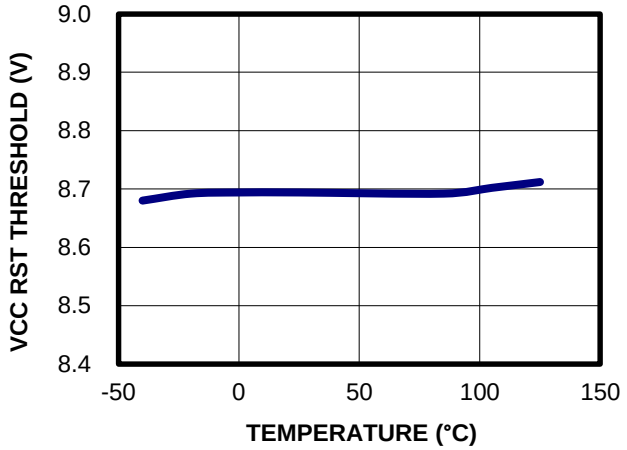
TYPICAL CHARACTERISTICS

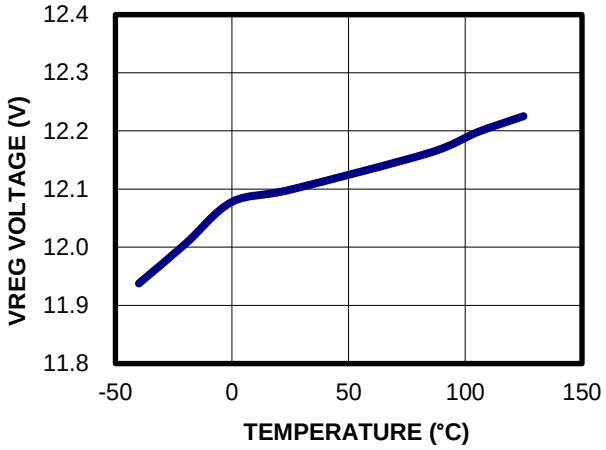
VCC Threshold and Under-Voltage Protection (UVP) vs. Temperature



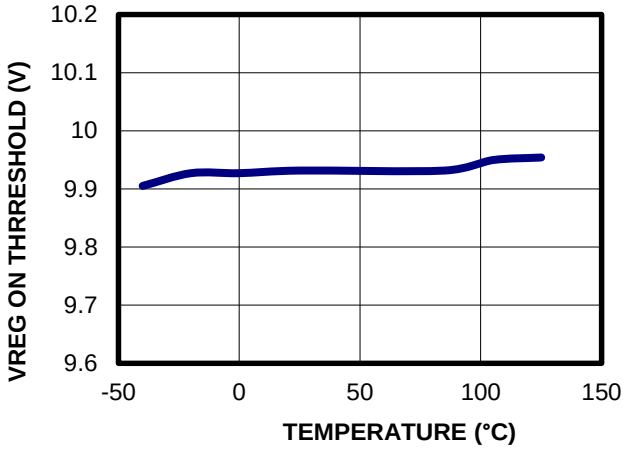
VCC RST Threshold vs. Temperature



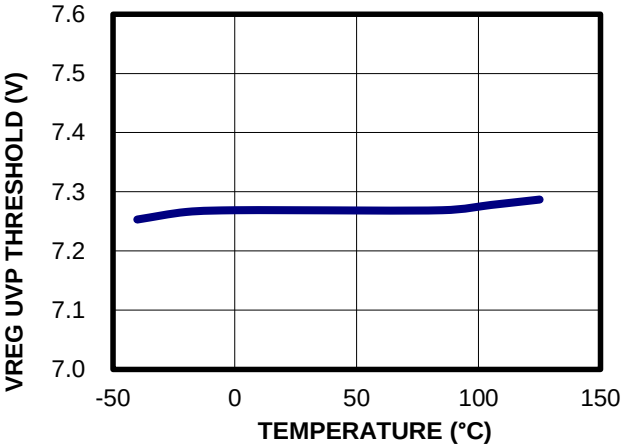
VREG Voltage vs. Temperature



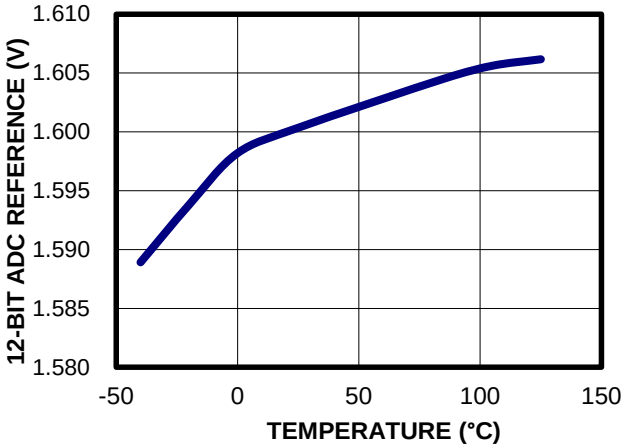
VREG On Threshold vs. Temperature



VREG UVP Threshold vs. Temperature



12-Bit ADC Reference vs. Temperature



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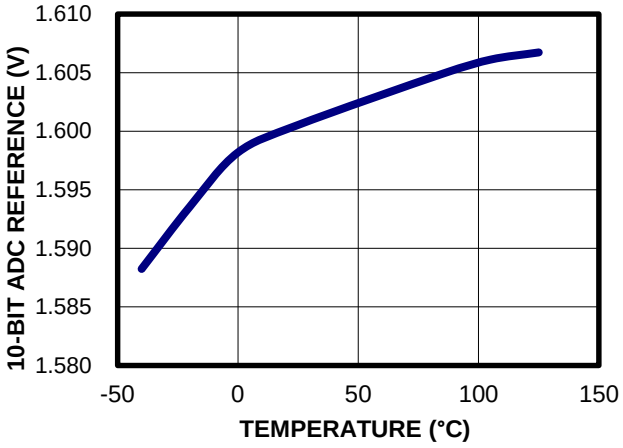
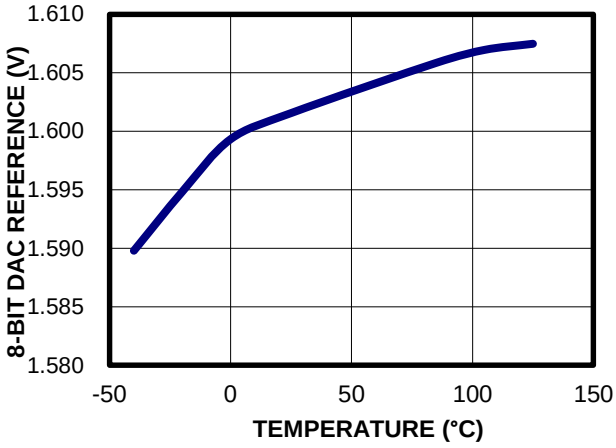
TYPICAL CHARACTERISTICS *(continued)*

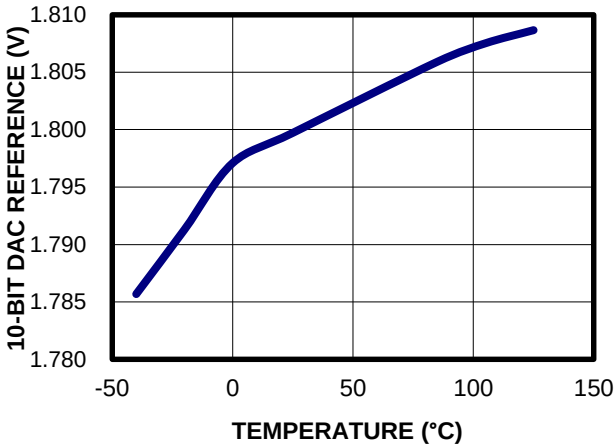
10-Bit ADC Reference vs. Temperature



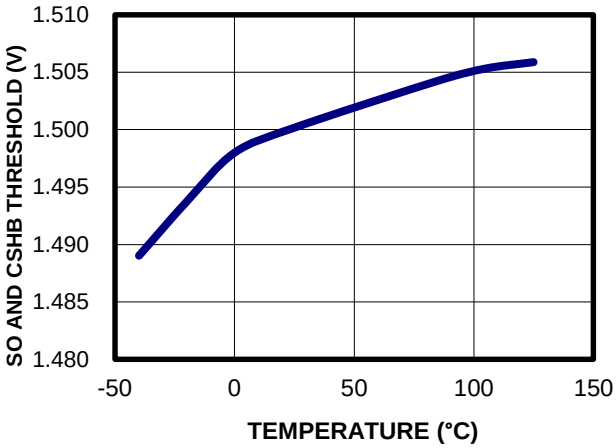
8-Bit DAC Reference vs. Temperature



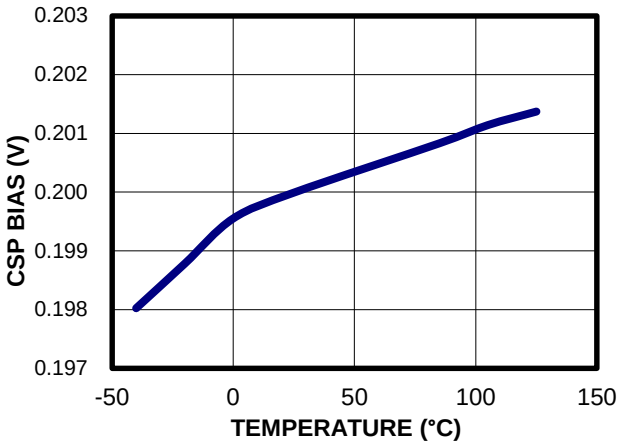
10-Bit DAC Reference vs. Temperature



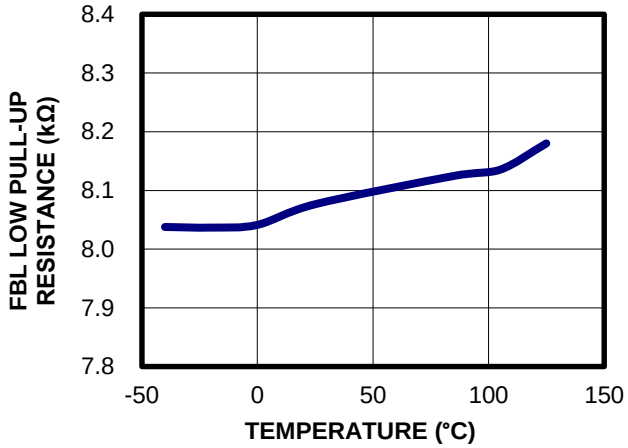
SO and CSHB Threshold vs. Temperature



CSP Bias vs. Temperature



FBL Low Pull-Up Resistance vs. Temperature



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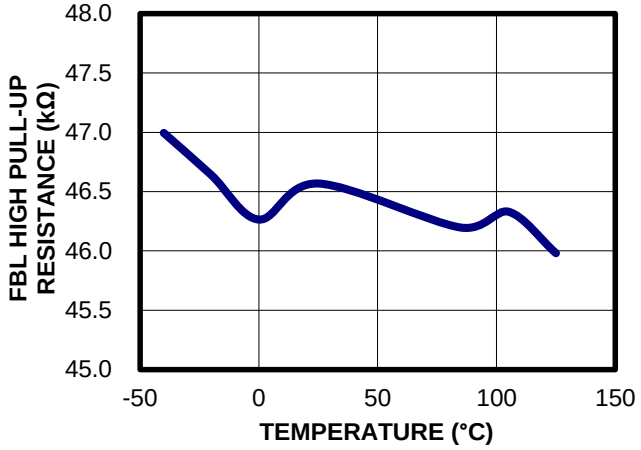
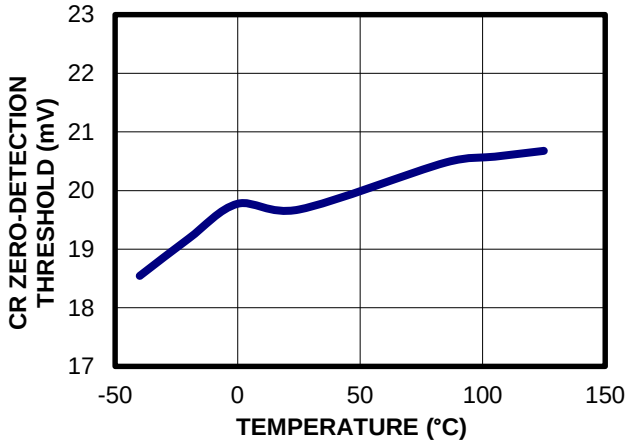
TYPICAL CHARACTERISTICS *(continued)*

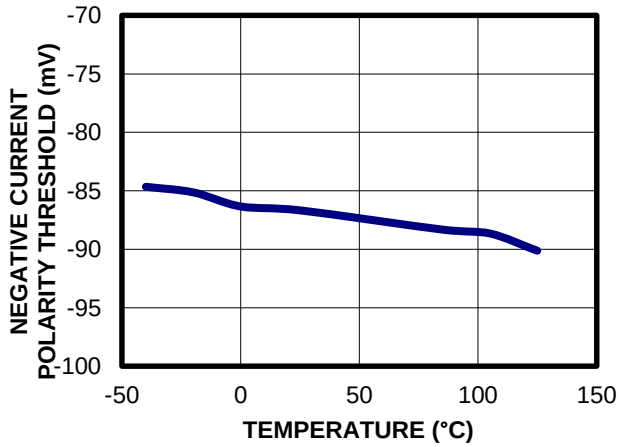
FBL High Pull-Up Resistance vs. Temperature



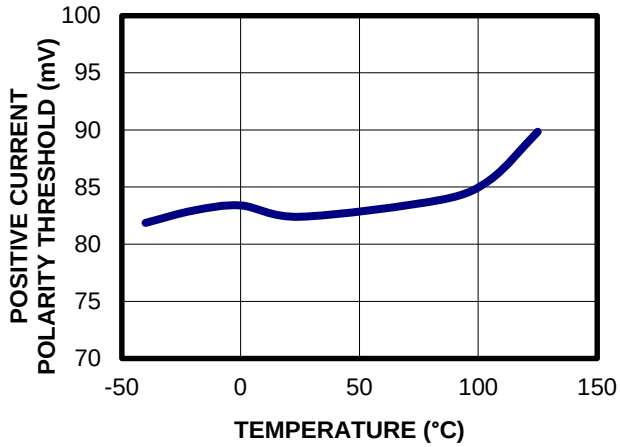
CR Zero-Detection Threshold vs. Temperature



Negative Current Polarity Threshold vs. Temperature



Positive Current Polarity Threshold vs. Temperature



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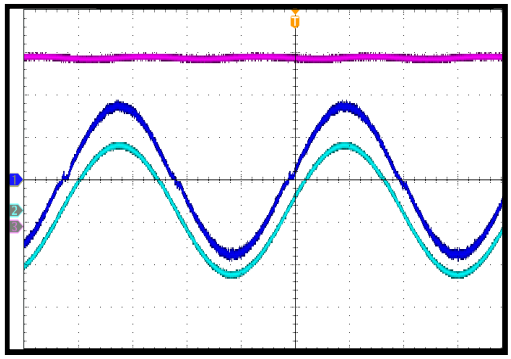
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 85V_{AC} to 265V_{AC}, V_{OUT} = 12V, I_{OUT} = 20A, T_A = 25°C, unless otherwise noted.

Steady State at Input

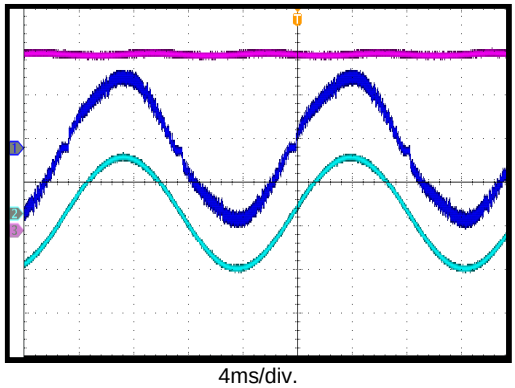
V_{IN} = 110V_{AC} at P_{OUT} = 240W



4ms/div.

Steady State at Input

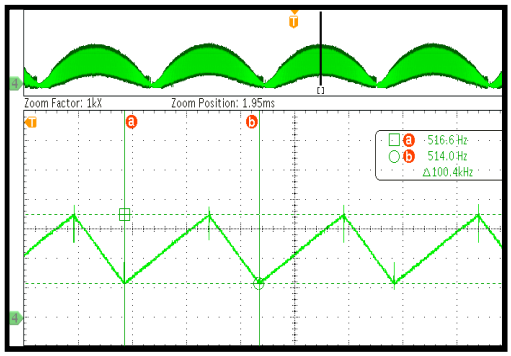
V_{IN} = 230V_{AC} at P_{OUT} = 240W



4ms/div.

Steady State at PFC Choke

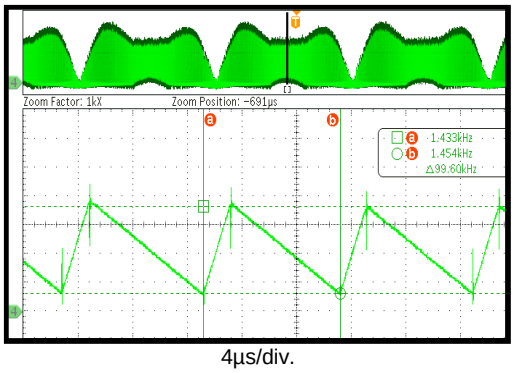
V_{IN} = 110V_{AC} at P_{OUT} = 240W



4µs/div.

Steady State at PFC Choke

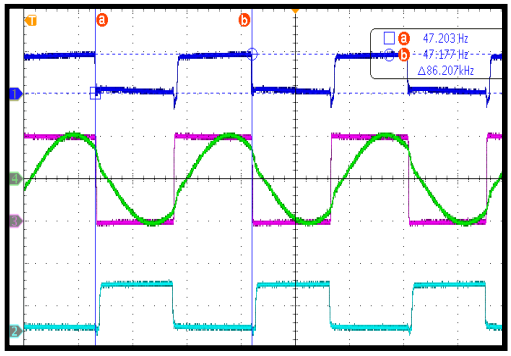
V_{IN} = 230V_{AC} at P_{OUT} = 240W



4µs/div.

Steady State at LLC

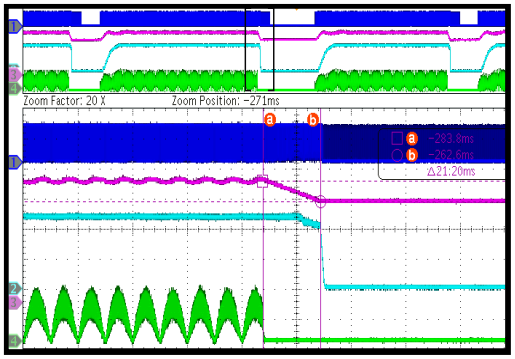
P_{OUT} = 240W



4µs/div.

Input Start-Up/Shutdown at PFC

V_{IN} = 110V_{AC}, P_{OUT} = 240W



20ms/div.

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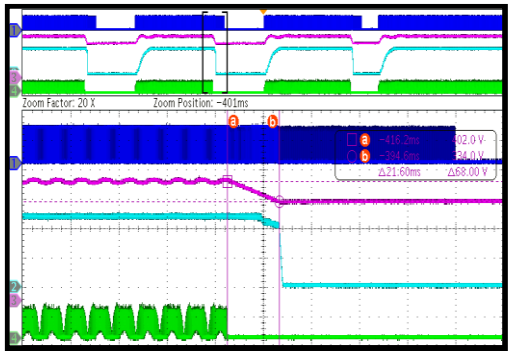
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 85V_{AC} to 265V_{AC}, V_{OUT} = 12V, I_{OUT} = 20A, T_A = 25°C, unless otherwise noted.

Input Start-Up/Shutdown at PFC

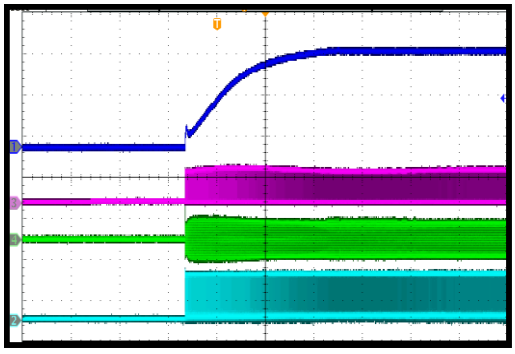
V_{IN} = 230V_{AC}, P_{OUT} = 240W



2ms/div.

Input Start-Up at LLC

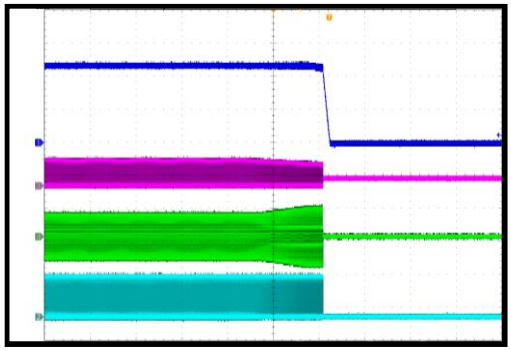
P_{OUT} = 240W



40ms/div.

Input Shutdown at LLC

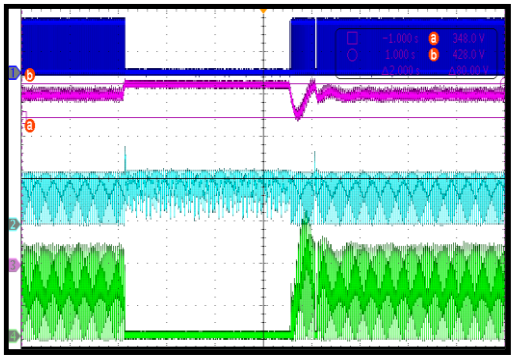
P_{OUT} = 240W



10ms/div.

Load Dynamic at PFC

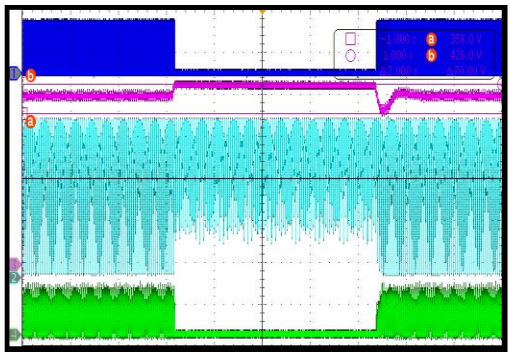
V_{IN} = 85V_{AC}, P_{OUT} = 0W to 240W, 1A/µs



200ms/div.

Load Dynamic at PFC

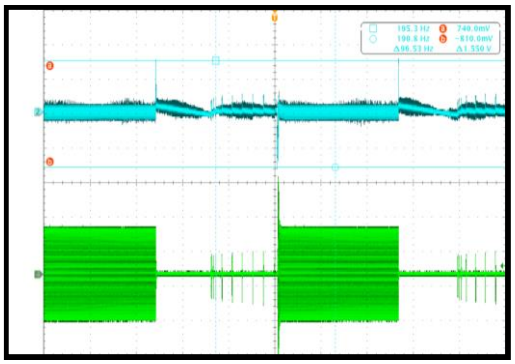
V_{IN} = 265V_{AC}, P_{OUT} = 0W to 240W, 1A/µs



200ms/div.

Load Dynamic at LLC

P_{OUT} = 0W to 240W, 6A/µs



4ms/div.

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FUNCTIONAL BLOCK DIAGRAM

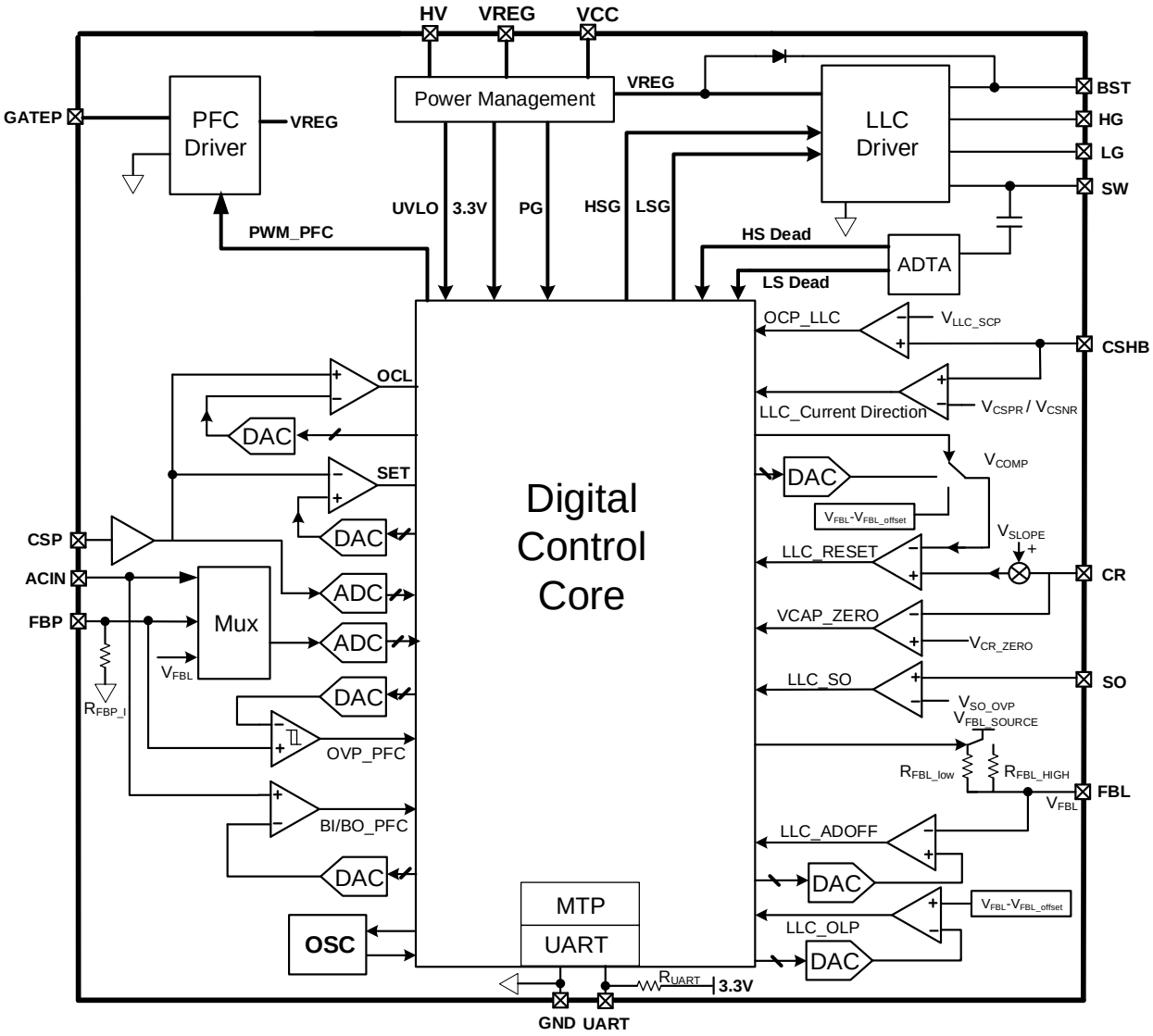

Figure 4: Functional Block Diagram

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OPERATION

The HR1213 is a high-performance combo controller that integrates a digital PFC and a digital half-bridge (HB) LLC controller.

MTP and UART Communication

The HR1213 implements a multiple-time programmable (MTP) memory as the non-volatile memory (NVM) for user data storage. The MTP memory is 128bitsx16bits, which can store a maximum 256 bytes of data. The MTP can be erased and rewritten 1,000 times.

When the digital core and MTP are on, the HR1213 automatically loads all of the data from MTP to the corresponding random access memory (RAM) to configure the IC's parameters. User data is also written to the MTP through the RAM.

The HR1213 provides a standard UART interface for communication. Communication is accomplished with a dedicated graphic user interface (GUI) (see Figure 5).

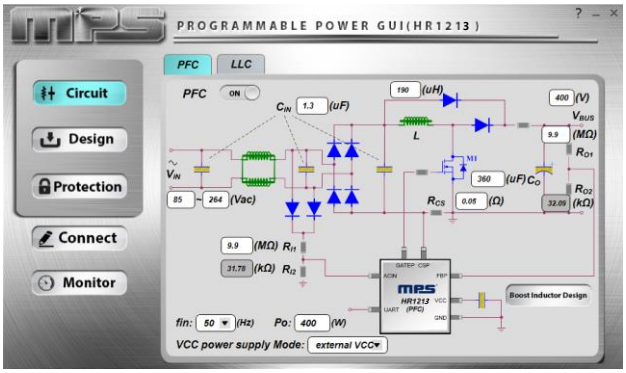

Figure 5: HR1213 GUI

The HR1213 can protect the MTP data from accidental reading and rewriting with a password. Once a non-zero, 16-bit password is written to the password register (address 01h), the MTP enters read-write protection. No data can be read or written until the user inputs the correct password into the specific unlock register (address 7Dh). This unlocks the read-write protection status.

Power Supply Management

Power supply management is implemented by the HV, VCC, and VREG pins. Figure 6 show the IC's power supply block diagram.

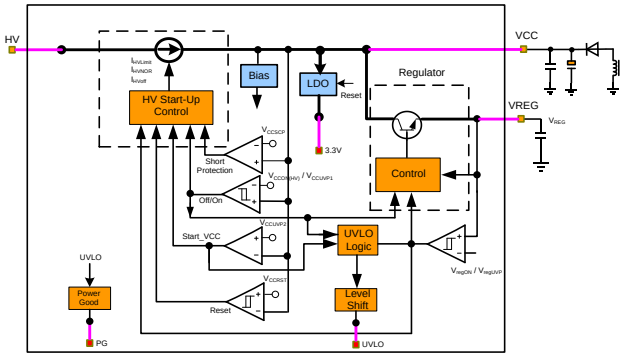

Figure 6: Power Supply Block Diagram

VCC Supply Mode

The HR1213 supports two VCC supply modes. The first is self-supply mode, in which VCC is powered by the HV current source supply at start-up, then auxiliary winding during normal operation. The second is external supply mode, in which VCC is powered by DC source. The VCC supply mode determines how the IC behaves, and can be configured via the GUI.

Start-Up with Self-Supply Mode

For self-supply mode, an internal, high-voltage current source charges VCC when a voltage input is applied to HV.

In normal operation, the voltage on VCC (V_{CC}) rises to V_{CCSCP}, then the HV current switches to the nominal current (I_{HVNOR}). The HV current source switches off when V_{CC} reaches the start-up level ($V_{CCON(HV)}$). Once the HV current source turns off, the leakage current going into HV should be below I_{HVOFF}.

The HV current source turns on again when V_{CC} drops below the under-voltage protection (UVP) level.

If V_{CC} drops below V_{CCSCP}, the charge current from HV is limited to $I_{HVLIMIT}$. This prevents excessive power dissipation caused by a V_{CC} short-circuit condition during start-up.

Figure 7 on page 20 shows the operating waveforms of self-supply mode.

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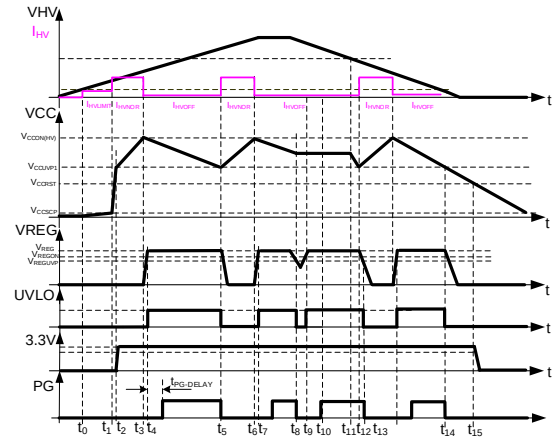

Figure 7: Self-Supply Mode Operation Waveform

Start-Up with External Supply Mode

For external supply mode, the DC source should exceed $V_{3V3ENABLE}$. When V_{CC} rises up to $V_{3V3ENABLE}$, the 3.3V power supply for the digital circuit rises. After this, the VREG voltage rises. Then the device turns on and starts operating after a brown-in condition.

Figure 8 shows the operating waveforms for external supply mode.

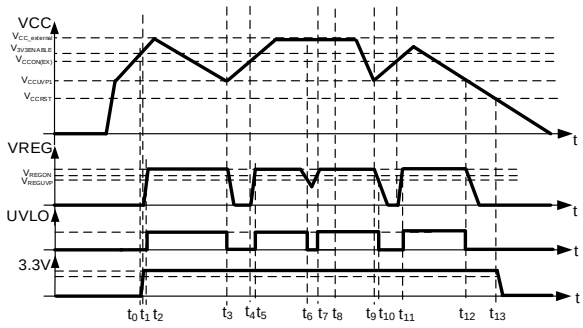

Figure 8: Operation Waveform of External Supply Mode

IC Supply Input (VCC)

VCC provides power to all of the internal circuits, including VREG and the V3.3 internal supply.

VCC can be powered either by the half-bridge (HB) transformer's auxiliary winding or by an external power supply.

If V_{CC} drops below the under-voltage protection (UVP) level, the following process occurs:

1. The IC stops operating, and the PFC driver stops switching immediately. The HB LLC continues to operate until the low-side MOSFET (LS-FET) turns on.
2. The VREG LDO is disabled.

There are two VCC UVP thresholds. If the LLC does not start switching in self-supply mode, the UVP level goes to V_{CCUVP2}. If the LLC starts switching in self-supply mode, the UVP level goes to V_{CCUVP1}. In external supply mode, the UVP levels is fixed to V_{CCUVP1}.

If the IC enters latch-off mode, the device remains latched until V_{CC} falls below V_{CCRST}.

Regulated Output (VREG Pin)

An internal LDO is adopted to stabilize the VREG pin so that VREG can achieve the following:

- Power the internal PFC driver
- Power the internal low-side driver of the HB LLC
- Charge the bootstrap capacitor, which powers the internal high-side driver of the HB LLC
- Be used as a voltage reference for external circuits

In self-supply mode, when V_{CC} reaches $V_{CCON(HV)}$, the internal LDO is enabled to charge the VREG capacitor. After VREG is completely charged, the IC starts operating if there is no fault. The LDO is enabled only when V_{CC} exceeds $V_{CCON(HV)}$. This ensures that any optional external circuitry connected to VREG does not dissipate additional current before the IC starts up.

During start-up in external supply mode, the internal LDO charges the VREG capacitor after the 3.3V power supply is charged. In normal operation, the internal LDO is enabled to charge the VREG capacitor only when V_{CC} exceeds $V_{CCON(EX)}$.

Once the voltage on the VREG pin (V_{REG}) exceeds V_{REGON}, the HR1213 starts working. If V_{REG} falls below V_{REGUVP}, the IC stops, and the PFC controller stops switching immediately. The HB LLC controller continues operating until the low-side gate becomes active.

V3.3 for Digital Logic

V3.3 is an internal, stabilized 3.3V power supply for digital circuits. It is derived from VCC via an internal LDO. When V_{CC} exceeds $V_{3V3ENABLE}$, the V3.3 LDO is enabled. It is disabled only when V_{CC} falls below V_{CCRST}.

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V3.3 is also the input for an internal 1.8V LDO, which is the power supply for the digital core.

Internal Under-Voltage Lockout (UVLO) Signal

Under-voltage lockout (UVLO) is an internal enable signal for both the PFC and LLC digital controllers. When V_{CC} exceeds V_{CCUVP1}, and V_{REG} exceed V_{REGON}, the UVLO signal goes high. The UVLO signal is pulled low if V_{REG} falls below V_{REGUVP}.

SYSTEM FUNCTIONS

Thermal Shutdown (TSD)

If the internal thermal sensor detects that the IC temperature has exceeded the thermal shutdown (TSD) threshold, the IC stops switching immediately. In thermal shutdown mode, the high-voltage current source is disabled so that VCC is not charged, and the internal LDOs for VREG and V3.3 are disabled. If the IC temperature drops below the thermal shutdown recovery threshold and V_{CC} drops below V_{CCRST}, the IC can start up again once V_{CC} is charged above $V_{CCON(HV)}$.

IC Enable/Disable Control

The IC (PFC and LLC operation) can be enabled and disabled by configuring the MTP via the GUI.

Digital PFC Controller

The state-of-the-art continuous conduction mode (CCM) and discontinuous conduction mode (DCM) control scheme reduces the RMS current drawn from the AC mains by ensuring good input current shaping during both CCM and DCM. The control scheme reduces the switching frequency when the load is decreased, which achieves higher efficiency and higher power factors under light-load conditions.

Timing Sequence of the Digital PFC

Figure 9 shows the digital PFC block timing sequence, described below.

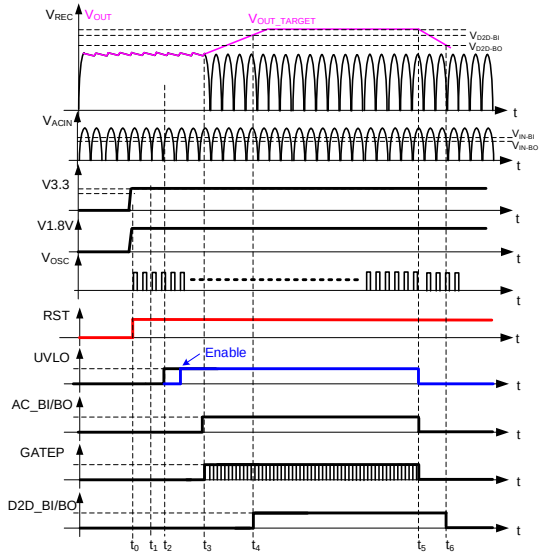

Figure 9: Digital PFC Block Power Supply Timing Sequence

Internal Power Supply Timing Sequence

Once V_{CC} exceeds $V_{3V3ENABLE}$, the V3.3 LDO is enabled and an internal LDO downstream produces a stable 1.8V power supply for the internal digital core and system clocks. Once both 3.3V and 1.8V are stable, the RST signal goes high. When the UVLO signal is high, the IC enables the oscillator (OSC), analog-to-digital converter (ADC), digital-to-analog converter (DAC), and the relative comparators. The enable signal goes high after a 20µs delay, which indicates that the digital core is ready to begin operation.

Digital Core Timing

When both the RST signal and enable signal (UVLO) are high, the digital system monitors the PG signal within a 150µs detection time window, which determines whether PFC and LLC start switching with a soft start. If no PG signal is detected, a switching soft start is applied. Otherwise, no soft start is applied for PFC and LLC switching.

After this PG detection time window, the digital system starts operating. First, the ADC starts sampling V_{ACIN} and V_{FBP}. If the AC brown-in condition is met and there is no open-loop fault on the FBP pin, then the AC brown-in/out signal goes high, and PFC starts switching until the output reaches the preset value. The LLC starts switching when the PFC output voltage ramps up to the LLC brown-in threshold.

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Oscillator

The system clock frequency for PFC is f_{OSC1_NOR}, and the system clock frequency for LLC is f_{OSC2_NOR}. When the system is in ultra-low power mode (both the PFC and LLC are burst off), the PFC and LLC clock frequencies drop to f_{OSC_NOPWM}. The PWM clock frequency falls to f_{OSC2_NOR} to reduce IC power consumption.

ADC Sampling

The HR1213 has two independent ADCs that sample the AC input voltage, PFC output voltage, LLC feedback voltage, and PFC switching peak current. The digital PFC controller obtains the PFC inductor peak current information on CSP via a 12-bit ADC.

A 3-channel, high-speed analog switch is used to switch between the AC input, V_{OUT} (PFC), and FB (LLC) signals for the other 10 bits of ADC sampling.

Figure 10 shows the ADC module block diagram.

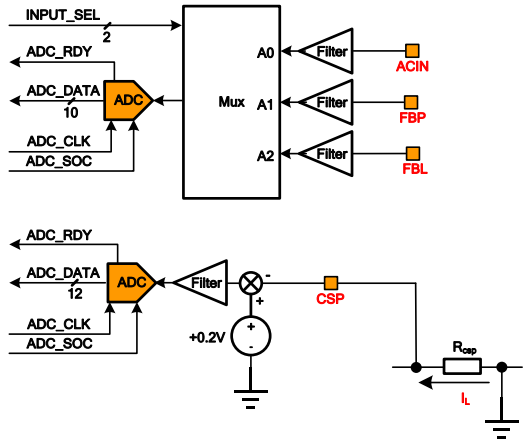

Figure 10: ADC Block Diagram

Figure 11 shows the sampling sequence of the 10-bit ADC. The ADC samples ACIN, FBL, and FBP with a fixed frequency, which can be adjusted by setting the idle time in the GUI.

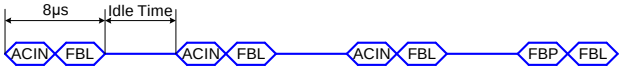

Figure 11: ADC Sampling Sequence

The LLC feedback voltage (on the FBL pin) is sampled during every sampling period. The AC input voltage (on the ACIN pin) is sampled three times in every four sampling periods. The PFC output voltage (on the FBP pin) is sampled once in every four sampling periods.

Input Voltage Sensing

V_{IN} is rectified and attenuated by a resistor divider with a fixed ratio (0.0032) before being provided to the ACIN input. Then the ADC samples the voltage on ACIN to get the instantaneous value, peak value, and the frequency of V_{IN}. This data is used to calculate the on time, monitor for AC brown-in and brownout protection, and determine the input capacitor current compensation.

Figure 10 shows the V_{IN} level that is defined for different functions. All parameters can be configured via the GUI.

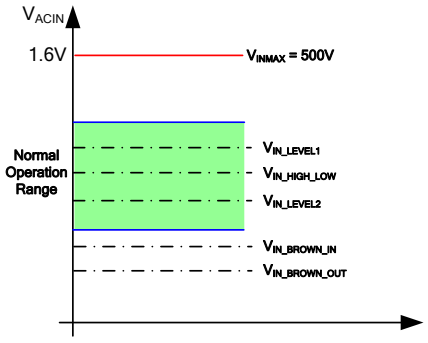

Figure 12: Input Voltage Level for Different Functions

Input Brown-In/Brownout

When the peak voltage on ACIN exceeds the brown-in threshold (V_{IN-BI}) and lasts for the brown-in time set by BI_Timer, the PFC starts switching. If the V_{ACIN} peak is below the brownout threshold (V_{IN-BO}) for the brownout time set by BO_Timer, the PFC stops switching. Figure 13 shows the operating waveforms.

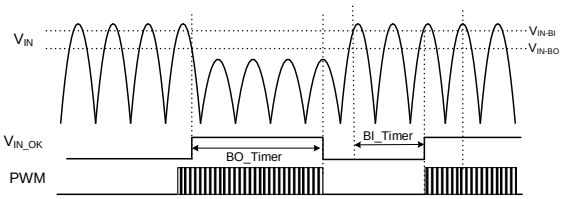

Figure 13: AC Brown-In and Brownout Control

High/Low Line

The system defines the input as the low-line condition when V_{IN} is below $V_{IN_HIGH/LOW}$. The high-line input condition is defined as when V_{IN} exceeds $V_{IN_HIGH/LOW}$ plus a hysteresis. Both the soft-start time and resonant time for PFC valley turn-on are implemented independently

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according to the high- or low-line input condition. The PFC output voltage and over-voltage protection (OVP) can also be regulated at different levels according to this high- or low-line input condition to optimize the PFC stage efficiency.

There are another two configurable thresholds for V_{IN}: V_{IN_LEVEL1} and V_{IN_LEVEL2}. Together with $V_{IN_HIGH/LOW}$, they divide V_{IN} into four ranges. The input capacitor current compensation values can be set to different values at different V_{IN} ranges to improve the power factor.

These three thresholds are comprised of 8 bits of data in the MTP, and can be configured via the GUI.

Output Voltage Sensing

Similar to V_{IN} sensing, V_{OUT} is also sampled through a resistor divider with a fixed ratio (0.0032) on FBP. The voltage on FBP is sampled by the 10-bit ADC, and the results are used for on-time calculation and several protection functions.

The internal pull-down resistor (about 3.3MΩ) should be considered when designing the external resistor divider. Calculate the total divider ratio (which should be about 0.0032) with Equation (1):

$$\frac{R_{FBP_L} // 3.3M\Omega}{R_{FBP_H} + R_{FBP_L} // 3.3M\Omega} = 0.0032 \quad (1)$$

Where R_{FBP_H} is the external resistor divider connected on the high side, and R_{FBP_L} is the external divider resistor connect on the low side.

Figure 14 shows the V_{OUT} level that is defined for different functions.

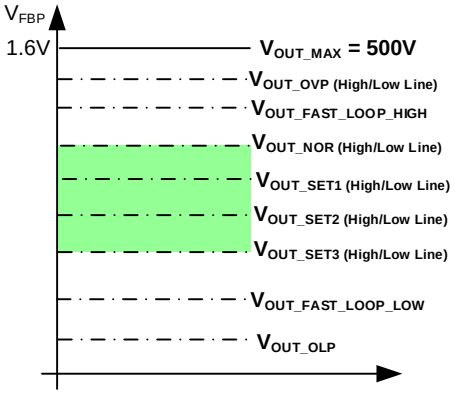

Figure 14: Output Voltage Level for Different Functions

Output Regulation

To optimize efficiency, V_{OUT} can be auto-regulated according to V_{IN} and the output power. V_{OUT} is set to two different options based on $V_{IN_HIGHLOW}$, and four different options according to the power levels. There are a total of eight different options for PFC output regulation. These options can be selected through the GUI.

Output Over-Voltage Protection (OVP)

The over-voltage protection (OVP) trigger threshold (V_{OUT_OVP}) is set in the MTP register via the GUI. The digital value is converted to an analog signal by a digital-to-analog converter (DAC). This value is compared to the FBP pin voltage. If V_{OUT} exceeds V_{OUT_OVP}, PFC switching stops. If V_{OUT} returns to the regulated target, the PFC resumes switching. Figure 15 shows the internal OVP block.

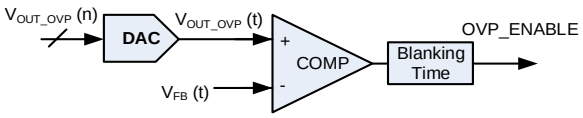

Figure 15: PFC OVP Circuit

A blanking time is also inserted into OVP. This keeps the IC immune to switching noise interference (see Figure 16) This blanking time can be configured by the GUI.

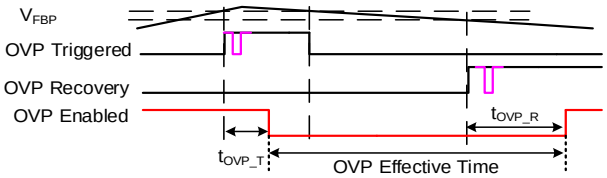

Figure 16: Output OVP

Fast Loop

In a dynamic load event, the PFC output voltage may drop or rise significantly due to the low bandwidth of the PFC control loop. This can lead to V_{OUT} exceeding or falling below its specification. A fast loop can be enabled to improve PFC dynamic performance. The fast loop is activated when V_{OUT} drops below $V_{OUT_FAST_LOOP_LOW}$ (if the fast loop low-level is enabled) or exceeds $V_{OUT_FAST_LOOP_HIGH}$ (if the fast loop high level is enabled). When fast loop is activated, K_I and K_P switch to the fast loop settings. The fast loop function can be enabled/disabled (and its parameters can be set) via the GUI.

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Open-Loop Protection (OLP)

An open-loop condition is defined as when the FBP voltage drops below V_{OUT_OLP} for longer than a configurable timer. The IC enters auto-retry or latch-off mode (selectable via the GUI) if this occurs.

If IC is in latch-off protection mode, switching latches off. The device can only restart once V_{CC} drops below V_{CCRST} then is charged above $V_{CCON(HV)}$.

If the IC is in auto-retry protection mode, the switching is suspended for an auto-restart timer that can be set via the GUI. The device restarts after the timer runs out. If the device is set to self-power mode in the GUI (which means the device uses auxiliary winding to power VCC), the IC must still wait for V_{CC} be charged above $V_{CCON(HV)}$ to restart.

Peak Current Sensing

The PFC inductor current is sensed by the CSP resistor (R_{CSP}), and produces a negative voltage (V_{CSP}). This value is internally converted into a positive voltage with a bias (V_{CS_S}) (see Figure 17 and Figure 18). The ADC samples V_{CS_S} when the PFC gate turns off. V_{CS_S} can be calculated with Equation (2):

$$V_{CS_S}(t) = V_{BIAS_CSP} - V_{CSP}(t) \quad (2)$$

Figure 17 shows the current-sense circuit on the CSP pin.

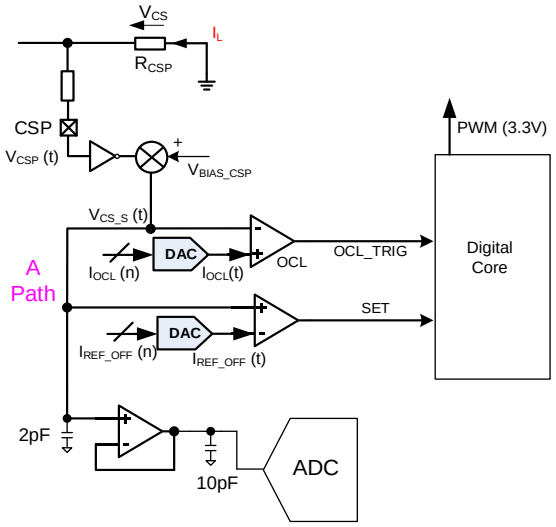

Figure 17: CSP Pin Current-Sense Circuit

Figure 18 shows the V_{CS_S} waveforms.

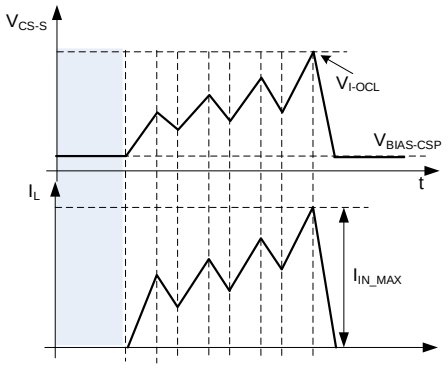

Figure 18: V_{CS_S} Voltage Waveforms

Over-Current Limit (OCL)

The HR1213 adopts cycle-by-cycle over-current limiting (OCL) to prevent the PFC MOSFET from overstress. OCL is implemented by comparing V_{CS_S} to the internal OCL threshold. The OCL threshold is an analog signal output from an 8-bit DAC. The internal OCL threshold can be calculated similarly to Equation (2). A leading edge blanking time (LEB1) is inserted to avoid switching noise. The OCL threshold is adjustable in the GUI.

Digital PFC Control Scheme

Figure 19 shows the digital control flowchart.

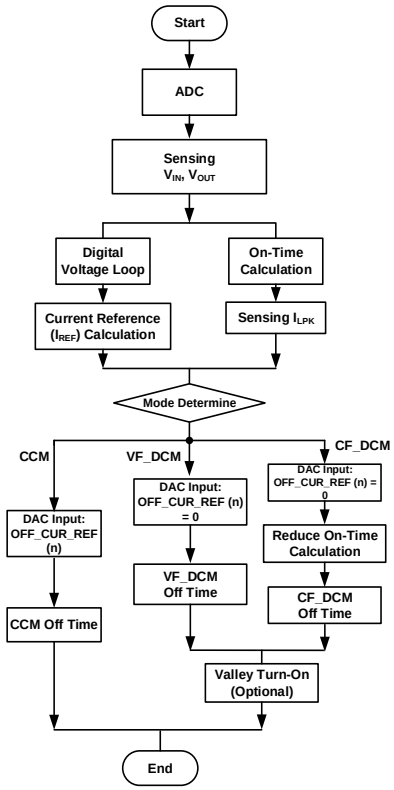

Figure 19: PFC Control Scheme Flowchart

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Digital Current Reference

The HR1213 adopts a digital PI that compensates for the voltage control loop. Its output (V_{COMP} (n)) is sent to the multiplier for the current reference calculation (see Figure 20).

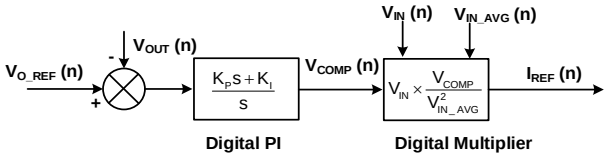

Figure 20: Current Reference

The digital current reference (I_{REF}) can be calculated with Equation (3):

$$I_{REF}(n) = V_{IN}(n) \times \frac{V_{COMP}(n)}{(0.5 \times V_{IN_PK}(n))^2} \quad (3)$$

On-Time Calculation

The on time can be estimated with Equation (4):

$$t_{ON}(n) = \frac{V_{O_REF} - V_{IN}(n)}{V_{O_REF}} \times t_S \quad (4)$$

Where t_S is the switching period that can be configured via the GUI.

PFC Operating Mode Selection

The HR1213 has three operation modes for the PFC: continuous conduction mode (CCM), variable frequency discontinuous conduction mode (VF-DCM), and constant frequency discontinuous conduction mode (CF-DCM). The peak inductor current value in CCM (I_{PK}) can be estimated with Equation (5):

$$I_{PK}(n) < 2 \times I_{REF}(n) \quad (5)$$

The peak inductor current value in VF-DCM can be calculated with Equation (6):

$$2 \times I_{REF}(n) < I_{PK}(n) < 2 \times I_{REF}(n) \times \frac{t_{S_MAX}}{t_S} \quad (6)$$

Where t_{S_MAX} is the maximum switching period set via the GUI. The peak inductor current value in CF-DCM can be estimated with Equation (7):

$$I_{PK}(n) > 2 \times I_{REF}(n) \times \frac{t_{S_MAX}}{t_S} \quad (7)$$

Continuous Conduction Mode (CCM) Operation

Figure 21 shows the CCM control signals.

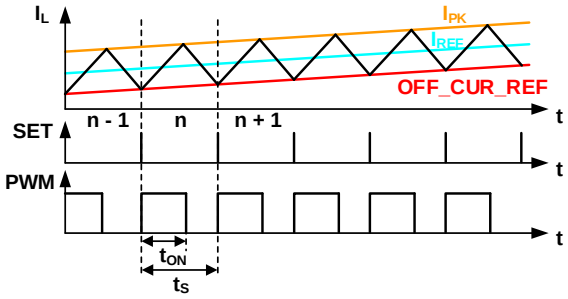

Figure 21: CCM Control Signals

When the converter operates in CCM, OFF_CUR_REF (n) is calculated and sent to the DAC. There is a digital filter with configurable cross-frequency for the OFF_CUR_REF (n) output. The DAC output has an analog signal (OFF_CUR_REF (t)) that is compared to V_{CS} (t). If V_{CS} (t) is below OFF_CUR_REF (t), the set signal is high, and the PWM is also set high (see Figure 21).

The off-current reference in CCM can be calculated with Equation (8):

$$OFF_CUR_REF(n) = 2 \times I_{REF}(n) - I_{PK}(n) \quad (8)$$

Variable Frequency Discontinuous Conduction Mode (VF-DCM) Operation

When the converter operates in VF-DCM, the off-current reference is set to zero. In this scenario, the set signal represents the DCM boundary (see Figure 22).

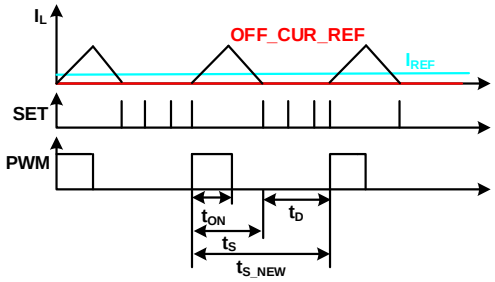

Figure 22: VF-DCM Control Signals

The new switching period can be estimated with Equation (9):

$$t_{S_NEW}(n) = \frac{I_{PK}(n)}{2 \times I_{REF}(n)} \times t_S \quad (9)$$

The delay time can be calculated with Equation (10):

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$$t_D(n) = t_{S_NEW}(n) - t_S = \left(\frac{I_{PK}(n)}{2 \times I_{REF}(n)} - 1\right) \times t_S \quad (10)$$

The calculated delay time has a digital filter with a configurable cross-frequency.

Constant Frequency Discontinuous Conduction Mode (CF-DCM) Operation

Figure 23 shows the CF-DCM control signals.

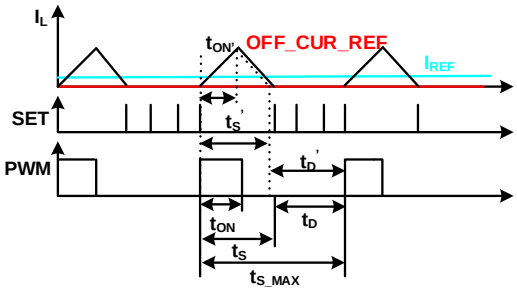

Figure 23: CF-DCM Control Signals

When the converter operates in CF_DCM, the off-current reference is also set to zero.

In this mode, the switching frequency is limited to the minimum switching frequency that can be set via the GUI. The PWM duty is modulated to achieve average current control. The new switching period can be calculated with Equation (11):

$$\frac{1}{2} \times I_{PK}'(n) \times t_S'(n) = I_{REF}(n) \times t_{S_MAX} \quad (11)$$

As t_{ON} changes, the peak inductor current value is relatively unchanged, and can be estimated with Equation (12):

$$I_{PK}'(t) = I_{PK}(t) \quad (12)$$

The switching period can be calculated with Equation (13):

$$t_S'(n) = \frac{2 \times I_{REF}(n)}{I_{PK}(n)} \times t_{S_MAX} \quad (13)$$

The new turn-on time can be estimated with Equation (14):

$$t_{ON}'(n) = \frac{V_{O_REF} - V_{IN}(n)}{V_{O_REF}} \times t_S'(n) \quad (14)$$

The delay time can be calculated with Equation (15):

$$t_D'(n) = t_{S_MAX} - t_S'(n) = \left(1 - \frac{2 \times I_{REF}(n)}{I_{PK}(n)}\right) \times t_{S_MAX} \quad (15)$$

The calculated delay time also has a digital filter with a configurable cross-frequency.

Soft-Start Procedure

Once the AC brown-in is triggered, the VIN_OK signal goes high and the HR1213 initiates a soft start (see Figure 24).

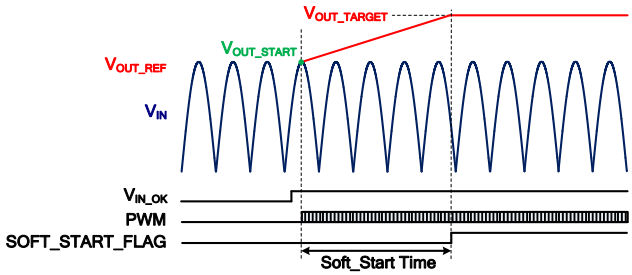

Figure 24: Soft-Start Sequence

During soft start, the internal voltage reference slowly ramps up to the regulation target. The ramp slew rate is determined by the soft-start time setting's high and low lines, which can be configured via the GUI. When the voltage reference on FBP reaches the regulation target value, SOFT_START_FLAG is set high and the soft-start sequence is complete. Generally, V_{OUT} cannot rise during soft start, so it is regulated afterward.

Note that the slew rate is different at the high line and low line.

Burst Mode

At light loads, the IC is always designed to run in burst mode for better efficiency and decreased no-load power consumption. Once the output load drops below the threshold (a percentage of the rated load), the PFC enters burst mode. The threshold can be configured via the GUI for both the high line and low line.

In burst mode, the switching duty is calculated based on the set threshold, and the output is regulated to V_{O_TARGET} with a typical 5V hysteresis. The PFC stops switching when V_{OUT} ramps up to V_{O_TARGET} + 5V, and resumes switching when V_{OUT} drops below V_{O_TARGET}.

Generally, the HR1213 is designed to exit burst mode only at the peak point of the AC line to minimize the current stress. Additionally, a threshold voltage can be selected via the GUI to

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prevent the bus voltage from dropping too low under transient. If the bus voltage drops below the threshold, the IC exits burst mode immediately without waiting for peak point detection.

Power Factor Compensation (PFC)

Traditional power factor compensation (PFC) control schemes only regulate the inductor current to match the value of V_{IN}. However, the input capacitor current is not controlled, which can cause power factor (PF) deterioration and a suboptimal phase delay. With a larger capacitor or a higher V_{IN}, the PF worsens, especially under light-load conditions.

To improve the PF, the HR1213 implements a patented method to compensate the input capacitor current. There are four V_{IN} ranges and input capacitors for the compensation setting, which can be configured via the GUI and stored in the MTP. With this function, the PF can be improved across the whole V_{IN} range.

Frequency Jittering

The HR1213 implements a jitter function that can reduce EMI noise. When jitter is enabled, the switching frequency (f_{SW}) is modulated by a triangular waveform with a modulation frequency (f_M). This frequency is modulated to the maximum value at the peak of the triangle, and to the minimum value at the valley of the triangle. Figure 25 shows the jitter switching frequency modulation. The modulation amplitude and f_M can both be configured via the GUI.

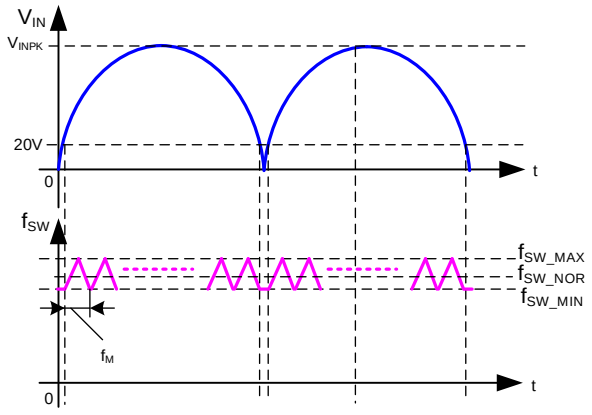

Figure 25: Jitter Switching Frequency Modulation

DIGITAL LLC CONTROLLER

LLC Brown-In/Brownout

The LLC starts to work when the bus voltage exceeds the brown-in threshold. The LLC shuts down when the bus voltage drops below the brownout threshold. There is a configurable timer delay set via the GUI for both brown-in and brownout LLC switching.

Soft-Start Operation

During LLC soft start, the internal V_{COMP} is overridden by a soft-start generator output voltage. The soft-start timer can be set via the GUI to define the soft-start duration.

At the beginning of soft start, the low-side gate (LSG) turns on first for a configurable time to charge the BST capacitor. Then the high-side gate (HSG) and LSG turn on and off alternately.

Because of the resonant capacitor (C_R) voltage imbalance during start-up, the current slew rate in the resonant tank is different between the HSG and LSG turn-on periods.

The HR1213's LSG driver does not turn off until the resonant tank current drops below zero ($V_{CSHB} < V_{CSNR}$) to avoid hard switching during soft start (see Figure 26).

If both the HSG and LSG are driven with a 50% duty cycle, the resonant tank current may not reverse in a switching half-cycle, which can lead to hard switching. Figure 26 shows the waveform difference between a 50% duty cycle and the HR1213's logic.

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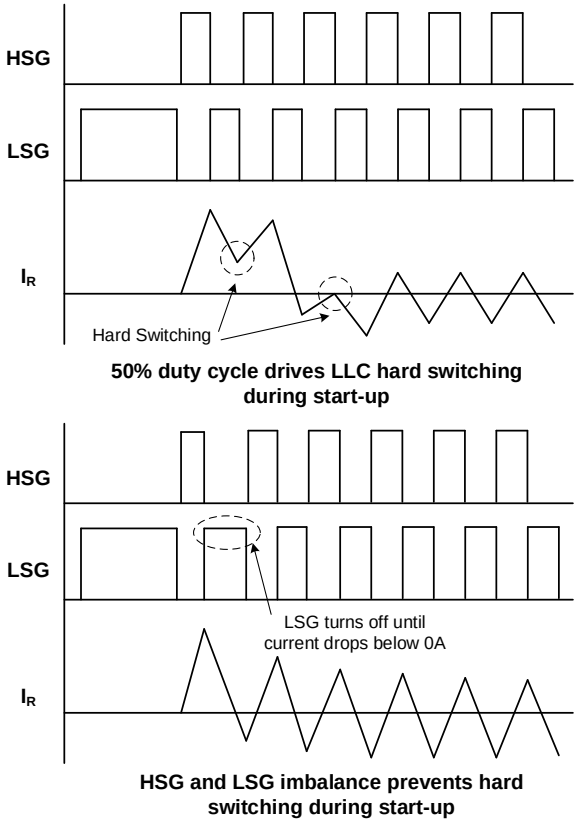

Figure 26: LLC Start-Up to Avoid Hard Switching

Current Mode Control

Figure 27 shows the control block diagram of the half-bridge (HB) LLC. The on-time comparator determines the HSG on time by comparing the voltage derived from the current sense (CR) with V_{COMP}. V_{COMP} is generated from the feedback voltage on an optocoupler (FBL).

The LSG follows the HSG on time. A digital counter with a minimum step (about 1 / f_{OSC1_NOR}) is implemented to ensure that the on time between the HSG and LSG matches.

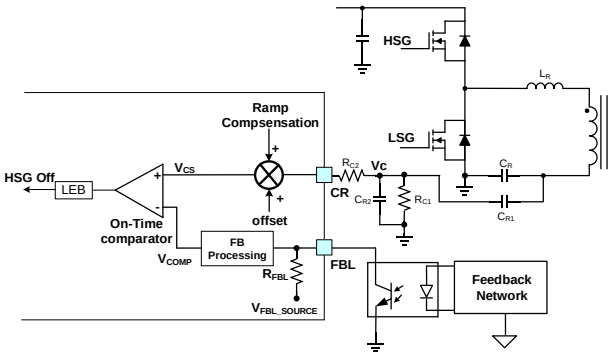

Figure 27: LLC Current Mode Control Block Diagram

Figure 28 shows the LLC current mode control waveform.

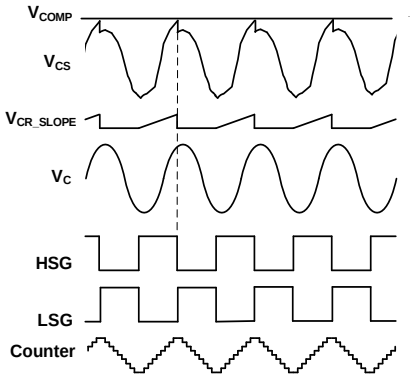

Figure 28: LLC Current Mode Control Waveform

The current-sense voltage (V_C) is proportional to the voltage on the resonant tank capacitor (C_R). The proportion is determined by the external capacitor divider (C_{R1} and C_{R2}). The capacitor dividing ratio should be set to ensure that the maximum output power (primary current) of the LLC stage can be delivered.

To prevent subharmonic oscillation, a digital, 4-bit, configurable slope compensation can be added. The compensation voltage (V_{CR_SLOPE}) is the product of the slope and on time. This value is added to the sensed voltage (V_C) to generate V_{CS}.

The HR1213 senses the voltage of the optocoupler on FBL that generated the reference (V_{COMP}) of the internal on-time comparator. The LSG follows the previous HSG on time, but the LSG does not turn off until V_{CS} drops below V_{COMP}. There is an internal pull-up resistor (R_{FBL}), and the FBL voltage increases when the output load increases. The sensed FBL voltage is also used for skip mode and burst mode operation detection, as well as over-power protection (OPP).

Operation Mode

The LLC can operate in three modes: continuous mode, skip mode, and burst mode. The controller samples the FBL pin voltage using the 10-bit ADC to determine which mode the LLC should operate in.

Figure 29 shows the LLC working mode based on the FBL voltage (V_{FBL}). When V_{FBL} reaches the skip mode entry threshold (V2), the LLC system enters skip mode. If V_{FBL} drops further

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(load decreases) below the burst mode entry threshold (V4), the LLC switch triggers burst off, then the LLC enters burst mode. Both the skip mode and burst mode thresholds have exit levels with a hysteresis (V3 and V5). If the LLC reaches these thresholds, it returns to continuous mode (if in skip mode) or skip mode (if in burst mode). All of the thresholds (V2, V3, V4, and V5) can be configured via the GUI.

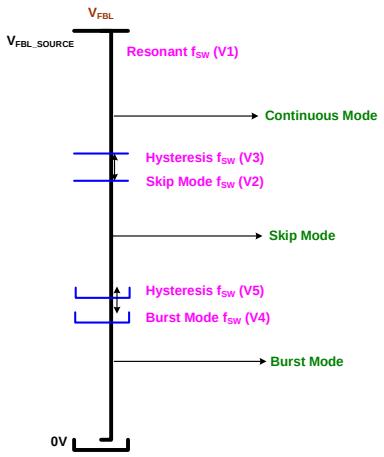

Figure 29: LLC Working Mode Determined by FBL

In skip mode and burst mode, V_{COMP} can be calculated with Equation (16):

$$V_{COMP} = A_X \times V_{FBL} + B_X \quad (16)$$

Where A_X is the proportional coefficient, and B_X is an offset for V_{COMP}. A_X and B_X can be set via the GUI. In continuous mode, V_{COMP} can be estimated with Equation (17):

$$V_{COMP} = V_{FBL} - V_{FBLOFFSET} \quad (17)$$

Figure 30 shows the V_{COMP} generation block diagram.

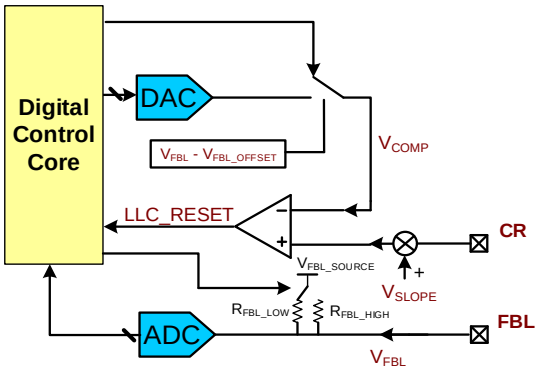

Figure 30: V_{COMP} Generation Block Diagram

Skip Mode

For HB LLC topology frequency control, the switching frequency rises as the load decreases. This means that the magnetization loss and switching loss increase under light-load conditions. To reduce power consumption while keeping the output under regulation, the HR1213 implements skip mode operation to greatly reduce the average switching frequency, as well as the magnetic loss.

When the system enters skip mode, a switch idle time is inserted between every N (configurable via the GUI) switching cycles. The skip period (t_{SKIP}) is kept at the configured value for stability. The first HSG after the idle time always turns on at the HB peak point (ZVS) to minimize the switching loss (see Figure 31).

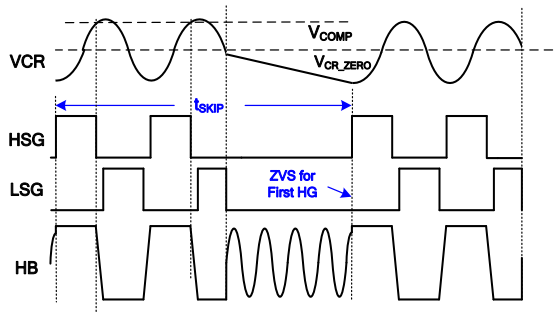

Figure 31: LLC Skip Mode Operation

The switching frequencies for HSG and LSG follow the current mode control scheme, except that the last LSG (during one skip cycle) on time ends when V_{CR} drops V_{CR_ZERO}.

Burst Mode

To further limit the average switching frequency as the load gets lighter, a longer switch idle time is inserted in skip mode. This is called burst mode operation (see Figure 32).

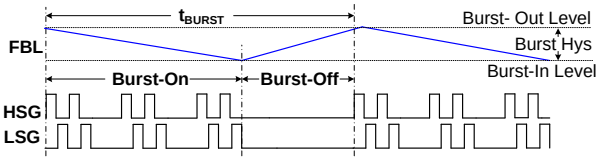

Figure 32: Burst Mode LLC Operation

During the burst on period, the LLC works in skip mode. During the burst off period, switching is completely off. When V_{FBL} rises high enough to trigger the configurable burst-out threshold, the burst off period ends and the LLC starts switching.

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To minimize the audible noise created during burst mode, users can select to activate the burst frequency control function via the GUI. This function allows users to limit the burst frequency to a low value. With this function activated, the burst frequency (1 / t_{BURST}) can be adjusted to a preset range by increasing or decreasing the switching pulses during the burst-on period.

The HR1213 has a switchable pull-up resistor on FBL to reduce the optocoupler current in deep burst mode. When the switching counts during one burst on period is less than the set value, which indicates that the load is light enough, the HR1213 gradually switches the FBL pull-up resistor from R_{FBL_LOW} to R_{FBL_HIGH}.

The HR1213 incorporates an ultra-low power mode. The device enters ultra-low power mode when both the PFC and LLC are in burst off mode. The device can also enter ultra-low power mode if the PFC is in burst off mode and FBL is below the ultra-low power mode entry threshold.

In ultra-low power mode, IC power consumption is further reduced by shutting down some of the internal circuits. This is implemented via an internal logic comparator that compares the FBL voltage with a configurable reference from the 8-bit DAC.

If the BST capacitor is deeply discharged during burst off mode in deep burst operation, the LSG turns on first for a configurable time ($t_{HSG-INI}$).

The burst-off time (t_{B-OFF}) can exceed the timer set via the GUI to charge the BST voltage.

Burst Frequency Control

The HR1213 incorporates burst frequency control to reduce the acoustic noise during burst mode. Generally, the acoustic noise is reduced when the burst frequency is low. Burst frequency control increases the switching counts in each burst cycle, so that the burst-off time becomes longer. This reduces the overall burst frequency.

If the burst frequency is below the set target, burst mode runs at the normal burst level. To increase the switching counts when the burst frequency exceeds the set target, the normal burst level is ignored until the actual switching count exceeds the internal calculation result, or V_{FBL} drops to the ultra-low power mode entry threshold.

If the device reaches the ultra-low power mode entry threshold, switching is terminated. This prevents V_{OUT} from overshooting under light to heavy load transients. However, this may lead to a higher burst frequency. Make the difference between the burst level and ultra-low power mode threshold as great as possible to increase the V_{FBL} range in burst mode.

Figure 33 shows burst frequency control waveforms.

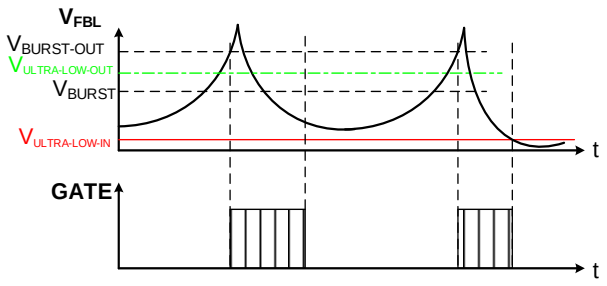

Figure 33: Burst Frequency Control Waveforms

Adaptive Dead Time Adjustment (ADTA)

A dead time between the HSG and LSG drivers is required in half-bridge (HB) topologies to prevent cross-conduction through the power stage MOSFETs. This prevents excessive current, high EMI noise, and damage in applications. A traditional, fixed dead time control scheme is widely used in resonant converters due to its simple implementation. However, this method may lead to hard switching under light loads, or under conditions with a larger-value magnetizing inductance (L_M), which eventually lead to thermal and reliability issues.

The HR1213 incorporates an intelligent adaptive dead time adjustment (ADTA) logic circuit that is capable of detecting the dV/dt of SW through an internal high-voltage capacitor. It automatically inserts a proper dead time with respect to the converter's actual operating conditions. Figure 34 on page 31 shows the simplified ADTA block diagram.

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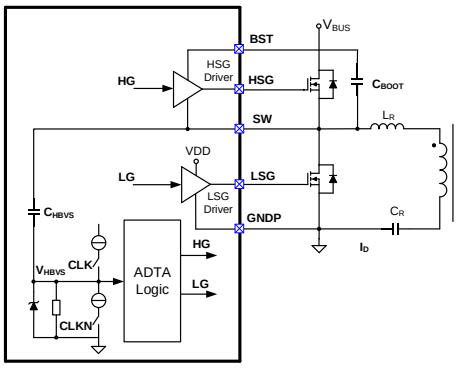

Figure 34: ADTA Block Diagram

Figure 35 shows the ADTA operation waveform.

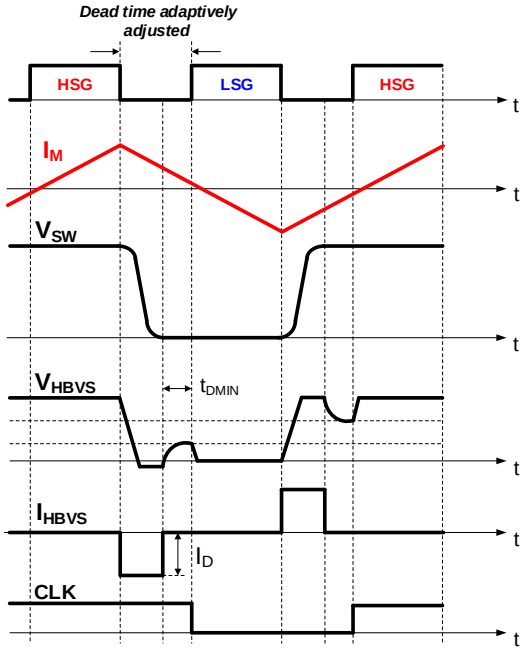

Figure 35: ADTA Operation Waveform

Once the HSG switches off, SW swings from a high voltage to a low voltage because it is driven by the resonant tank current (I_R). A negative dV/dt draws a current from C_{HBVS}, which pulls V_{HBVS} down. If the current exceeds the internal bias current, V_{HBVS} is pulled down to 0V and clamped. When the SW slew rate becomes slower, the current decreases and V_{HBVS} starts to ramp up. This change in V_{HBVS} is used for dead time detection, so that the LSG switches on after a delay.

The dead time is defined as the time between the HSG switching off and the LSG switching on, which relies on the completion of SW's transition.

When the LSG switches off, SW swings from zero to high, creating an input current from C_{HBVS}. The dead time also adjusts automatically with the opposite logic.

Figure 36 shows the possible dead time via ADTA logic. Note that there are three possible dead times: a minimum dead time (t_{DMIN}), maximum dead time (t_{DMAX}), and an adaptive dead time, which is between t_{DMIN} and t_{DMAX}. When the SW transition time is shorter than t_{DMIN}, the next HSG or LSG does not turn until the dead time reaches t_{DMIN}. This prevents shoot-through between the high-side and low-side MOSFETs. If the dead time is too long, it may lead to duty cycle loss and the loss of soft switching. When the SW transition time is too long, it may lead to a long dead time; a maximum dead time (t_{DMAX}) is set to force the gate to switch on under this condition. Both t_{DMIN} and t_{DMAX} can be configured via the GUI.

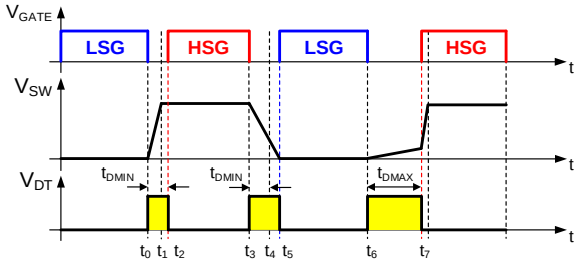

Figure 36: Minimum, Maximum, and Adaptive Dead Time

Capacitive Mode Protection (CMP)

Under fault conditions such as an overload or short circuit (or any load transient condition), the LLC converter may run in capacitive mode. In capacitive mode, the voltage applied on the resonant tank lags behind the current, which makes the MOSFETs lose zero-voltage switching (ZVS) capability. It can also damage the device, so it is recommended to avoid using this mode.

Figure 37 on page 32 shows the principles of capacitive mode protection (CMP). CSPOS and CSNEG are the current polarity flags, which are generated by comparing the voltage on the CSHB pin with the internal V_{CSPR} and V_{CSNR} thresholds.

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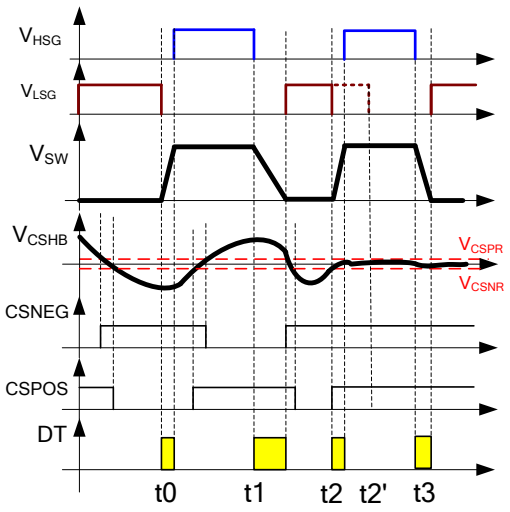

Figure 37: Operating Principle of CMP

At t0, the converter operates in inductive mode. V_{CSNR} exceeds V_{CSHB} when the LSG driver is turned off, which indicates that current is flowing at the right polarity (negative). Capacitive mode protection is not triggered.

At t1, the converter operates in inductive mode. V_{CSHB} > V_{CSPR} when the HSG driver turns off, which also indicates that current is flowing at the right polarity (positive). Capacitive mode protection is not triggered.

At t2, the LLC converter works in capacitive mode, and V_{CSHB} reaches V_{CSNR}. The LSG is forced off in order to avoid capacitive mode operation. If CMP is not enabled, the LSG does not turn off until t2.

If V_{CSHB} never exceeds V_{CSPR} while the HSG is on, the CMP function is not activated when the HSG turns off. If V_{CSHB} never drops below V_{CSNR} while the LSG is on, the CMP function is not activated when the LSG turns off.

Over-Current Protection (OCP)

The HR1213 provides over-current protection (OCP) when V_{CSHB} reaches V_{CS_OCP}. An internal counter begins each time V_{CS_OCP} is triggered, and OCP is triggered if the counter reaches its set value (configured via the GUI). OCP is typically triggered when the CSHB pin voltage continues to rise during a short circuit (see Figure 38).

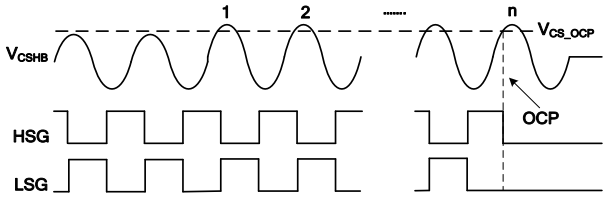

Figure 38: OCP Timing Sequence

The IC can be set for latch-off or auto-retry mode if LLC OCP occurs. The GUI can be used to select the protection mode.

For details on the latch-off and auto-retry protection modes, see the Open-Loop Protection (OLP) section on page 24.

Over-Power Protection (OPP)

Over-power protection (OPP) protects the LLC converter from excessive over-power conditions.

If V_{FBL} exceeds V_{OPP_LLC} (configurable via the GUI), an internal configurable timer turns on. This timer is reset once V_{FBL} falls below V_{OPP_LLC}. OPP is triggered if the timer counts to the end without resetting. V_{OPP_LLC} should not exceed the minimum value of V_{FBL_SOURCE}.

OPP can activate latch-off mode or auto-retry mode. This parameter is configured via the GUI.

For details on the latch-off and auto-retry protection modes, see the Open-Loop Protection (OLP) section on page 24.

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APPLICATION INFORMATION

Current Sensing on CSHB

Both CMP and OCP detect the current signal on CSHB, so a proper current-sense circuit should be designed on CSHB.

There are two kinds of current-sense circuits: lossless current sensing from a small capacitor parallel with the resonant capacitor, and sensing the resonant tank current directly with a series sensing resistor. Lossless current sensing is typically recommended for most applications (see Figure 39)

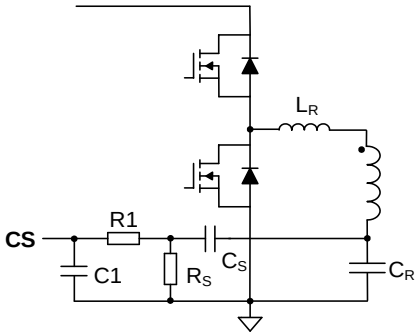

Figure 39: Lossless Current-Sensing Network

To design the lossless current-sensing network, follow the equations listed below.

C_S can be calculated with Equation (18):

$$C_S \le \frac{C_R}{100} \quad (18)$$

To avoid mistriggering the capacitive detection threshold for V_{CSPR} (or V_{CSNR}) during normal light-load operation, R_S should fulfill the following conditions, estimated with Equation (19):

$$R_S > \frac{V_{CSPR}}{I_M} \times (1 + \frac{C_R}{C_S}) \quad (19)$$

Where I_M is the peak magnetizing current, calculated with Equation (20):

$$I_M = \frac{V_{BUS}}{8 \times L_M \times f_{MAX}} \quad (20)$$

Where V_{BUS} is the LLC input voltage, L_M is the transformer winding inductance, and f_{MAX} is the maximum switching frequency.

R_S should also meet the following condition, estimated with Equation (21):

$$R_S < \frac{V_{CS_OCP}}{I_{CR_PK}} \times (1 + \frac{C_R}{C_S}) \quad (21)$$

Where I_{CR_PK} is the peak current of the resonant tank under low input voltages and full loads. I_{CR_PK} can be calculated with Equation (22):

$$I_{CR_PK} = \sqrt{\left(\frac{N \times V_{OUT}}{4 \times L_M \times f_{SW}}\right)^2 + \left(\frac{I_{OUT} \times \pi}{2 \times N}\right)^2} \quad (22)$$

Where N is the turn ratio of the transformer, I_{OUT} is the output current, V_{OUT} is the output voltage, f_{SW} is the switching frequency, and L_M is the magnetizing inductance.

The R1 and C1 network attenuates the switching noise on the CSHB pin.

The current-sense resistor circuit uses a current-sense resistor placed in series with the resonant tank (see Figure 40). This method is simpler with fewer external components, but it can cause suboptimal power consumption on the current-sense resistor.

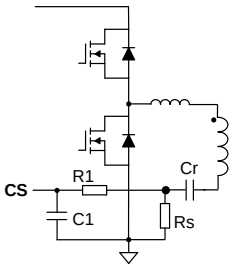

Figure 40: Current Sensing with a Sense Resistor

The current-sense resistor value can be calculated with Equation (23):

$$R_S < \frac{V_{CS_OCP}}{I_{CR_PK}} \quad (23)$$

High-Side Gate Driver (HSG)

Figure 41 on page 34 shows the high-side gate driver.

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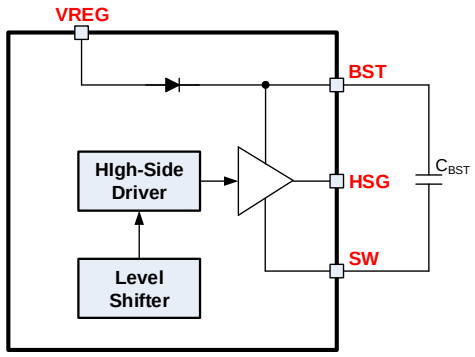

Figure 41: High-Side Gate Driver

An external bootstrap (BST) capacitor is required to provide energy for the high-side gate driver. An integrated bootstrap diode charges this capacitor through VREG. This diode simplifies the external driving circuit for the high side MOSFET, and allows the BST capacitor to be charged when the low side MOSFET is on.

Consider the BST capacitor charging time. To provide enough gate driver energy, a BST capacitor between 100nF and 470nF is recommended.

External Protection on the SO Pin

The HR1213 monitors the voltage on the SO pin and provides a protection function when the SO pin voltage (V_{SO}) exceeds V_{SO_PRO} for a configurable timer (t_{OVP_STABLE}).

The SO pin can be connected to the primary auxiliary winding by a resistor divider to sense the output voltage, which is used for over voltage protection (OVP). V_{SO} be calculated with Equation (24):

$$V_{SO} = \frac{R_{SO1}}{R_{SO1}+R_{SO2}} \times \frac{N_{PAU}}{N_S} \times (V_{OUT}+V_F) \quad (24)$$

Where N_{PAU} is the turns of auxiliary winding, N_S is the turns of secondary winding, V_{OUT} is the output voltage, and V_F is forward voltage drop of output rectifier or SR. R_{SO1} and R_{SO2} comprise the voltage divider for sampling.

The secondary-side OVP with an optocoupler is more simple and accurate. When the optocoupler turns on, V_{SO} should be high enough to trigger a protection. In this scenario, calculate V_{SO} with Equation (25):

$$V_{SO} = \frac{R_{SO1}}{R_{SO1}+R_{SO2}} \times (V_{REG}-V_{OPTO}) \quad (25)$$

An external NTC can also be used on this pin for an external thermal shutdown (TSD) function. Pull the SO pin up to a constant voltage source (e.g. VREG) with an NTC resistor. Then V_{SO} can be calculated with Equation (26):

$$V_{SO} = \frac{R_{SO}}{R_{NTC}+R_{SO}} \times V_{REG} \quad (26)$$

Where R_{SO} is the external pull-down resistor connected from the SO pin to GND, and V_{REG} is the VREG pin voltage.

Figure 42 shows how to use the SO pin for OVP or external TSD.

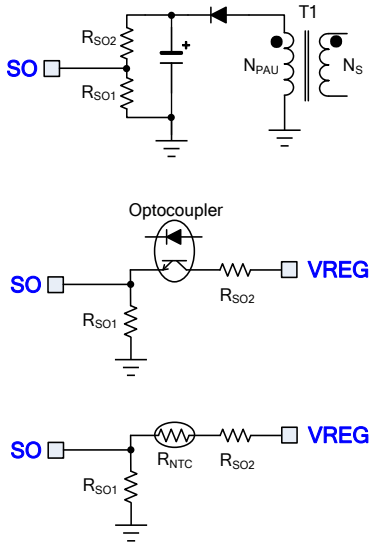

Figure 42: SO Application Circuit for OVP and External TSD

Protecting CSP from Negative Voltage Stress

The HR1213's PFC current-sense resistor is in the input power loop to sense the full waveform of the PFC inductor. This means that the current from the input bridge to the output capacitor flows through the sense resistor. Generally, there is inrush current during start-up and a surge current during a surge condition. Therefore, there can be a large voltage drop on the current-sense resistor that leads to an over-voltage condition on the CSP pin.

The CSP pin's internal ESD device is capable of clamping in the event of over-voltage stress, though only for a short time. For more details on the current limit of the CSP pin's internal ESD device under different over-voltage conditions, see the Absolute Maximum Ratings section on

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page 8. It is recommended to connect a 500Ω resistor between the current-sense resistor and the CSP pin.

If clamping on the current-sense resistor is required, connect two diodes in series, and place them in parallel with the current-sense resistor (see Figure 43). The voltage is clamped by diodes when the current-sense resistor voltage drop exceeds the forward voltage drop of the two diodes. These two diodes should be carefully chosen so that the forward voltage drop is high enough under a small forward current and high temperatures. Do not use a Schottky diode. The over-current limit (OCL) setting voltage should not exceed the diode clamping voltage.

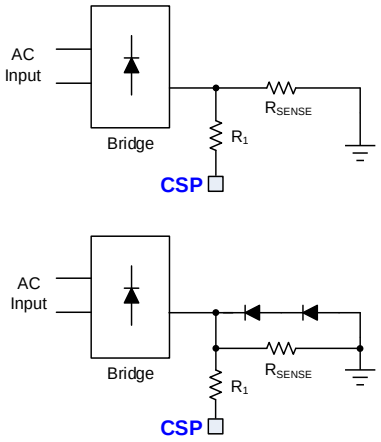

Figure 43: CSP Pin Protection from Overstress

VCC Supply On/Off Control

A special circuit must be implemented to control the VCC supply in external supply mode. (see Figure 44 below and Figure 3 on page 4). The primary side of the photocoupler is controlled by Q1 and the VCC on/off signal. The secondary side is connected in series with the voltage regulator. When Q2 is on, the series voltage regulator starts to work and supply power to VCC. When VCC supplied by an external power supply, short UART to GND.

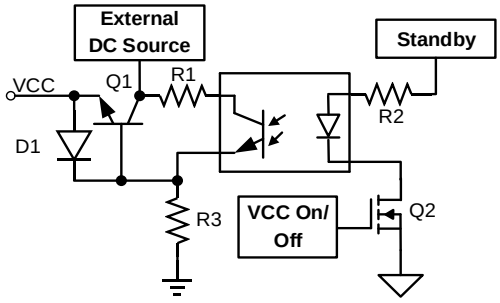

Figure 44: VCC Supply On/Off Control

PCB Layout Guidelines

For the best results, refer to Figure 45 and follow the guidelines below:

1. Use the bulk capacitor's negative terminal as the ground for the PFC, LLC power loop, and the IC's ground. Ensure that the ground layout overlap is as small as possible.
2. Make the IC ground trace short and wide to reduce its voltage drop.
3. Keep all the areas of the power loop and signal loop as small as possible.
4. Keep the signal traces far away from the switching point.
5. CSP and CSHB are key signals that should be treated with the highest priority.

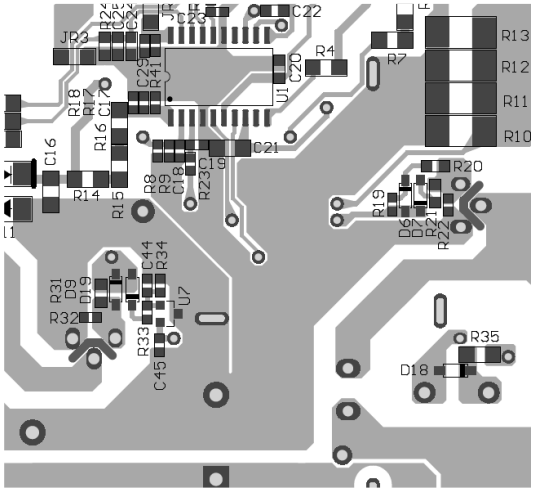

Figure 45: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS

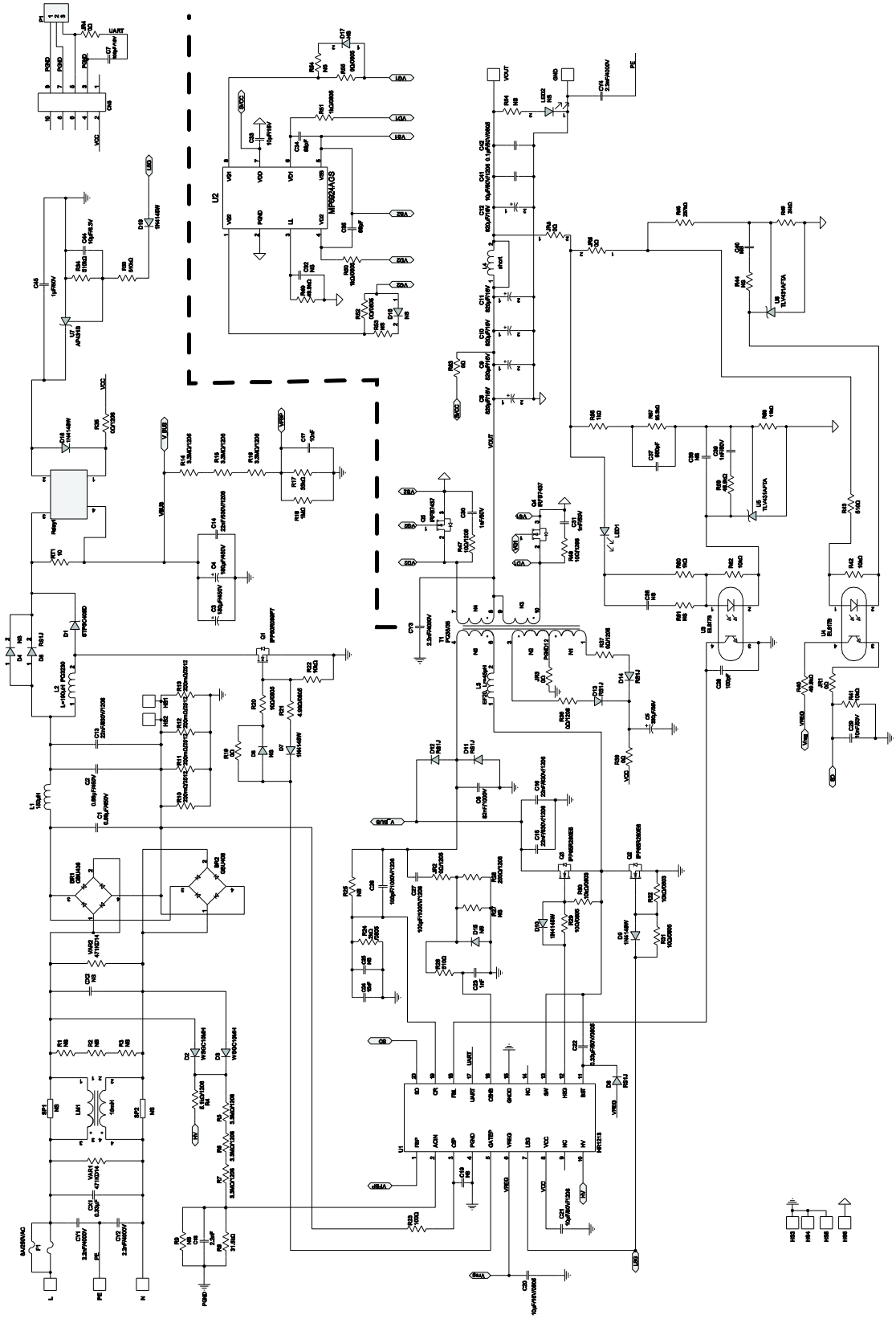

Figure 46: 90V_{AC} to 265 V_{AC} Input and 12V/34A Output Application

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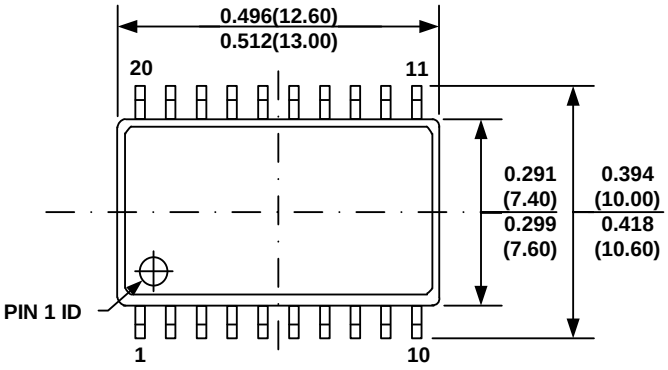
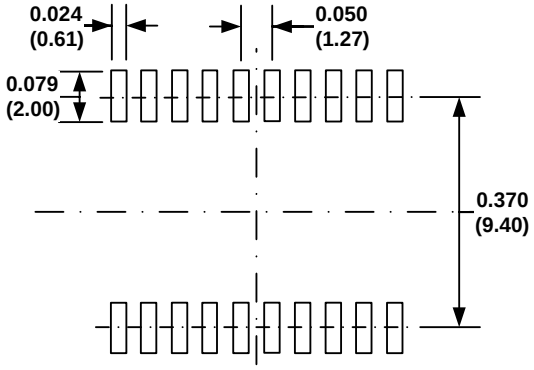
SOIC-20



TOP VIEW



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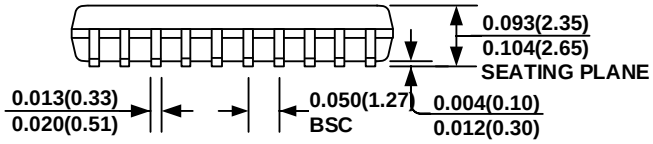

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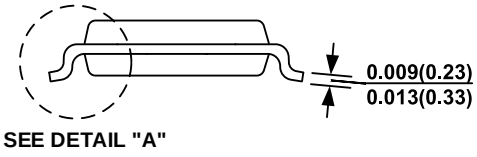
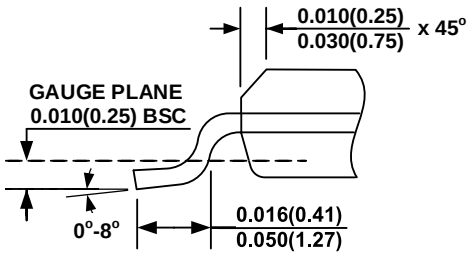


SIDE VIEW



DETAIL "A"

NOTES:

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3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
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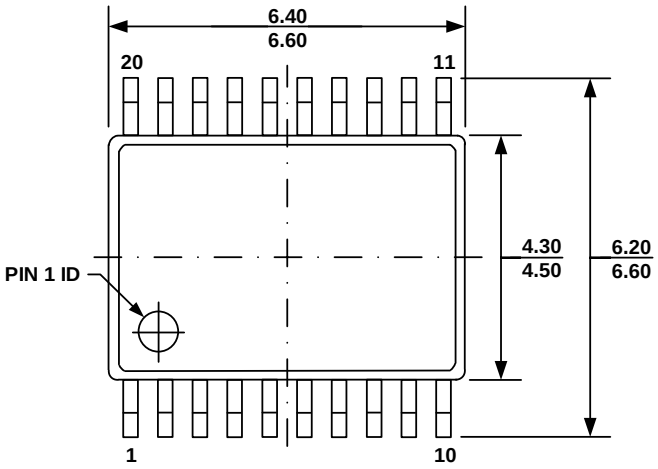
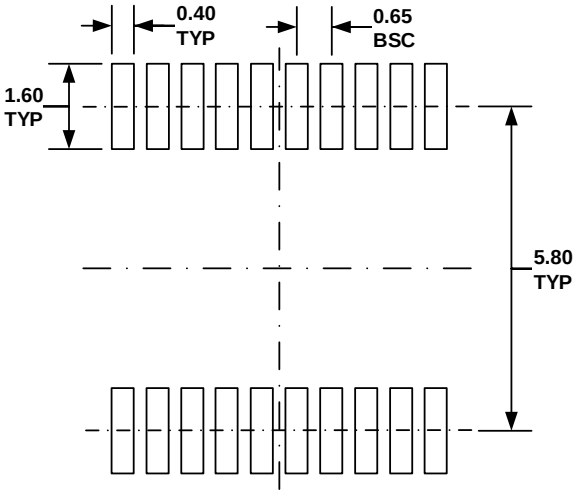


TOP VIEW



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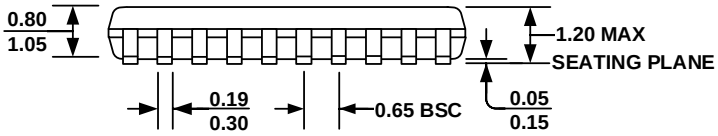
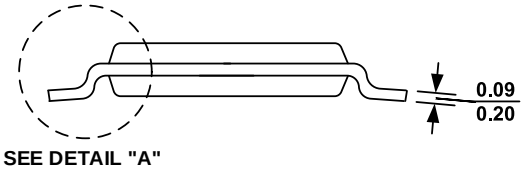
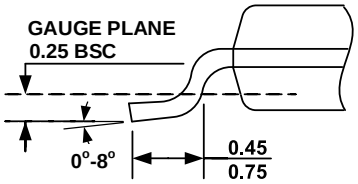


FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTES:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
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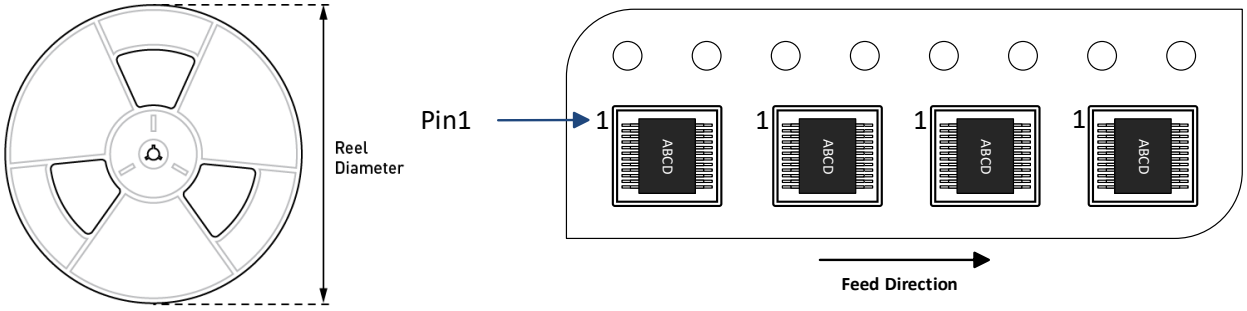

Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
HR1213GY-xxxx-Z	SOIC-20 (wide body)	1000	37	N/A	13in	24mm	12mm
HR1213GM-xxxx-Z	TSSOP-20	2500	75	N/A	13in	16mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	10/18/2021	Initial Release	-

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