HR1001C

Enhanced LLC Controller with Adaptive Dead-Time Control, Capacitive Mode Protection and Enhanced Surge Protection

The Future of Analog IC Technology

DESCRIPTION

The HR1001C is an enhanced LLC controller that provides adaptive dead-time adjustment (ADTA) and capacitive mode protection (CMP) features, as well as functional improvements on surge performance.

ADTA inserts a dead time between the two complimentary gate outputs automatically. This is ensured by keeping the outputs off while sensing the dV/dt current of the half-bridge switching node. ADTA features easier design, lower EMI, and higher efficiency.

The HR1001C incorporates anti-capacitive mode protection, which prevents potentially destructive capacitive mode switching if the output is shorted or has a severe overload. This feature protects the MOSFET during abnormal conditions, making the converter robust.

The HR1001C has a programmable oscillator that sets both the maximum and minimum switching frequencies. It starts up at a programmed maximum switching frequency and decays until the control loop takes over to prevent excessive inrush current.

The HR1001C enters a controlled burst mode at light load to minimize power consumption and tighten the output regulation.

Full protection features include two-level over-current protection (OCP) with external latch shutdown, auto-recovery, brown-in and brown-out, capacitive mode protection (CMP), and over-temperature protection (OTP), improving converter design safety with minimal extra components.

FEATURES

- Over-Current Protection (OCP) with Programmable Delay for Enhanced Surge Performance
- Adaptive Dead-Time Adjustment (ADTA)
- Capacitive Mode Protection (CMP)
- 50% Duty Cycle, Variable Frequency Control for Resonant Half-Bridge Converter
- 600V High-Side Gate Driver with Integrated Bootstrap Diode with a High-Accuracy Oscillator of High dV/dt Immunity
- Operates up to 600kHz
- Two-Level Over-Current Protection (OCP): Frequency Shift and Latched Shutdown with Programmable Duration Time
- Latched Disable Input for Easy Protection
- Remote On/Off Control and Brown-Out Protection through BO
- Programmable Burst Mode Operation at Light Load
- Non-Linear Soft Start for Monotonic Output Voltage Rise
- Available in a SOIC-16 Package

APPLICATIONS

- LCD and PDP TVs
- Desktop PCs and Servers
- Telecom SMPS
- AC/DC Adapter, Open-Frame SMPS
- Video Game Consoles
- Electronic Lighting Ballasts

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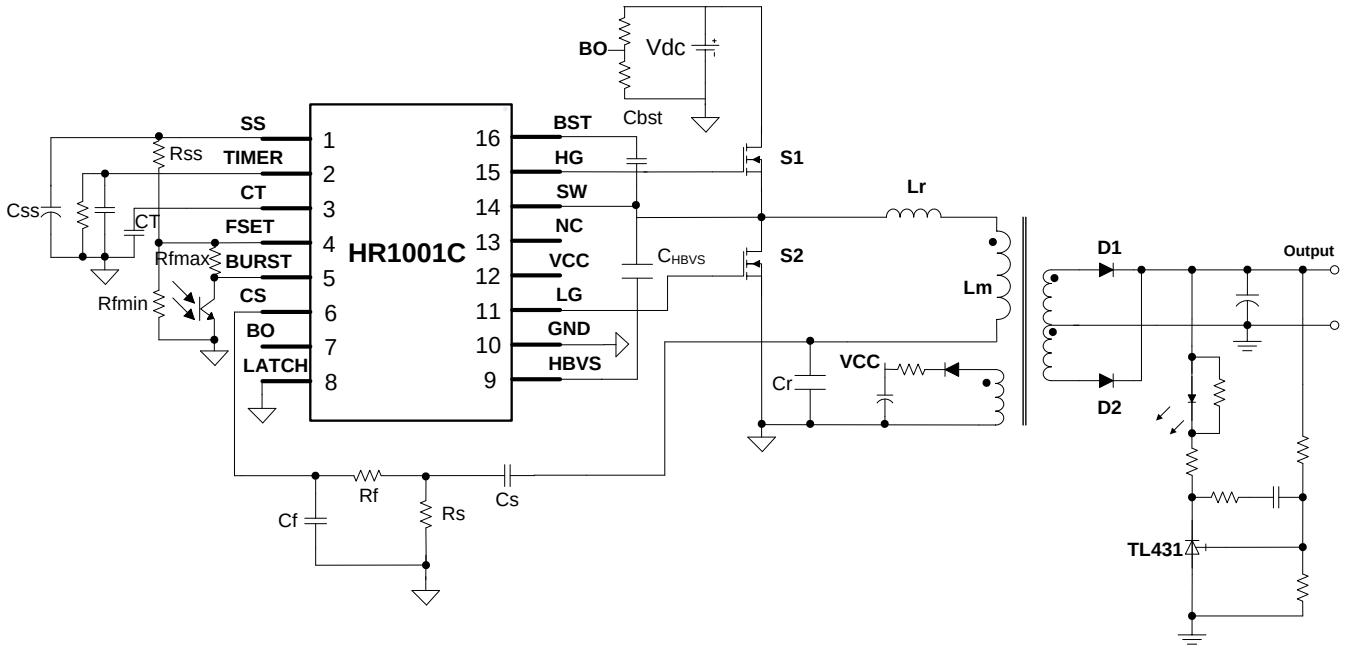
Typical Application



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ORDERING INFORMATION

Part Number*	Package	Top Marking
HR1001CGS	SOIC-16	*See Below*

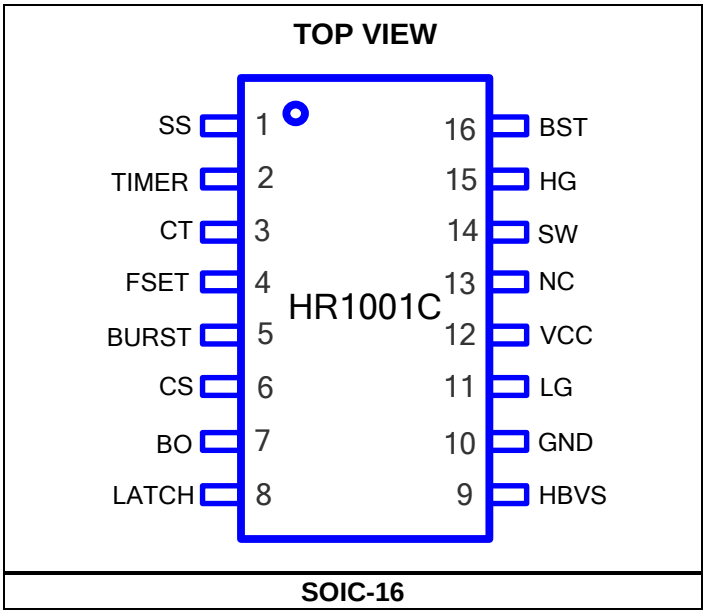
* For Tape & Reel, add suffix –Z (e.g. HR1001CGS–Z)

TOP MARKING

MPSYYWW
HR1001C
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
HR1001C: Part number
LLLLLLLLL: Lot number

PACKAGE REFERENCE



SOIC-16

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ABSOLUTE MAXIMUM RATINGS (1)

BST voltage ..... -0.3V to 618V
SW voltage ..... -3V to 600V
Max voltage slew rate of SW..... 50V/ns
Supply voltage (VCC) ..... Self-limited
Sink current of HBVS..... ±65mA
Voltage on HBVS..... -0.3V to self-limit
Source current of FSET 2mA
Voltage rating LG..... -0.3V to VCC
Voltage on CS ..... -3V to 6V
Other analog inputs and outputs..... -0.3V to 6V
Continuous power dissipation (T_A = +25°C) (2)
P_{IC}..... 1.56W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature..... -65°C to +150°C
ESD immunity: BST, HG, SW passes HBM 2.5kV, other pins can pass HBM 4kV.

RECOMMENDED OPERATING CONDITIONS (3)

Supply voltage (VCC) ..... 13V to 15.5V
Analog inputs and outputs ..... -0.3V to 6V
Operating junction temp (T_J) ... -40°C to + 125°C

THERMAL RESISTANCE (4) Θ_{JA} Θ_{JC}

	Θ_{JA}	Θ_{JC}	
SOIC-16	80	35	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

VCC = 13V, C_{HG} = C_{LG} = 1nF, CT = 470pF, R_{FSET} = 12kΩ, T_J = -40°C ~ 125°C, min and max values guaranteed by characterization, typical value tested under 25°C, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Units
IC Supply Voltage (VCC)						
VCC operating range			8.9		15.5	V
VCC high threshold, IC switch on	V_{CCH}		10.3	11	11.7	V
VCC low threshold, IC switch off	V_{CCL}		7.5	8.2	8.9	V
Hysteresis	V_{CC-hys}			2.8		V
IC Supply Current (VCC)						
Start-up current	$I_{start-up}$	Before the device turns on, VCC = VCC_H - 0.2V		250	320	µA
Quiescent current	I_q	Device on, V_{Burst} < 1.23V, R_{FSET} = 12kΩ, F_{MIN} = 60kHz		1.2	1.5	mA
	I_{q-f}	Device on, V_{Burst} < 1.23V, R_{FSET} = 3.57kΩ, F_{BURST} = 200kHz		1.42	1.8	mA
Operating current	I_{CC-nor}	Device on, V_{Burst} = V_{FSET}		3	5	mA
Residual consumption	I_{Fault}	VCC < 8.2V or V_{LATCH} > 1.85V or V_{CS} > 1.5V or V_{TIMER} > 3.5V or V_{BO} < 1.81V or V_{BO} > 5.5V or OTP	240	350	420	µA
High-Side Floating Gate Driver Supply (BST and SW)						
BST leakage current	I_{LK-BST}	V_{BST} = 600V, T_J = 25°C			14	µA
SW leakage current	I_{LK-SW}	V_{SW} = 582V, T_J = 25°C			14	µA
Current Sensing (CS)						
Input bias current	I_{CS}	V_{CS} = 0 to V_{CS-OCP}			2	µA
Frequency shift threshold	V_{CS-OCR}		0.71	0.78	0.85	V
OCP threshold	V_{CS-OCP}		1.41	1.5	1.59	V
Current polarity comparator reference when HG turns off	V_{CSPR}		50	85	131	mV
Current polarity comparator reference when LG turns off	V_{CSNR}		-131	-85	-50	mV
Line Voltage Sensing (BO)						
Start-up threshold voltage	V_{BO-On}			2.30	2.40	V
Turn-off threshold voltage	V_{BO-Off}		1.72	1.81		V
Clamp level	$V_{BO-Clamp}$		5.1	5.5	5.9	V
Latch Function (LATCH)						
Input bias current (V_{LATCH} = 0 to V_{th})	I_{LATCH}				1	µA
LATCH threshold	V_{LATCH}		1.72	1.85	1.95	V

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ELECTRICAL CHARACTERISTICS *(continued)*

VCC = 13V, C_{HG} = C_{LG} = 1nF, CT = 470pF, R_{FSET} = 12kΩ, T_J = -40°C ~ 125°C, min and max values guaranteed by characterization, typical value tested under 25°C, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Oscillator						
Output duty cycle	D	T_J = 25°C	48	50	52	%
		T_J = -40 ~ 125°C	47	50	53	%
Oscillation frequency	f_{osc}	CT ≤ 150pF, R_{FSET} ≤ 2kΩ			600	kHz
CT peak value	V_{CFp}			3.8		V
CT valley value	V_{CFv}			0.9		V
Voltage reference at FSET	V_{REF}		1.87	2	2.05	V
Dead time	t_{DMIN}	C_{HBVS} = 5pF typically	180	235	290	ns
	t_{DMAX}			1		µs
	$t_{D\text{-}float}$	HBVS floating	250	350	450	ns
Timer for CMP	t_{CMP}			52		µs
Half-Bridge Voltage Sense (HBVS)						
Voltage clamp	$V_{HBVS\text{-}Clamp}$			7.6		V
Minimum voltage change rate that can be detected	dv_{min}/dt	C_{HBVS} = 5pF, typically			180	V/µs
Turn-on delay	T_d	Slope finish to turn-on delay		100		ns
Soft-Start Function (SS)						
Discharge resistance	R_{SS}	V_{CS} > $V_{CS\text{-}OCR}$		130		Ω
Threshold for OCP latch	$V_{SS\text{-}OCP}$	V_{CS} > $V_{CS\text{-}OCP}$	1.64	1.73	1.82	V
Standby Function (BURST)						
Disable threshold	V_{Burst}		1.17	1.23	1.28	V
Hysteresis	$V_{Burst\text{-}hys}$			30	100	mV
Delayed Shutdown (TIMER)						
Charge current	I_{TIMER}	V_{TIMER} = 1V, V_{CS} = 0.85V, T_J = 25°C	80	130	180	µA
Threshold for forced operation at maximum frequency	$V_{TIMER\text{-}fmax}$		1.80	2	2.10	V
Shutdown threshold	$V_{TIMER\text{-}SD}$		3.2	3.5	3.7	V
Restart threshold	$V_{TIMER\text{-}R}$		0.21	0.28	0.35	V
Low-Side Gate Driver (LG, Referenced to GND)						
Peak source current (5)	$I_{LG\text{-}source\text{-}pk}$			0.75		A
Peak sink current (5)	$I_{LG\text{-}sink\text{-}pk}$			0.87		A
Sourcing resistor	$R_{LG\text{-}source}$	LG_R @ Isrc = 0.01A		4		Ω
Sinking resistor	$R_{LG\text{-}sink}$	LG_R @ Isnk = 0.01A		2		Ω
Fall time	$t_{LG\text{-}f}$			30		ns
Rise time	$t_{LG\text{-}r}$			30		ns
UVLO saturation		VCC = 0 to V_{CCH}, I_{sink} = 2mA			1	V

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ELECTRICAL CHARACTERISTICS *(continued)*

VCC = 13V, C_{HG} = C_{LG} = 1nF, CT = 470pF, R_{FSET} = 12kΩ, T_J = -40°C ~ 125°C, min and max values guaranteed by characterization, typical value tested under 25°C, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Units
High-Side Gate Driver (HG, Referenced to SW)						
Peak source current (5)	$I_{HG-source-pk}$			0.74		A
Peak sink current (5)	$I_{HG-sink-pk}$			0.87		A
Sourcing resistor	$R_{HG-source}$	HG_R @ Isrc = 0.01A		4		Ω
Sinking resistor	$R_{HG-sink}$	HG_R @ Isnk = 0.01A		2		Ω
Fall time	t_{HG-f}			30		ns
Rise time	t_{HG-r}			30		ns
Thermal Shutdown						
Thermal shutdown threshold (5)				150		°C
Thermal shutdown recovery threshold (5)				120		°C

NOTE:

5) Guaranteed by design.

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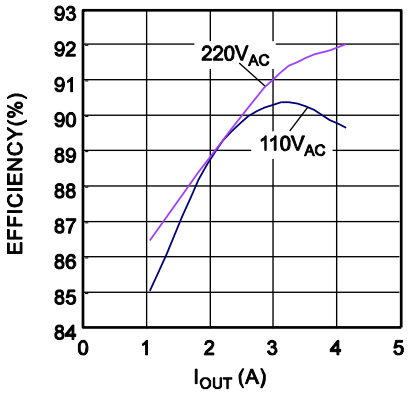
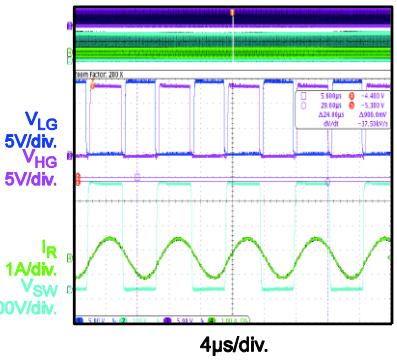
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are generated using the evaluation board built with the design example on page 22. V_{AC} = 120V, V_{OUT} = 24V, I_{OUT} = 4.16A, T_A = 25°C, unless otherwise noted.

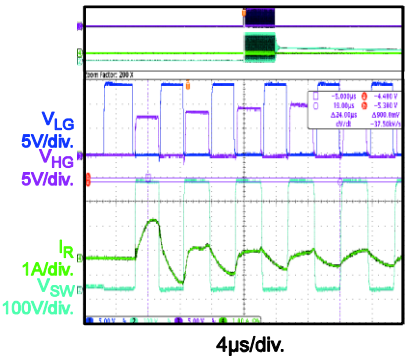
Efficiency



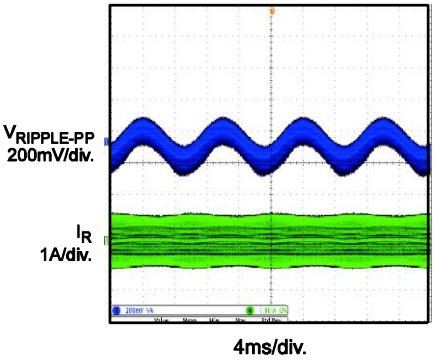
Steady State
V_{OUT}=24V, I_{OUT}=4.16A



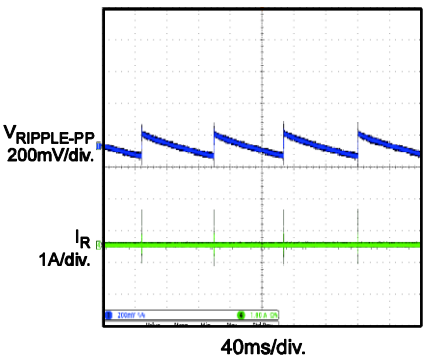
Steady State
V_{OUT}=24V, I_{OUT}=0A



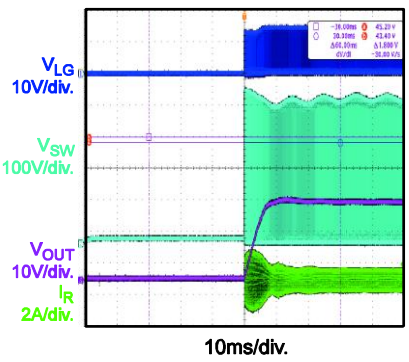
Steady State
V_{OUT}=24V, I_{OUT}=4.16A



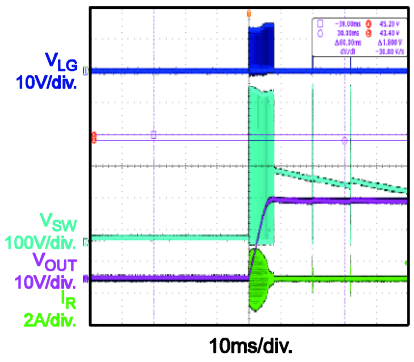
Steady State
V_{OUT}=24V, I_{OUT}=0A



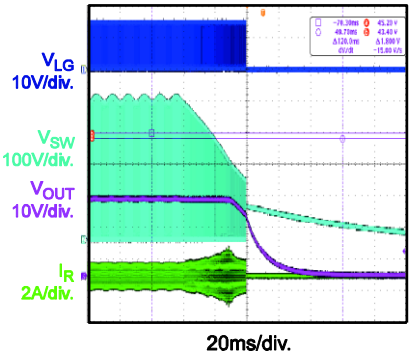
Start-Up
V_{OUT}=24V, I_{OUT}=4.16A



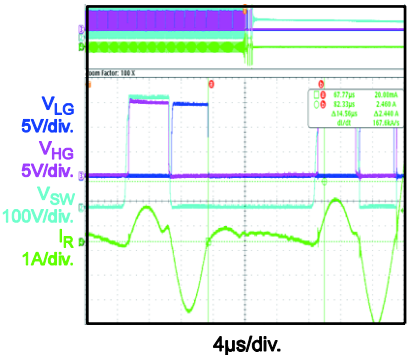
Start-Up
V_{OUT}=24V, I_{OUT}=0A



Shutdown
V_{OUT}=24V, I_{OUT}=4.16A



Capacitive Mode Protection
V_{OUT} Short



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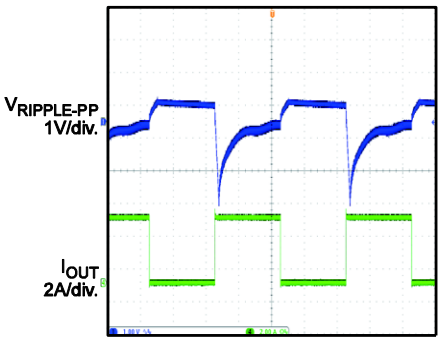
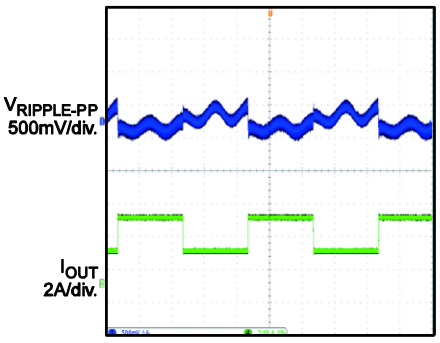
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are generated using the evaluation board built with the design example on page 22. V_{AC} = 120V, V_{OUT} = 24V, I_{OUT} = 4.16A, T_A = 25°C, unless otherwise noted.

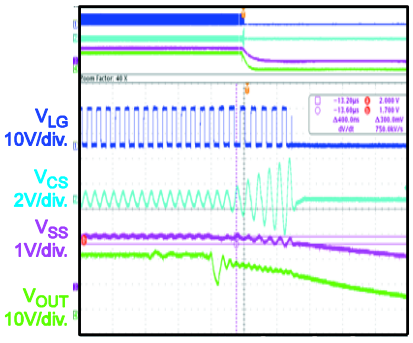
Transient
0A to 4.16A



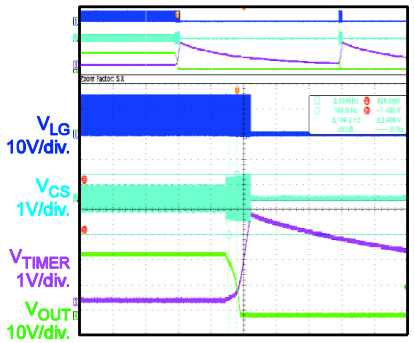
Transient
2.08A to 4.16A



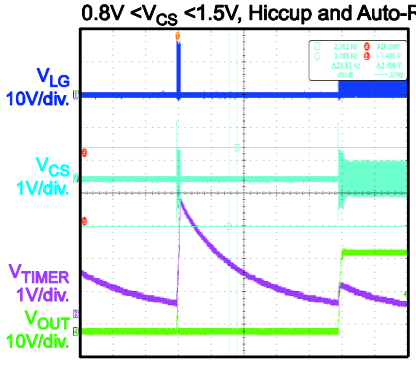
Short-Circuit Protection
V_{CS} >1.5V, Latch Off



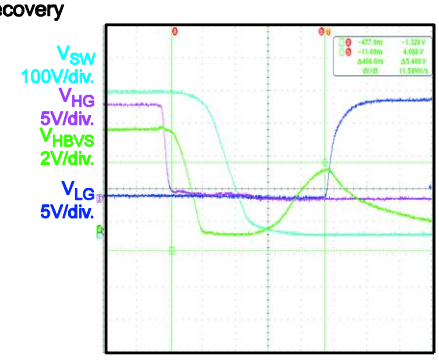
Over-Current Protection Entry
0.8V <V_{CS} <1.5V, Hiccup and Auto-Recovery



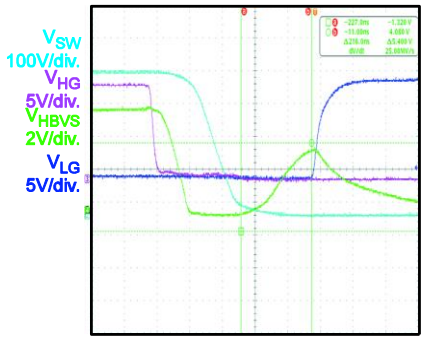
Over-Current Protection Recovery
0.8V <V_{CS} <1.5V, Hiccup and Auto-Recovery



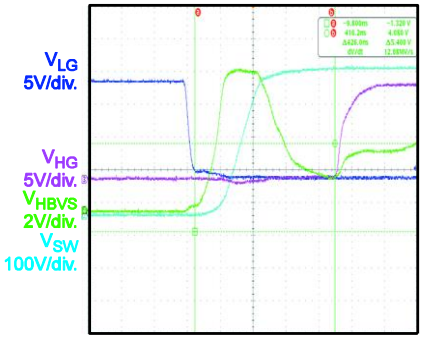
Dead Time when HG Turns Off



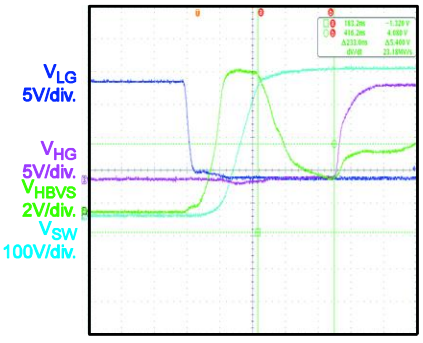
Delay Time when HG Turns Off



Dead Time when LG Turns Off



Delay Time when LG Turns Off



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PIN FUNCTIONS

Pin #	Name	Description
1	SS	**Soft start.** Connect an external capacitor from SS to GND and a resistor to FSET to set the maximum oscillator frequency and the time constant for the frequency shift during start-up. An internal switch discharges the capacitor when the chip turns off (VCC < UVLO, BO < V_{BO-Off} or > $V_{BO-Clamp}$, LATCH > V_{LATCH}, CS > V_{CS-OCP}, TIMER > $V_{TIMER-fmax}$, thermal shutdown) to guarantee a soft start.
2	TIMER	**Period between over-current and shutdown.** Connect a capacitor and a resistor from TIMER to GND to set both the maximum duration from an over-current condition before the IC stops switching and the delay before the IC resumes switching. Whenever the voltage on CS exceeds V_{CS-OCR}, an internal current source (I_{TIMER}) charges the capacitor. An external resistor discharges this capacitor slowly. If the voltage on TIMER reaches $V_{TIMER-fmax}$, the soft-start capacitor discharges completely, raising its switching frequency to its maximum value. I_{TIMER} remains on. When the voltage exceeds $V_{TIMER-SD}$, the IC stops switching, the internal current source turns off, and the voltage decays. The IC enters soft start when the voltage drops below $V_{TIMER-R}$. This converter works intermittently with very low average input power under short-circuit conditions.
3	CT	**Time set.** An internal current source programmed by an external network connected to FSET charges and discharges a capacitor connected to GND. This determines the converter's switching frequency.
4	FSET	**Switching frequency set.** FEST provides a precise 2V reference. A resistor connected from FSET to GND defines a current that sets the minimum oscillator frequency. Connect the phototransistor of an optocoupler to FSET through a resistor to close the feedback loop that modulates the oscillator frequency, which regulates the converter's output voltage. The value of this resistor sets the maximum operating frequency. An R-C series connected from FSET to GND sets the frequency shift at start-up to prevent excessive inrush energy.
5	BURST	**Burst mode operation threshold.** BURST senses the voltage related to the feedback control, which is compared to an internal reference (V_{Burst}). When the voltage on BURST is lower than this reference, the IC enters an idle state and reduces its quiescent current. When the feedback drives BURST above V_{Burst} + 30mV ($V_{Burst-hys}$), the chip resumes switching. There is no soft start. This function enables burst mode operation when the load falls below a programmed level determined by connecting an appropriate resistor to the optocoupler to FSET (see the Block Diagram on page 12). Connect BURST to FSET if burst mode is not used.
6	CS	**Current sense of the half-bridge.** CS uses a sense resistor or a capacitive divider to sense the primary current. CS has the following functions: • Over-current regulation: If the voltage exceeds V_{CS-OCR}, the soft-start capacitor on SS discharges internally. The frequency increases, limiting the power throughout. During an output short circuit, this normally results in a nearly constant peak primary current. TIMER limits the duration of this condition. • Over-current protection (OCP): If the current continues to build despite the frequency increase, when V_{CS} > V_{CS-OCP}, SS is discharged continuously, and OCP is not triggered immediately until V_{SS} < V_{SS-OCP}. If the condition for V_{CS} > V_{CS-OCP} remains once V_{SS} drops below V_{SS-OCP}, OCP is triggered in latch mode. This requires cycling the IC supply voltage to restart. The latch is removed once the VCC voltage drops below the UVLO threshold. This prevents OCP from mistriggering in surge tests or other transient tests. • Capacitive mode protection (CMP): Once LG turns off, CS is compared to the V_{CSNR} CMP threshold. If V_{CS} > V_{CSNR}, the HG gate is blocked from turning on until the slope is detected or the CMP timer is complete. Once HG turns off, CS is compared to the V_{CSPR} CMP threshold. If V_{CS} < V_{CSPR}, the low-side gate is blocked from turning on until the slope is detected or the CMP timer is completed. If a capacitive mode status is detected, SS is not discharged immediately; there is a 1µs delay. After the blanking delay, SS is discharged if the fault condition in capacitive mode remains. This prevents the influence of CS noise. Connect CS to GND if the CMP function is not used.

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PIN FUNCTIONS *(continued)*

Pin #	Name	Description
7	BO	**Input voltage sense and brown-in/brown-out protection.** If the voltage on BO is over V_{BO-On}, the IC enables the gate driver. If the voltage on BO is below V_{BO-Off}, the IC is disabled.
8	LATCH	**IC latch off.** When the voltage on LATCH exceeds V_{LATCH}, the IC shuts down and lowers its bias current almost to its pre-start-up level. LATCH is reset when the voltage on VCC is discharged below its UVLO threshold. Connect LATCH to GND if the function is not used.
9	HBVS	**Half-bridge dV/dt sense.** To detect the dV/dt of the half-bridge, a high-voltage capacitor is connected between SW and HBVS. The dV/dt current through HVBS is used to adjust the dead-time adaptively between the high-side gate and the low-side gate.
10	GND	**Ground.** GND is the current return for both the low-side gate driver and the IC bias. Connect all external ground connections with a trace to GND—one for signals and a second for pulsed current return.
11	LG	**Low-side gate driver output.** The driver is capable of a 0.8A source/sink peak current to drive the lower MOSFET of the half-bridge. LG is pulled to GND during UVLO.
12	VCC	**Supply voltage.** VCC supplies both the IC bias and the low-side gate driver. Use a small bypass capacitor (e.g.: 0.1µF) to achieve a clean bias voltage for the IC signal.
13	NC	**High-voltage spacer.** No internal connection. NC isolates the high-voltage pin (SW) and eases compliance with safety regulations (creepage-distance) on the PCB.
14	SW	**High-side switch source.** SW is the current return for the high-side gate drive current. SW requires careful layout to avoid large spikes below ground.
15	HG	**High-side floating gate driver output**. HG is capable of a 0.8A source/sink peak current to drive the upper MOSFET of the half-bridge. Connect an internal resistor to SW to ensure that HG does not float during UVLO.
16	BST	**Bias for floating voltage supply of high-side gate driver.** Connect a bootstrap capacitor between BST and SW. This capacitor is charged by an internal bootstrap diode driven in-phase with the low-side gate driver.

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block diagram

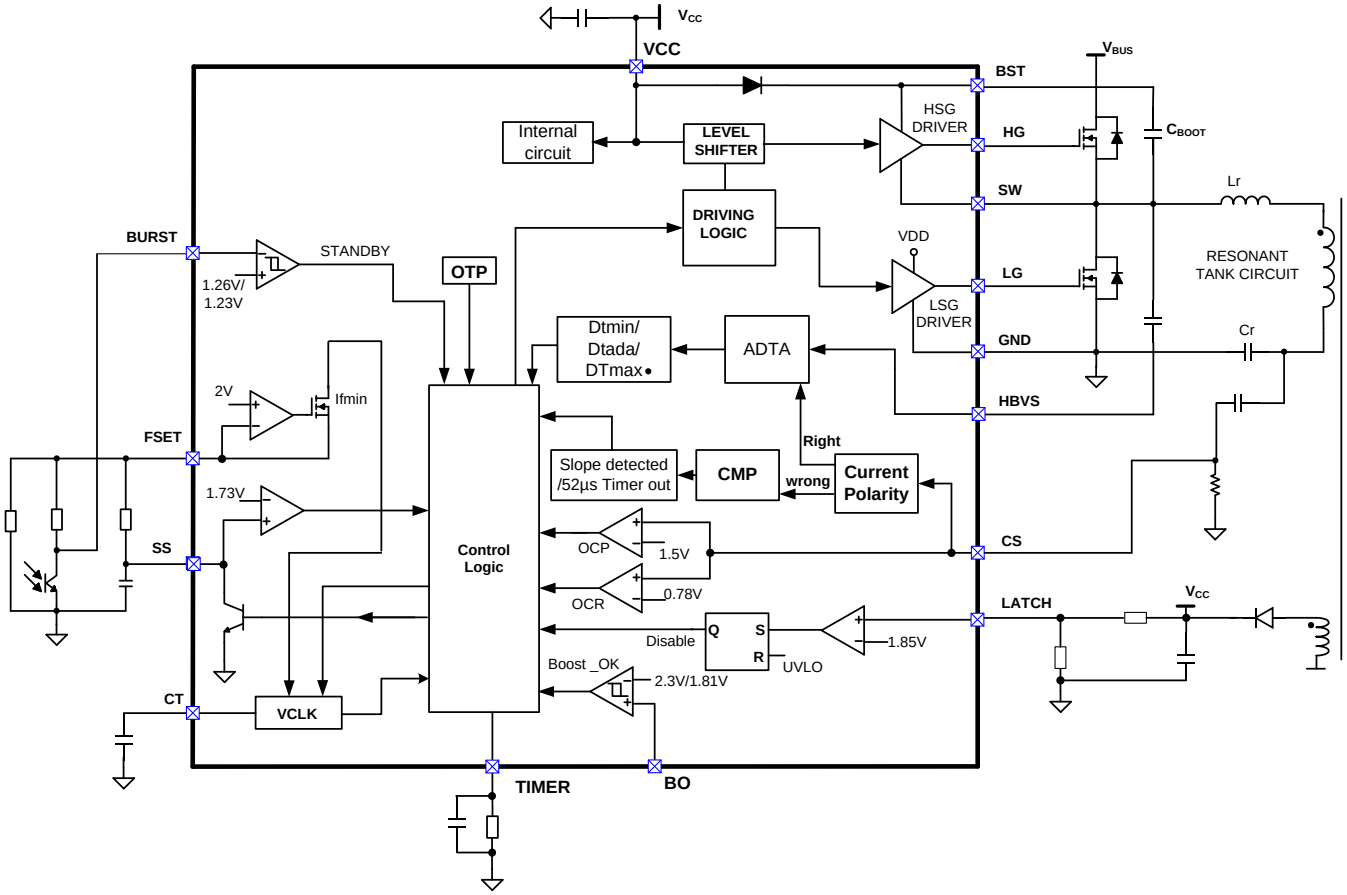

Figure 1: Functional Block Diagram

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APPLICATION INFORMATION

Oscillator

Figure 2 shows the oscillator block diagram. A modulated current charges and discharges the CT capacitor repeatedly between its peak valley thresholds, which determines the oscillator frequency.

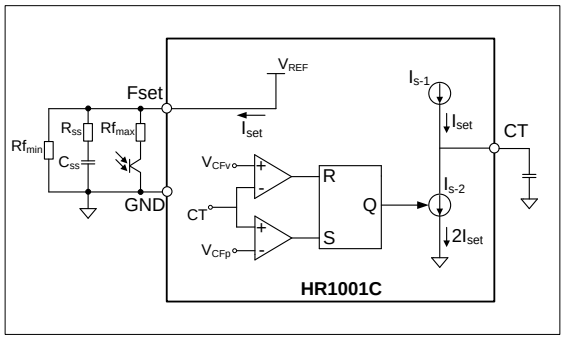

Figure 2: Oscillator Block Diagram

FSET sets the CT charging current, I_{set} (I_{S-1}). When CT passes its peak threshold (V_{CFp}), the flip-flop is set, and a discharge current source twice the charge current is enabled. The difference between these two currents forces the charge and discharge of CT to be equal. When the voltage on the CT capacitor falls below its valley threshold (V_{CFv}), the flip-flop is reset and turns off I_{S-2}. This starts a new switching cycle. Figure 3 shows the detailed waveform of the oscillator.

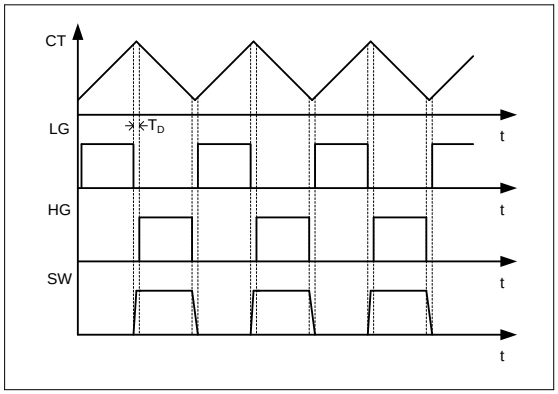

Figure 3: CT Waveform and Gate Signal

An R-C network connected to FSET externally determines the normal switching frequency and the soft-start switching frequency.

Rf_{min} from FSET to GND contributes to the maximum resistance of the external R-C network when the phototransistor does not conduct. This sets the FSET minimum source current, which defines the minimum switching frequency.

Under normal operation, the phototransistor adjusts the current flow through Rf_{max} to modulate the frequency for output voltage regulation. When the phototransistor is saturated, the current through Rf_{max} is at its maximum, which sets the frequency at its maximum.

An R-C in series connected between FSET and GND shifts the frequency at start-up. Please see the Soft-Start Operation section on page 14 for details.

Set the minimum and maximum frequencies with Equation (1) and Equation (2):

$$f_{min} = \frac{1}{3 \cdot CT \cdot Rf_{min}} \quad (1)$$

$$f_{max} = \frac{1}{3 \cdot CT \cdot (Rf_{min} \,||\, Rf_{max})} \quad (2)$$

Typically, the CT capacitance is between 0.1nF and 1nF. Calculate the values of Rf_{min} and Rf_{max} with Equation (3) and Equation (4):

$$Rf_{min} = \frac{1}{3 \cdot CT \cdot f_{min}} \quad (3)$$

$$Rf_{max} = \frac{Rf_{min}}{\frac{f_{max}}{f_{min}} - 1} \quad (4)$$

It is recommended to use a CT capacitor (≤330pF) for best overall temperature performance.

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Soft-Start Operation (SS)

For the resonant half-bridge converter, the power delivered is inversely proportional to its switching frequency. To ensure that the converter starts or restarts with safe currents, the soft start forces a high initial switching frequency until the value is controlled by the closed loop.

Soft start is achieved by using an external R-C series circuit (see Figure 4).

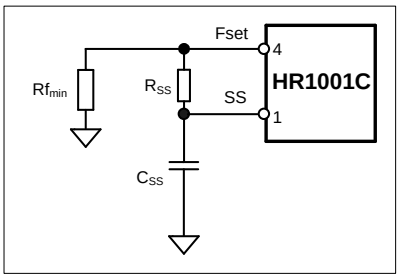

Figure 4: Soft-Start Block

When start-up begins, the SS voltage is 0V, so the soft-start resistor (R_{SS}) is in parallel to Rf_{min}. Rf_{min} and R_{SS} determine the initial frequency, which can be calculated with Equation (5):

$$f_{start} = \frac{1}{3 \cdot CT \cdot (Rf_{min} || R_{SS})} \quad (5)$$

During start-up, C_{SS} charges until its voltage reaches the reference (V_{REF}), and the current through R_{SS} decays to zero. This period takes about $5x(R_{SS}xC_{SS})$. During this period, the switching frequency change follows an exponential curve. Initially, the C_{SS} charge reduces the frequency relatively quickly, but the rate decreases gradually.

After the soft-start period, the switching frequency is dominated by the feedback loop to regulate the output voltage. With the soft start, the current of the resonant tank increases during the start-up gradually.

Select the soft-start R-C network with Equation (6) and Equation (7):

$$R_{SS} = \frac{Rf_{min}}{\frac{f_{start}}{f_{min}} - 1} \quad (6)$$

$$C_{SS} = \frac{3 \cdot 10^{-3}}{R_{SS}} \quad (7)$$

Select an initial frequency (f_{start}) at least four times f_{min}. When selecting C_{SS}, there is a trade-off between the desired soft-start operation and the over-current protection (OCP) speed. See the Over-Current Protection section on page 17 for details.

Adaptive Dead-Time Adjustment (ADTA)

When operating in inductive mode, the soft switching of the power MOSFETs results in high efficiency of the resonant converter. A fixed dead time may result in hard switching in light load, especially if the magnetizing inductance (Lm) is too large. A dead time that is too long may lead to ZVS loss. The current may change polarity during the dead time, resulting in capacitive mode switching. The adaptive dead-time control adjusts the dead time automatically by detecting the dV/dt of the half-bridge switching node (SW).

The HR1001C incorporates an intelligent adaptive dead-time adjustment (ADTA) logic circuit, which detects SW's dV/dt and inserts a proper dead time automatically. For the external circuit, connect a capacitor (C_{HBVS}, typically 5pF) between SW and HBVS to sense dV/dt. Figure 5 shows the simplified block diagram of ADTA. Figure 6 shows the operation waveform of ADTA.

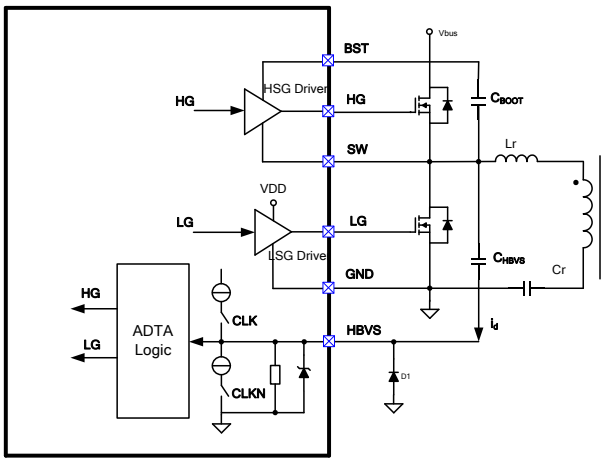

Figure 5: Block Diagram of ADTA

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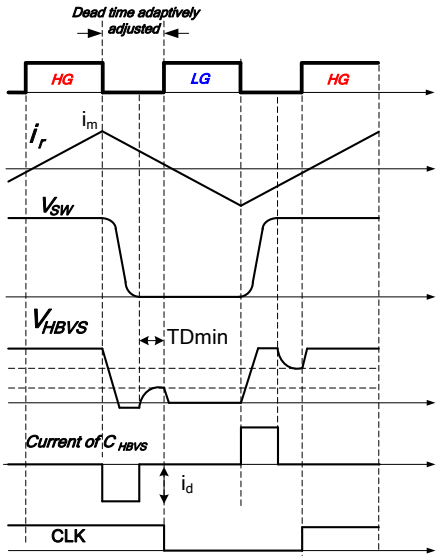

Figure 6: Operation Waveform of ADTA

When HG switches off, SW voltage swings from high to low due to the resonant tank current (*ir*). Accordingly, this negative dV/dt pulls current from HBVS via C_{HBVS}. If the dV/dt current is higher than the internal comparison current, the voltage on HBVS (V_{HBVS}) is pulled down and clamped at zero. When SW stops slewing and differential current stops, V_{HBVS} starts to ramp up. LG turns on after a delay (minimum dead time). Dead time is the duration between the moment HG turns off and the moment LG turns on.

When LG switches off, the SW voltage swings from low to high, and a positive dV/dt current is detected via C_{HBVS}. The dead time between LG turning off and HG turning on is maintained automatically by sensing the dV/dt current.

To avoid damaging HBVS, C_{HBVS} should be selected carefully. Keep the dV/dt current below 65mA using Equation (8):

$$i_d = \left| C_{HBVS} \frac{dv}{dt} \right| < 65mA \quad (8)$$

If C_{HBVS} is designed too low to sense the dV/dt, the minimum voltage change rate (dV_{min}/dt) must be accounted for to design a proper C_{HBVS} value.

First, calculate the peak magnetizing current (*Im*) with Equation (9):

$$I_m = \frac{V_{in}}{8 \cdot L_m \cdot f_{max}} \quad (9)$$

Then design C_{HBVS} with Equation (10):

$$C_{HBVS} > \frac{700uA}{I_m} \frac{C_{oss}}{2} \quad (10)$$

Where C_{oss} is the output capacitance when drain-source voltage on the MOSFET is almost zero volts (refer to the C_{oss} characteristics curve in the MOSFET's datasheet).

In a typical design, Lm = 870µH, V_{IN} = 450Vdc, and f_{max} = 140kHz. C_{HBVS} is calculated at 4.5pF, indicating that 5pF is suitable for most MOSFETs.

Figure 7 illustrates a possible dead time by ADTA logic. Note that there are three kinds of dead time: minimum dead time (t_{Dmin}), maximum dead time (t_{Dmax}), and adjusted dead time (t_{Dadj}), which is between t_{Dmin} and t_{Dmax}. ADTA logic sets t_{Dmin} = 235ns. When the SW transition time is smaller than t_{Dmin}, the logic does not let the gate turn on, which prevents a shoot-through between the low-side and high-side MOSFETs. A maximum dead time (t_{Dmax} = 1µs) forces the gate to turn on, preventing duty cycle losses or soft switching.

ADTA adjusts the dead time automatically and ensures zero-voltage switching (ZVS), which enables more flexibility in the MOSFET and Lm selection. ADTA also prevents hard switching if the design does not carefully account for light load or no load. At light load, the switching frequency goes high, and the magnetizing current goes low, risking hard switching that can lead to a thermal or reliability issue.

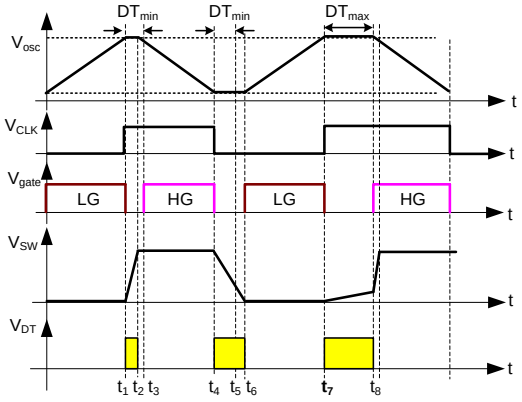

Figure 7: Dead Time in ADTA

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If HBVS is not connected, the internal circuit cannot detect the differential current from HBVS, so the dead time remains fixed at 350ns.

Figure 8 shows the dead-time waveform when HG turns off, and Figure 9 shows the dead-time waveforms when LG turns off. ADTA logic inserts the dead time automatically according to the transition shape of SW.

If V_{HBVS} is pulled down too low by the negative current of C_{HBVS}, the dead time from HG turning off to LG turning on may be too long. To clamp HBVS at zero and ensure an optimum dead time, connect a Schottky diode (D1) (such as BAT54) on HBVS to GND.

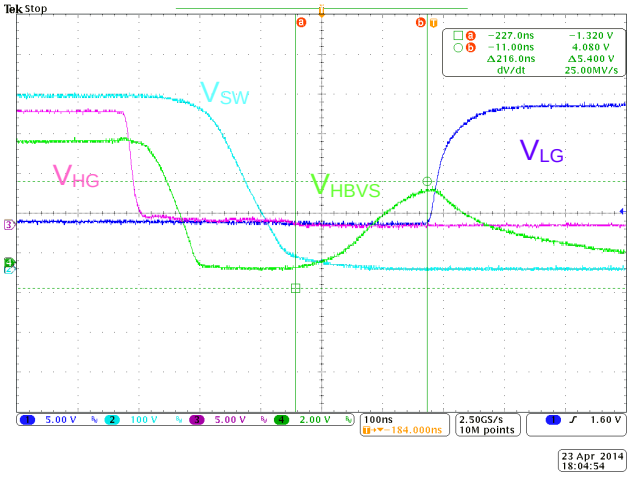

Figure 8: Dead Time at High-to-Low Transition

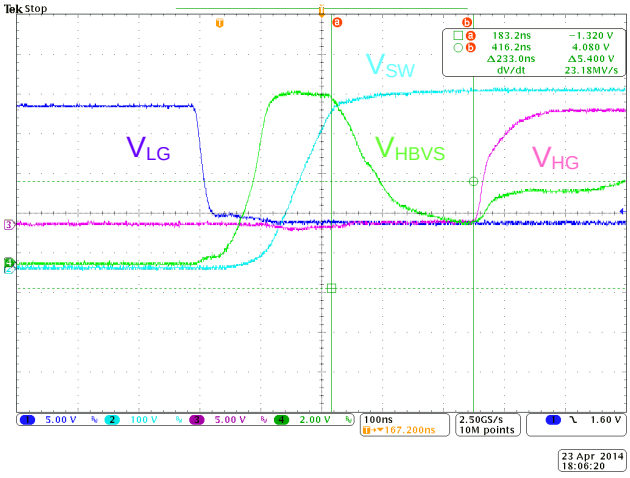

Figure 9: Dead Time at Low-to-High Transition

Capacitive Mode Protection (CMP)

When the resonant HB converter output is in an overload or short circuit, it may cause the converter to run into a capacitive region. In capacitive mode, the voltage applied to the resonant tank causes the current of the resonant tank to lag. Under this condition, the body diode of one of the MOSFETs is conducting. The other MOSFET should not be turned on to prevent device failure. The functional block diagram of capacitive mode protection (CMP) is shown in Figure 10.

Figure 11 shows the operating current principle of CMP. CSPOS and CSNEG stand for the current polarity, which is generated by comparing the voltage on CS with the internal V_{CSNR} and V_{CSPR} voltage reference.

At t0, LG turns off. CSNEG is high, which means the current is in the correct direction and is operating in inductive mode.

At t1, HG turns off. CSPOS is high, which means the current is in the correct direction and is operating in inductive mode.

At t2, LG turns off for the second time. CSNEG is low, indicating the current is in the wrong direction (the low-side MOSFET body diode is conducting), and the converter is operating in capacitive mode.

SW does not swing high until the current returns to the correct polarity. DT stays high and V_{OSC} is stopped, preventing the other MOSFET from turning on. This prevents capacitive switching.

At t3, the current returns to the correct polarity, and the other MOSFET turns on after the dV/dt current is detected.

Between t2 to t5, the correct current polarity cannot be detected, or there is so little current that SW cannot be pulled up or down.

Eventually, the timer (t_{CMP}) for CMP expires, and the other MOSFET is forced to switch on (see Figure 11).

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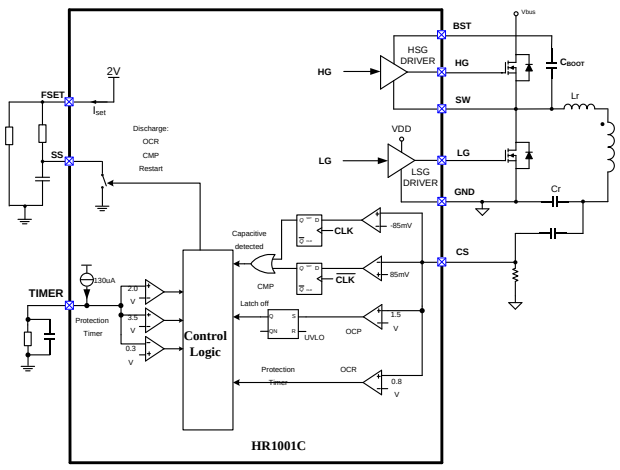

Figure 10: Block Diagram of CMP and OCP

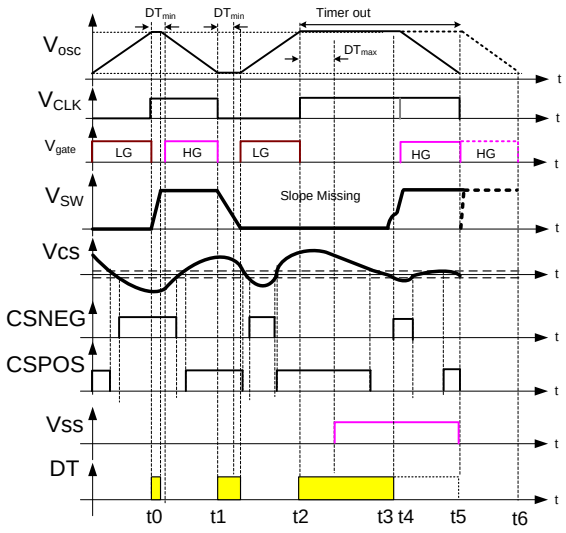

Figure 11: Operating Principle of CMP

When capacitive mode operation is detected, the V_{SS} control signal goes high, turning on an internal transistor to discharge C_{SS} after a 1µs blanking delay. This causes the frequency to increase to a very high level quickly to limit the output power. The V_{SS} control is reset, and soft start is activated when the first gate driver is switched off after CMP. The switching frequency decreases smoothly until the control loop takes over.

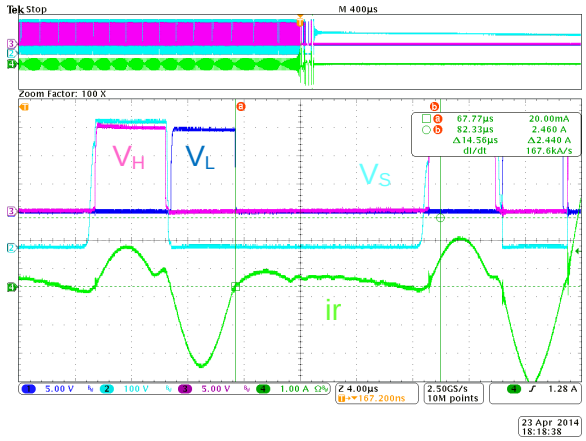

Figure 12: Capacitive Mode Protection Waveform

Figure 12 shows CMP behavior when the output is shorted. The current polarity goes in the wrong direction when LG switches off. The CMP logic detects this capacitive mode immediately and prevents HG from turning on. This prevents destructive capacitive switching. Once the current (*ir*) returns to the correct polarity, SW ramps up, the dV/dt current is detected, and HG turns on at the ZVS condition.

Over-Current Protection (OCP)

The HR1001C provides two levels of over-current protection (see Figure 13).

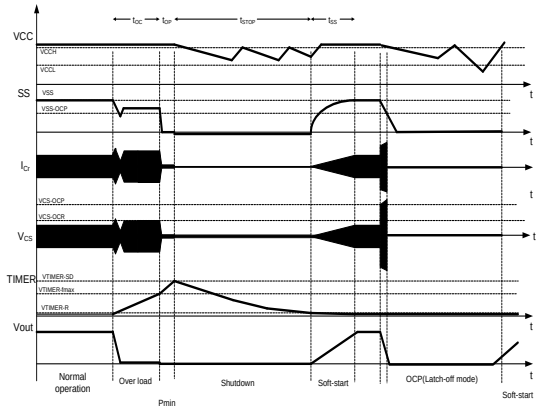

Figure 13: OCP Timing Sequence

The first level of protection occurs when the voltage on CS (V_{CS}) exceeds V_{CS-OCR}. Once this occurs, two actions take place. First, the internal transistor connected between SS and GND turns on for at least 10µs, which discharges C_{SS}. This creates a sharp increase in the oscillator frequency, reducing the energy transferred to the output. Second, an internal current source (I_{TIMER}) turns on to charge C_{TIMER}, ramping the TIMER voltage.

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If V_{CS} drops below V_{CS-OCR} before the voltage on TIMER (V_{TIMER}) reaches $V_{TIMER-fmax}$, both the discharge of C_{SS} and the charge of C_{TIMER} are stopped. The converter resumes normal operation.

t_{OC} is the time for V_{TIMER} to rise from 0V to $V_{TIMER-fmax}$. t_{OC} is also a delay time for over-current regulation. There is no simple relationship between t_{OC} and C_{TIMER}. Select C_{TIMER} based on experimental results. Based on experiments, C_{TIMER} may increase the operating time by 100ms.

If V_{CS} is still larger than V_{CS-OCR} after V_{TIMER} rises to $V_{TIMER-fmax}$, C_{SS} is discharged completely. Simultaneously, I_{TIMER} continues to charge C_{TIMER} until V_{TIMER} reaches $V_{TIMER-SD}$ and then turns off all gate drivers.

Calculate the time V_{TIMER} takes to rise from $V_{TIMER-fmax}$ to $V_{TIMER-SD}$ with Equation (11):

$$t_{OP} = 10^4 \cdot C_{TIMER} \quad (11)$$

The IC maintains the condition until V_{TIMER} decreases to $V_{TIMER-R}$, and then the IC restarts. Calculate this time period with Equation (12):

$$t_{OFF} = R_{TIMER} \cdot C_{TIMER} \cdot \ln\frac{3.5}{0.3} \approx 2.5 R_{TIMER} \cdot C_{TIMER} \quad (12)$$

The second level of over-current protection is triggered when V_{CS} rises to V_{CS-OCP}. Typically, this condition occurs when V_{CS} continues to rise during a short circuit. Once V_{CS} reaches V_{CS-OCP}, the HR1001C does not stop switching immediately, and C_{SS} is discharged by an internal transistor continuously. If V_{CS} remains above V_{CS-OCP} until V_{SS} drops below V_{SS-OCP}, the IC shuts down in latch-off mode (see Figure 14). While V_{SS} is dropping, the converter resumes normal operation if V_{CS} decreases below V_{CS-OCR}. This is a particular characteristic of the HR1001C and prevents instantaneous interference on CS to trigger any protection when the converter suffers a surge or other transient waves. Once the latch is triggered, it is not reset until VCC drops below UVLO.

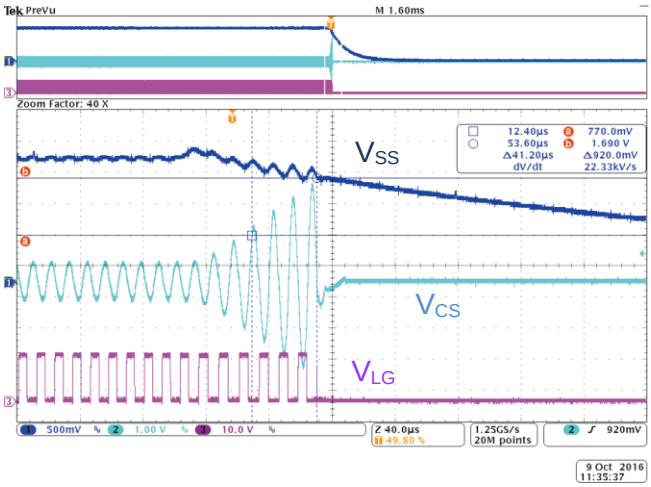

Figure 14: SCP Waveform

OCP limits the energy transferred from the primary side to the secondary side during an overload or short-circuit condition. Excessive power consumption due to high continuous currents can damage the secondary-side windings and rectifiers. TIMER provides additional protection to reduce the average power consumption. When OCP is triggered (except in a V_{CS} > V_{CS-OCP} condition), the converter enters a hiccup-like protection mode that operates intermittently.

Current Sensing

There are two current sensing methods: lossless current sensing and current sensing with a sense resistor.

Generally, a lossless current sensing solution is used in high-power applications (see Figure 15).

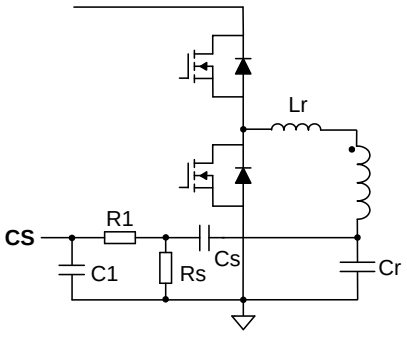

Figure 15: Current Sensing with a Lossless Network

Design a lossless current sensing network with Equation (13) and Equation (14):

$$Cs \le \frac{Cr}{100} \quad (13)$$

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Choose Rs with Equation (14):

$$Rs<\frac{0.8}{I_{Crpk}}\cdot(1+\frac{C_r}{C_s}) \quad (14)$$

Where I_{Crpk} is the peak current of the resonant tank at a low input voltage and full load. Calculate I_{Crpk} with Equation (15):

$$I_{Crpk}=\sqrt{(\frac{NV_O}{4L_m f_s})^2+(\frac{I_O\pi}{2N})^2} \quad (15)$$

Where N is the turns ratio of the transformer, lo is the output current, Vo is the output voltage, f_S is the switching frequency, and Lm is the magnetizing inductance.

For capacitive mode detection in no load or tiny-load conditions, Rs should fulfill the condition in Equation (16):

$$R_S>\frac{85mV}{I_m}(1+\frac{C_r}{C_S}) \quad (16)$$

In some conditions, especially where a large Lm is used, it can be difficult to fulfill both Equation (14) and Equation (16). The IC operates without a CMP function at light load if it does not have the restriction of Equation (16).

The R1 and C1 network is used to attenuate switching noise on CS. The time constant should be in the range of 100ns.

An alternate solution uses a sense resistor in series with the resonant tank (see Figure 16). This method is simple but causes unnecessary power loss on the sense resistor.

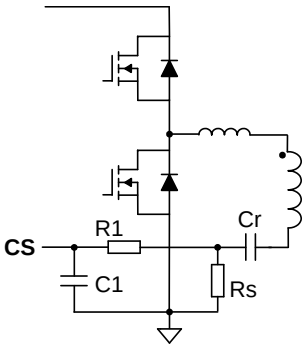

Figure 16: Current Sensing with a Sense Resistor

Design the sense resistor using Equation (17):

$$R_S=\frac{0.8}{I_{Crpk}} \quad (17)$$

Input Voltage Sensing (BI/BO)

The HR1001C stops switching when the input voltage drops below a specified value and restarts when the input voltage returns to normal. This function guarantees that the resonant half-bridge converter always operates within the specified input voltage range. The IC senses the voltage on BO (V_{BO}) through the tap of a resistor divider connected to the rectified AC voltage or the PFC output.

Figure 17 shows the line-sensing internal block diagram.

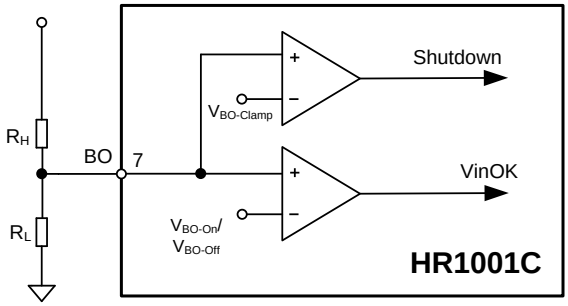

Figure 17: Input Voltage Sensing Block

If V_{BO} is higher than V_{BO-On}, the IC provides the gate driver outputs. The IC does not stop the gate driver until V_{BO} drops below V_{BO-Off}.

For a minimum operation input voltage of the half-bridge (V_{IN-min}), select a value for R_H that is large enough to reduce power consumption at no load. Then calculate R_L with Equation (18):

$$R_L=R_H\cdot\frac{1.81}{V_{IN-min}-1.81} \quad (18)$$

For additional protection, the IC shuts down when V_{BO} exceeds the internal clamp voltage ($V_{BO-Clamp}$). When V_{BO} is between V_{BO-On} and $V_{BO-Clamp}$, the IC operates normally.

Burst Mode Operation

At light load or in the absence of a load, the maximum frequency limits the resonant half-bridge switching frequency. To control the output voltage and limit power consumption, the HR1001C enables compatible converters to operate in burst mode. This reduce the average switching frequency greatly, thus reducing the average residual magnetizing current and associated losses.

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Operating in burst mode requires setting BURST. If the voltage on BURST (V_{BURST}) drops below the internal threshold (V_{Burst}), the HR1001C shuts down the HG and LG gate drive outputs, leaving only the 2V reference voltage on FSET and SS to retain the previous state and minimize the power consumption. When V_{BURST} exceeds V_{Burst} over 30mV ($V_{Burst-hys}$), the HR1001C resumes normal operation.

Based on the burst mode operating principle, BURST must be connected to the feedback loop. Figure 18 shows a typical circuit connecting BURST to the feedback signal for narrow input voltage range applications.

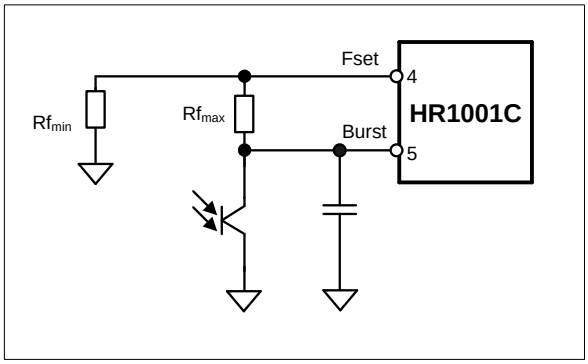

Figure 18: Burst Mode Operation Set-Up

In addition to setting the oscillator maximum frequency at start-up, Rf_{max} and determines the maximum burst mode frequency. After confirming f_{max}, calculate Rf_{max} with Equation (19):

$$Rf_{max} = \frac{3}{8} \cdot \frac{Rf_{min}}{\frac{f_{max}}{f_{min}} - 1} \quad (19)$$

Here, f_{max} corresponds to a load point (P_{Burst}), where the peak current flow through the transformer is too low to cause audible noise.

So far, this section has been based on a narrow input voltage range. As a property of the resonant circuit, the input voltage determines the switching frequency. This means P_{Burst} has a large variance over the wide input voltage range. To stabilize P_{Burst} over the input range, use the circuit in Figure 19 to insert the input voltage signal into the feedback loop.

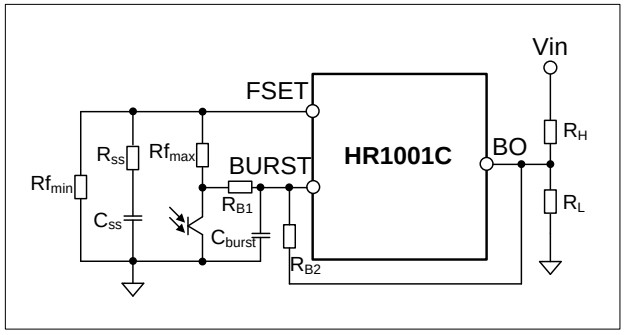

Figure 19: Burst Mode Operation Set-Up for a Wide Input Voltage Range

R_{B1} and R_{B2} in Figure 19 correct against the wide input voltage range. Select both resistors based on experimental results. The total resistance of R_{B1} and R_{B2} should be much larger than R_H to minimize the effect on V_{BO}. During burst mode operation, when the load is lower than P_{Burst}, the switching frequency is clamped at the maximum frequency. The output voltage must rise over the setting value, which increases the current flowing through the optocoupler. Therefore, the voltage on Rf_{max} rises due to the increased phototransistor current. Then V_{BURST} drops below V_{Burst}, triggering the gate signal off state. Until the output voltage falls below the setting value, the current flow through the optocoupler decreases, causing V_{BURST} to rise. When V_{BURST} exceeds V_{Burst} over 30mV, the IC restarts to generate the gate signal. The IC operates in this mode under no load or light load to decrease average power consumption.

Latch Operation

The HR1001C provides a simple latch-off function through LATCH. Applying an external voltage over V_{LATCH} causes the IC to enter a latched shutdown. After the IC is latched, its consumption drops, as shown by the residual current in the Electrical Characteristics table on page 5. Resetting the IC requires dropping the VCC voltage below the UVLO threshold (see the latch internal block diagram in Figure 20).

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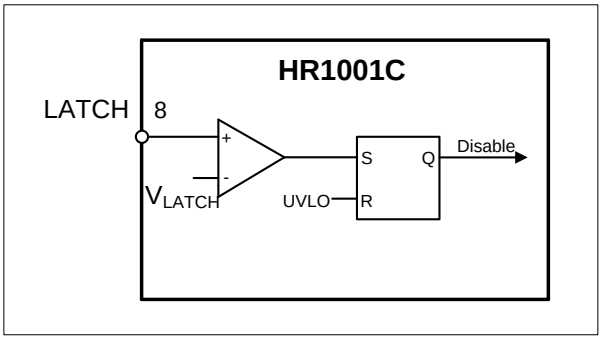

Figure 20: Latch Function Block

High-Side Gate Driver

The external BST capacitor provides energy to the high-side gate driver. An integrated bootstrap diode charges this capacitor through VCC. This diode simplifies the external driving circuit for the high-side switch, allowing the BST capacitor to charge when the low-side MOSFET is on (see the high-side gate driver internal block diagram in Figure 21).

To provide enough gate driver energy (considering the BST capacitor charge time), use a 100nF to 470nF capacitor for the BST capacitor.

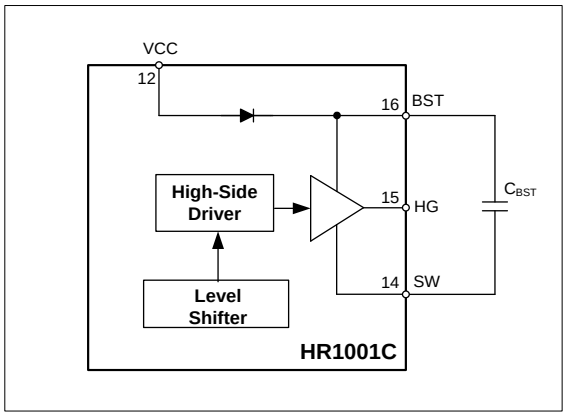

Figure 21: High-Side Gate Driver

Low-Side Gate Driver

LG provides the gate driver signal for the low-side MOSFET. The maximum absolute rating table shows the maximum voltage on LG is 16V. Under some conditions, a large voltage spike occurs on LG due to oscillations from the long gate driver wire, the MOSFET parasitic capacitance, and the small gate driver resistor. This voltage spike is dangerous to LG, so a 15V Zener diode close to LG and GND is recommended (see Figure 22).

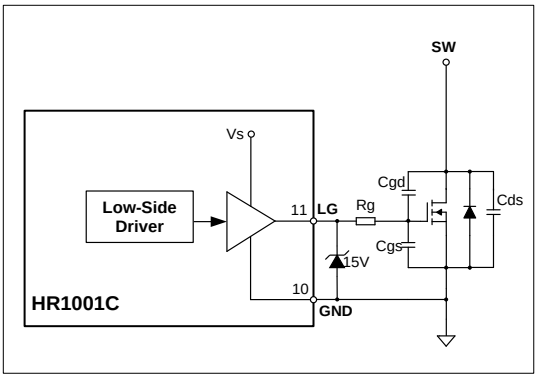

Figure 22: Low-Side Gate Driver

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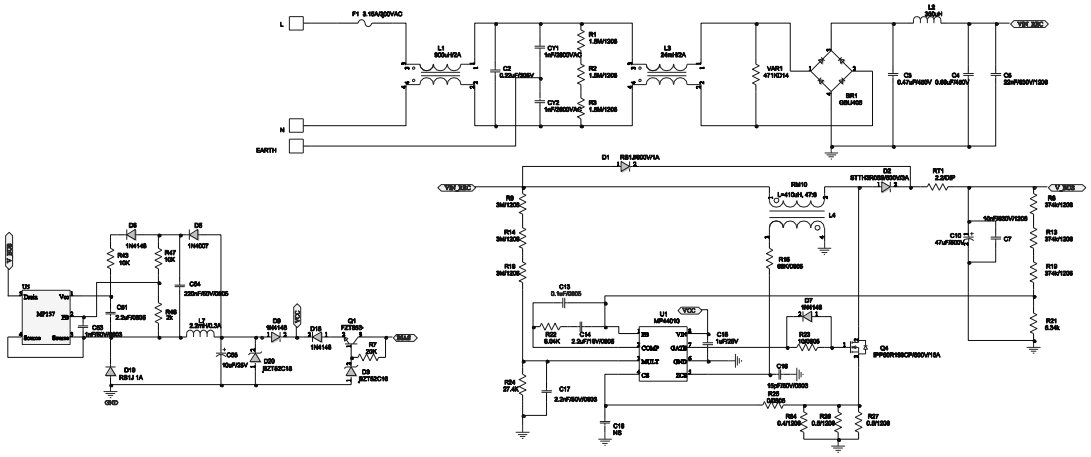
Design Example

A 100W LED driver is designed with the specifications below (see Table 1).

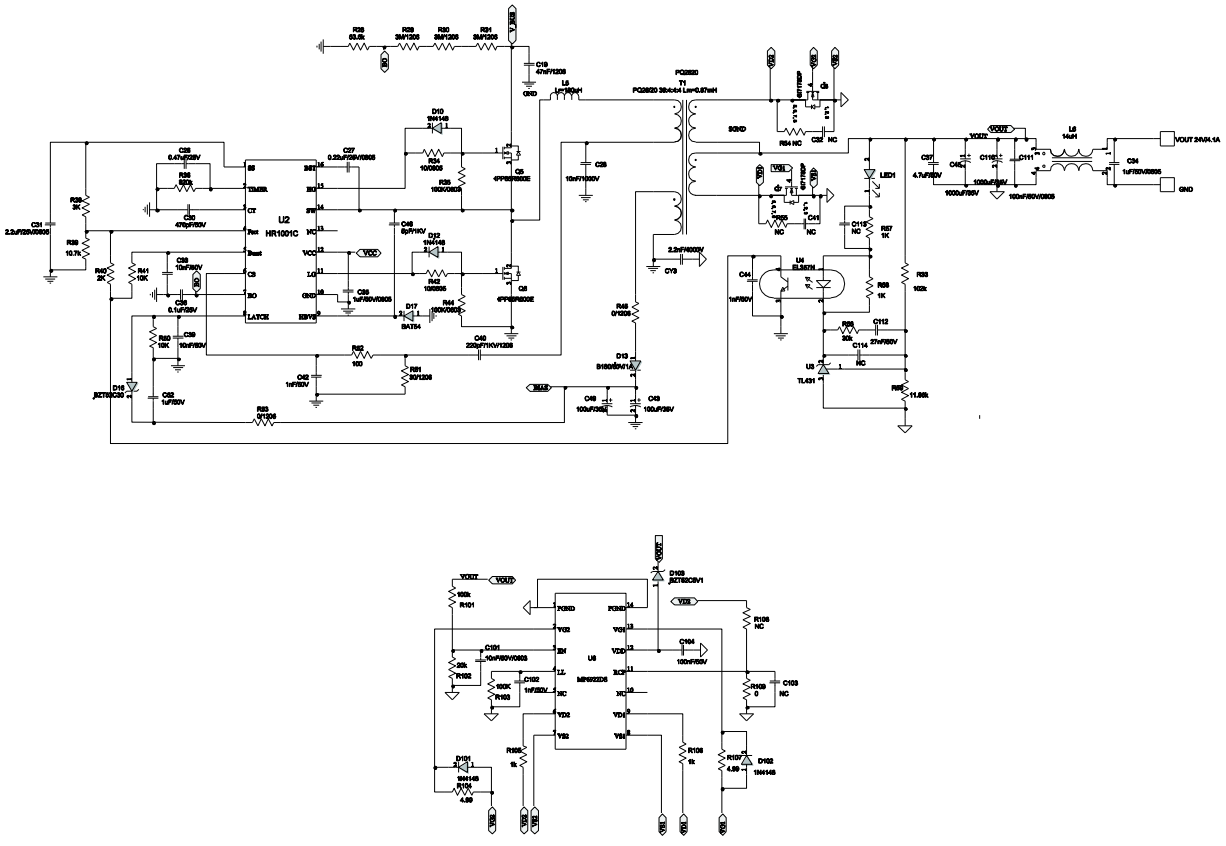
Table 1: Design Example

Input AC Voltage	90-305V_{AC}
Output Voltage	24V
Output Current	4.16A

Figure 23 shows the detailed application schematic. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section. The HR1001C has passed 4kV surge test for 30s duration on the EV44010-S + HR1001 - S - 00A evaluation board built with the design example.



PFC Stage



LLC Stage

Figure 23: Design Example for a 24V/4.16A Output

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CONTROL FLOW CHARTS

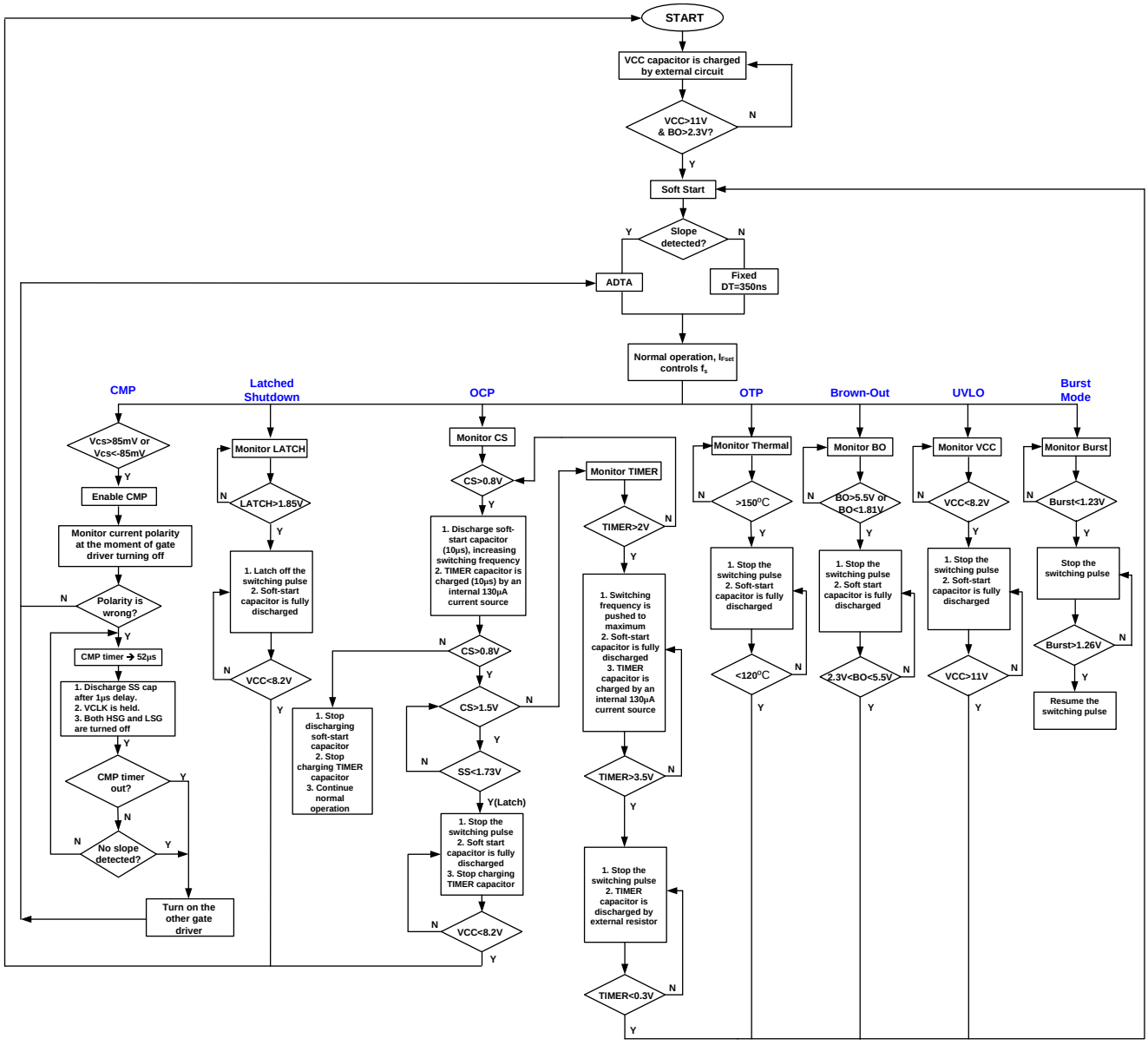

Figure 24: Control Flow Chart

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TYPICAL APPLICATION CIRCUIT

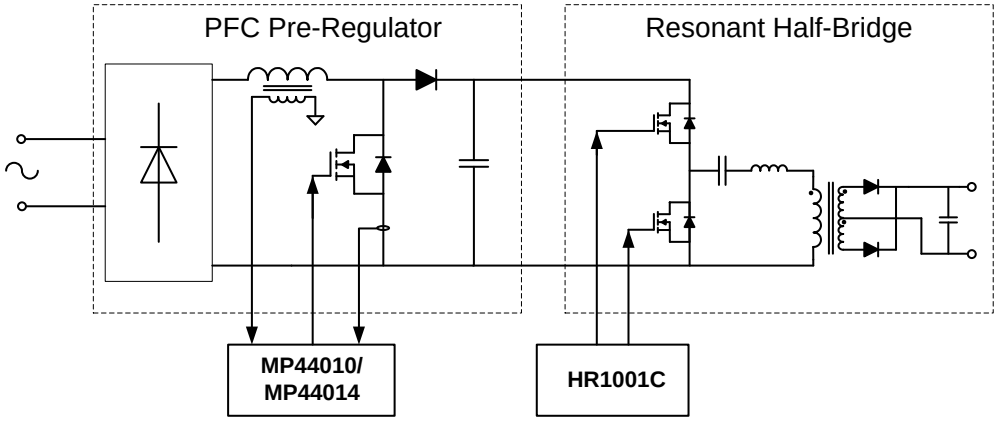

Figure 25: Application Circuit

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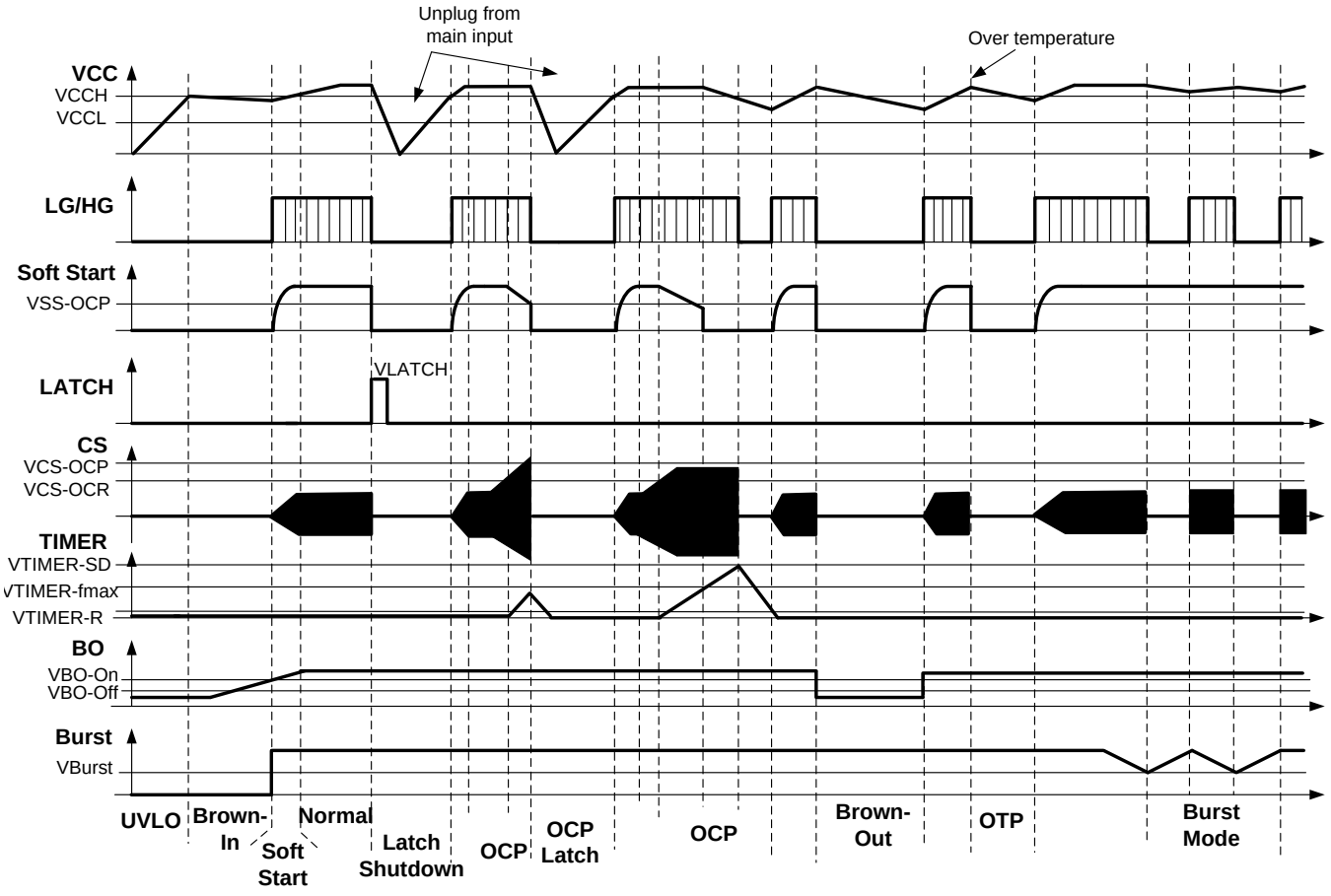
SYSTEM TIMING



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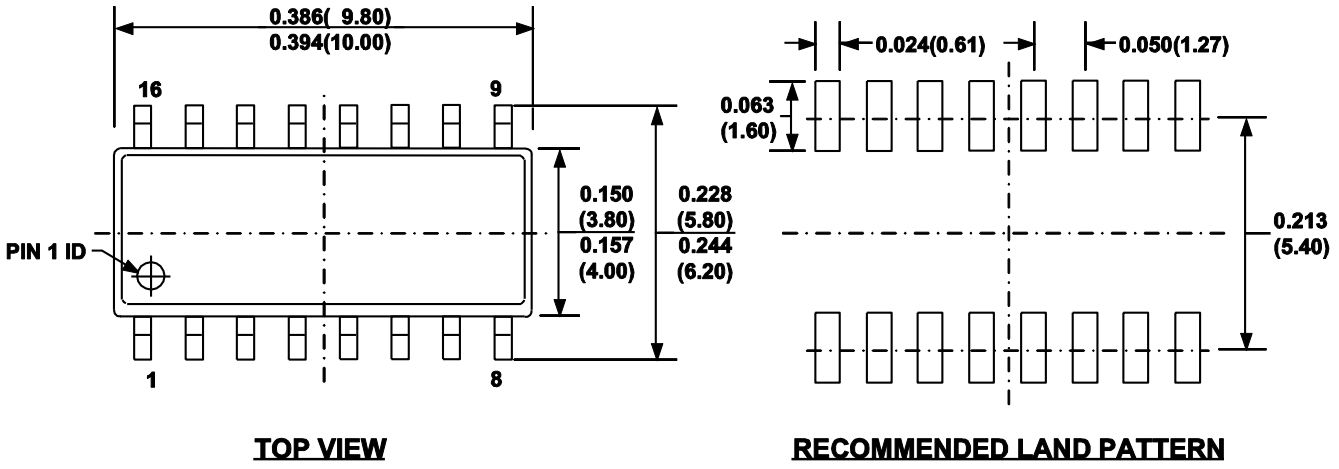
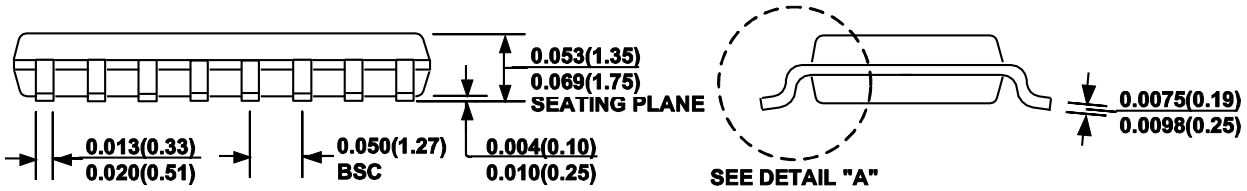
PACKAGE INFORMATION

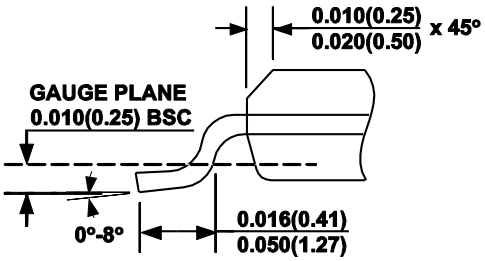
SOIC-16



TOP VIEW **RECOMMENDED LAND PATTERN**



FRONT VIEW **SIDE VIEW**



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AC.
6) DRAWING IS NOT TO SCALE.

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