HFC0502

Fixed-Frequency, Flyback Controller with Low Standby Power Consumption for both AC and DC Input Applications

DESCRIPTION

The HFC0502 is a fixed-frequency, flyback, current-mode controller with current control mode and internal slope compensation. It is designed for medium-power, offline, flyback, switch-mode power supply applications. The HFC0502 is a highly efficient, green-mode controller. At light loads, the controller freezes the peak current (I_{PEAK}) and reduces the switching frequency (f_{SW}) to 25kHz for excellent light-load efficiency. At very light loads, the controller enters burst mode to achieve low standby power consumption.

Frequency jittering (f_{JITTER}) helps dissipate energy generated by conducted noise, which reduces electromagnetic interference (EMI). The HFC0502 employs over-power compensation (OPC) to reduce the difference between the over-power (OP) protection point at the low line and the OP protection point at the high line.

Full protection features include thermal shutdown, V_{CC} under-voltage lockout (UVLO) protection, overload protection (OLP), over-voltage protection (OVP), and brownout protection.

The HFC0502 is available in an SOIC8-7A package.

FEATURES

- Fixed Frequency, Current Mode Control, and Internal Slope Compensation
- Frequency Foldback Down to 25kHz at Light Loads
- Burst Mode for Low Standby Power Consumption, Meets EuP Lot 6 Standards
- Frequency Jittering (f_{JITTER}) for Reduced Electromagnetic Interference (EMI)
- Compatible with DC and AC Inputs
- Adjustable Over-Power Compensation (OPC)
- Internal High-Voltage Current Source
- V_{CC} Under-Voltage Lockout (UVLO) Protection with Hysteresis
- Brownout Protection via the HV Pin
- Configurable Soft Start (SS)
- Overload Protection (OLP) with Configurable Delay
- Short-Circuit Protection (SCP)
- Latch-Off Protections:
  - V_{CC} Over-Voltage Protection (OVP)
  - External OVP or Over-Temperature Protection (OTP) via the TIMER Pin
- Thermal Shutdown with Auto-Restart and Hysteresis
- Available in an SOIC8-7A Package

APPLICATIONS

- AC/DC Powered Appliances
- AC/DC Adapters for Notebooks Computers, Tablets, and Smartphones
- Offline Battery Chargers
- Liquid Crystal Display (LCD) Televisions and Monitors

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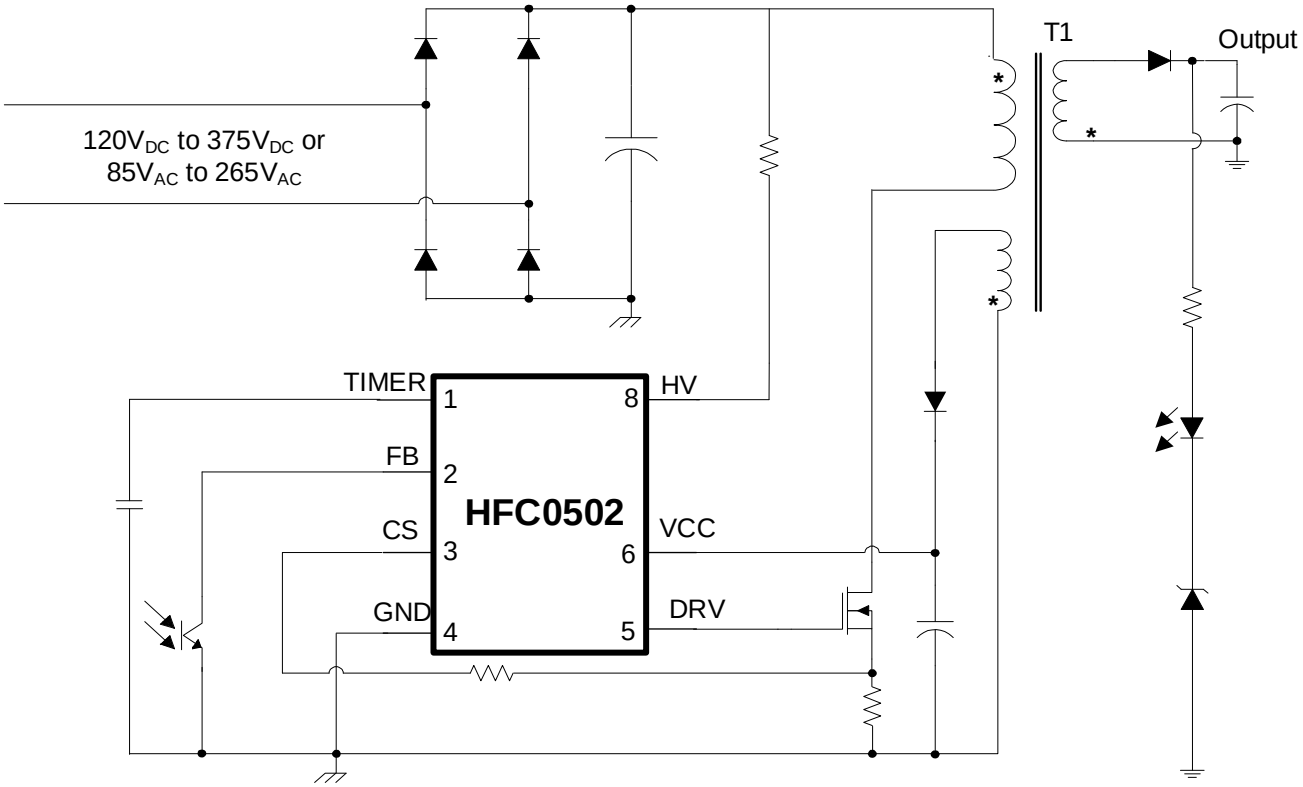
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
HFC0502GS	SOIC8-7A	*See Below*	2

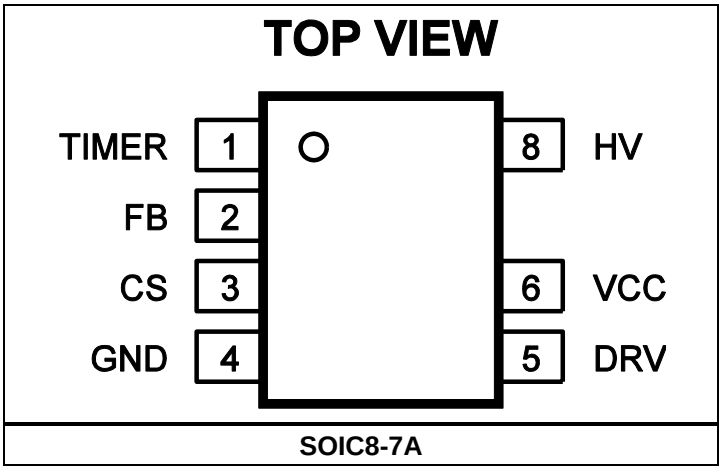
* For Tape & Reel, add suffix -Z (e.g. HFC0502GS-Z).

TOP MARKING

HFC0502
LLLLLLLL
MPSYWW

HFC0502: Part number
LLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code

PACKAGE REFERENCE



SOIC8-7A

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PIN FUNCTIONS

Pin #	Name	Description
1	TIMER	**Timer.** The TIMER pin provides overload protection (OLP) and brownout protection with soft start (SS), frequency jittering (f_{JITTER}), and the timer functions. Pull TIMER low to turn the controller off.
2	FB	**Feedback.** Use a pull-down opto-coupler to control the output regulation.
3	CS	**Current sense.** The CS pin senses the primary-side current during current-mode control for over-power compensation (OPC) adjustment.
4	GND	**Ground.**
5	DRV	**Driver signal output.**
6	VCC	**Power supply.**
8	HV	**High-voltage current source.** The HV pin is a high-voltage current source that includes a brownout function.

ABSOLUTE MAXIMUM RATINGS (1)

HV .....-0.7V to +700V
VCC, VDRV to GND .....-0.3V to +30V
FB, TIMER, CS to GND .....-0.3V to +7V
Continuous power dissipation (T_A = 25°C) (2)…….
……1.3W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -60°C to +150°C

ESD Ratings

Human body model (HBM)
DRV 3.5kV
HV……1.8kV
All other pins 4kV
Charged device model (CDM)
All pins 2kV
ESD capability for machine model
All pins 400V

Recommended Operation Conditions (3)

Operating junction temp (T_J).... -40°C to +125°C
Operating V_{CC} range .....9V to 24V

Thermal Resistance (4) θ_{JA} θ_{JC}

	θ_{JA}	θ_{JC}	
SOIC8-7A	96	45	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, which may cause the device to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERICS

V_{CC} = 18V, T_J = -40°C to 125°C, typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min (5)	Typ	Max (5)	Unit
Start-Up Current Source (HV)						
HV supply current	I_{HV}	V_{CC} = 12V, V_{HV} = 400V	1.5	2.8	5	mA
		V_{CC} = 12V, V_{HV} = 120V	1.5	2.7	5	mA
HV leakage current	I_{HV_LKG}	V_{HV} = 400V; V_{CC} increases to 18V, then decreases to 14V	1	16	25	µA
		V_{HV} = 200V; V_{CC} increases to 18V, then decreases to 14V	1	13	22	µA
Breakdown voltage	V_{BR}	T_J = 25°C	700	790		V
Supply Voltage (V_{CC}) Management						
V_{CC} rising threshold (current source turns off)	$V_{CC_RISING_OFF}$		12.5	15.5	18	V
V_{CC} falling threshold (SS is initiated)	$V_{CC_FALLING_SS}$	SS is initiated once V_{HV} > V_{HV_SU}	10.5	12	13	V
V_{CC} brown-in detection hysteresis	$V_{CC_BI_HYS}$	$V_{CC_RISING_OFF}$ - $V_{CC_FALLING_SS}$	1.35	3.5		V
V_{CC} falling threshold (current source turns on)	$V_{CC_FALLING_ON}$		7.3	8.5	9.6	V
V_{CC} under-voltage lockout (UVLO) hysteresis	$V_{CC_UVLO_HYS}$	$V_{CC_RISING_OFF}$ - $V_{CC_FALLING_ON}$	5	7		V
V_{CC} recharge threshold during protections	V_{CC_PRO}	If any protection with auto-restart is triggered	4.9	5.5	6.2	V
V_{CC} latch threshold (latch-off phase is complete)	V_{CC_LATCH}			2.5		V
Internal IC consumption	I_{CC}	V_{FB} = 2V, C_L = 1nF, V_{CC} = 12V	1.1	1.8	2.7	mA
Internal IC consumption during latch-off phase	I_{CC_LATCH}	V_{CC} = $V_{CC_RISING_OFF}$ - 1V, T_J = 25°C	520	700	880	µA
V_{CC} over-voltage protection threshold (OVP)	V_{CC_OVP}		24	26.5	28.5	V
OVP blanking time	t_{OVP}			60		µs
Brownout						
HV start-up threshold	V_{HV_SU}	V_{HV} increasing, T_J = 25°C	95	107	119	V
HV shutdown threshold	V_{HV_SD}	V_{HV} decreasing, T_J = 25°C	86	97	110	V
Brownout hysteresis	ΔV_{HV}	T_J = 25°C	7.5	10	12.5	V
HV line cycle dropout timer	t_{HV}	C_{TIMER} = 47nF	40			ms
Switching Frequency (f_{SW})						
Switching frequency	f_{SW}	V_{FB} > 1.85V, T_J = 25°C	62	65	68	kHz
Frequency jittering amplitude	Δf_{JITTER}	V_{FB} > 1.85V, T_J = 25°C	±4.7	±6.5	±8.3	% of f_{SW}
Frequency jittering entry	V_{FB_JITTER}				1.95	V
Frequency jittering modulation period	t_{JITTER}	C_{TIMER} = 47nF		3.7		ms

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ELECTRICAL CHARACTERICS *(continued)*

V_{CC} = 18V, T_J = -40°C to 125°C, typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min (5)	Typ	Max (5)	Unit
Current Sense						
Current limit voltage reference	V_{ILIMIT}		0.92	1	1.08	V
Short-circuit protection (SCP) threshold	V_{SCP}		1.3	1.47	1.63	V
Current limit point during frequency foldback	V_{FOLD}	V_{FB} = 1.85V	0.63	0.68	0.73	V
Current limit point during burst mode entry	$V_{ILIM_BURST_ENTRY}$	V_{FB} = 0.7V, entering burst mode		0.11		V
Current limit point during burst mode exit	$V_{ILIM_BURST_EXIT}$	V_{FB} = 0.8V, exiting burst mode		0.15		V
Leading edge blanking time for V_{ILIMIT}	t_{LEB1}			350		ns
Leading edge blanking time for V_{SCP}	t_{LEB2}			270		ns
Compensation ramp slope	S_{RAMP}		18	25	32	mV/μs
Feedback (FB)						
FB internal pull-up resistor	R_{FB}	T_J = 25°C	12	13.5	15	kΩ
FB internal pull-up voltage	V_{DD}			4.3		V
V_{FB} to internal current setpoint division ratio	K_{FB1}	V_{FB} = 2V	2.55	2.8	3.05	
	K_{FB2}	V_{FB} = 3V	2.8	3.1	3.4	
V_{FB} falling threshold (burst mode entry)	$V_{FB_FALLING_BURST}$	Entering burst mode	0.63	0.7	0.77	V
V_{FB} rising threshold (burst mode exit)	$V_{FB_RISING_BURST}$	Exiting burst mode	0.72	0.8	0.88	V
Overload Protection (OLP)						
OLP entry voltage	V_{OLP}	The IC enters OLP after t_{OLP}		3.7		V
OLP entry delay	t_{OLP}	C_{TIMER} = 47nF, V_{FB} increasing to reach the OLP point	40			ms
Over-Power Compensation (OPC)						
V_{HV} to I_{OPC} ratio	K_{OPC}			0.45		μA/V
OCP current	I_{OPC}	V_{HV} = 120V, V_{FB} = 2.5V		0		μA
		V_{HV} = 155V, V_{FB} = 2.5V		13		
		V_{HV} = 310V, V_{FB} = 2.5V		85		
		V_{HV} = 380V, V_{FB} = 2.5V, T_J = 25°C	90	119	148	
V_{FB} below which compensation is fully removed	V_{OPC_OFF}	OPC compensation	0.55			V
V_{FB} above which compensation is fully applied	V_{OPC_ON}	No OPC opmensation			2.2	V
Frequency Foldback						
V_{FB} threshold during frequency foldback entry	V_{FB_FOLD}	Entering frequency foldback		1.8		V
Minimum f_{SW}	f_{SW_MIN}	T_J = 25°C	21	25	30	kHz
V_{FB} threshold during frequency foldback exit	$V_{FB_FF_EXIT}$	Exiting frequency foldback		1		V

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ELECTRICAL CHARACTERICS *(continued)*

V_{CC} = 18V, T_J = -40°C to 125°C, typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min (5)	Typ	Max (5)	Unit
Latch-Off Input (TIMER)						
Latch-off threshold	V_{TIMER_LATCH}		0.7	1	1.3	V
Blanking time during latch detection	t_{LATCH}			12		µs
Driver Voltage (V_{DRV})						
DRV high voltage	V_{HIGH}	C_L = 1nF, V_{CC} = 12V		10.3		V
DRV clamped voltage	V_{CLAMP}	C_L = 1nF, V_{CC} = 24V		13.4		V
DRV low voltage	V_{LOW}	C_L = 1nF, V_{CC} = 24V		16		mV
DRV rise time	t_{RISE}	C_L = 1nF, V_{CC} = 16V		13		ns
DRV fall time	t_{FALL}	C_L = 1nF, V_{CC} = 16V		23		ns
DRV pull-up resistance	R_{DRV_PU}	C_L = 1nF, V_{CC} = 16V		8		Ω
DRV pull-down resistance	R_{DRV_PD}	C_L = 1nF, V_{CC} = 16V		10		Ω
Thermal Shutdown						
Thermal shutdown (6)	T_{SD}			150		°C
Thermal shutdown hysteresis (6)	T_{SD_HYS}			25		°C

Notes:

5) Guaranteed by characterization.
6) Guaranteed by design.

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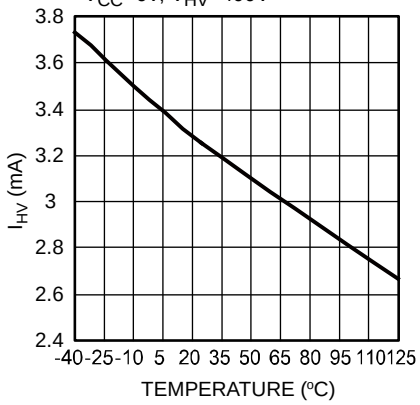
TYPICAL CHARACTERISTICS

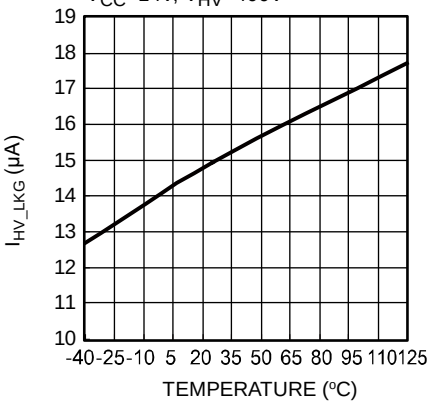
HV Supply Current vs. Temperature

V_{CC}=6V, V_{HV}=400V

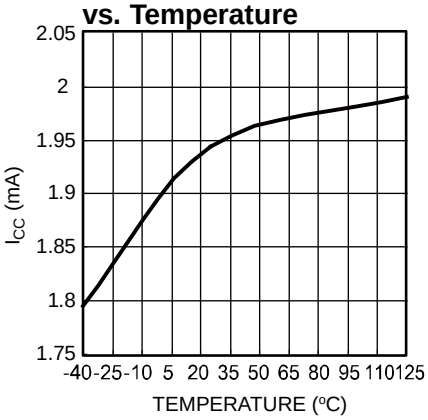


HV Leakage Current vs. Temperature

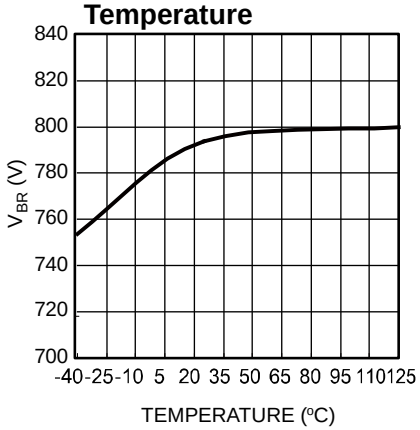
V_{CC}=14V, V_{HV}=400V



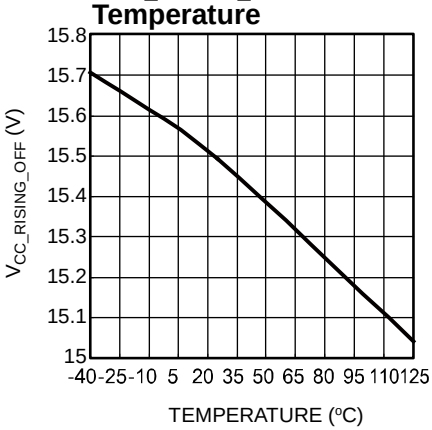
Internal IC Consumption vs. Temperature



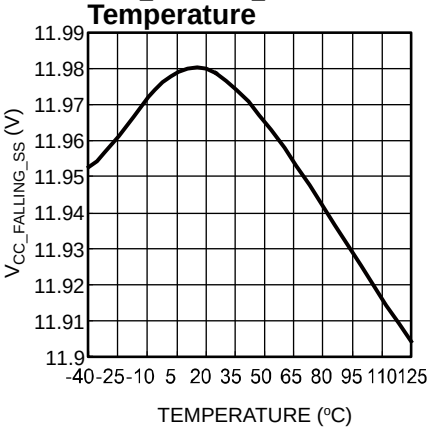
Breakdown Voltage vs. Temperature



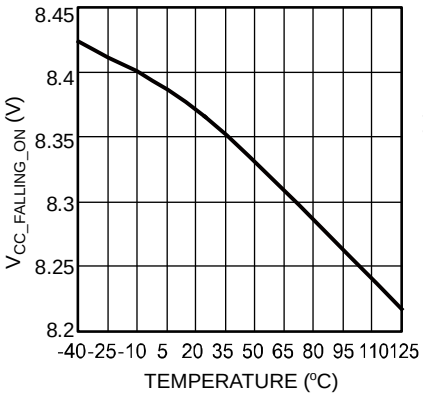
$V_{CC_RISING_OFF}$ vs. Temperature



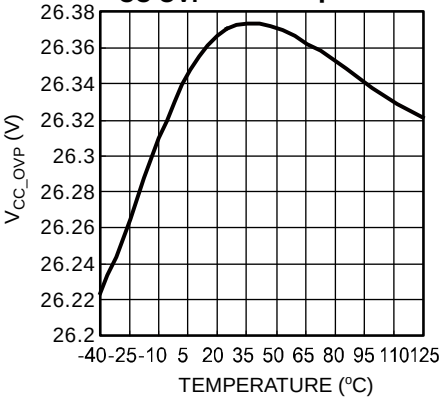
$V_{CC_FALLING_SS}$ vs. Temperature



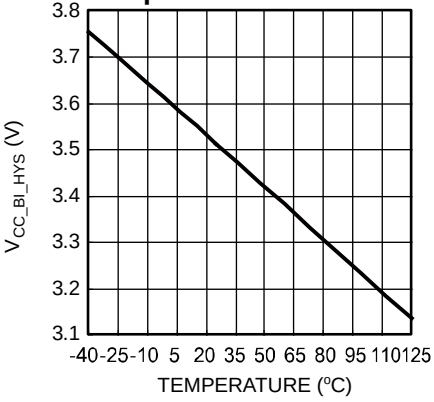
$V_{CC_FALLING_ON}$ vs. Temperature



$V_{CC\ OVP}$ vs. Temperature



V_{CC} Brown-In Detection Hysteresis vs. Temperature



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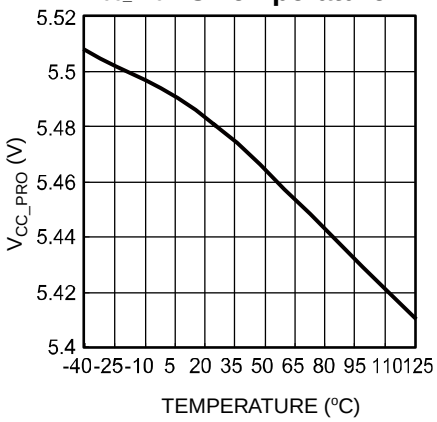
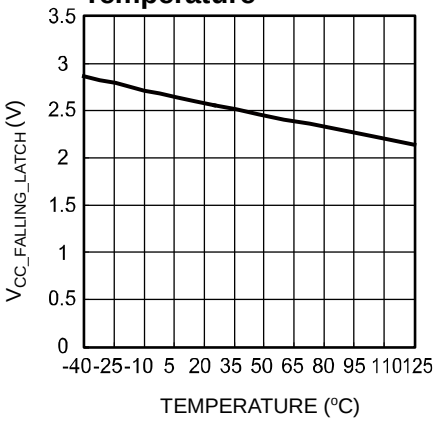
TYPICAL CHARACTERISTICS *(continued)*

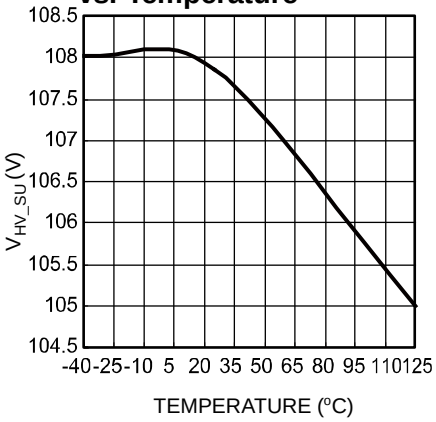
V_{CC_PRO} vs.Temperature



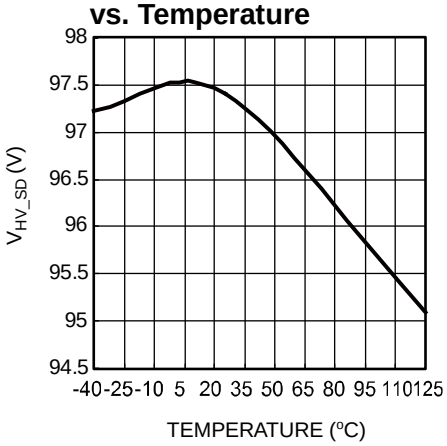
$V_{CC_FALLING_LATCH}$ vs. Temperature



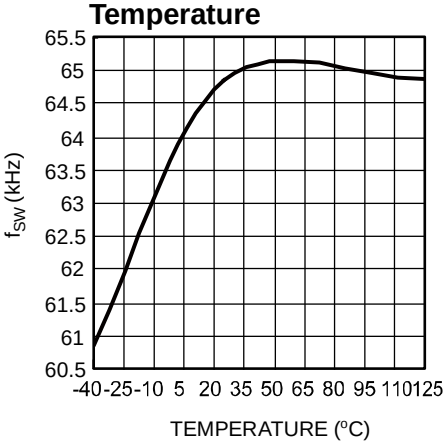
HV Start-Up Threshold vs. Temperature



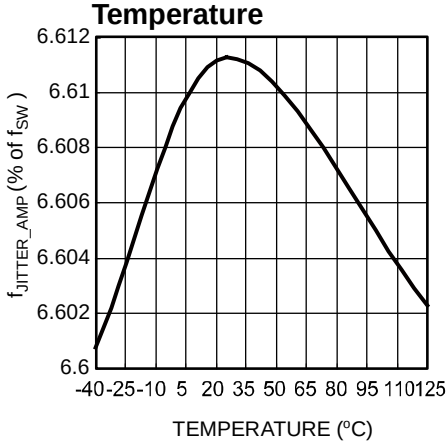
HV Shutdown Threshold vs. Temperature



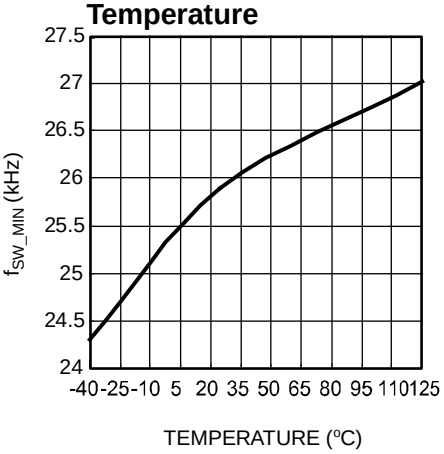
Switching Frequency vs. Temperature



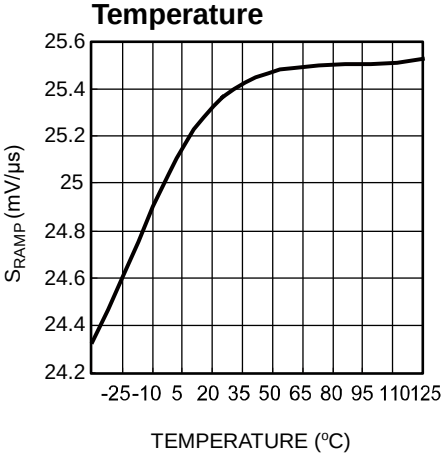
Frequency Jittering Amplitude vs. Temperature



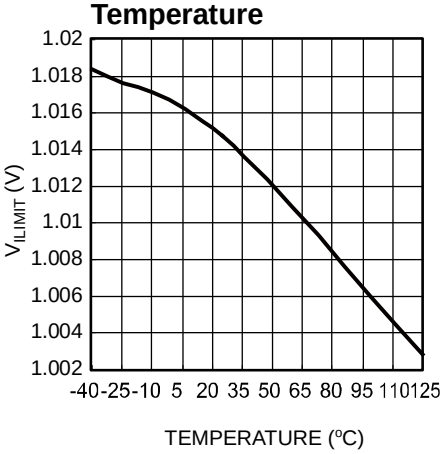
Minimum Switching Frequency vs. Temperature



Compensation Ramp Slope vs. Temperature



Current Limit Point vs. Temperature



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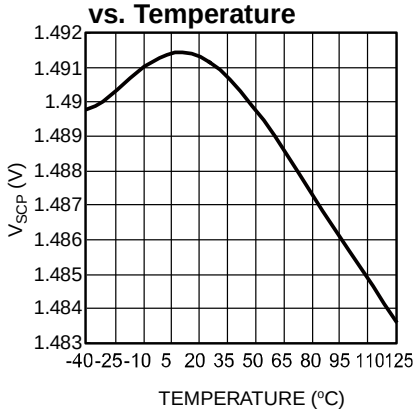
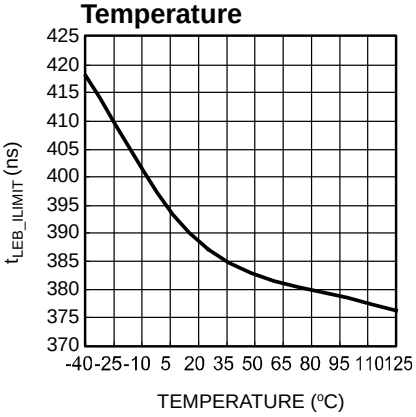
TYPICAL CHARACTERISTICS *(continued)*

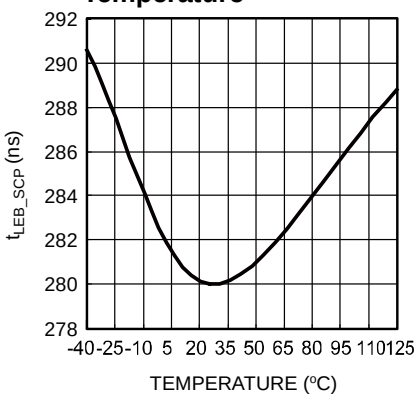
Short Circuit Protection vs. Temperature



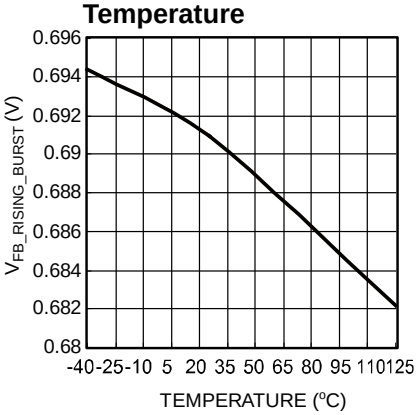
Leading Edge Blanking Time for V_{ILIMIT} vs. Temperature



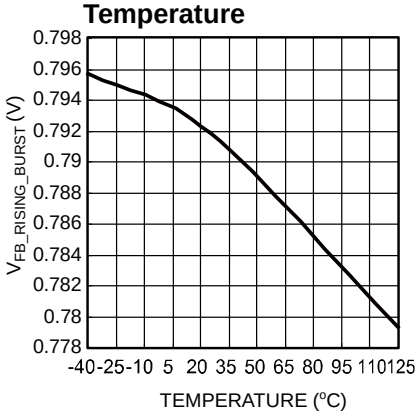
Leading Edge Blanking Time for V_{SCP} vs. Temperature



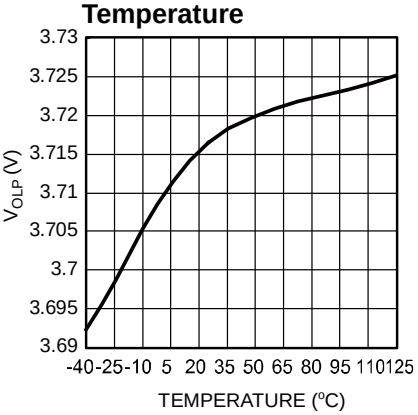
V_{FB} Falling during Burst Mode Entry vs. Temperature



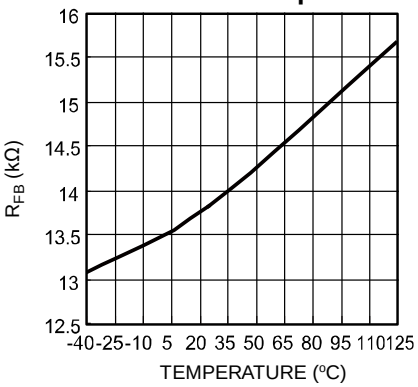
V_{FB} Rising during Burst Mode Exit vs. Temperature



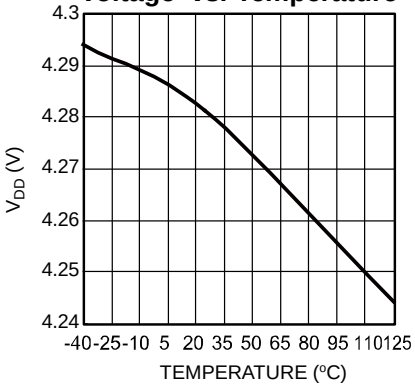
V_{FB} during OLP Entry after Blanking Time vs. Temperature



FB Internal Pull-Up Resistor vs. Temperature



FB Internal Pull-Up Voltage vs. Temperature



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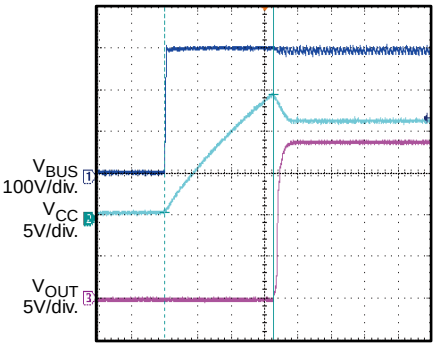
TYPICAL PERFORMANCE CHARACTERISICS

V_{IN} = 230V_{AC}, V_{OUT} = 19V, I_{OUT} = 2.35A, unless otherwise noted.

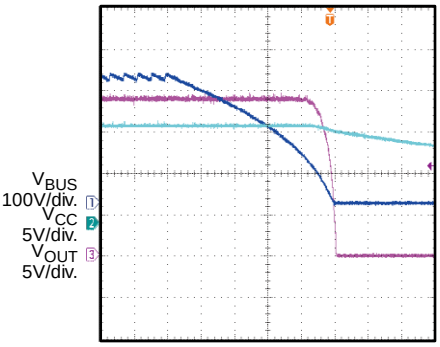
Start-Up

230V_{AC} full load

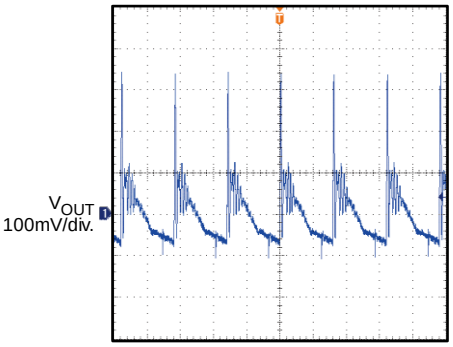


Shutdown

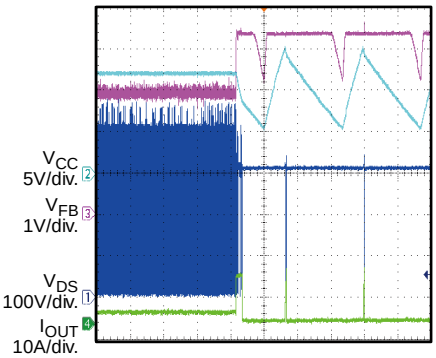
230V_{AC} full load



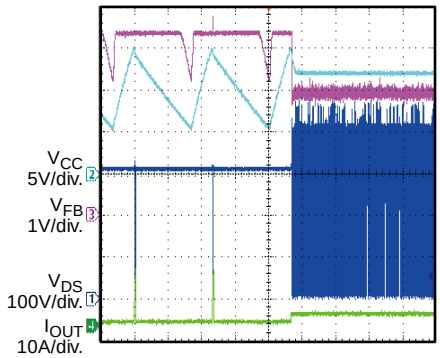
Output Voltage Ripple



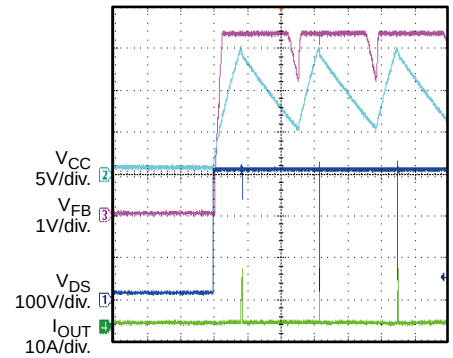
SCP Entry



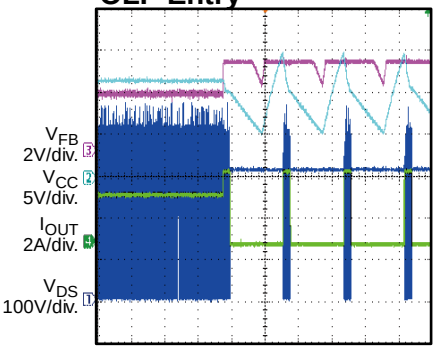
SCP Recovery



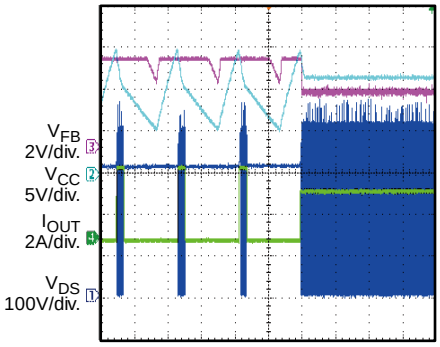
Start-Up through SCP



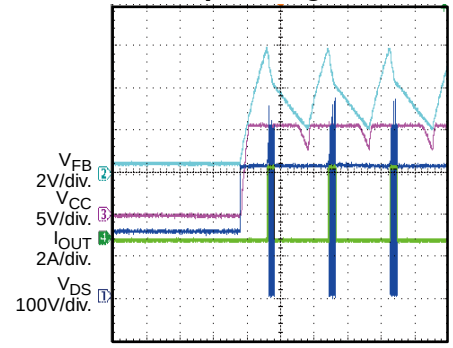
OLP Entry



OLP Rescovery



Start-Up through OLP



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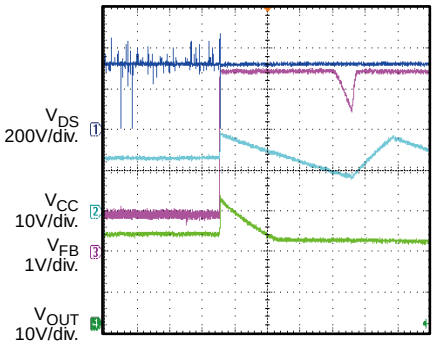
TYPICAL PERFORMANCE CHARACTERISICS *(continued)*

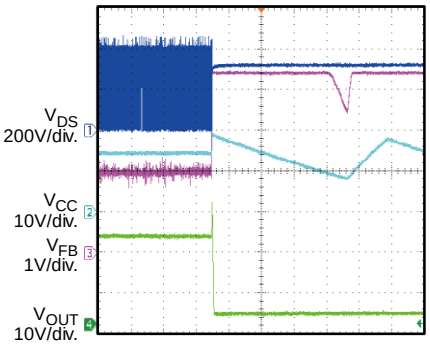
V_{IN} = 230V_{AC}, V_{OUT} = 19V, I_{OUT} = 2.35A, unless otherwise noted.

OVP
No load



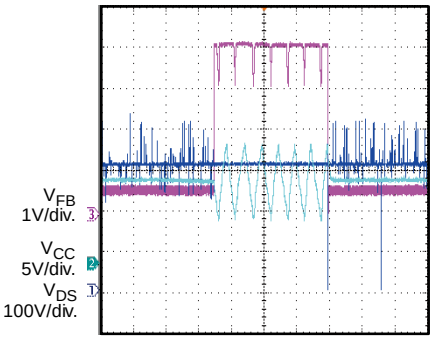
200ms/div.

OVP
Full load



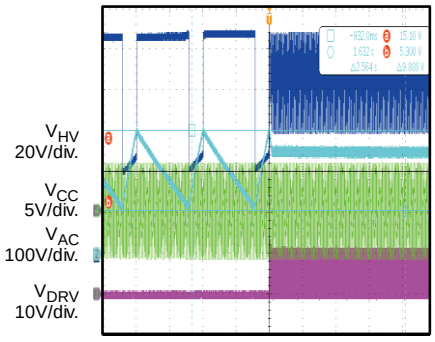
200ms/div.

OTP
No load



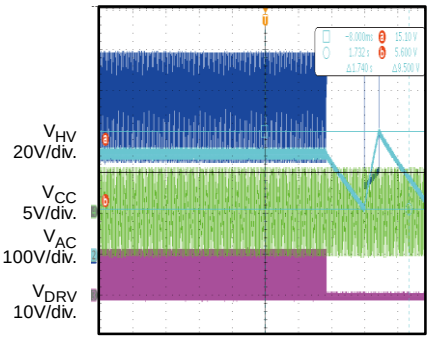
2s/div.

Brown-In



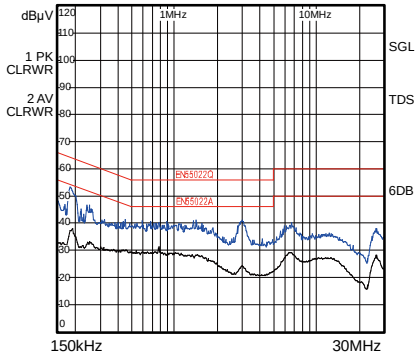
400ms/div.

Brownout

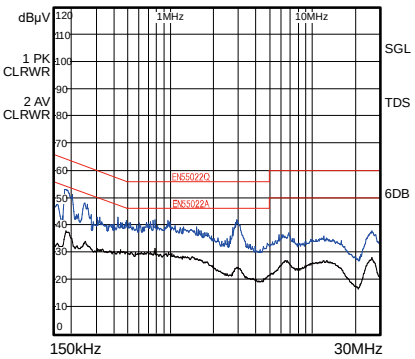


400ms/div.

Conducted EMI
230V_{AC}, L wire



Conducted EMI
230V_{AC}, N wire



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TYPICAL PERFORMANCE CHARACTERISICS *(continued)*

V_{IN} = 230V_{AC}, V_{OUT} = 19V, I_{OUT} = 2.35A, unless otherwise noted.

Table 1: No-Load Power Consumption

V_{IN} (V_{AC}/Hz)	85/60	115/60	230/50	265/50
P_{IN} (mW)	73.63	67.31	72.37	78.86

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FUNCTIONAL BLOCK DIAGRAM

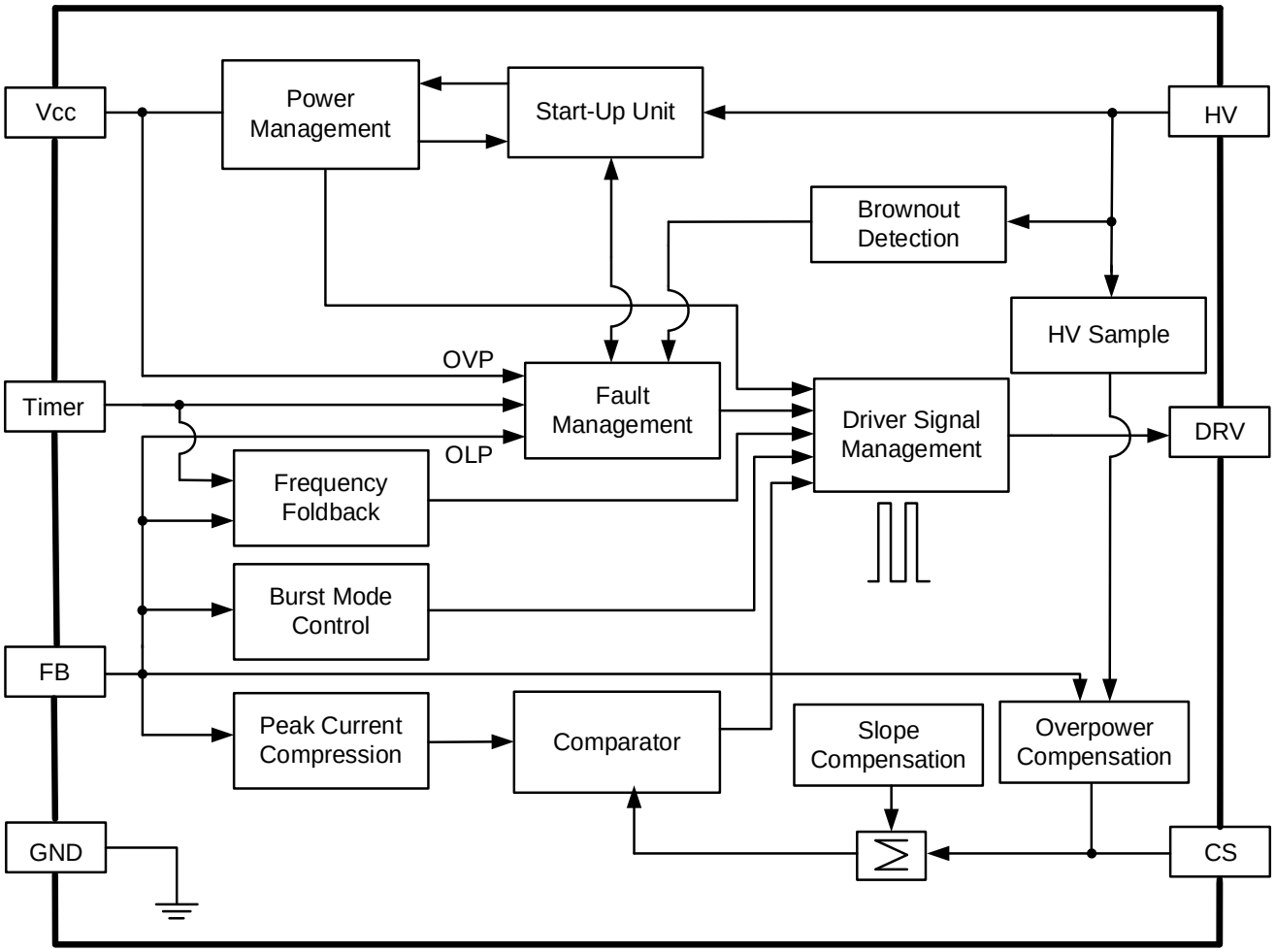

Figure 1: Functional Block Diagram

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OPERATION

The HFC0502 is a fixed-frequency, current-mode controller with internal slope compensation incorporates all the necessary functions to build a reliable switch-mode power supply. At light loads, the controller maintains the peak current (I_{PEAK}) at its present value and reduces the switching frequency (f_{SW}) to 25kHz to minimize switching losses. If the output voltage (V_{OUT}) drops below a set level, then the controller enters burst mode. Frequency jittering (f_{JITTER}) reduces electromagnetic interference (EMI).

The controller requires a minimal number of readily available, standard external components.

Fixed-Frequency with Frequency Jittering

Frequency jittering (f_{JITTER}) reduces EMI by dissipating the energy across the f_{JITTER} range. Figure 2 shows a f_{JITTER} circuit.

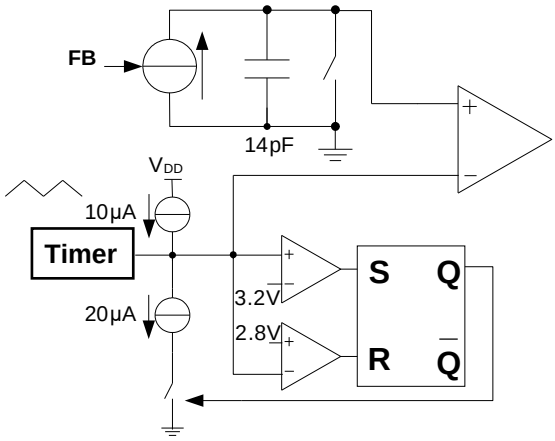

Figure 2: Frequency Jittering Circuit

A controlled current source (fixed 2.72μA when V_{FB} = 2V) charges the internal 14pF capacitor. Comparing the capacitor voltage to the TIMER pin voltage (V_{TIMER}) determines f_{SW}. f_{SW} can be calculated with Equation (1):

$$f_{SW} = \frac{1}{14pF \times V_{TIMER} / 2.72\mu A + 0.2\mu s} \quad (1)$$

f_{JITTER} is set by varying V_{TIMER} between 3.2V and 2.8V. The f_{JITTER} modulation period (t_{JITTER}) can be calculated with Equation (2):

$$t_{JITTER} = 2 \times \frac{C_{TIMER} \times (3.2V - 2.8V)}{10\mu A} \quad (2)$$

Figure 3 shows the f_{JITTER} function.

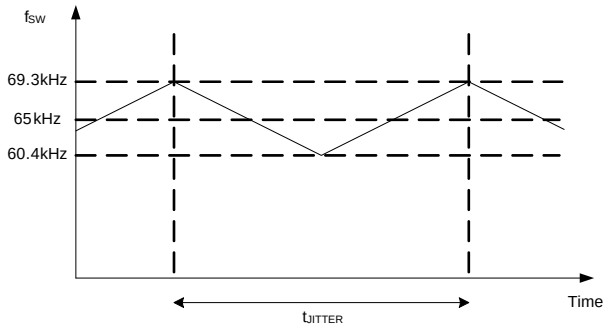

Figure 3: Frequency Jittering

Frequency Foldback

Frequency foldback improves efficiency under light-load conditions.

If the load decreases to a set level (1V < V_{FB} < 1.8V), then the controller maintains I_{PEAK} at its present level (as measured by the CS pin) (typically 0.7V), and f_{SW} drops to 25kHz. This reduces switching loss. If the load continues to decrease, then I_{PEAK} decreases with the 25kHz fixed frequency to reduce audible noise. Figure 4 shows f_{SW} vs. the feedback voltage (V_{FB}), as well as I_{PEAK} vs. V_{FB}.

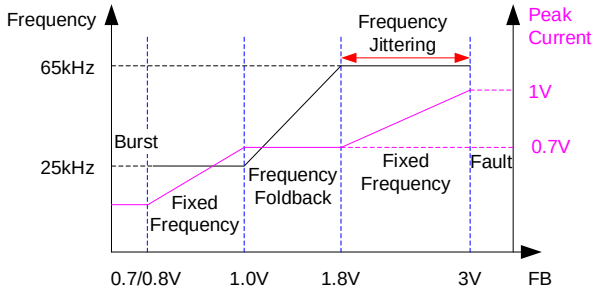

Figure 4: f_{SW} vs. V_{FB} and I_{PEAK} vs. V_{FB}

Current Mode Control and Slope Compensation

V_{FB} controls the primary I_{PEAK}. If I_{PEAK} reaches the level determined by V_{FB}, then the driver signal output (DRV) turns off. Internal slope compensation (25mV/μs) allows the controller to operate in continuous conduction mode (CCM), with a wide input voltage (V_{IN}) range. Internal compensation reduces sub-harmonic oscillations above 50% of the duty cycle.

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High-Voltage Start-Up Current Source and Brownout Detection

During start-up, the internal high-voltage current source (HV) supplies power to the controller. The IC detects the HV pin voltage (V_{HV}) once V_{CC} reaches its rising threshold as the current source shuts down ($V_{CC_RISING_OFF}$).

If V_{HV} exceeds the HV start-up threshold (V_{HV_SU}) before V_{CC} drops to its falling threshold to initiate a SS ($V_{CC_FALLING_SS}$) (12V), then the controller starts up. If V_{HV} does not exceed V_{HV_SU}, then a brownout occurs and DRV is pulled low. If V_{CC} drops to its falling threshold when a protection is triggered (V_{CC_PRO}) (5.3V), then HV turns on and recharges V_{CC}.

After start-up, the auxiliary transformer winding supplies the IC. The IC stops switching and the current source turns on again once V_{CC} drops below its threshold as the current source starts up ($V_{CC_FALLING_ON}$).

Figure 5 shows V_{CC} under-voltage lockout (UVLO).

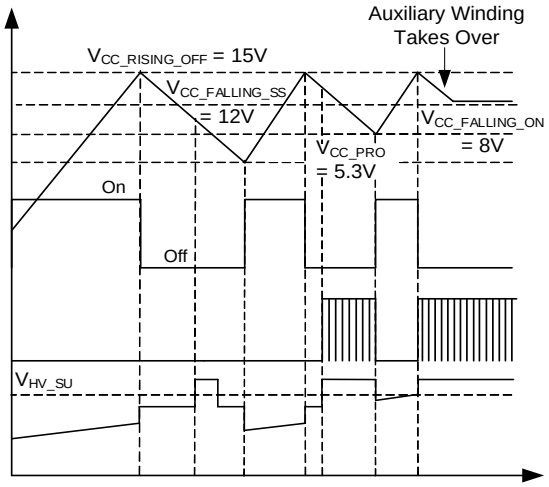

Figure 5: V_{CC} UVLO

If a fault protection is triggered (e.g. overload protection [OLP], short-circuit protection [SCP], brownout, or over-temperature protection [OTP]), then the lower V_{CC} UVLO threshold drops from 8V to 5.3V.

Soft Start (SS)

The HFC0502 features configurable external soft start (SS) via the TIMER capacitor (C_{TIMER}). C_{TIMER} can be charged between 1V and 1.75V via 25% of the normal charge current. The I_{PEAK} limit (I_{LIMIT_PEAK}) increases from 0.25V to 1V slowly, which also increases f_{SW} slowly. Figure 6 shows the soft-start function.

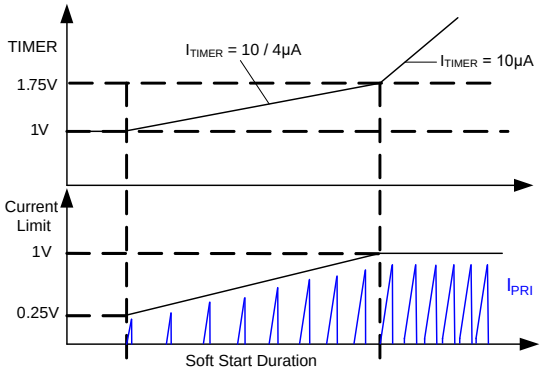

Figure 6: Soft Start

C_{TIMER} determines the soft-start time (t_{SS}). t_{SS} can be calculated with Equation (3).

$$t_{SS} = \frac{C_{TIMER} \times (1.75V - 1V)}{10/4\mu A} \quad (3)$$

Burst Mode

The HFC0502 employs burst mode to minimize power dissipation under no-load or light-load conditions. As the load decreases, V_{FB} decreases. If V_{FB} drops below its falling threshold ($V_{FB_FALLING_BURST}$) (0.7V), then the IC enters burst mode. The IC stops switching and V_{OUT} drops, which causes V_{FB} to increase. If V_{FB} exceeds its rising threshold ($V_{FB_RISING_BURST}$) (0.8V), the IC resumes starts switching. Burst mode alternately enables and disables MOSFET switching, which reduces switching losses at no load or light loads.

Adjustable Over-Power Compensation (OPC)

An offset current proportional to V_{IN} is added to current-sense voltage (V_{CS}). The amount of compensation can be adjusted by choosing the resistance in series with CS. This allows for a more accurate output power limit across the entire total V_{IN} range. Figure 7 shows the compensation current vs. V_{FB} and V_{HV}.

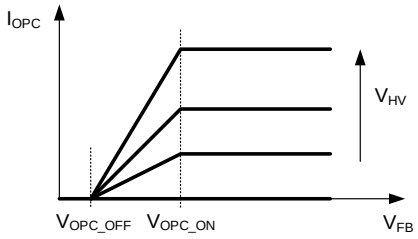

Figure 7: Compensation Current vs. V_{FB} and V_{HV}

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Figure 8 shows the compensation current vs. V_{HV}.

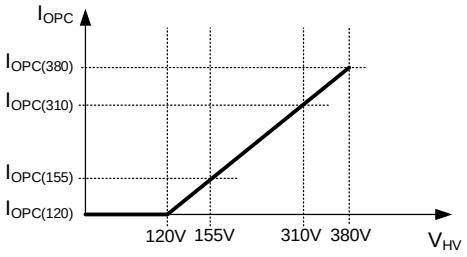

Figure 8: Compensation Current vs. HV Voltage

Over-Load Protection via the TIMER Pin

If f_{SW} is fixed in a flyback converter, then the maximum V_{OUT} should be limited by I_{PEAK}. If the output power exceeds the power limit, then V_{OUT} drops below the set value. This reduces the current flowing through the optocoupler, which pulls V_{FB} high.

If V_{FB} exceeds the OLP entry voltage (V_{OLP}) (3.7V), then the OLP timer (t_{OLP}) starts. This is considered an error flag. If the error flag is removed during t_{OLP}, then the timer resets. t_{OLP} counting is implemented through the TIMER pin. The counter increments once V_{TIMER} reaches 3.2V. If the counter reaches 18, then OLP is triggered. t_{OLP} avoids triggering OLP during the start-up and short load transients. Figure 9 shows the OLP function.

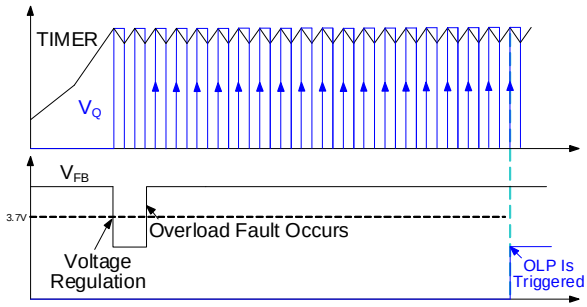

Figure 9: Overload Protection

Brownout Protection via the TIMER Pin

The brownout protection block is similar to the OLP block. If V_{HV} drops below V_{HV_SD} (98V), then the brownout timer (t_{BO}) starts counting. This is considered as an error flag. Once V_{HV} exceeds the V_{HV} shutdown threshold (V_{HV_SD}), the timer resets. If the t_{BO} counter reaches 18, brownout protection is triggered and the IC stops switching.

Short-Circuit Protection (SCP)

The HFC0502 features short-circuit protection (SCP). If V_{CS} reaches the SCP threshold (V_{SCP}) (1.45V) after a reduced leading-edge blanking time (t_{LEB2}), then SCP is triggered. The IC initiates an SS and resumes normal operation once the short-circuit is removed.

Thermal Shutdown

Thermal shutdown protects the IC from operating at exceedingly high temperatures by internally monitoring the junction temperature (T_J). If T_J exceeds the thermal shutdown threshold (typically 150°C), then the controller shuts down. Once T_J drops below 125°C, then the IC initiates a SS to resume normal operation. During thermal shutdown, the V_{CC} UVLO falling threshold drops from 8V to 5.3V.

V_{CC} Over-Voltage Protection (OVP)

If V_{CC} exceeds the over-voltage protection (OVP) threshold (V_{OVP}) (26.5V) for 60µs, then OVP is triggered**.** The controller latches until V_{CC} drops below the V_{CC} latch threshold (V_{CC_LATCH}) (2.5V). (e.g. when the user unplugs the power supply from the main input and then plugs it in again). OVP typically occurs when the optocoupler fails, which results in the loss of V_{OUT} regulation.

TIMER Latch-Off Protection for OVP and OTP

Pull TIMER below 1V for 12µs to latch off the IC. This function can be used for external OVP and OTP.

Clamped Driver

If V_{CC} exceeds 16V, then DRV is clamped at 13.4V. This allows the use of any standard MOSFET.

Leading-Edge Blanking

An internal leading-edge blanking (LEB) unit with two LEB times (t_{LEB1} and t_{LEB2}) is connected between the CS pin and the current comparator to avoid premature switching pulse termination due to parasitic capacitance. During the blanking time (t_{BLANK}), the current comparator is disabled. This means that the current comparator cannot turn the external MOSFET off.

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Figure 10 shows the LEB functions.

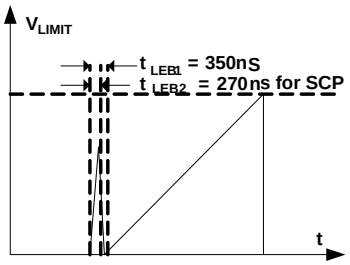

Figure 10: Leading-Edge Blanking

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APPLICATION INFORMATION

Selecting the VCC Capacitor

The VCC capacitor (C_{VCC}) is charged by the HV pin once V_{IN} is applied. V_{CC} should exceed $V_{CC_FALLING_ON}$ until V_{OUT} is high enough for the auxiliary winding to supply VCC. If V_{OUT} is not high enough for the auxiliary winding to supply VCC, then the IC stops switching and V_{OUT} cannot be set normally. For most applications, choose a C_{VCC} that exceeds 10μF. C_{VCC} can be estimated with Equation (4):

$$C_{VCC} > \frac{I_{CC} \times t_{RISE}}{V_{CC_RISING_OFF} - V_{CC_FALLING_ON}} \quad (4)$$

Where I_{CC} is the internal IC consumption current and t_{RISE} is the V_{OUT} rise time.

Figure 11 shows the start-up circuit.

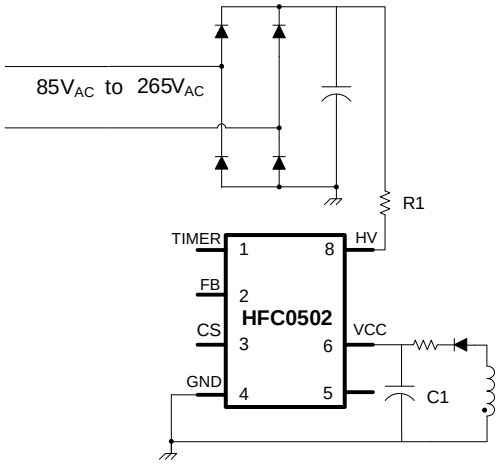

Figure 11: Start-Up Circuit

R1 and C1 determine the system's start-up delay (t_{DELAY_SU}). A larger R1 or C1 increases t_{DELAY_SU}.

A higher R1 decreases the internal HV current (I_{HV}), especially at low-inputs. Ensure that I_{HV} exceeds I_{CC}. It is recommended that R1 be between 20kΩ and 80kΩ.

Primary-Side Inductor Design

The If the duty cycle exceeds 50%, then the HFC0502 can operate in CCM with internal slope compensation. Set a ratio of (K_P) the primary inductor ripple current (ΔI_L) and I_{PEAK} to $0 < K_P \leq 1$. For DCM, set K_P to 1.

Figure 12 shows the typical primary current waveform.

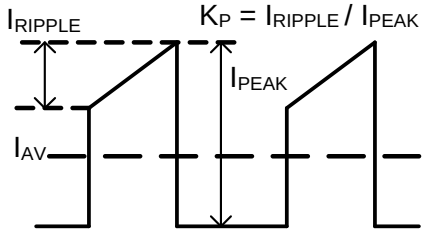

Figure 12: Typical Primary Current

A larger inductor creates a smaller K_P, which reduces RMS current, but increases transformer size. It is recommended that K_P be between 0.6 and 0.8 for the universal input range and between 0.8 to 1 for a 230V_{AC} input.

The input power (P_{IN}) at the minimum input can be estimated with Equation (5):

$$P_{IN} = \frac{V_{OUT} \times I_{OUT}}{\eta} \quad (5)$$

Where I_{OUT} is the rated output current, η is the estimated efficiency between 75% and 85%, depending on the V_{IN} range and output application.

The duty cycle (D) during CCM at the minimum V_{IN} can be estimated with Equation (6):

$$D = \frac{(V_{OUT} + V_F) \times N}{(V_{OUT} + V_F) \times N + V_{IN_MIN}} \quad (6)$$

Where V_F is the secondary diode's forward voltage, N is the transformer turn ratio, and V_{IN_MIN} is the minimum voltage on the bulk capacitor.

The MOSFET turn-on time (t_{ON}) can be calculated with Equation (7):

$$t_{ON} = D \times t_S \quad (7)$$

Where t_S is the f_{JITTER} dominant switching period.

t_S can be calculated with Equation (8):

$$\frac{1}{t_S} = f_{SW} = 65kHz \quad (8)$$

The average current (I_{AV}) can be calculated with Equation (9):

$$I_{AV} = \frac{P_{IN}}{V_{IN_MIN}} \quad (9)$$

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The peak current (I_{PEAK}) can be calculated with Equation (10):

$$I_{PEAK} = \frac{I_{AV}}{(1-\frac{K_P}{2})\times D} \quad (10)$$

The ripple current (I_{RIPPLE}) can be calculated with Equation (11):

$$I_{RIPPLE} = K_P \times I_{PEAK} \quad (11)$$

The valley current (I_{VALLEY}) can be calculated with Equation (12):

$$I_{VALLEY} = (1-K_P)\times I_{PEAK} \quad (12)$$

The magnetic inductance of the transformer (L_m) can be calculated with Equation (13):

$$L_m = \frac{V_{IN_MIN}\times t_{ON}}{I_{RIPPLE}} \quad (13)$$

Current-Sense Resistor

If the sensing resistor voltage (V_{SENSE}) and the slope compensation equal V_{PEAK}, then the comparator goes high to reset the reset/set (RS) flip-flop. DRV is pulled low to turn the MOSFET off. The maximum current limit (V_{LIMIT}) is 0.95V. The slope compensation (V_{SLOPE}) is about 25mV/µs. At full loads, V_{PEAK} should equal 0.95 x V_{LIMIT}. Then the V_{SENSE} can be calculated with Equation (14):

$$V_{SENSE} = 95\%\times V_{LIMIT} - V_{SLOPE}\times T_{on} \quad (14)$$

Figure 13 shows the I_{PEAK} comparator logic.

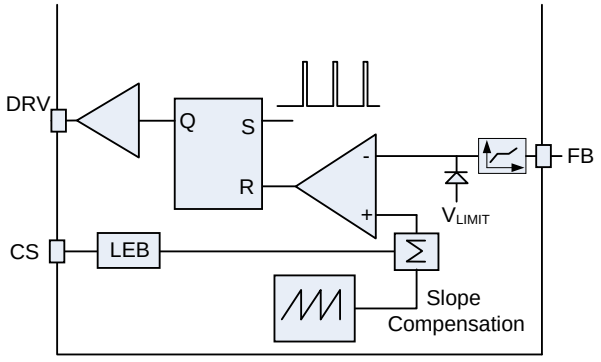

Figure 13: Peak Current Comparator Logic

Figure 14 shows the typical I_{PEAK} comparator waveform.

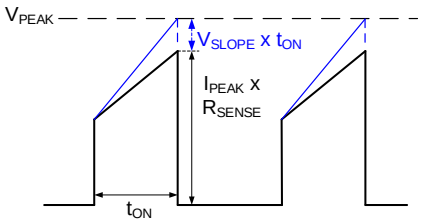

Figure 14: Peak Current Comparator Waveform

The sense resistor (R_{SENSE}) can be calculated with Equation (15):

$$R_{SENSE} = \frac{V_{SENSE}}{I_{PEAK}} \quad (15)$$

Choose and R_{SENSE} that has an appropriate power rating. The R_{SENSE} power loss can be calculated with Equation (16):

$$P_{SENSE} = \left[\left(\frac{I_{PEAK}+I_{VALLEY}}{2}\right)^2 + \frac{1}{12}(I_{PEAK}-I_{VALLEY})^2\right]\times D\times R_{SENSE} \quad (16)$$

Low-Pass Filter on CS

A small capacitor connected to CS via R_{SERIES} forms a low-pass filter for noise filtering as the MOSFET turns on and off (see Figure 15).

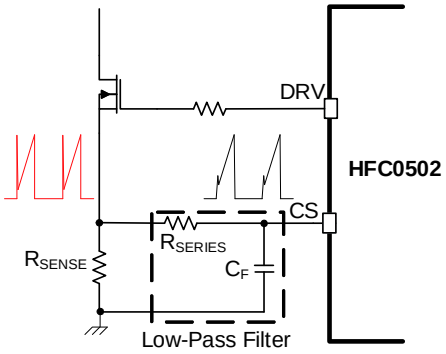

Figure 15: Low-Pass Filter on CS

The low-pass filter's R×C constant should not exceed 1/3 of the leading-edge blanking period for SCP (t_{LEB2}, 270ns, typical), otherwise the filtered sensed voltage cannot reach the SCP point (1.45V) to trigger SCP if an output short circuit occurs.

Over-Power Compensation (OPC)

The HFC0502 has an OPC function via the CS pin (OCP draws current from CS). OPC minimizes the OLP difference caused by different input voltages. The offset current is proportional to the input peak voltage sensed by HV. The CS compensation voltage (V_{COMP}) can be calculated with Equation (17):

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$$V_{COMP} = R_{SERIES} \times I_{OPC} \quad (17)$$

Where R_{SERIES} is the OCP resistor, I_{OPC} is the OPC current when V_{HV} is 310V, and V_{IN} is 220V_{AC}.

The compensation criteria is to have V_{FB} be similar to either the high line or low line under full-load conditions.

Frequency Jittering Period

f_{JITTER} is an effective method to reduce EMI by dissipating energy on the IC. The n_{th}-order harmonic noise bandwidth (B_{Tn}) can be calculated with Equation (18):

$$B_{Tn} = n \times (2 \times \Delta f_{JITTER} + f_{JITTER}) \quad (18)$$

Where Δf_{JITTER} is the f_{JITTER} amplitude.

If B_{Tn} exceeds the resolution bandwidth (RBW) of the spectrum analyzer, then the spectrum analyzer receives less noise energy. (7)

C_{TIMER} determines the f_{JITTER} period. A 10μA current source charges the capacitor. If V_{TIMER} reaches 3.2V, then another 10μA current source discharges C_{TIMER} to 2.8V. This charging and discharging cycle repeats.

Equation 2 on page 16 describes the f_{JITTER} period (t_{JITTER}) in theory. A smaller f_{JITTER} reduces EMI; however, the measurement bandwidth requires a larger f_{JITTER} for the spectrum analyzer's RBW to effectively reduce EMI. There is a trade-off between a smaller and larger f_{JITTER}. f_{JITTER} should be below the control loop gain crossover frequency to avoid disturbing V_{OUT} regulation.

Consider the practical application when selecting C_{TIMER}. Too large a capacitor may cause start-up failure at full loads due to a long t_{SS} (see Equation 3 on page 16). Too small a capacitor can cause a shortened timer period, and the timer capability may overload, which can cause logic problems. For most applications, an f_{JITTER} between 200Hz and 400Hz is sufficient.

Internal Ramp Compensation

When adopting peak current control, subharmonic oscillations can occur if the duty cycle exceeds 50% in CCM. The HFC0502 is equipped with internal ramp compensation to reduce subharmonic oscillations. R_{SENSE} can be estimated with Equation (20):

$$\alpha = \frac{\frac{D_{MAX} \times V_{IN_MIN}}{(1-D_{MAX}) \times L_m} \times R_{SENSE} - m_a}{\frac{V_{IN_MIN}}{L_m} \times R_{SENSE} + m_a} \quad (20)$$

Where m_a is the minimum internal slope value of the compensation ramp (18mV/μs), $\frac{V_{IN_MIN}}{L_m} \times R_{SENSE}$ is the primary-side slew rate, and $\frac{D_{MAX} \times V_{IN_MIN}}{(1-D_{MAX}) \times L_m} \times R_{SENSE}$ is the secondary-side equivalent voltage sensed by slew rate of the primary-side and equivalent secondary-side voltage sensed by the CS resistor (R_{CS}) respectively.

For stable operation, α should be below 1.

Design Example

Below is a design example of HFC0502 for power adapter applications.

Table 2: Design Example

V_{IN}	85V_{AC} to 265V_{AC}
V_{OUT}	19V
I_{OUT}	2.35A

Note:

7) The spectrum analyzer's RBW is 200kHz for frequencies below 150kHz, and 9kHz for frequencies between 150kHz to 30MHz).

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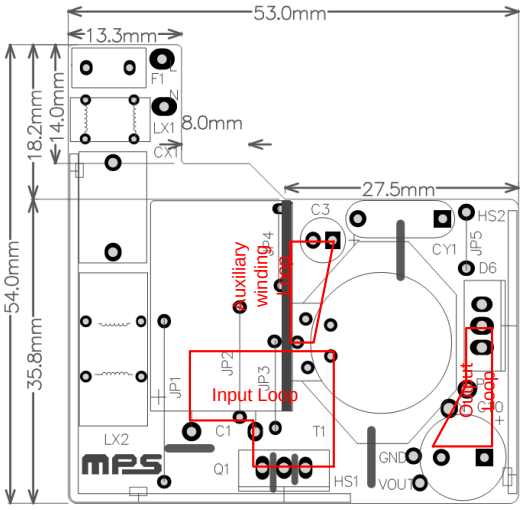
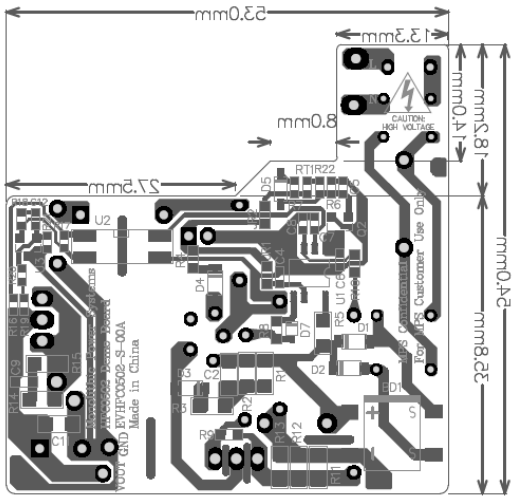
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. A well-designed layout can also reduce EMI and improve thermal performance. For the best performance, refer to Figure 16 and follow the guidelines below:

1. Minimize the power stage loop area, which includes the input loop (C1 to T1 to Q1 to R11/R12/R13 to C1), the auxiliary winding loop (T1 to D4 to R4 to C3 to T1), and the output loop (T1 to D6 to C10 to T1).
2. Separate the input loop ground and the control circuit. Connect either the input ground loop or the control circuit to C1. Do not connect both to C1.
3. Connect the Q1 heat sink to the primary ground plane to reduce EMI.
4. Place the control circuit decoupling capacitors (e.g. C_{FB}, C_{CS} and C_{VCC}) close to IC to decouple noise.



Top Layer



Bottom Layer

Figure 16: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUIT

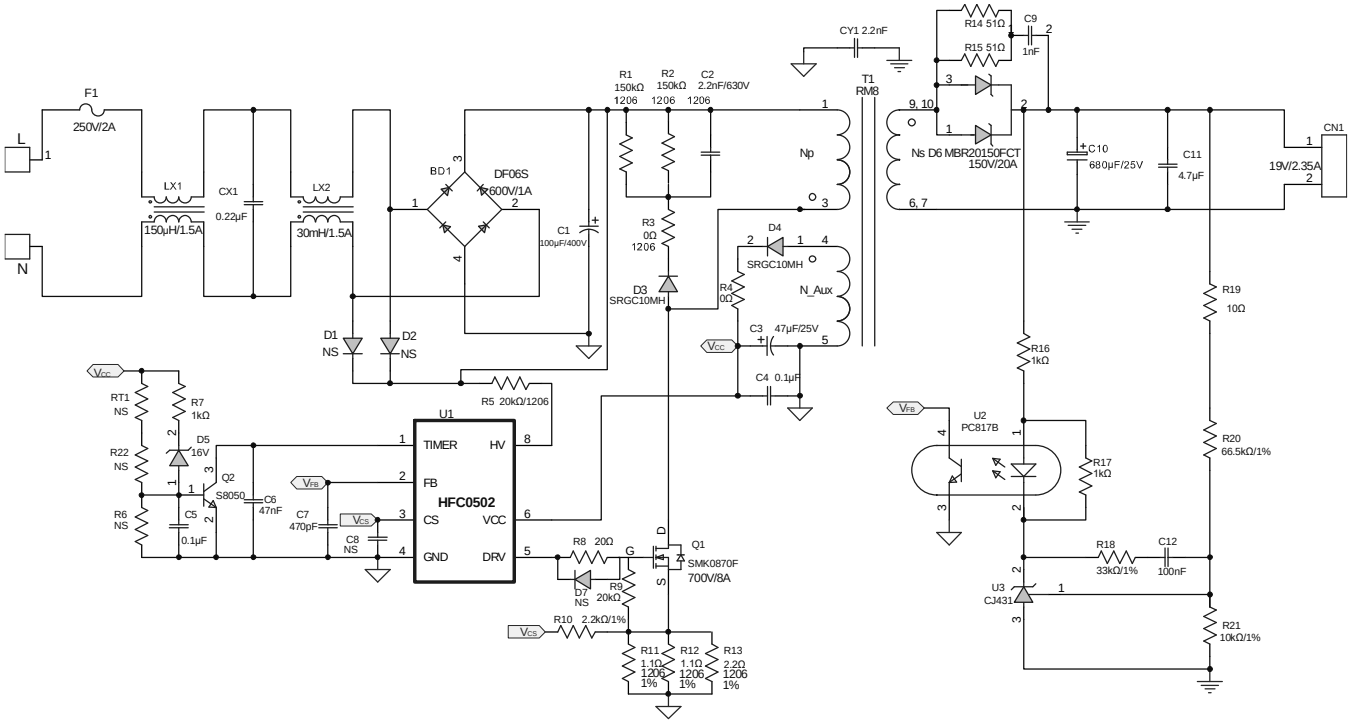
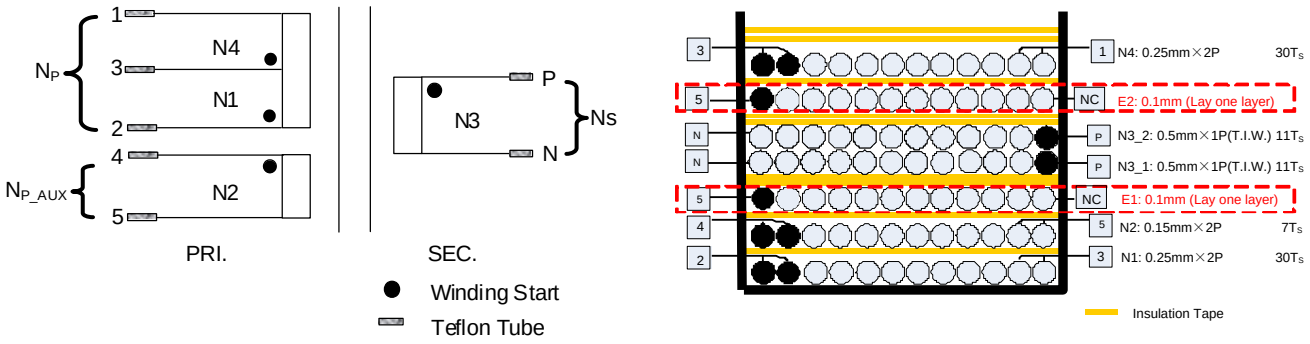


Figure 17: Typical Application Circuit



Connection Diagram **Winding Diagram**

Figure 18: Transformer Structure

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Table 3: Winding Order

Tape (T)	Winding	Terminal (Start to End)	Wire Size (φ)	Turns (T)	Tube
1	N1	2 to 3	0.25mm x 2	30	Matches wire
1	N2	4 to 5	0.15mm x 2	7	Matches wire
2	E1	5 to NC	0.1mm x 12	Wind with tight tension across the entire bobbin evenly	-
2	N3	P to N	0.5mm x 2 (T. I. W)	11	-
2	E2	5 to NC	0.1mm x 2	Wind with tight tension across the entire bobbin evenly	-
1	N4	3 to 1	0.25mm x 2	30	Matches wire

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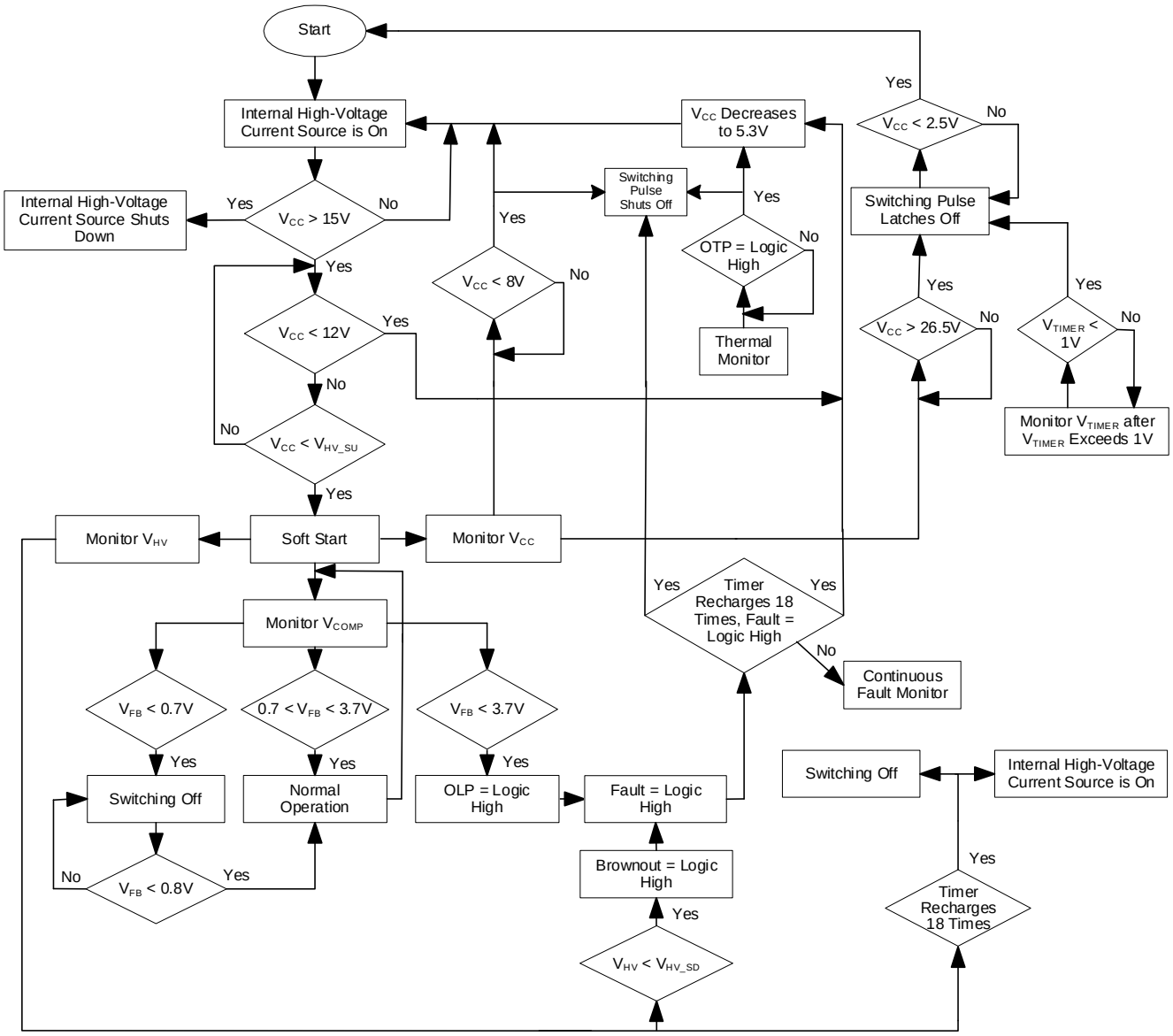
CONTROL FLOW CHART



UVLO, brownout, OTP, and OLP have auto-restart. V_{CC} OVP and the TIMER latch-off input have latch mode. To release a fault latch, unplug the main input.

Figure 19: Control Flow Chart

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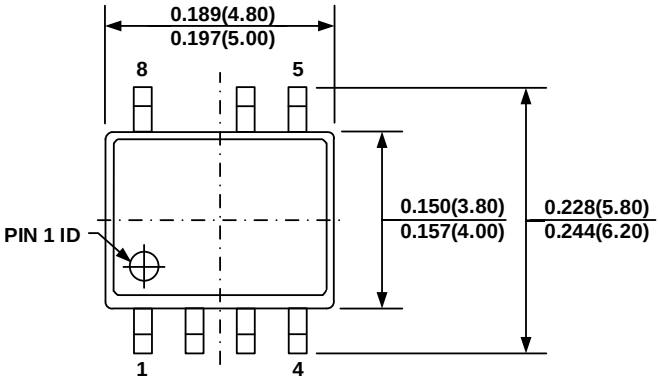
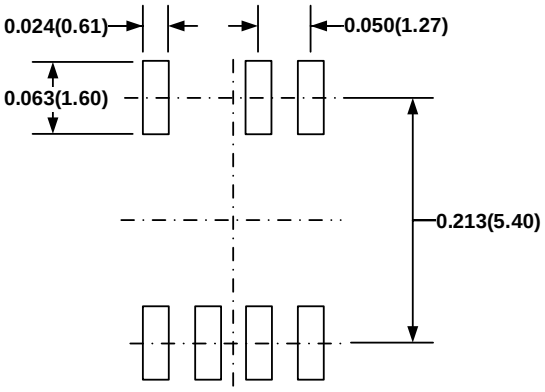
PACKAGE INFORMATION

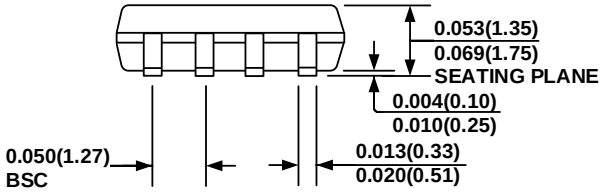
SOIC8-7A



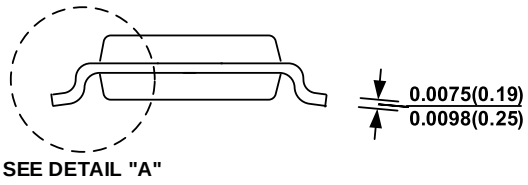
TOP VIEW



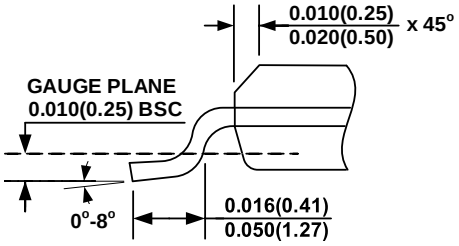
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSIONS ARE IN INCHES. DIMENSIONS IN THE BRACKETS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITIES (BOTTOM OF THE LEADS AFTER FORMING) SHALL BE 0.004 INCHES MAX.
5) JEDEC REFERENCE IS MS-012.
6) DRAWING IS NOT TO SCALE.

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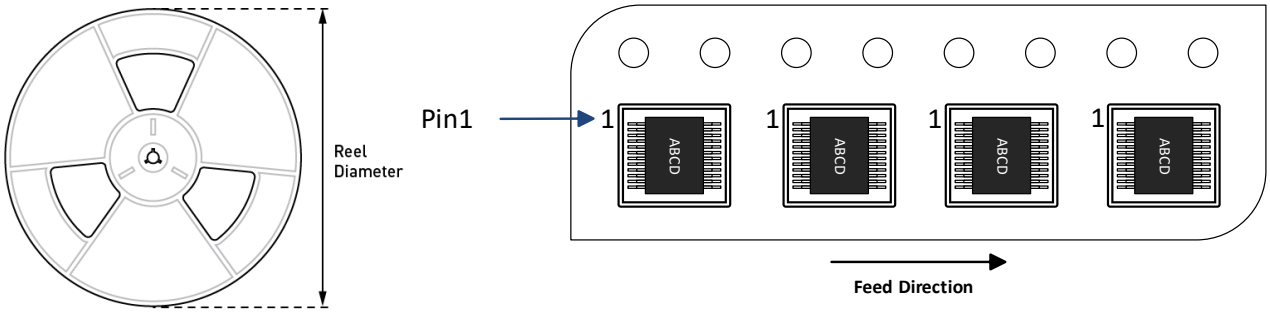
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
HFC0502GS-Z	SOIC8-7A	2500	100	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	4/21/2023	Initial Release	-

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