HFC0310A

Configurable, Fixed-Frequency Flyback Controller Suitable for SiC MOSFETs

DESCRIPTION

The HFC0310A is a flyback controller with configurable fixed-frequency operation. The controller uses peak current mode to provide excellent transient response and ease loop compensation. When the output power (P_{OUT}) decreases, leading to the FB voltage (V_{FB}) to drop to the falling FB threshold at which the regulator enters burst mode ($V_{FB\_BUR\_L}$), the controller enters burst mode to reduce standby power consumption.

An external capacitor connected between the FSET and GND pins configures the switching frequency (f_{SW}). Otherwise, the HFC0310A uses a frequency shaping function to significantly reduce the noise level and EMI filter cost.

The HFC0310A provides various protections, including thermal shutdown, VCC voltage (V_{CC}) under-voltage lockout (UVLO), overload protection (OLP), over-voltage protection (OVP), and short-circuit protection (SCP).

The HFC0310A is available in an SOIC-8 package.

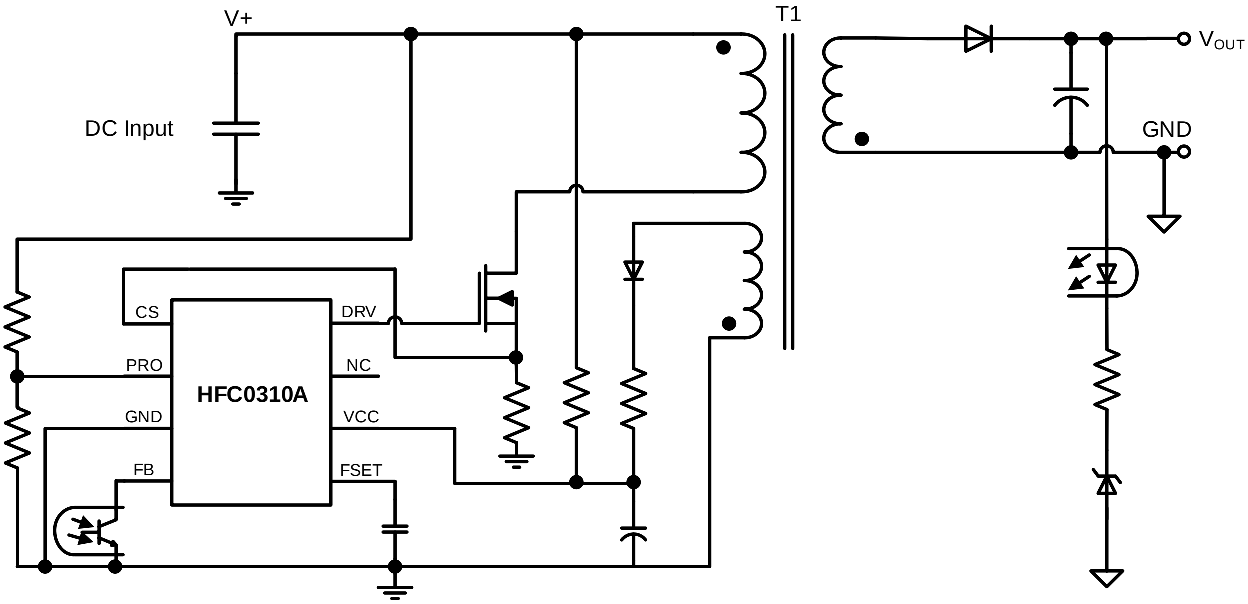
FEATURES

- Configurable Switching Frequency (f_{SW}) Up to 600kHz
- High Clamped DRV Voltage (V_{DRV}), Suitable for SiC MOSFETs
- Frequency Shaping
- Current Mode
- Very Low Start-Up Current (I_{ST})
- Very Low Standby Power Consumption via Active Burst Mode
- Internal Leading-Edge Blanking (LEB)
- Built-In Soft Start (SS)
- Internal Slope Compensation
- External Protection with Recovery Hysteresis on the PRO Pin
- Over-Temperature Protection (OTP)
- VCC Voltage (V_{CC}) Under-Voltage Lockout (UVLO) with Hysteresis
- Over-Voltage Protection (OVP) on VCC
- Time-Based Overload Protection (OLP)
- Short-Circuit Protection (SCP)

APPLICATIONS

- Switched-Mode Power Supplies (SMPS)
- Industry and Solar Auxiliary Power Supplies

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
HFC0310AGS	SOIC-8	*See Below*	2

* For Tape & Reel, add suffix -Z (e.g. HFC0310AGS-Z).

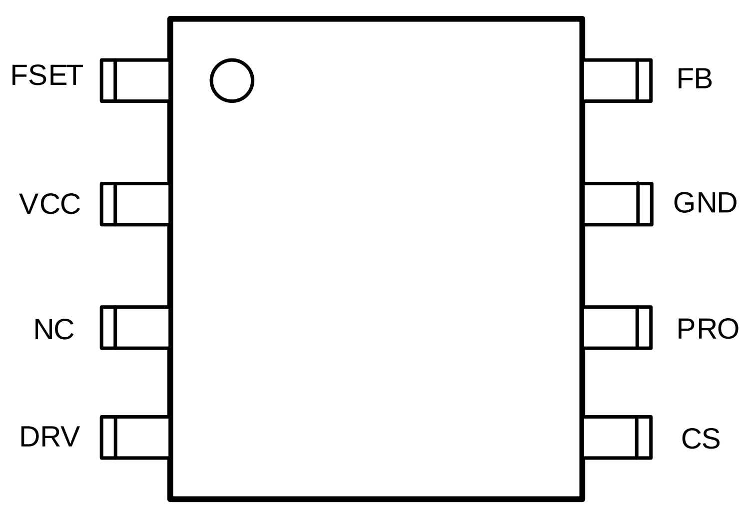
TOP MARKING

HFC0310A
LLLLLLLL
MPSYWW

MPS: MPS prefix
Y: Year code
WW: Week code
HFC0310A: Part number
LLLLLLLL: Lot number

PACKAGE REFERENCE

TOP VIEW



SOIC-8

PIN FUNCTIONS

Pin #	Name	Description
1	FSET	**Switching frequency setting.** Connect a capacitor between the FSET and GND pins to set the switching frequency (f_{SW}) up to 600kHz.
2	VCC	**IC power supply.** Connect the VCC pin to a bulky capacitor and a ceramic capacitor for most applications.
3	NC	**Not connected.**
4	DRV	**Driver signal output.**
5	CS	**Primary current sense.**
6	PRO	**Protection management.** Pull up the PRO pin to shut down the IC with hysteresis.
7	GND	**Ground.**
8	FB	**Feedback.** The output voltage (V_{OUT}) from the external compensation circuit is fed into the FB pin. FB and the current-sense signal from the source determine the pulse-width modulation (PWM) duty cycle. Burst mode and overload protection (OLP) are also detected on FB.

ABSOLUTE MAXIMUM RATINGS (1)

VCC or DRV to GND.....................-0.3V to +30V
All other pins to GND ....-0.3V to +7V
Continuous power dissipation (T_A = 25°C) (2)
SOIC-8.. 1.3W
Junction temperature (T_J) ....150°C
Lead temperature ....260°C
Storage temperature .... -60°C to +150°C

ESD Ratings

Human body model (HBM) 2kV
Charged-device model (CDM) 750V

Recommended Operating Conditions (3)

V_{CC} to GND ....18V to 23V
Operating junction temp (T_J)…..-40°C to +125°C

Thermal Resistance (4) *θJA* *θJC*

SOIC-8.................................... 96 ...... 45... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, which may cause the controller to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on a JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{CC} = 20V, T_J = -40°C to +110°C, min and max values are guaranteed by characterization, typical values are tested at 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Driving Signal (DRV Pin)						
Sourcing resistor	R_H		13	23	35	Ω
Sinking resistor	R_L		7	13	17	Ω
High driver voltage	V_{HIGH}	V_{CC} = V_{CC_L} + 0.1V		14.5		V
		V_{CC} = 20V	14.4	15.2		
Supply Voltage Management (VCC Pin)						
V_{CC} upper turn-on/-off threshold	V_{CC_H}		15.8	17.8	19.6	V
V_{CC} lower turn-on/-off threshold	V_{CC_L}		14.2	15.7	17.2	V
V_{CC} under-voltage lockout (UVLO) hysteresis	V_{CC_H} - V_{CC_L}		1.6	2	2.4	V
Start-up current	I_{ST}	V_{CC} = V_{CC_H} - 0.5V, before start-up	10	22	34	μA
V_{CC} clamp threshold	V_{CC_CLAMP}			24		V
V_{CC} over-voltage protection (OVP) threshold	V_{CC_OVP}		24.6	26.3	28.6	V
V_{CC} protection-enabled recharge threshold	V_{CC_RECHG}		9.6	10.6	11.6	V
Internal IC consumption (protection phase)	I_{PRO}	V_{CC} = 10V		12	19	μA
Feedback Management (FB Pin)						
Internal FB pull-up resistor	R_{FB}		12.5	14.5	17	kΩ
Internal FB pull-up voltage	V_{FB_UP}		4.25	4.55	4.85	V
FB to current-setting point division ratio	I_{FB_DIV}		3	3.5	4	-
Internal soft-start time	t_{SS}			6		ms
Falling FB threshold at which the controller enters burst mode	$V_{FB\_BUR\_L}$		0.43	0.5	0.57	V
Rising FB threshold at which the controller exits burst mode	$V_{FB\_BUR\_H}$		0.66	0.73	0.8	V
Overload setting point	V_{OLP}		3.5	3.75	4	V
Overload delay time	t_{DELAY}	f_{SW} = 100kHz		82		ms
Timing Capacitor (FSET)						
Maximum voltage on the FSET capacitor	V_{FSET_MAX}		0.82	0.87	0.92	V
Source current	I_{FSET}		40	55	65	μA
FSET capacitor discharge time (active at driver turn-on)	t_{DISCH}			500		ns
Frequency spread spectrum (FSS) shaping range	$R_{SHAPING}$			±4		% of f_{SW}
Frequency shaping modulation period [5]	$t_{SHAPING}$			256		cycles
Current-Sampling Management (CS Pin)						
Leading-edge blanking (LEB) period for current sensor	t_{LEB1}		155	230	300	ns
LEB period for short-circuit protection (SCP)	t_{LEB2}		145	210	280	ns
Maximum current-setting point	V_{CS_MAX}		0.87	0.94	1.02	V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{CC} = 20V, T_J = -40°C to +110°C, min and max values are guaranteed by characterization, typical values are tested at 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SCP setting point	V_{SCP}		1.53	1.64	1.84	V
Internal slope compensation ramp	S_{RAMP}	f_{SW} = 100kHz	27	42	57	mV/µs
Protection Management (PRO Pin)						
PRO pin voltage	V_{PRO}		3	3.25	3.5	V
PRO pin hysteresis	V_{PRO_HYS}			0.2		V
Thermal Shutdown						
Thermal shutdown threshold (5)				150		°C
Thermal shutdown recovery hysteresis (5)				40		°C

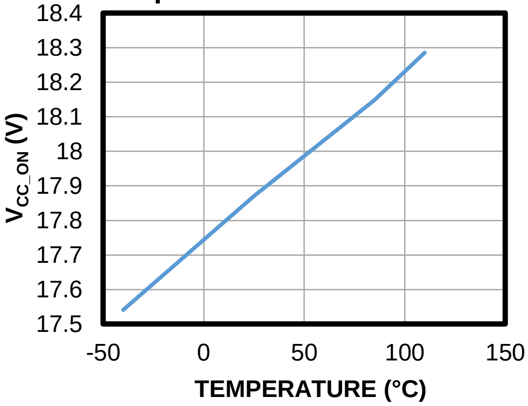
Note:

5) This parameter is guaranteed by design.

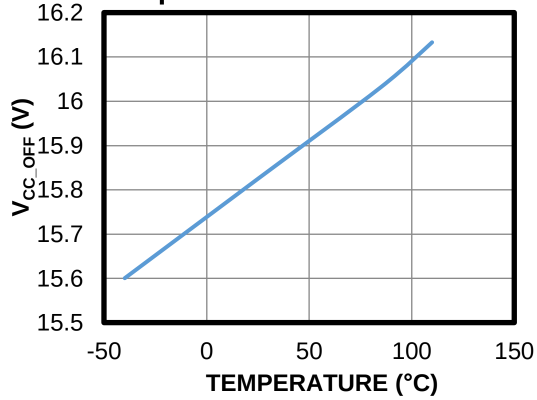
TYPICAL CHARACTERISTICS

V_{CC} = 20V, unless otherwise noted.

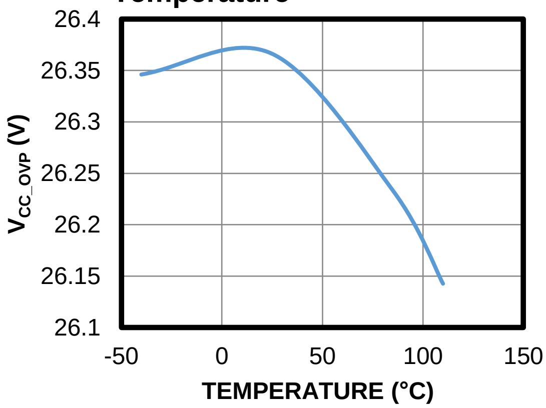
V_{CC} Upper Threshold at Which the IC Switches On vs. Temperature



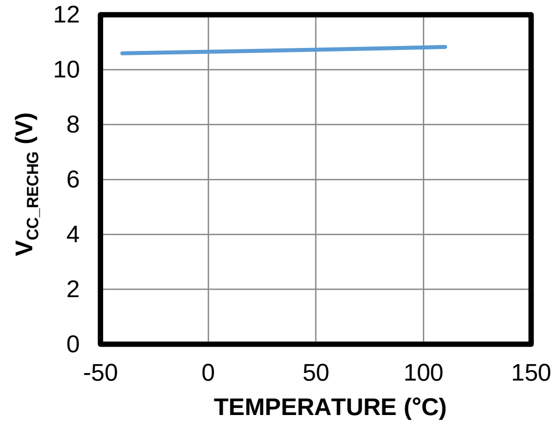
V_{CC} Lower Threshold at Which the IC Switches Off vs. Temperature



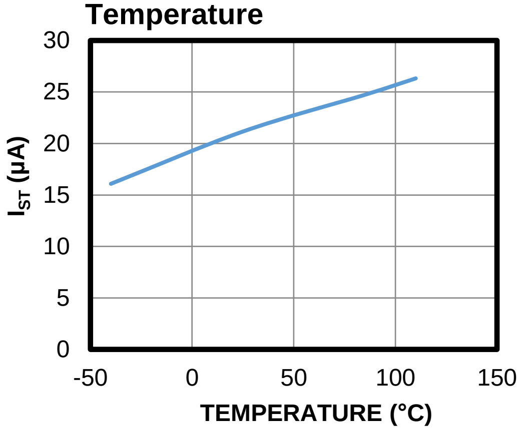
V_{CC} OVP Threshold vs. Temperature



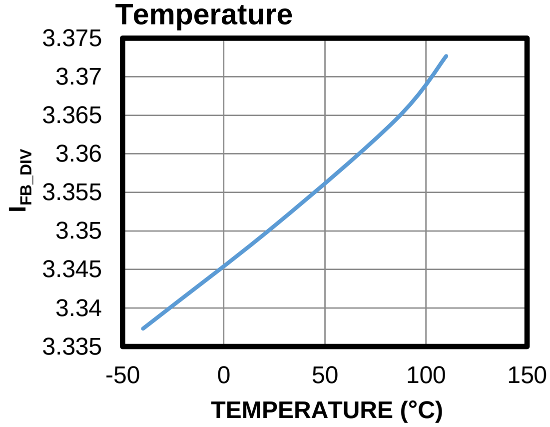
V_{CC} Recharge Threshold at Which the Protections Occur vs. Temperature



Start-Up Current vs. Temperature



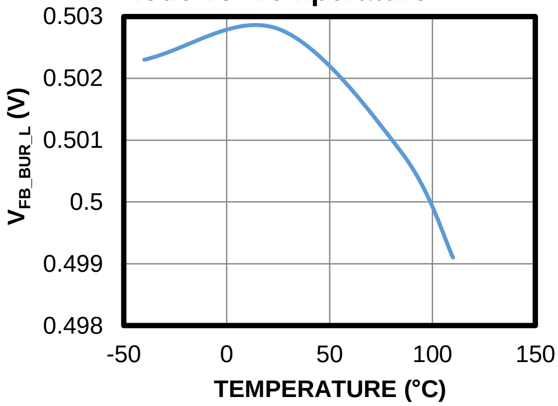
FB to Current-Setting Point Division Ratio vs. Temperature



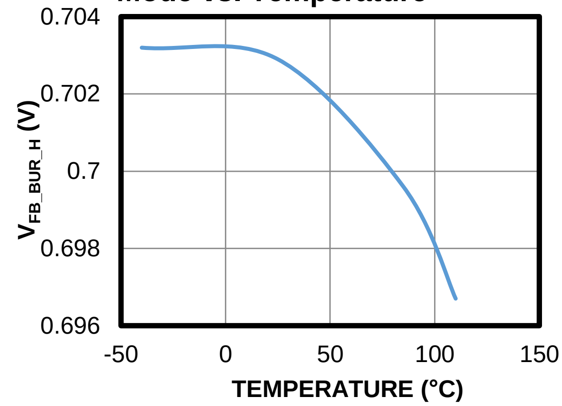
TYPICAL CHARACTERISTICS *(continued)*

V_{CC} = 20V, unless otherwise noted.

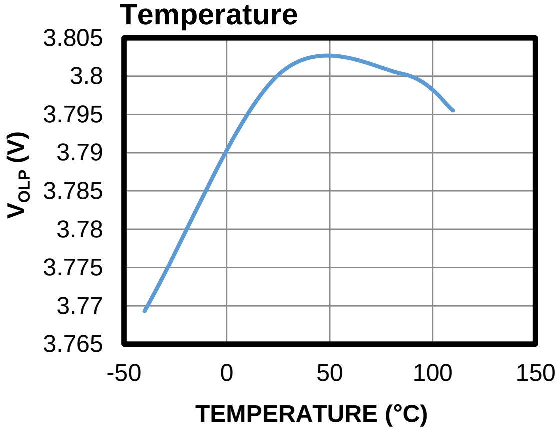
Falling FB Threshold at Which the Regulator Enters Burst Mode vs. Temperature



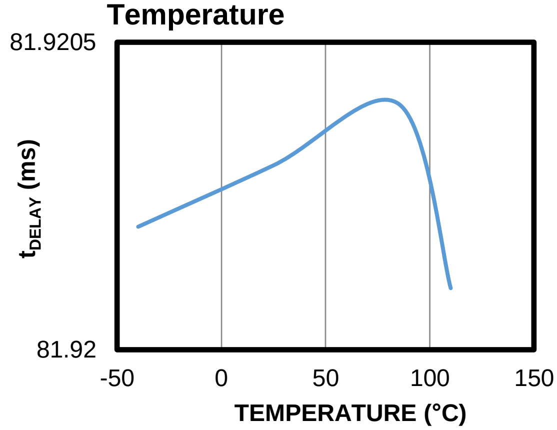
Rising FB Threshold at Which the Regulator Exits Burst Mode vs. Temperature



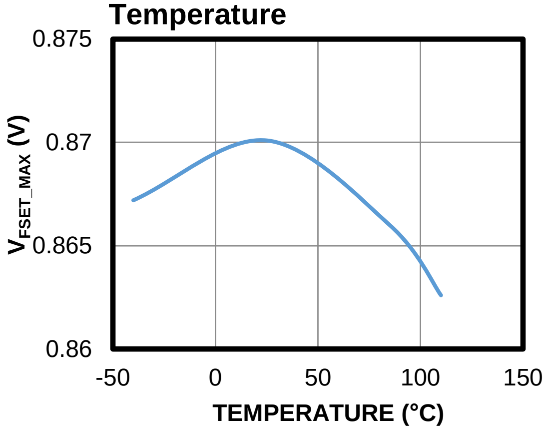
Overload Setting Point vs. Temperature



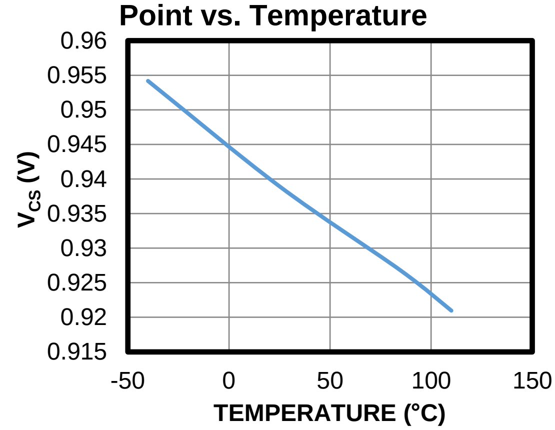
Overload Delay Time vs. Temperature



Maximum Voltage on the FSET Capacitor vs. Temperature



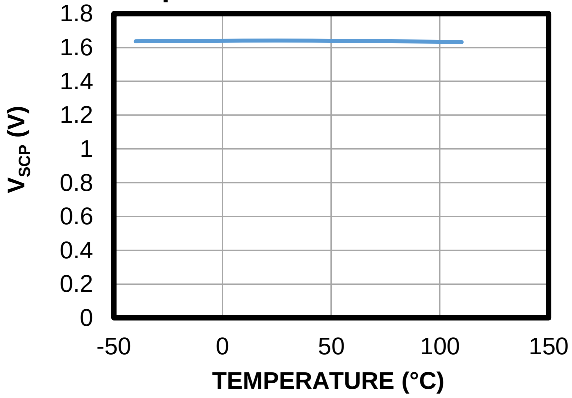
Maximum Current-Setting Point vs. Temperature



TYPICAL CHARACTERISTICS *(continued)*

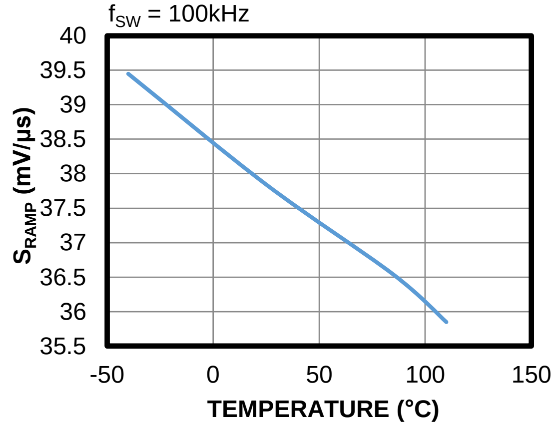
V_{CC} = 20V, unless otherwise noted.

SCP Setting Point vs. Temperature

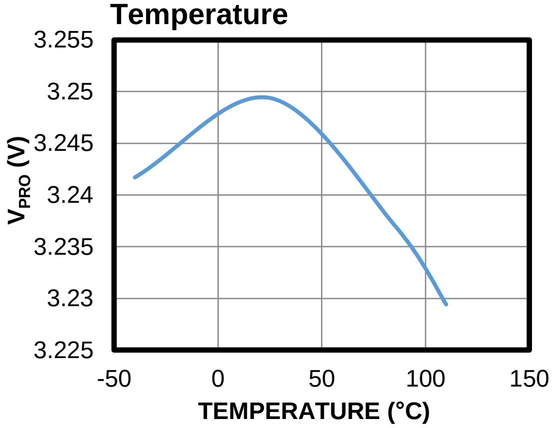


Internal Slope Compensation Ramp vs. Temperature

f_{SW} = 100kHz

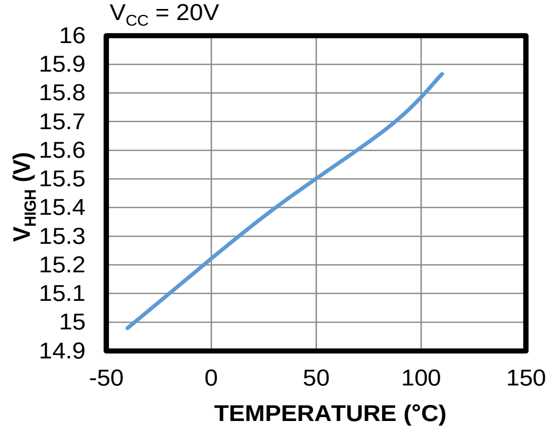


Protection Voltage vs. Temperature



High Driver Voltage vs. Temperature

V_{CC} = 20V

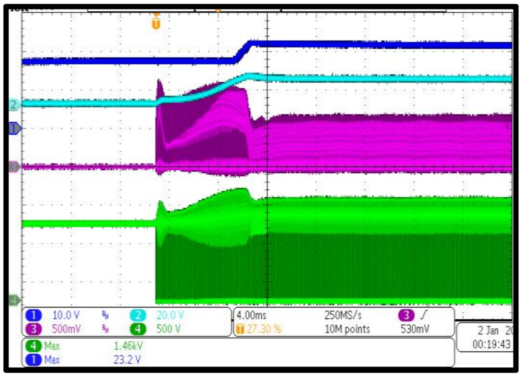


TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board. V_{IN} = 1000V_{DC}, V_{OUT1} = 12.5V, I_{OUT1} = 3A, V_{OUT2} = 12.5V, I_{OUT2} = 3A, V_{OUT3} = 24V, I_{OUT3} = 0.1A, T_A = 25°C, unless otherwise noted.

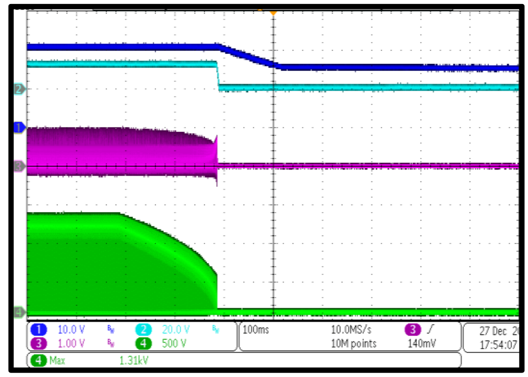
Start-Up

CH2: V_{OUT1}
CH1: V_{CC}
CH3: V_{CS}
CH4: V_{DS}



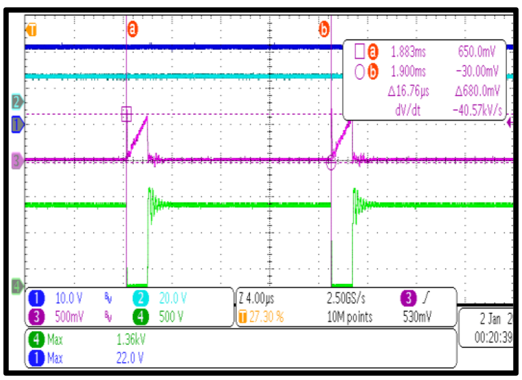
Shutdown

CH2: V_{OUT1}
CH1: V_{CC}
CH3: V_{CS}
CH4: V_{DS}



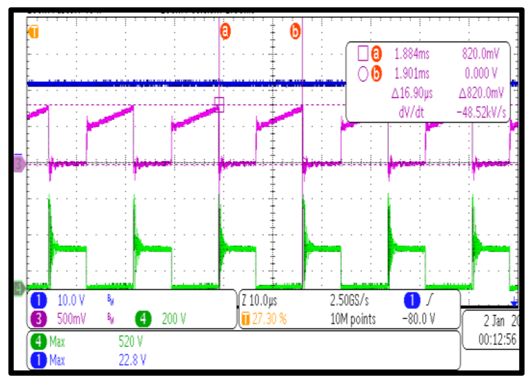
Steady State
V_{IN} = 1000V_{DC}

CH2: V_{OUT1}
CH1: V_{CC}
CH3: V_{CS}
CH4: V_{DS}



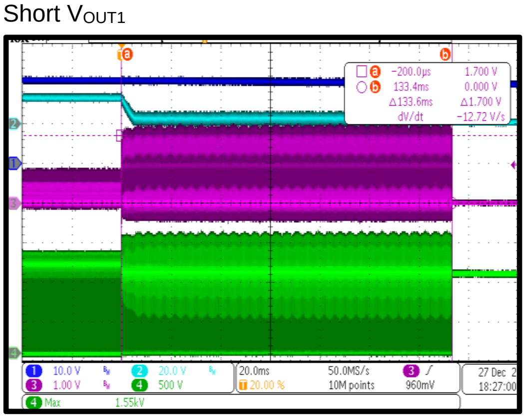
Steady State
V_{IN} = 100V_{DC}

CH1: V_{CC}
CH2: V_{OUT1}
CH3: V_{CS}
CH4: V_{DS}



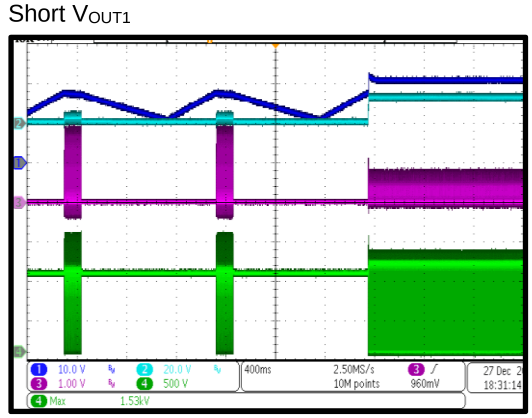
OLP Entry
Short V_{OUT1}

CH2: V_{OUT2}
CH1: V_{CC}
CH3: V_{CS}
CH4: V_{DS}



OLP Recovery
Short V_{OUT1}

CH2: V_{OUT2}
CH1: V_{CC}
CH3: V_{CS}
CH4: V_{DS}

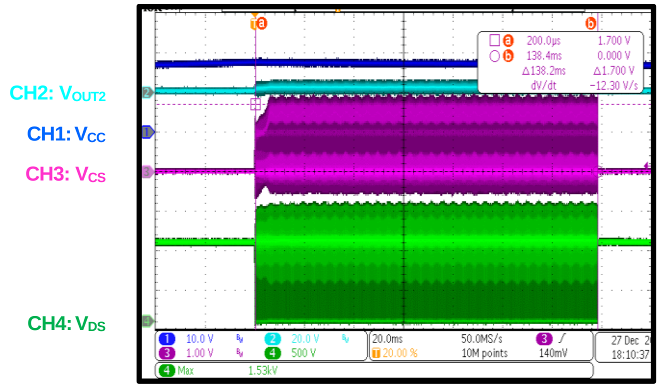


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

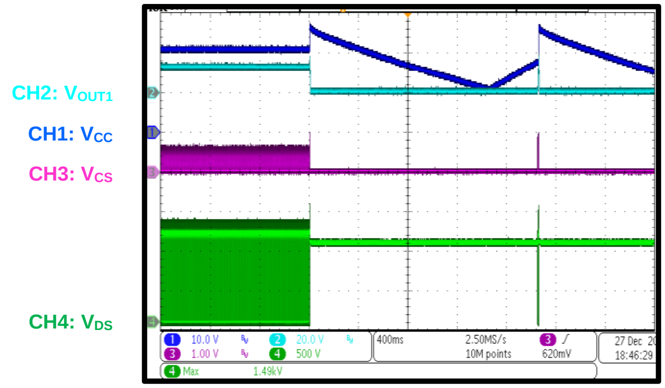
Performance waveforms are tested on the evaluation board. V_{IN} = 1000V_{DC}, V_{OUT1} = 12.5V, I_{OUT1} = 3A, V_{OUT2} = 12.5V, I_{OUT2} = 3A, V_{OUT3} = 24V, I_{OUT3} = 0.1A, T_A = 25°C, unless otherwise noted.

OLP Start-Up

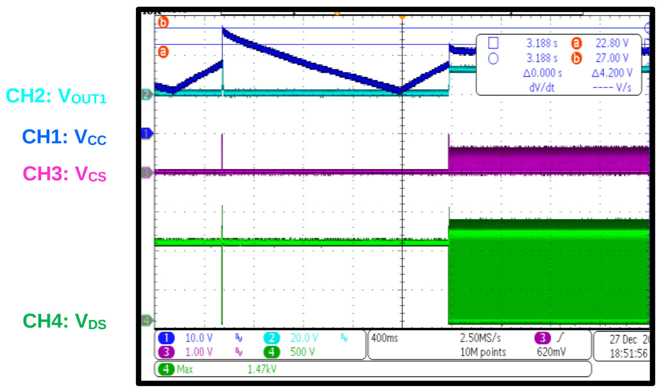
Short V_{OUT1}



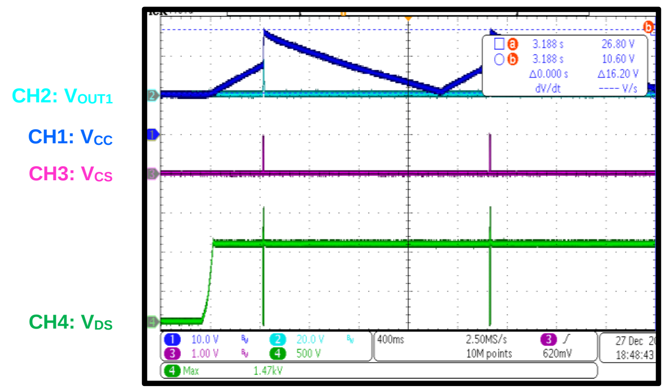
OVP Entry



OVP Recovery

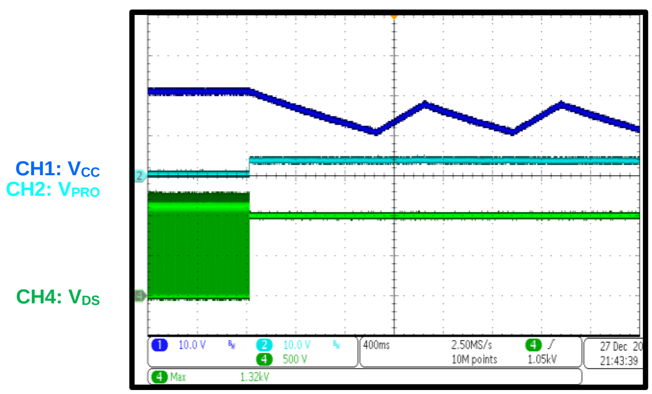


OVP Start-Up



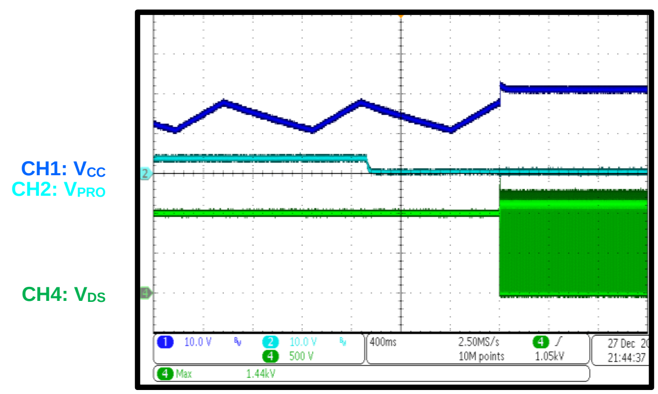
PRO Protection Entry

Set PRO = 3.5V



PRO Protection Recovery

Set PRO = 0V

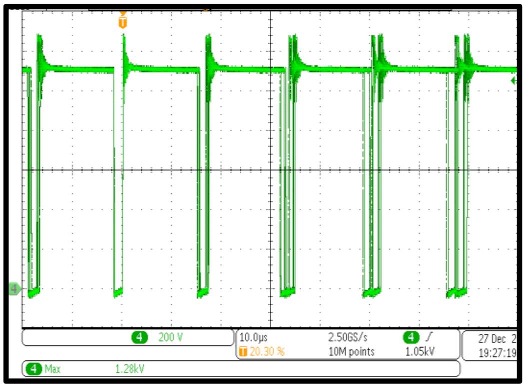


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. V_{IN} = 1000V_{DC}, V_{OUT1} = 12.5V, I_{OUT1} = 3A, V_{OUT2} = 12.5V, I_{OUT2} = 3A, V_{OUT3} = 24V, I_{OUT3} = 0.1A, T_A = 25°C, unless otherwise noted.

Jitter

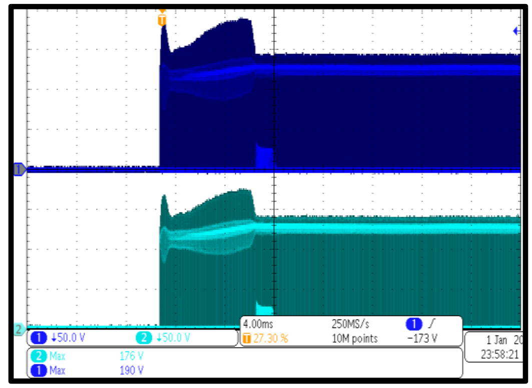
CH4: V_{DS}



Secondary Diode Stress

CH1: V_{D2}

CH2: V_{D4}

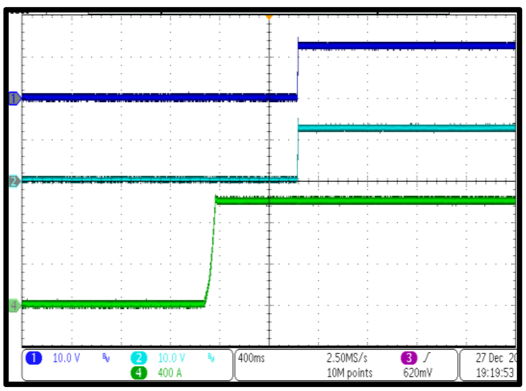


Input Power Start-Up

CH1: V_{OUT1}

CH2: V_{OUT2}

CH4: V_{IN}

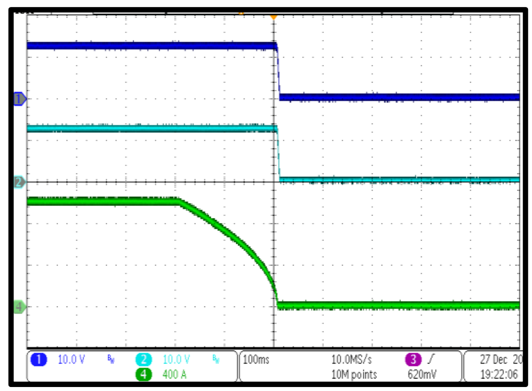


Input Power Shutdown

CH1: V_{OUT1}

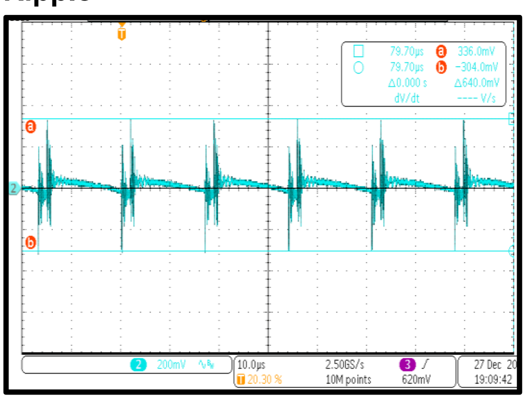
CH2: V_{OUT2}

CH4: V_{IN}



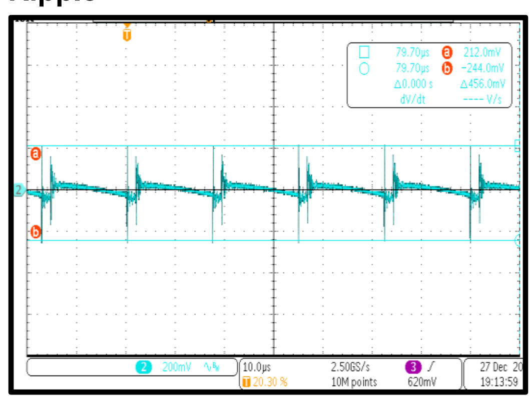
Ripple

CH2: V_{OUT1}



Ripple

CH2: V_{OUT2}



FUNCTIONAL BLOCK DIAGRAM

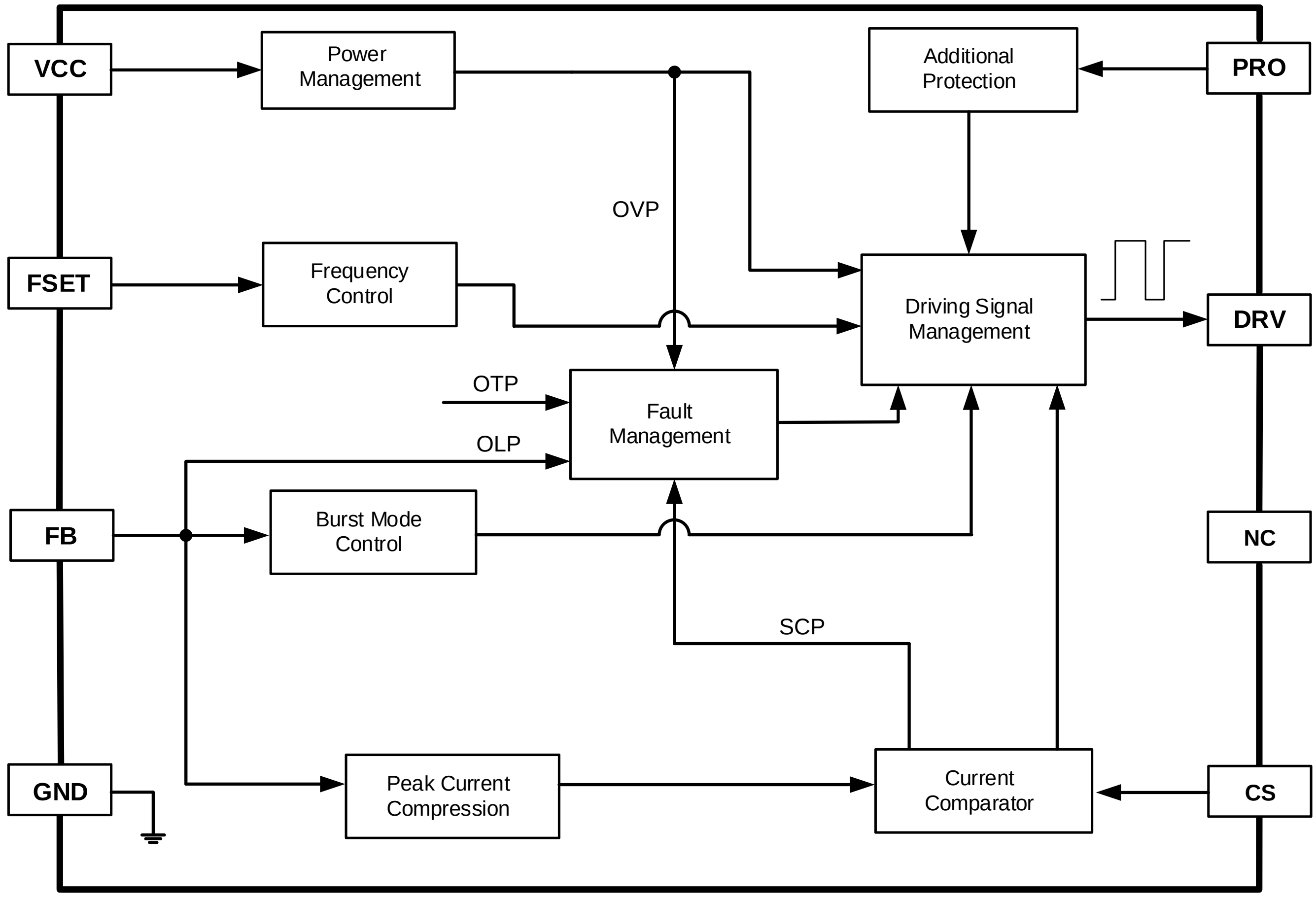


Figure 1: Functional Block Diagram

OPERATION

The HFC0310A incorporates all the necessary features to build a reliable switch-mode power supply. Its high level of integration requires very few external components. The device provides burst mode to minimize standby power consumption at light loads. Protection features including auto-recovery for overload protection (OLP), short-circuit protection (SCP), over-voltage protection (OVP), or thermal shutdown for over-temperature protection (OTP) contribute to a safer converter design without increasing circuit complexity.

Pulse-Width Modulation (PWM) Operation

The HFC0310A is a fully integrated converter with adjustable-frequency, peak current mode control, pulse-width modulation (PWM) switching regulators. The output voltage (V_{OUT}) is measured at the FB pin through a voltage resistor divider, amplifier, and optocoupler. The voltage at FB (V_{FB}) is compared to the internally measured switch current to control V_{OUT}. The external MOSFET turns on at the beginning of each clock cycle. The inductor current (I_L) increases until it reaches the value set by V_{FB}, then the external MOSFET turns off.

Start-Up and V_{CC} Under-Voltage Lockout (UVLO)

During start-up, the start-up current (I_{ST}) indicates the IC consumption, and the current supplied through the start-up resistor charges the VCC capacitor (C_{VCC}).

The IC starts switching and the operating current increases when the VCC voltage (V_{CC}) reaches its upper turn-on/-off threshold (V_{CC_H}). At this point, the transformer's auxiliary winding powers the IC. When V_{CC} drops below its lower turn-on/-off threshold (V_{CC_L}), the controller stops switching, and the current through the start-up resistor charges C_{VCC} again.

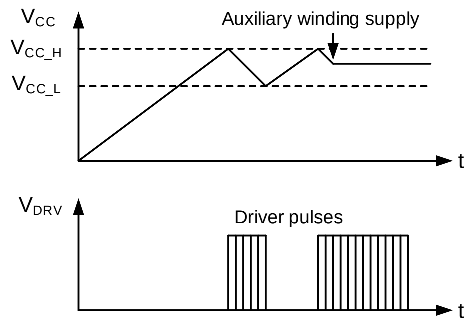


Figure 2: V_{CC} UVLO

The lower threshold of V_{CC} under-voltage lockout (UVLO) decreases from V_{CC_L} to the V_{CC} protection-enabled recharge threshold (V_{CC_RECHG}) if fault conditions occur, such as OLP, OVP, and OTP.

High DRV Voltage

The high DRV voltage (V_{DRV}) is clamped at the high driver voltage (V_{HIGH}, typically 15.2V) when V_{CC} exceeds V_{CC_H}. It is recommended to select 20kΩ for the resistor connected between the DRV and CS pins (R_{GS}).

Soft Start (SS)

To reduce stress on the primary MOSFET and secondary diode during start-up and to smoothly establish V_{OUT}, the HFC0310A provides an internal soft-start (SS) circuit that gradually increases the primary current-sense threshold. This threshold determines the MOSFET's peak current during start-up. The power switching device's pulse-width progressively increases to establish optimal operating conditions until the feedback control loop takes charge. Figure 3 shows soft start.

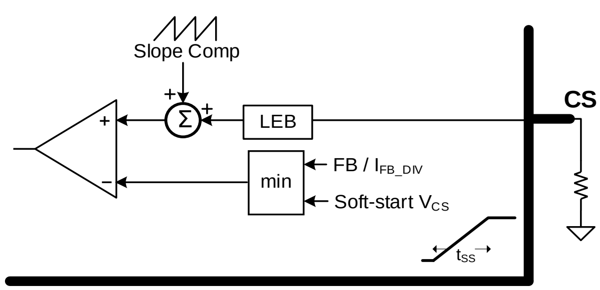


Figure 3: Soft Start

Switching Frequency with Shaping

The capacitor between the FSET and GND pins sets the HFC0310A's switching frequency (f_{SW}). f_{SW} can be calculated with Equation (1):

$$f_{SW} = \frac{1}{t_{DISCH} + C \times \frac{V_{FSET\_MAX}}{I_{FSET}}} \text{ (in Hz)} \qquad (1)$$

The capacitor must be placed close to FSET and GND to ensure stable frequency.

Frequency shaping reduces EMI by spreading the energy across the shaping frequency ($t_{SHAPING}$) range. Figure 4 shows the frequency shaping circuit, where $t_{SHAPING}$ is about 256 switching cycles.

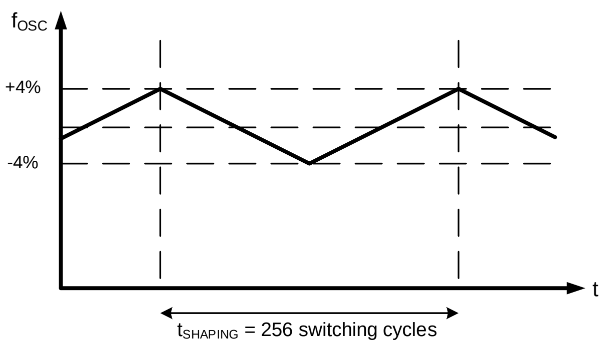


Figure 4: Frequency Shaping

Slope Compensation

Slope compensation is added to avoid subharmonic oscillation. If there is a longer on time (t_{ON}), then higher compensation voltage is added to the real current-sensing voltage.

Slope compensation (V_{RAMP}) can be calculated with Equation (2):

$$V_{RAMP} = D_{ON} \times (S_{RAMP} \times 10\mu s) \text{ (in mV)} \qquad (2)$$

Where the on time duty is D_{ON}.

Over-Voltage Protection (OVP)

Monitoring the VCC pin with a delay time of about 20µs allows the HFC0310A to enter OVP under an over-voltage (OV) condition when V_{CC} exceeds its OVP threshold (V_{CC_OVP}). The HFC0310A resumes operation after the fault is removed.

Overload Protection (OLP)

The HFC0310A continuously monitors the FB pin. If FB is pulled up to the overload setting point (V_{OLP}) and the fault signal is still present after a switching cycle delay of 8,192 cycles passes, then the HFC0310A shuts down. Once the fault is removed, the power supply resumes operation.

Short-Circuit Protection (SCP)

By monitoring the CS pin, the HFC0310A shuts down when CS voltage (V_{CS}) exceeds the SCP setting point (V_{SCP}) to indicate a short circuit. The HFC0310A then enters a safe low-power mode (LPM) to prevent any significant thermal or stress damage. Once the fault disappears, the power supply resumes operation.

Thermal Shutdown

If the IC temperature exceeds the thermal shutdown threshold, then OTP is triggered. Once the junction temperature (T_J) drops to the thermal shutdown recovery threshold, the IC resumes operation.

Burst Mode

To minimize standby power consumption, the HFC0310A implements burst mode at no load or light loads. As the load decreases, V_{FB} decreases. The IC stops switching when V_{FB} drops below its lower threshold ($V_{FB\_BUR\_L}$). Then V_{OUT} drops at a rate dependent on the load, causing V_{FB} to rise again due to the negative feedback control loop. Once V_{FB} exceeds its upper threshold ($V_{FB\_BUR\_H}$), the switching pulse resumes. V_{FB} then decreases and the whole process repeats. Burst mode alternately enables and disables the MOSFET's switching pulse. As a result, switching loss at no-load or light-load conditions is significantly reduced.

Figure 5 shows the signals generated by burst mode.

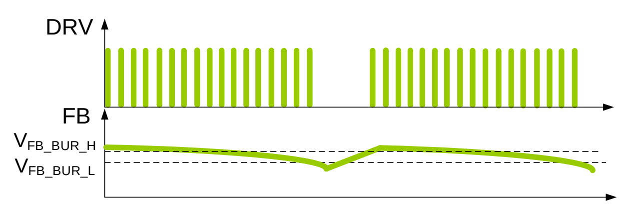


Figure 5: Burst Mode

PRO Pin

The PRO pin provides additional protection against abnormal conditions. Apply PRO for input OVP or other protections. After VCC reaches V_{CCH}, once the voltage input to PRO exceeds the PRO pin voltage (V_{PRO}) (3.25V), the IC shuts down. As soon as the fault is removed, the power supply resumes operation.

Leading-Edge Blanking (LEB)

In normal operation, a resistor is placed between the MOSFET source and ground to sense the primary peak current. V_{FB} sets the MOSFET's turn-off threshold, where $V_{SENSE} = V_{FB} / I_{FB\_DIV}$. The HFC0310A turns off the MOSFET once the sensing resistor voltage (V_{RSENSE}) rises to the sensing voltage (V_{SENSE}).

During start-up and overload conditions, the maximum primary peak current threshold is internally limited to the maximum current-setting point (V_{CS_MAX}) to avoid excessive output power (P_{OUT}) and lower the switch voltage stress. The IC implements a leading-edge blanking (LEB) period (t_{LEB}) to avoid turning off the MOSFET by mistriggered spikes shortly after the switch turns on. During blanking time, any trigger signal on the CS pin is blocked. Figure 6 shows the primary current-sense waveform and LEB.

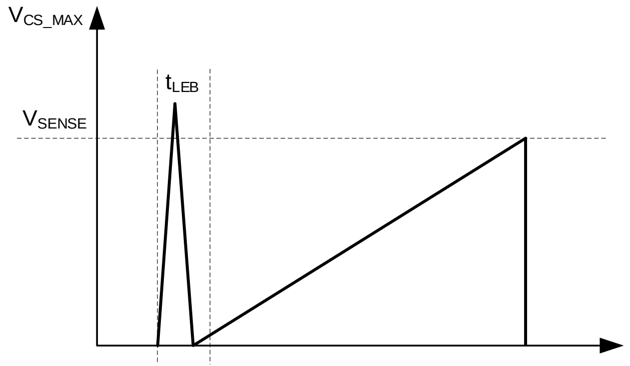


Figure 6: Leading-Edge Blanking

APPLICATION INFORMATION

VCC Capacitor Selection

Figure 7 shows the HFC0310A's VCC start-up circuit.

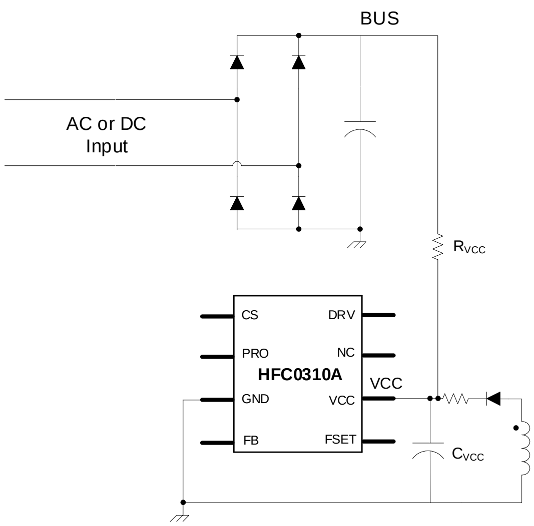


Figure 7: HFC0310A's VCC Start-Up Circuit

C_{VCC} is charged by the start-up resistor once the input voltage (V_{IN}) is applied. The maximum start-up resistance between BUS and the VCC pin can be estimated with Equation (3):

$$R_{VCC} < 0.9 \times \frac{BUS\_MIN}{I_{ST}} \quad (3)$$

Where I_{ST} is a maximum of 34µA, and BUS_{MIN} is the minimum voltage on the BUS input capacitor.

In addition, the start-up resistance (R_{VCC}) must not be too small. Otherwise, when the bus voltage (V_{BUS}) is high, the V_{CC} start-up current may be too high to increase V_{CC} to the OVP threshold.

If V_{OUT} is not high enough for the auxiliary winding to supply VCC, then the IC stops switching and V_{OUT} cannot be set normally. For most applications, choose a C_{VCC} that exceeds 10µF. C_{VCC} can be estimated with Equation (4):

$$C_{VCC} > \frac{(I_{CC} - V_{IN\_MIN} / R_{VCC}) \times t_{RISE}}{V_{CC\_H} - V_{CC\_L}} \quad (4)$$

Where I_{CC} is the IC internal consumption after the IC starts switching, t_{RISE} is the time for V_{OUT} to rise high enough to allow the auxiliary winding to supply VCC, and V_{CC_H} - V_{CC_L} is the V_{CC} UVLO hysteresis (typically 2V).

Primary-Side Inductor Design

With internal slope compensation, the HFC0310A can support continuous conduction mode (CCM) when the duty cycle exceeds 50%. Set a ratio (K_P) of the primary inductor's ripple current amplitude compared to the peak current value to $0 < K_P \leq 1$, where $K_P = 1$ for discontinuous conduction mode (DCM). Figure 8 shows the relevant waveforms.

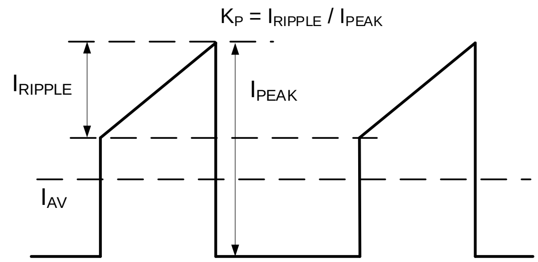


Figure 8: Typical Primary-Current Waveform

A larger inductance leads to a smaller K_P. This can reduce the RMS current but increases the transformer size. Considering the circuit performance under a high DC input voltage, an optimal K_P is between 0.5 and 0.7 for the universal input range, and between 0.7 and 1 for an input range exceeding $160V_{DC}$.

The input power (P_{IN}) at the minimum input can be estimated with Equation (4):

$$P_{IN} = \frac{V_{OUT} \times I_{OUT}}{\eta} \quad (4)$$

Where I_{OUT} is the rated output current, and η is the estimated efficiency, which is generally between 0.85 and 0.9 depending on the input range and output application.

At the minimum input in CCM, the converter duty cycle (D) can be calculated with Equation (5):

$$D = \frac{(V_{OUT} + V_F) \times N}{(V_{OUT} + V_F) \times N + V_{IN\_MIN}} \quad (5)$$

Where V_F is the secondary diode's forward voltage, and N is the transformer turn ratio.

The MOSFET's on time (t_{ON}) can be calculated with Equation (6):

$$t_{ON} = D \times t_S \quad (6)$$

Where t_S is the switching period.

The average value of the primary current (I_{AV}) can be calculated with Equation (7):

$$I_{AV} = \frac{P_{IN}}{V_{IN\_MIN}} \quad (7)$$

The peak value of the primary current (I_{PEAK}) can be calculated with Equation (8):

$$I_{PEAK} = \frac{I_{AV}}{\left(1 - \frac{K_P}{2}\right) \times D} \quad (8)$$

The ripple value of the primary current (I_{RIPPLE}) can be calculated with Equation (9):

$$I_{RIPPLE} = K_P \times I_{PEAK} \quad (9)$$

The valley threshold of the primary current (I_{VALLEY}) can be calculated with Equation (10):

$$I_{VALLEY} = (1 - K_P) \times I_{PEAK} \quad (10)$$

The primary-side inductor (L_M) can be estimated with Equation (11):

$$L_M = \frac{V_{IN\_MIN} \times t_{ON}}{I_{RIPPLE}} \quad (11)$$

Current-Sense Resistor

Figure 9 shows the peak current comparator logic and the subsequent waveform.

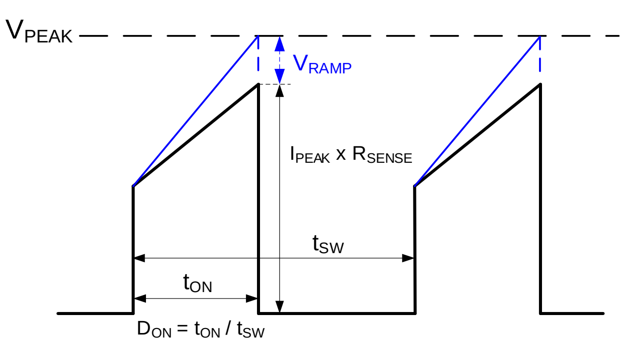


Figure 9: Typical Waveform of the Peak Current Comparator

When the sum of V_{RSENSE} and the slope compensator reaches the peak voltage (V_{PEAK}), the comparator goes high to reset the RS flip-flop, and DRV is pulled down to turn off the MOSFET. The maximum current-setting point (V_{CS_MAX}) is 0.94V. V_{RAMP} can be calculated by Equation (2) on page 15. Given a certain margin, use 0.95 x V_{CS_MAX} as V_{PEAK} at full load.

Then V_{RSENSE} can be calculated with Equation (12):

$$V_{RSENSE} = 95\% \times V_{CS\_MAX} - V_{RAMP} \quad (12)$$

Then the sensing resistance (R_{SENSE}) can be calculated with Equation (13):

$$R_{SENSE} = \frac{V_{RSENSE}}{I_{PEAK}} \quad (13)$$

Low-Pass Filter on the CS Pin

A small capacitor connected to the CS pin with the feed resistor (R_{FEED}) forms a low-pass filter for noise filtering when the MOSFET turns on and off (see Figure 10).

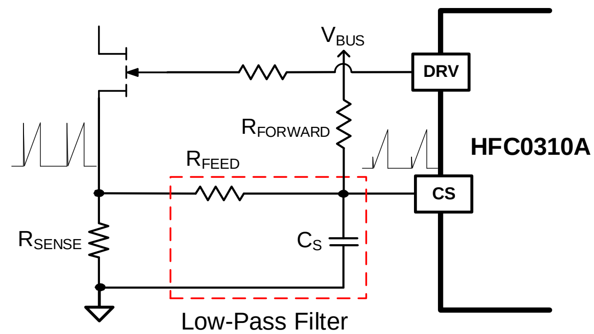


Figure 10: Low-Pass Filter on CS

The low-pass filter's R_{FEED} x C_S constant should not exceed 1/3 of the LEB period for SCP (t_{LEB2}, typically 210ns). Otherwise, the filtered sensed voltage cannot reach the SCP threshold to trigger SCP if an output short circuit occurs.

Feed-Forward Compensation

At high V_{IN}, the turn-off delay time causes the peak primary current to exceed the V_{CS} setting point (see Figure 11).

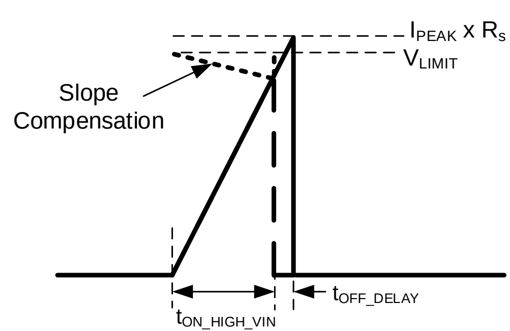


Figure 11: Turn-Off Delay Impact

To reduce the turn-off delay time impact at high V_{IN}, a feed-forward compensation circuit (see Figure 10) is recommended to be added on CS.

It is composed by the forward resistor ($R_{FORWARD}$) and R_{FEED}. The compensation CS voltage (V_{CS_COMP}) can be calculated with Equation (14):

$$V_{CS\_COMP} = \frac{R_{FEED} \times V_{IN}}{R_{FEED} + R_{FORWARD}} \quad (14)$$

The maximum V_{CS_COMP} should not exceed $V_{FB\_BUR\_H}$ / I_{FB_DIV} (typically about 0.2V).

Design Example

Table 1 shows a design example using the application guidelines for the given specifications.

Table 1: Design Example

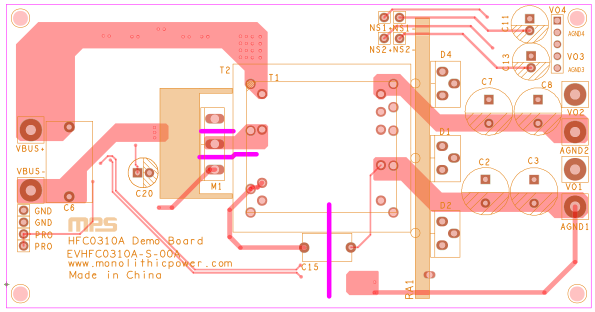
V_{IN}	V_{OUT1}	V_{OUT2}	V_{OUT3}	f_{SW}
$100V_{DC}$ to $1000V_{DC}$	12.5V/ 3A	12.5V/ 3A	24V/ 100mA	60kHz

Figure 12 on page 21 shows the detailed typical application circuit. See the Typical Performance Characteristics section on page 10 for the typical performance and circuit waveforms. For more applications, refer to the related evaluation board datasheets.

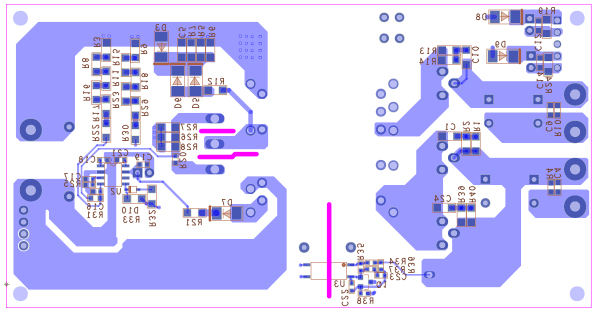
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation as well as good EMI and thermal performance. For the best results, refer to Figure 12 and follow the guidelines below:

1. Minimize the power stage loop area, including the input loop, auxiliary winding loop, and output loop.
2. Keep the input loop ground and control circuit separate.
3. Place the control circuit capacitors (such as the capacitors for FB, CS, and VCC) close to the IC to decouple noise.
4. Place the ground of the FSET capacitor (C_{FSET}) close to the IC ground to maintain stable f_{SW}.



Top Layer



Bottom Layer

Figure 12: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

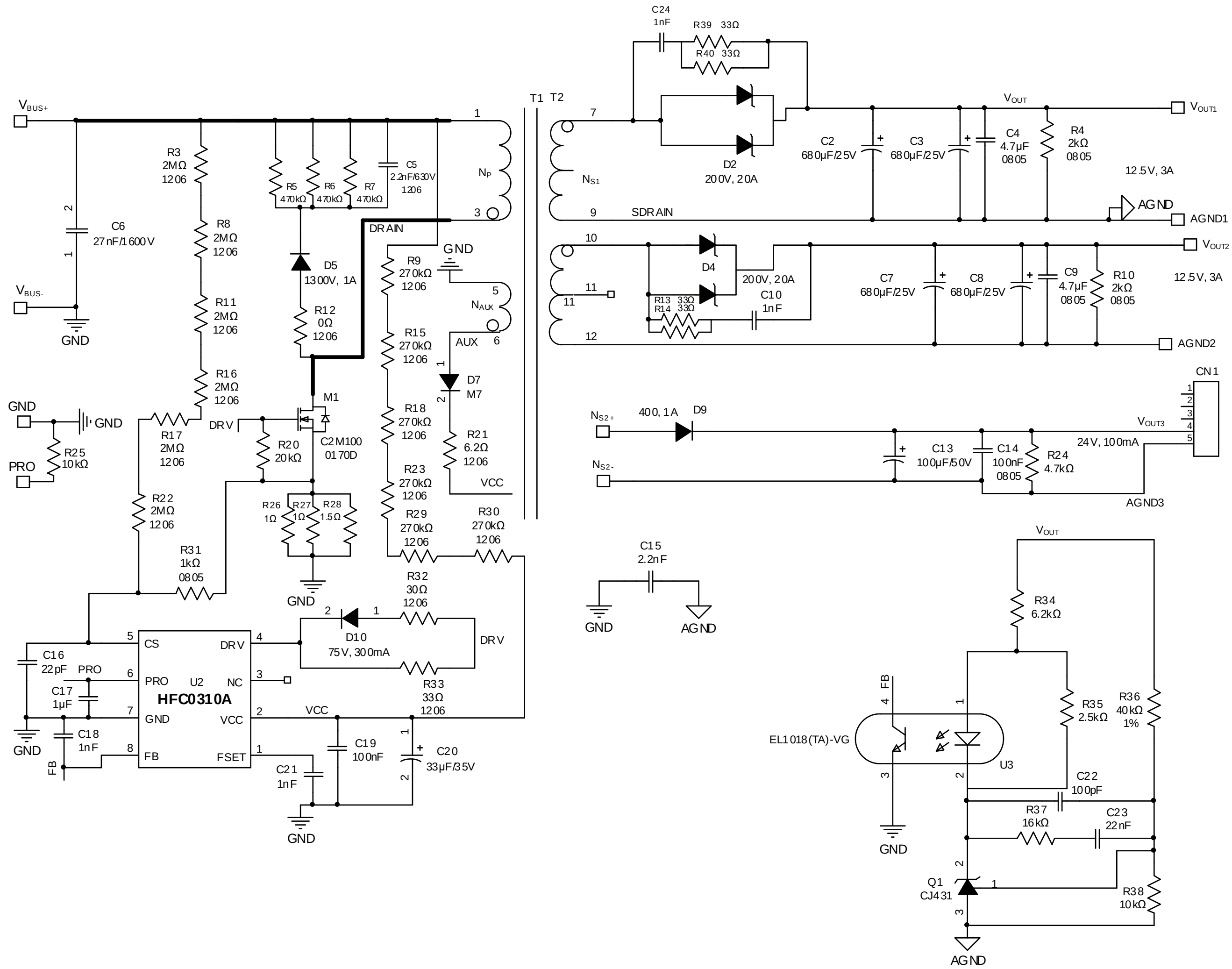


Figure 13: Typical Application Circuit

FLOWCHART

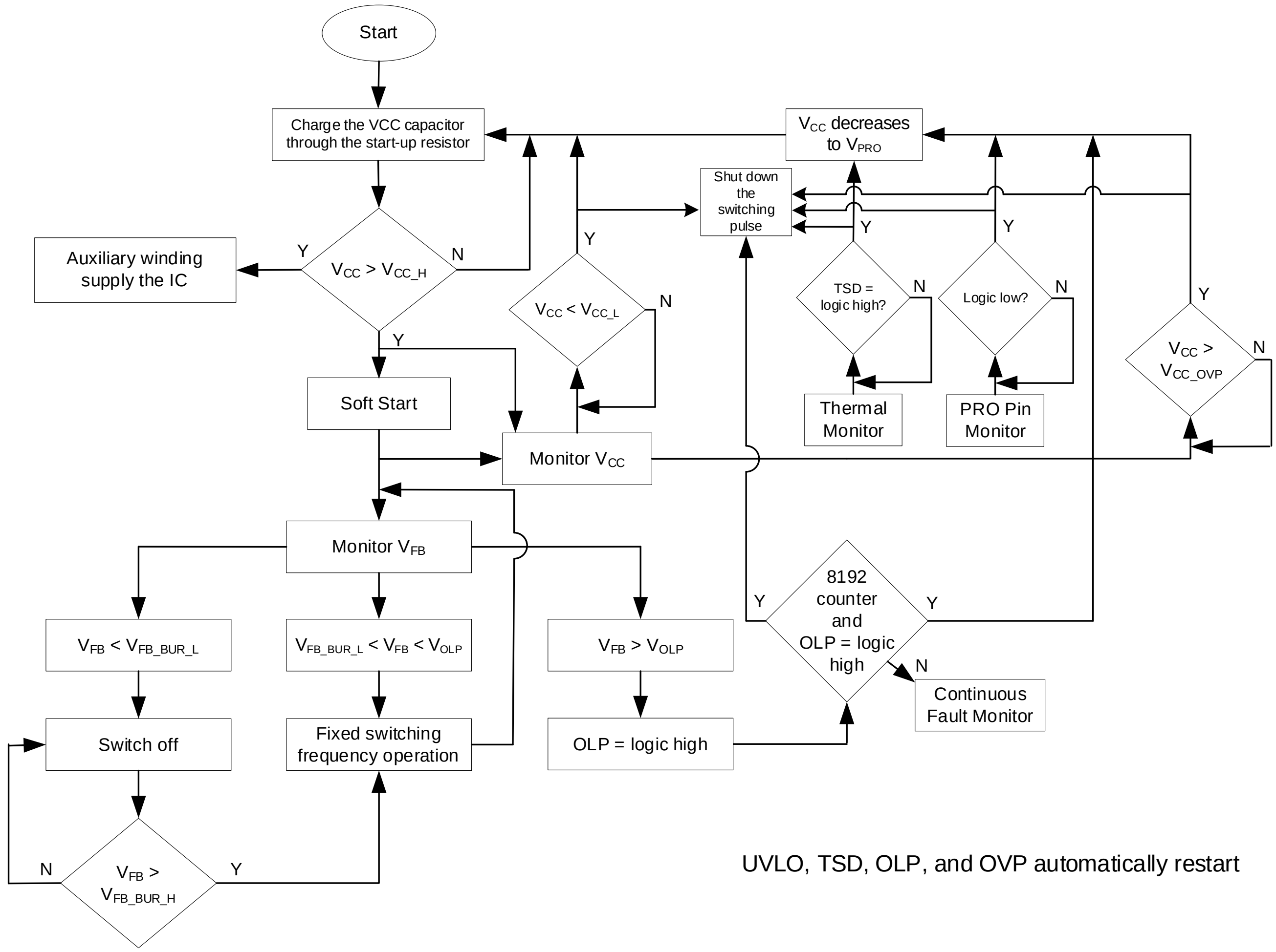


Figure 14: HFC0310A Logic Flowchart

SIGNAL EVOLUTION IN THE PRESENCE OF FAULTS

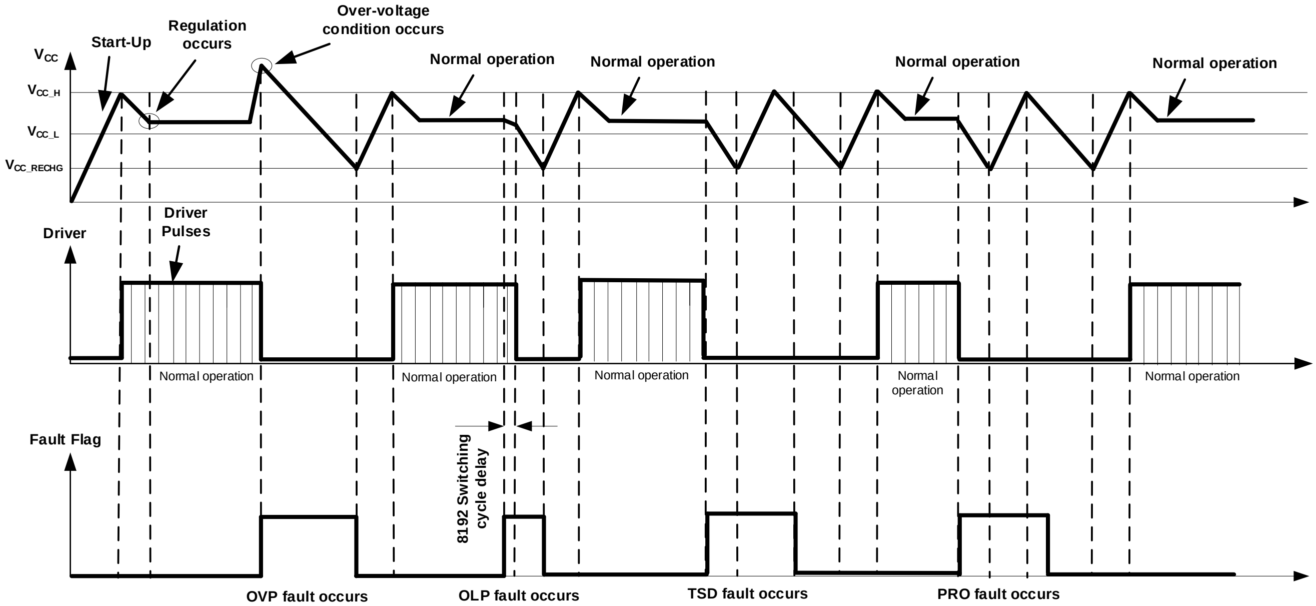
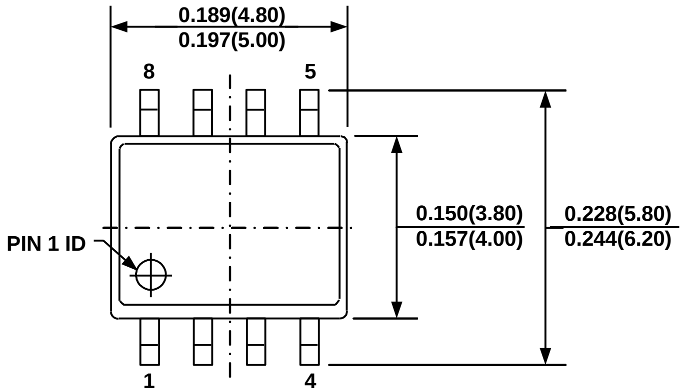


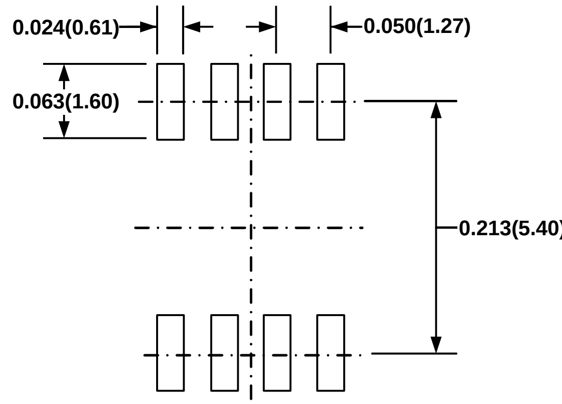
Figure 15: HFC0310A Protection Performance

PACKAGE INFORMATION

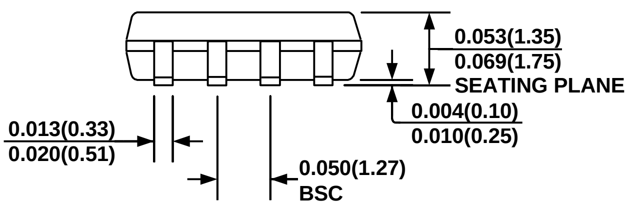
SOIC-8



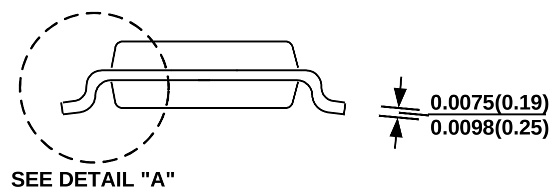
TOP VIEW



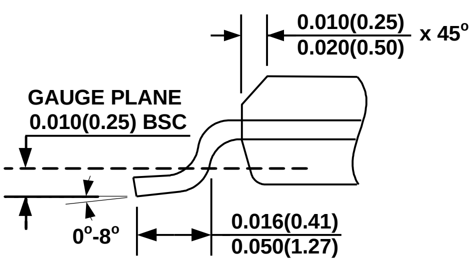
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

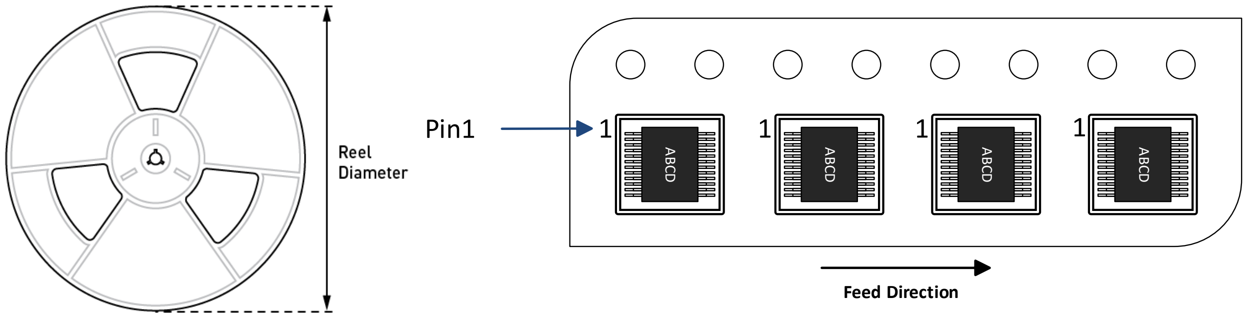


DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
HFC0310AGS-Z	SOIC-8	2500	100	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	1/15/2025	Initial Release	-