



The Future of Analog IC Technology®

# HFC0100

## Quasi-Resonant Controller

### DESCRIPTION

The HFC0100 is a peak current mode controller with green mode operation. It offers high efficiency across over the entire line and load range, and meet stringent worldwide energy efficiency requirements.

The HFC0100 is integrated with a high-voltage current source, and its valley detector ensures minimum drain-source voltage switching (quasi-resonant operation). When the output power falls below a set level, the controller enters burst mode.

The HFC0100 features protection features including thermal shutdown (TSD),  $V_{CC}$  under-voltage lockout (UVLO), overload protection (OLP), and over-voltage protection (OVP).

The HFC0100 is available in a compact SOIC-8 package.

### FEATURES

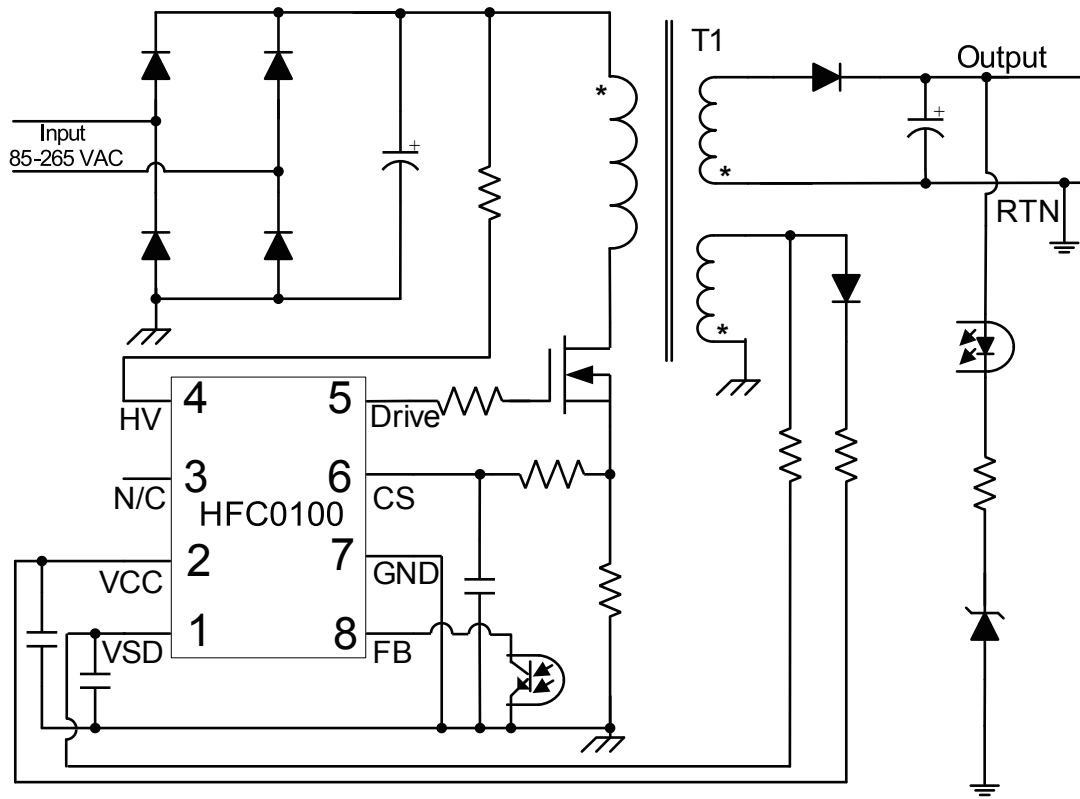
- Universal Main Input Voltage (85V<sub>AC</sub> to 265V<sub>AC</sub>)
- Quasi-Resonant Operation
- Valley Switching for High Efficiency and EMI Minimization
- Active Burst Mode for Low Standby Power Consumption
- Internal High-Voltage Current Source
- High Level of Integration Decreases Required External Component Count
- Maximum Frequency Limit
- Internal Soft Start
- Internal 250nS Leading-Edge Blanking
- Thermal Shutdown (Auto-Restart with Hysteresis)
- $V_{CC}$  Under-Voltage Lockout with Hysteresis (UVLO)
- Over-Voltage Protection
- Overload Protection
- Available in an SOIC-8 Package

### APPLICATIONS

- Battery Chargers for Cell Phones, Digital Cameras, Video Cameras, Electric Shavers, Emergency Lighting Systems, etc.
- Standby Power Supplies for CRT TVs, Projection TVs, LCD TVs, PDP TVs, Desktop PCs, Audio Systems, etc.
- SMPS for Ink Jet Printers, DVD Players/Recorders, VCRs, CD Players, Set-Top Boxes, Air Conditioners, Refrigerators, Washing Machines, Dishwashers, NB Adapters, etc.

All MPS parts are lead-free, halogen free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. "MPS", the MPS logo, and "Simple, Easy Solutions" are registered trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

TYPICAL APPLICATION



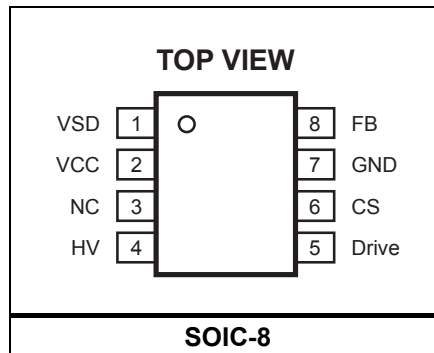
### ORDERING INFORMATION

Part Number*	Package	Top Marking	Ambient Temperature (T <sub>A</sub> )
HFC0100HS	SOIC-8	HFC0100	-40°C to +125°C

\*For Tape & Reel, add suffix -Z (e.g. HFC0100HS-Z).

For RoHS compliant packaging, add suffix -LF (e.g. HFC0100HS-LF-Z).

### PACKAGE REFERENCE



#### ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

HV breakdown voltage.....	-0.7V to +700V
V <sub>CC</sub> , DRV to GND.....	-0.3V to +22V
FB, CS, VSD to GND.....	-0.3V to +7V
Continuous power dissipation...(T <sub>A</sub> = 25°C) <sup>(2)</sup>	1.3W
Junction temperature .....	150°C
Thermal shutdown .....	150°C
Thermal shutdown hysteresis.....	50°C
Lead temperature.....	260°C
Storage temperature .....	-60°C to +150°C

#### ESD Ratings

Human body model (all pins except HV) .....	2kV
Machine model.....	200V

#### Recommended Operation Conditions <sup>(3)</sup>

Operating V <sub>CC</sub> range .....	8V to 20V
Maximum junction temp (T <sub>J</sub> ) .....	125°C

Thermal Resistance <sup>(4)</sup>	$\theta_{JA}$	$\theta_{JC}$
SOIC-8 .....	96	45 ... °C/W

#### Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature T<sub>J</sub> (MAX), the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature T<sub>A</sub>. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P<sub>D</sub> (MAX) = (T<sub>J</sub> (MAX) - T<sub>A</sub>) /  $\theta_{JA}$ . Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operating conditions.
- Measured on JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

Typical values at  $T_J = 25^\circ\text{C}$ , unless otherwise noted.

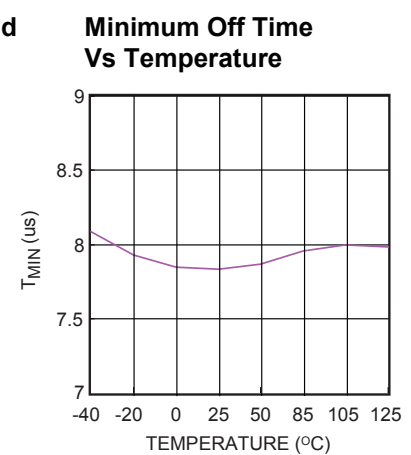
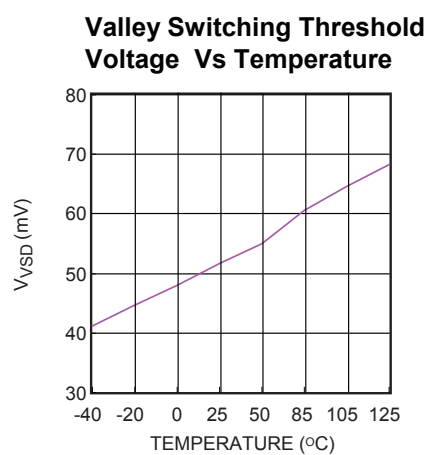
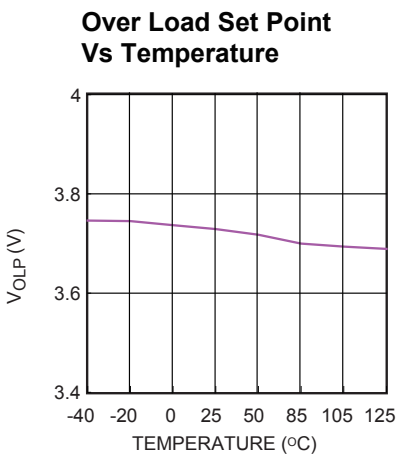
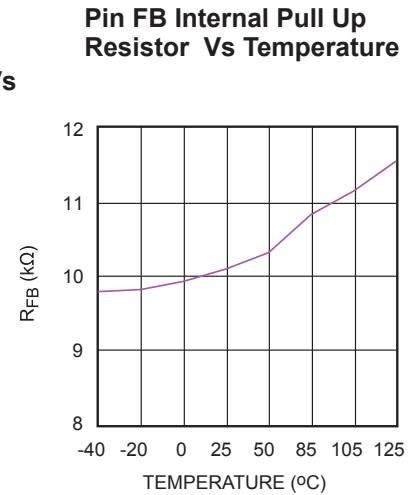
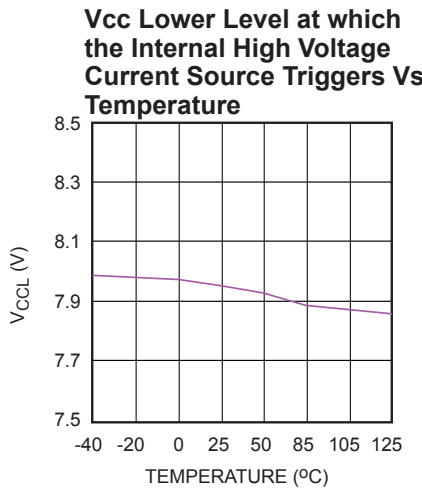
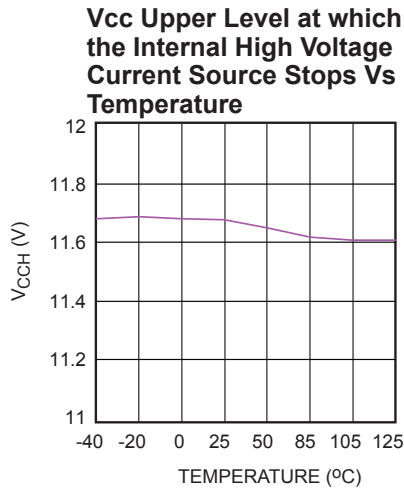
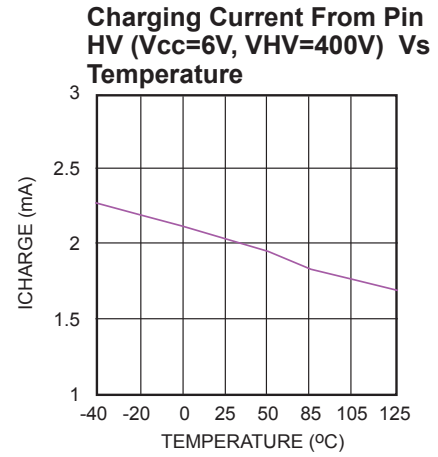
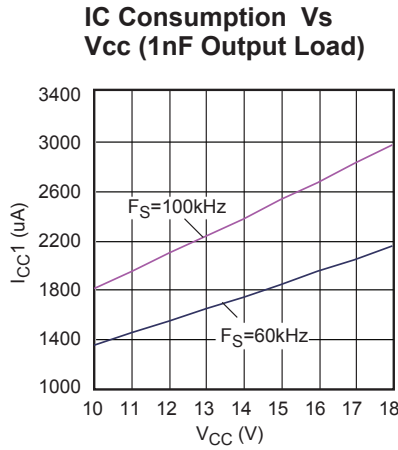
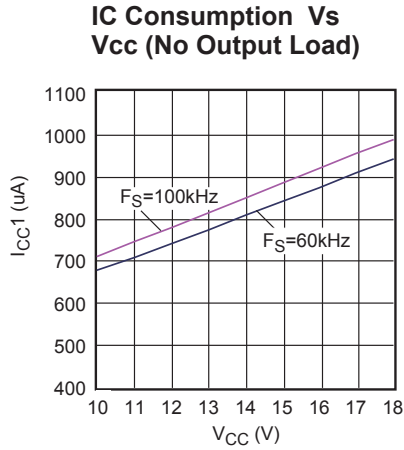
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>Start-Up Current Source (HV Pin)</b>						
HV charging current	$I_{\text{CHARGE}}$	$V_{\text{CC}} = 6\text{V}$ , $V_{\text{HV}} = 400\text{V}$	1.4	2	2.6	mA
HV leakage current	$I_{\text{LEAK}}$	With auxiliary supply, $V_{\text{HV}} = 400\text{V}$ , $V_{\text{CC}} = 13\text{V}$		20		$\mu\text{A}$
Breakdown voltage	$V_{\text{BR}}$		700			V
<b>Supply Voltage Management (VCC Pin)</b>						
VCC upper level at which the internal high-voltage current source stops	$V_{\text{CCH}}$		10.6	11.8	13	V
VCC lower level at which the internal high-voltage current source triggers	$V_{\text{CCL}}$		7.2	8	8.8	V
VCC recharge level at which the protection occurs	$V_{\text{CCP}}$			5.5		V
Internal IC consumption, 1nF load on the DRIVE pin	$I_{\text{CC1}}$	$f_{\text{sw}} = 100\text{kHz}$ , $V_{\text{CC}} = 12\text{V}$		2.0		mA
Internal IC consumption, latch-off phase	$I_{\text{CC2}}$	$V_{\text{CC}} = 6\text{V}$		450		$\mu\text{A}$
<b>Feedback Management (FB Pin)</b>						
Internal pull-up resistor	$R_{\text{FB}}$			10		k $\Omega$
Internal pull-up voltage	$V_{\text{UP}}$			4.5		V
FB pin to current limit division ratio	$I_{\text{DIV}}$			3		
Internal soft-start time	$t_{\text{SS}}$			2.4		ms
FB decreasing level at which the controller enters burst mode	$V_{\text{BURL}}$			0.5		V
FB increasing level at which the controller exits burst mode	$V_{\text{BURH}}$			0.7		V
Overload set point	$V_{\text{OLP}}$			3.7		V
<b>Valley Switching Management (VSD Pin)</b>						
Valley switching threshold voltage	$V_{\text{VSD}}$		40	55	70	mV
Valley switching hysteresis	$V_{\text{HYS}}$			10		mV
VSD clamp voltage	$V_{\text{VSDH}}$	High State; $I_{\text{pin2}}=3.0\text{mA}$	7	7.5	8	V
	$V_{\text{VSDL}}$	Low State; $I_{\text{pin2}}=-2.0\text{mA}$	-0.8	-0.65	-0.5	
Valley switching propagation delay	$t_{\text{VSD}}$	Pull down from 2V to -100mV	100	160	200	ns
Minimum off time	$t_{\text{MIN}}$		6.6	7.8	9	$\mu\text{s}$
Restart time after last valley detection transition	$t_{\text{RESTART}}$			4.6		$\mu\text{s}$
OVP sampling delay	$t_{\text{OVPS}}$			3.5		$\mu\text{s}$
VSD OVP reference level	$V_{\text{OVP}}$			6		V
Internal impedance	$R_{\text{INT}}$			24		k $\Omega$
<b>Current-Sense Management (CS Pin)</b>						
Leading-edge blanking time	$t_{\text{LEB}}$			250		ns
<b>Driving Signal (DRIVE Pin)</b>						
Sourcing resistor	$R_{\text{H}}$			17		$\Omega$
Sinking resistor	$R_{\text{L}}$			7		$\Omega$

**PIN FUNCTIONS**

Pin #	Name	Description
1	VSD	<b>Auxiliary flyback signal input.</b> This pin ensures discontinuous operation and valley switching. It also offers fixed over-voltage protection (OVP) detection.
2	VCC	<b>Supply voltage.</b> This pin is connected to an external bulk capacitor (typically 22 $\mu$ F) and a ceramic capacitor (typically 0.1 $\mu$ F).
3	NC	<b>No connection.</b> This pin ensures an adequate creepage distance.
4	HV	<b>Input for the start-up current unit.</b>
5	DRIVE	<b>Driving signal output.</b>
6	CS	<b>Current-sense input.</b>
7	GND	<b>Ground.</b>
8	FB	<b>Feedback.</b> This pin sets the peak current limit. Connect an optocoupler to FB. A 3.7V feedback voltage ( $V_{FB}$ ) triggers overload protection, and a 0.5V $V_{FB}$ triggers burst mode operation.

## TYPICAL PERFORMANCE CHARACTERISTICS

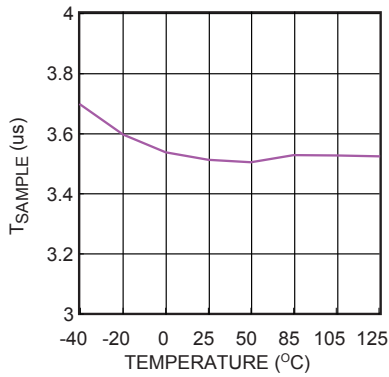
$T_A = 25^\circ\text{C}$ , unless otherwise noted.



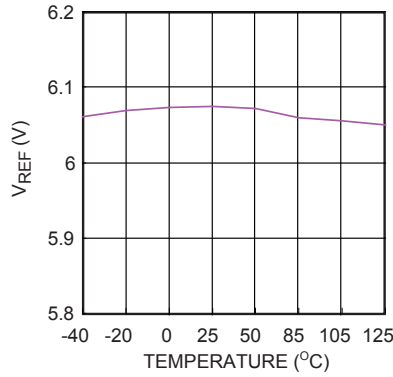
**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

T<sub>A</sub> = 25°C, unless otherwise noted.

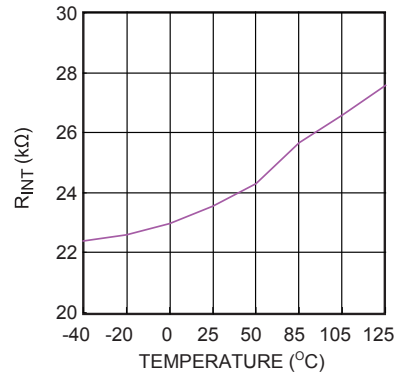
**OVP Sampling Delay Vs Temperature**



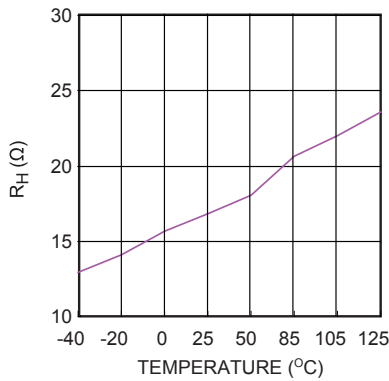
**Pin VSD OVP reference level Vs Temperature**



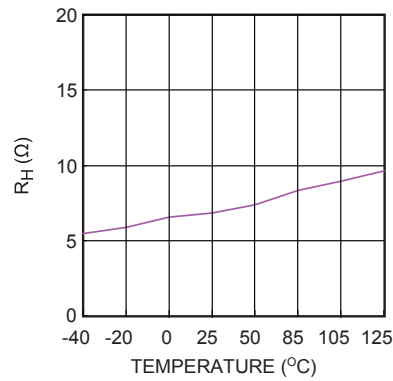
**Pin VSD Internal Impedance Vs Temperature**



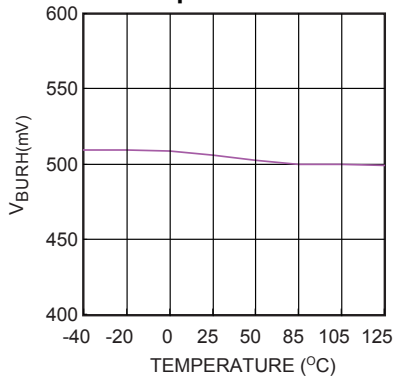
**Sourcing Resistor Vs Temperature**



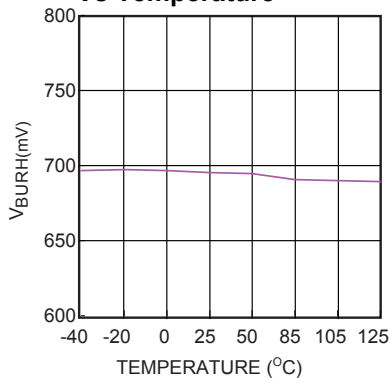
**Sinking Resistor Vs Temperature**



**FB Decreasing Level at which the controller enter the Burst Mode Vs Temperature**



**FB Increasing Level at which the controller leave the Burst Mode Vs Temperature**



FUNCTIONAL BLOCK DIAGRAM

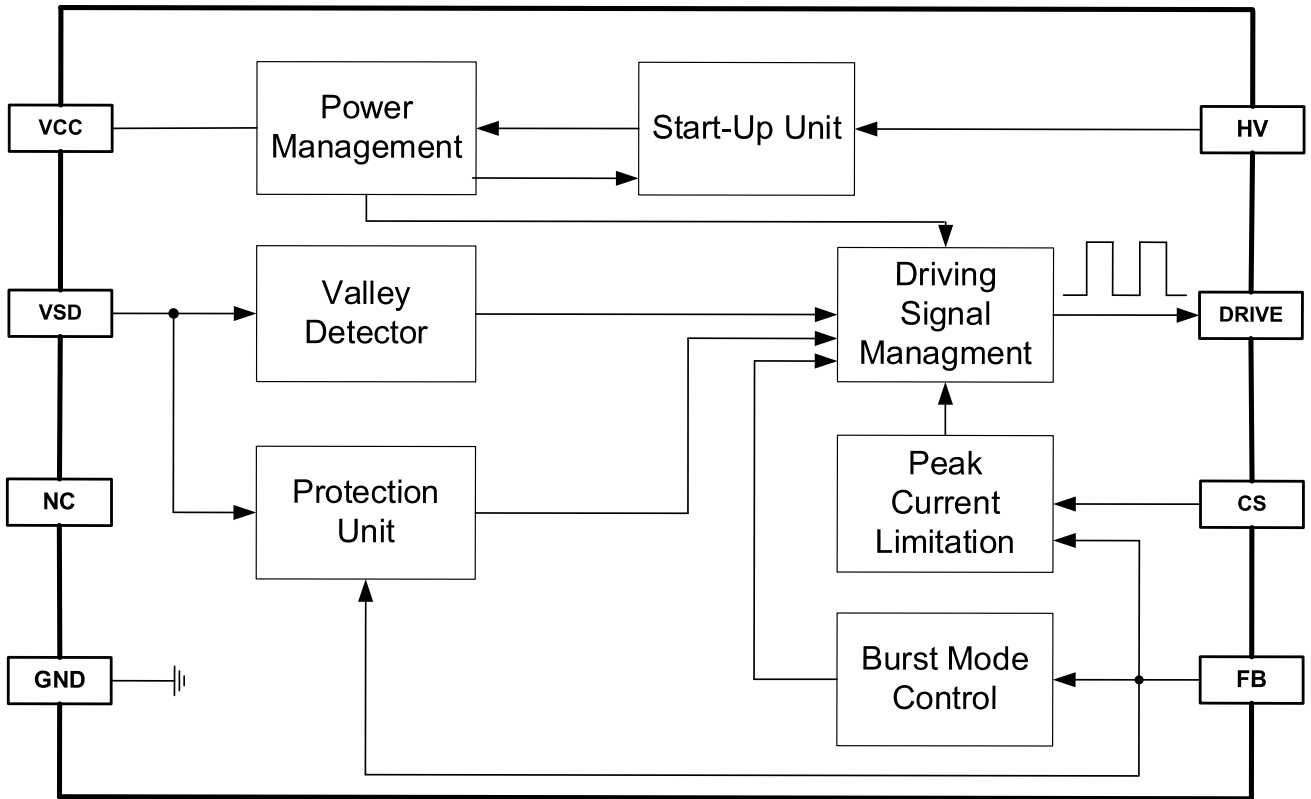


Figure 1: Functional Block Diagram



**OPERATION**

The HFC0100 incorporates all the necessary features needed for a reliable switch-mode power supply. Its valley detection feature ensures minimum drain-source voltage switching (quasi-resonant operation). When the output power falls below a set level, the regulator enters the burst mode. An internal minimum off time limit prevents the frequency from exceeding 150kHz.

**Start-Up**

Initially, the IC is self-supplied from the internal high-voltage current source unit, which draws from the HV pin. The IC starts switching and turns off the internal high-voltage current source unit as soon as the voltage on the VCC pin reaches the V<sub>CCH</sub> threshold (11.8V).

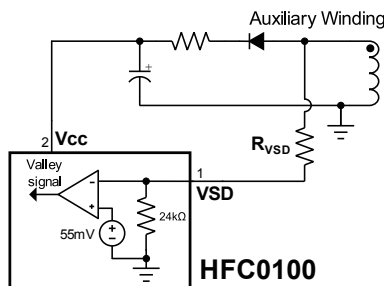
To start up the IC, the VCC ramping up slew rate should be slower than 2V/ms before V<sub>CC</sub> reaches 2V. Taking into account the internal current source capability, a minimum 4.7µF capacitor is required. In addition, the VCC capacitor should be able to maintain the VCC level over V<sub>CCL</sub> (8V) before the FB level down to V<sub>OLP</sub> (3.7V). This ensures that the start-up process is not interrupted by overload protection (OLP) detection.

**Quasi-Resonant Operation**

The HFC0100 operates in discontinuous conduction mode (DCM). Valley detection ensures minimum drain-source voltage switching (quasi-resonant operation).

As a result, there are virtually no primary switch turn-on losses and no secondary diode recovery losses. This helps reduce EMI noise.

Figure 2 shows the valley detection unit.



**Figure 2: Valley Detection**

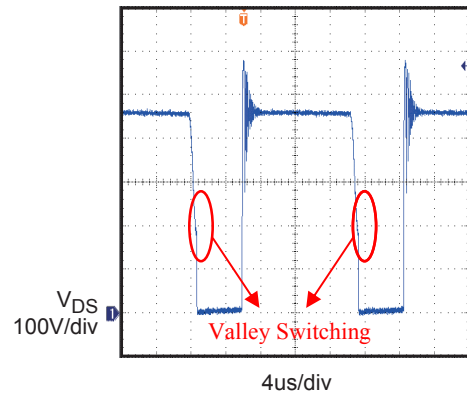
The voltage conditions for valley detection can be calculated with Equation (1):

$$(V_{DS} - V_{in}) \times \frac{N_{aux}}{N_{pri}} \times \frac{24k\Omega}{24k\Omega + R_{VSD}} < 55mV \quad (1)$$

Where V<sub>DS</sub> is the drain-source voltage of the primary FET, V<sub>IN</sub> is the input voltage, N<sub>AUX</sub> is the auxiliary winding turns of the transformer, and N<sub>PRI</sub> is the primary winding turns of the transformer.

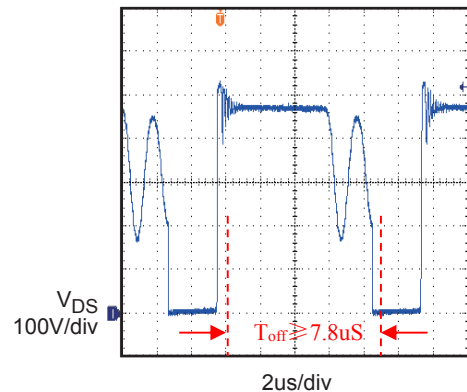
The valley detector sends out a valley signal to turn on the primary FET.

Figure 3 shows a typical drain-source voltage waveform with valley switching.



**Figure 3: V<sub>DS</sub> with Valley Switching**

To ensure the switching frequency remains below the EN5022 start limit (150kHz), the HFC0100 employs a 7.8µs internal minimum off time limit (see Figure 4).

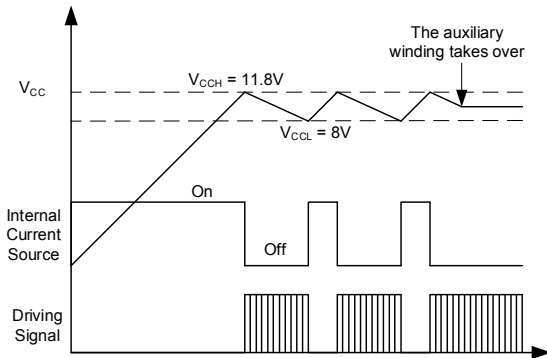


**Figure 4: Minimum Off Time Limit**

**V<sub>CC</sub> Under-Voltage Lockout (UVLO)**

When V<sub>CC</sub> falls below the UVLO threshold (V<sub>CCL</sub> - 8V), the HFC0100 stops switching. The internal high-voltage current source unit also restarts, and the V<sub>CC</sub> external bulk capacitor is recharged by it.

Figure 5 shows the typical waveform with V<sub>CC</sub> under-voltage lockout.

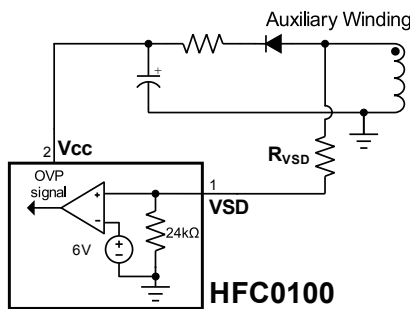


**Figure 5: V<sub>CC</sub> Under-Voltage Lockout**

**Over-Voltage Protection (OVP)**

If positive plateau of the auxiliary winding voltage is proportional to the output voltage (V<sub>OUT</sub>), then over-voltage protection (OVP) is triggered and the HFC0100 uses the auxiliary winding voltage instead of directly monitoring V<sub>OUT</sub>.

Figure 6 shows the OVP sample unit.



**Figure 6: OVP Sample Unit**

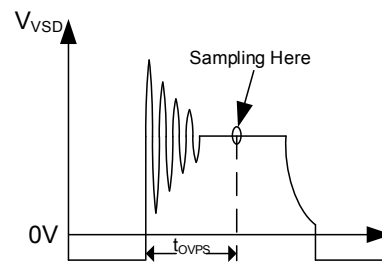
V<sub>OUT</sub> can be calculated with Equation (2):

$$V_O \times \frac{N_{aux}}{N_{SEC}} \times \frac{24k\Omega}{24k\Omega + R_{VSD}} > 6V \quad (2)$$

Where V<sub>OUT</sub> is the output voltage, N<sub>AUX</sub> is the auxiliary winding turns of the transformer, and N<sub>SEC</sub> is the secondary winding turns of the transformer.

If the OVP circuit is triggered, the HFC0100 stops switching and latches off. The controller remains latched off until V<sub>CC</sub> falls to 3V, e.g. when the user unplugs the power supply from the main supply and replugs it in.

To avoid an accidental mistrigger due to the oscillation of the leakage inductance and the parasitic capacitance, the OVP sampling has a t<sub>OVPS</sub> blanking time (typically 3.5μs) (see Figure 7).



**Figure 7: t<sub>OVPS</sub> Blanking Time**

**Overload Protection (OLP)**

The maximum output power is limited by the maximum switching frequency and the maximum primary peak current. If the output consumes more than the maximum output power, V<sub>OUT</sub> is drawn below the set point. This reduces the current through the optocoupler LED, which also reduces the transistor current, thus increases the FB voltage (V<sub>FB</sub>).

V<sub>FB</sub> is continuously monitored. If V<sub>FB</sub> exceeds the threshold (V<sub>OLP</sub> = 3.7V), the HFC0100 shuts off the switching cycle. The device enters a safe low-power mode operation that prevents any serious thermal or stress damage to the part. Once the fault is removed, the devices resumes normal operation.

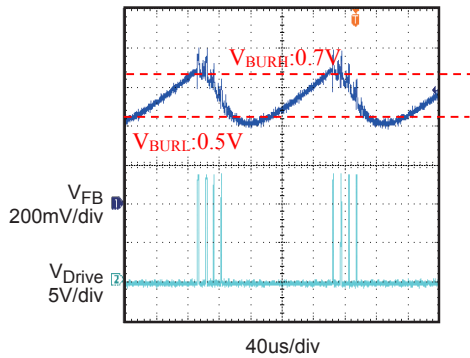
During start-up or load transient, V<sub>FB</sub> can rise high enough temporarily to mistrigger overload protection (OLP). To prevent this, the OLP circuit is designed to be triggered only after V<sub>CC</sub> falls below (V<sub>CCL</sub> = 8V).

**Burst Operation**

To minimize the power dissipation under no-load and light-load conditions, the HFC0100 enters burst mode operation.

As the load decreases,  $V_{FB}$  decreases. The HFC0100 stops switching if  $V_{FB}$  drops below the threshold ( $V_{BURL} = 0.5V$ ).  $V_{OUT}$  then starts to drop at a rate that is proportional to the load, which causes  $V_{FB}$  to rise again. Once  $V_{FB}$  exceeds the threshold ( $V_{BURH} = 0.7V$ ), switching resumes.  $V_{FB}$  then falls and rises repeatedly. Burst mode operation alternately enables and disables switching cycle of the MOSFET, thereby reducing switching loss under no-load and light-load conditions.

Figure 8 shows the typical FB and DRIVE waveform during the burst mode.



**Figure 8: Burst Mode**

**Thermal Shutdown (TSD)**

To protect the device from serious thermal damage, the HFC0100 shuts down switching if the inner temperature exceeds 150°C. Once the inner temperature drops below 100°C, the device resumes normal operation.

**Soft Start**

To reduce stress on the primary MOSFET and secondary diode during start-up and to smoothly establish  $V_{OUT}$ , the HFC0100 has an internal soft-start circuit that increases the current comparator inverting the input voltage and the MOSFET current slowly after the device starts up. The pulse width is progressively increased to establish the correct working conditions for the transformers, inductors, and capacitors.

**Current Limit Setting**

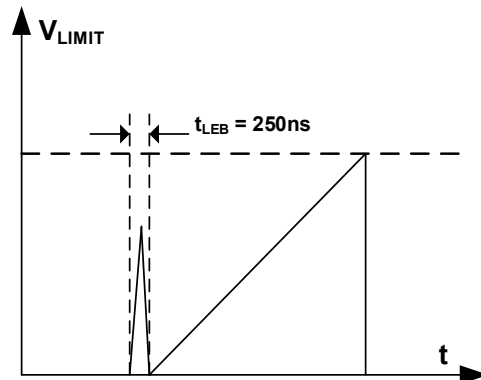
The switching current is sensed by the resistor series between the source of the FET and ground. The current limit is determined by the FB signal, calculated with Equation (3):

$$V_{LIMIT} = \frac{V_{FB}}{I_{DIV}} = \frac{V_{FB}}{3} \tag{3}$$

To limit the maximum output power, the current limit is clamped at 1V when  $V_{FB}$  is above 3.3V.

**Leading-Edge Blanking Time**

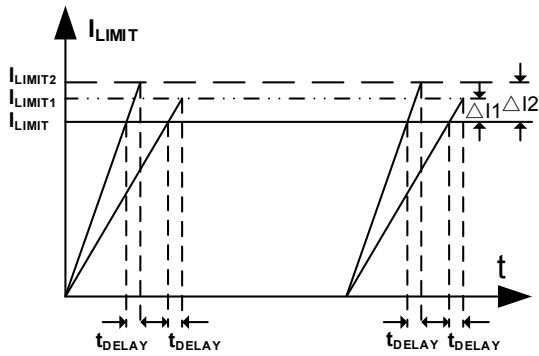
In order to avoid premature termination of the switching pulse due to the parasitic capacitance, an internal leading-edge blanking (LEB) unit is employed between the CS pin and the current comparator input. During this blanking time ( $t_{LEB}$ ), the path from the CS pin to the current comparator input is blocked. Figure 9 shows the leading-edge blanking time.



**Figure 9: Leading-Edge Blanking Time**

**Over-Power Compensation**

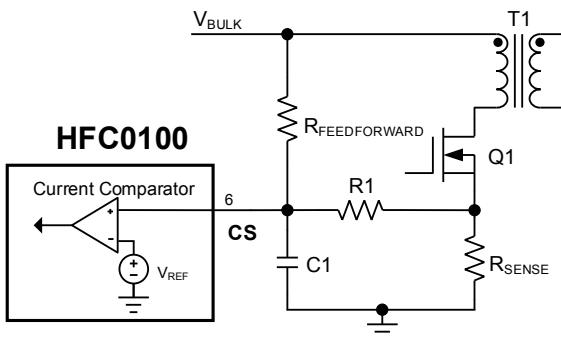
In the case of current sensing, the FET turning is delayed due to the control circuit's propagation delay. The delay time ( $t_{DELAY}$ ) is the inherent characteristic of the control circuit (see Figure 10).



**Figure 10: Current Limit Propagation Delay**

This delay can cause an overshoot of the peak current.  $\Delta I2$  is greater than  $\Delta I1$  due to the greater rising ratio (the higher the input voltage, the greater the rising ratio).

The propagation delay is set by the feedforward resistor (see Figure 11). This method allows the user to add an offset voltage at the CS pin (the higher the input voltage, the greater the offset voltage).



**Figure 11: Over-Power Compensation**

Figure 12 on page 13 shows the HFC0100's control flowchart. Figure 13 on page 14 shows the signal evolution in the presence of faults in the HFC0100.

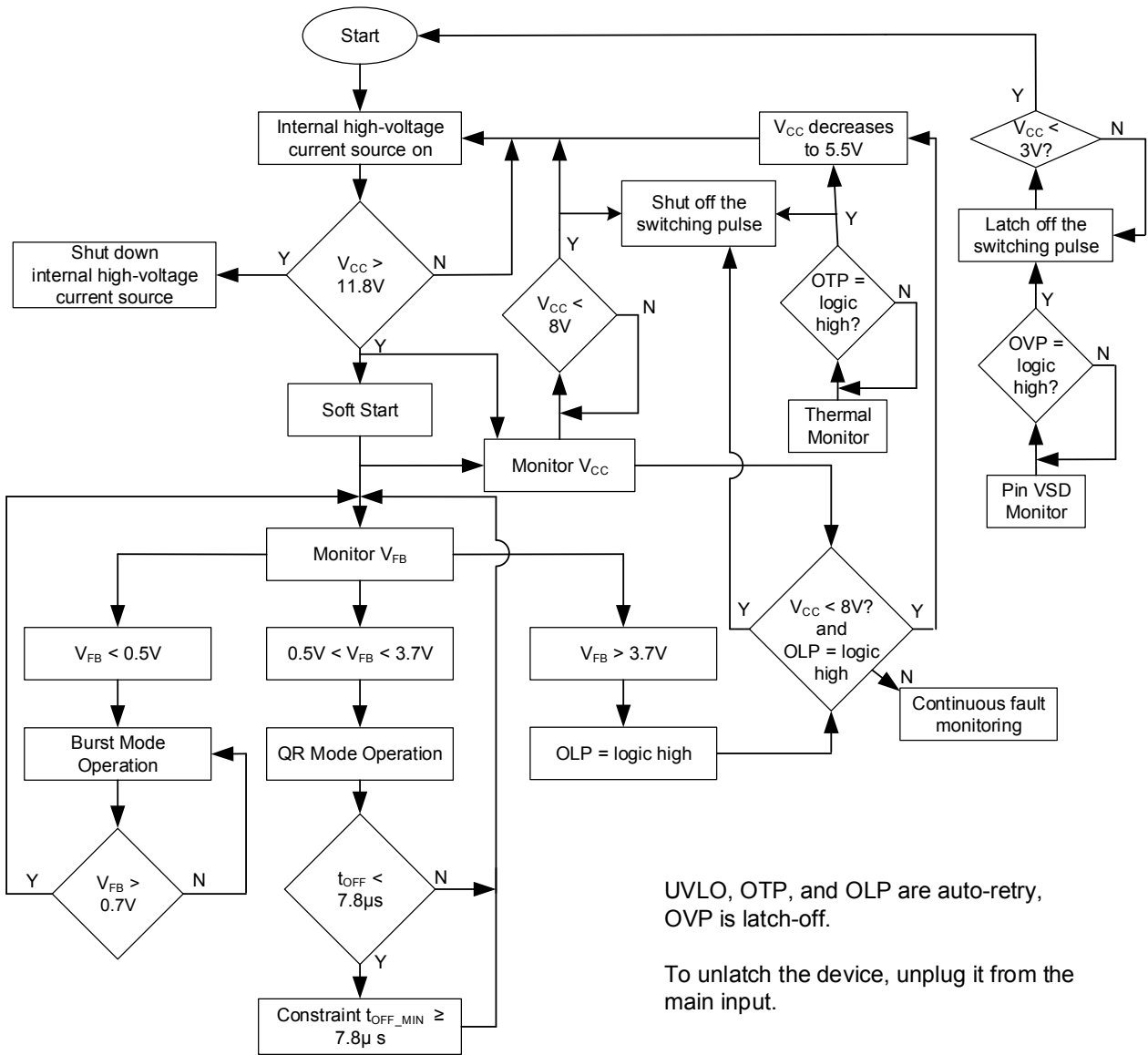


Figure 12: Control Flowchart

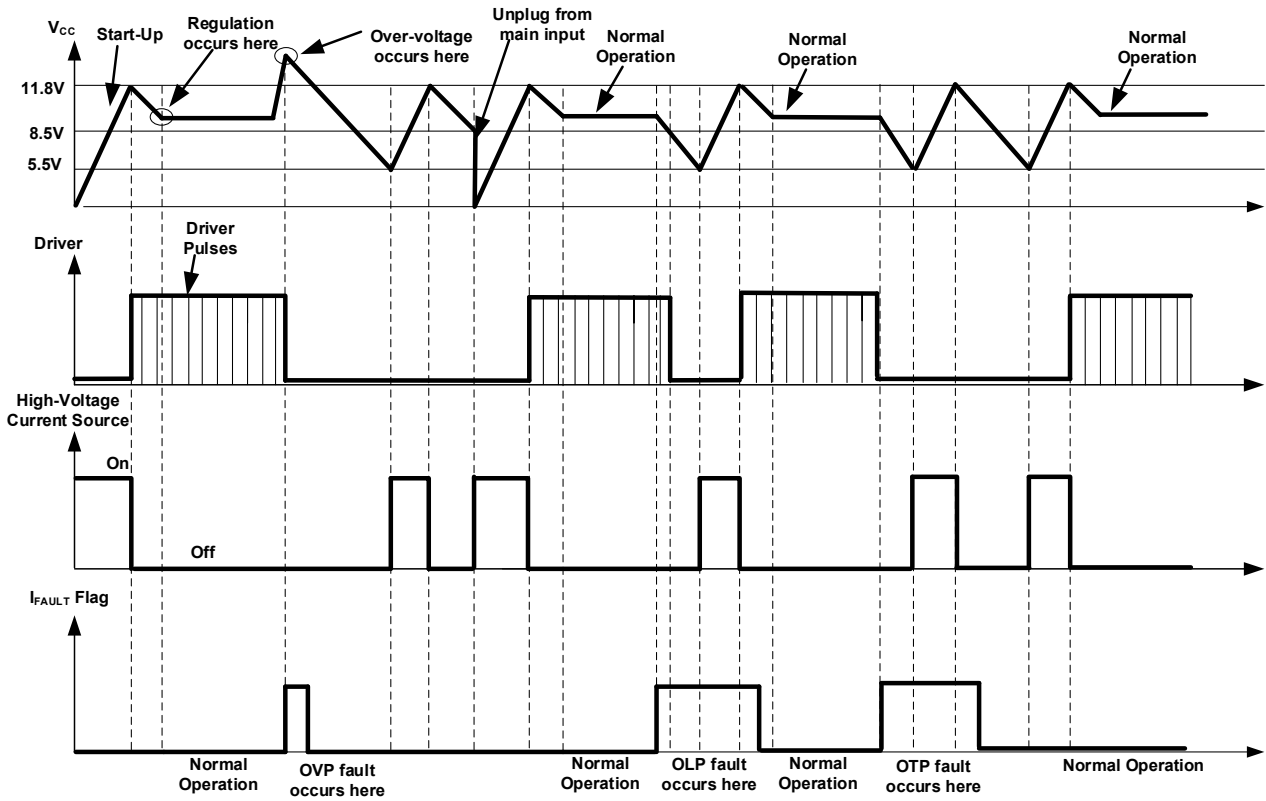
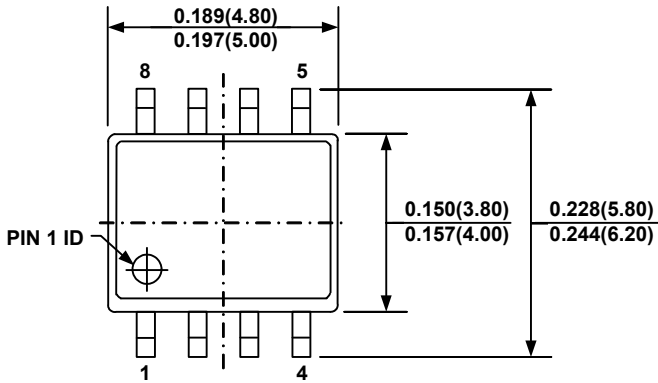
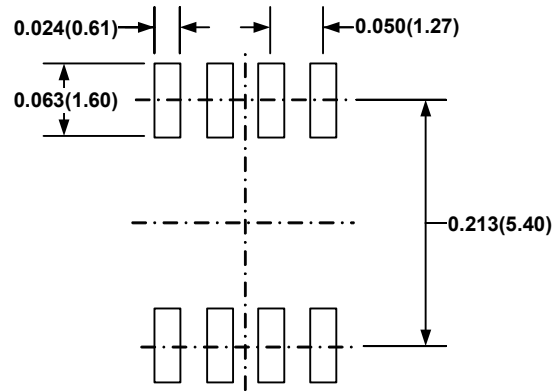
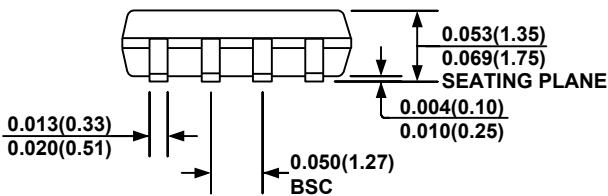
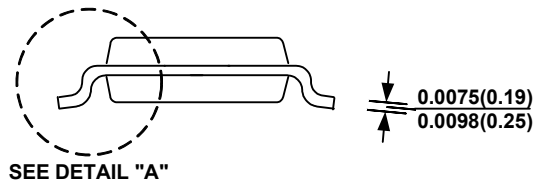
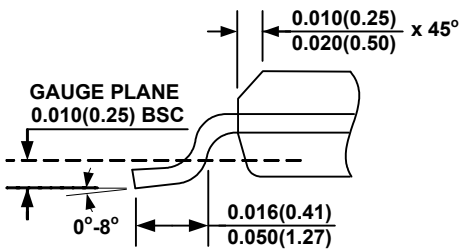


Figure 13: Signal Evolution in the Presence of Faults

**PACKAGE INFORMATION**
**SOIC-8**

**TOP VIEW**

**RECOMMENDED LAND PATTERN**

**FRONT VIEW**

**SIDE VIEW**

**DETAIL "A"**
**NOTE:**

- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
- 6) DRAWING IS NOT TO SCALE.

**REVISION HISTORY**

Revision #	Revision Date	Description	Pages Updated
1.0	01/05/2011	Initial Release	-
1.01	02/13/2011	Updated the MOSFET BV voltage from 650V to 700V.	3, 4
1.02	11/25/2015	Limited the $t_{VSD}$ minimum value to 100ns.	4
1.03	11/28/2017	Corrected the top marking.	3
1.04	08/06/2019	Added some application key points in the Start-Up section: "To start up the IC, the VCC ramping up slew rate should be slower than 2V/ms before $V_{CC}$ reaches 2V. Taking into account the internal current source capability, a minimum 4.7 $\mu$ F capacitor is required."	9
1.05	10/28/2021	Added some application key points in the Start-Up section: "In addition, the VCC capacitor should be able to maintain the VCC level over $V_{CCL}$ (8V) before the FB level down to $V_{OLP}$ (3.7V). This ensures that the start-up process is not interrupted by overload protection (OLP) detection." Changed the typical VCC threshold for OLP triggering from 8.5V to 8V.	9, 10, 13
		Grammar and formatting updates	All

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