



EVL8883-Q-00A

45V, 3A, High-Efficiency, Digital, Configurable, Synchronous Step-Down Converter Evaluation Board

DESCRIPTION

The EVL8883-Q-00A evaluation board is designed to demonstrate the capabilities of the MP8883, a high-frequency, synchronous, rectified step-down converter with an I²C control interface and multi-page one-time programmable (OTP) memory. The MP8883 can achieve up to 3A of continuous output current (I_{OUT}) across a wide input voltage (V_{IN}) supply range, with excellent load and line regulation.

The MP8883 is designed to be very versatile. The output voltage (V_{OUT}) can be set between

0.8V and 12V via the I²C serial interface. The switching slew rate, switching frequency (f_{sw}), enable (EN) control, and power-save mode can also be configured via the I²C. This allows users to optimize each output for the specific application requirements.

The MP8883 is available in a QFN-16 (3mmx3mm) package. It is recommended to read the MP8883 datasheet prior to making any changes to the EVL8883-Q-00A.

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C, unless otherwise noted.

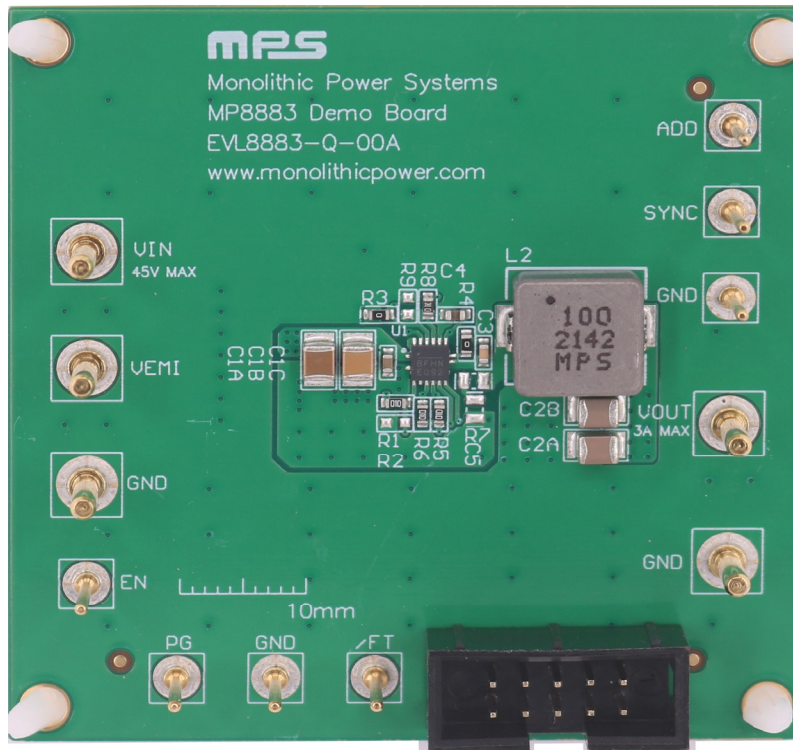
Parameters	Conditions	Value
Input voltage (V _{IN}) range		3.5V to 45V
Output voltage (V _{OUT})	V _{IN} = 3.5V to 45V, I _{OUT} = 0A to 3A	5V ⁽²⁾
Maximum output current (I _{OUT})	V _{IN} = 3.5V to 45V	3A
Full-load efficiency	V _{IN} = 12V, V _{OUT} = 5V, I _{OUT} = 3A, f _{sw} = 500kHz	92.6%
Peak efficiency	V _{IN} = 12V, V _{OUT} = 5V, I _{OUT} = 0.8A, f _{sw} = 500kHz	95.9%
Default switching frequency (f _{sw})		500kHz

Notes:

- 1) For different V_{IN} and V_{OUT} specifications with different inductors, the application circuit parameters may require changes.
- 2) V_{OUT} can be adjusted between 0.8V to 12V via the digital interface. Refer to the MP8883 datasheet for more information.

 Optimized Performance with MPS Inductor MPL-AY1050 Series

EVL8883-Q-00A EVALUATION BOARD



LxWxH (6.35cmx6.35cmx1.8cm)

4 Layers (2oz, 1oz, 1oz, and 2oz)

Board Number	MPS IC Number
EVL8883-Q-00A	MP8883GQ-0001

DEFAULT ONE-TIME PROGRAMMABLE (OTP) CONFIGURATIONS

Table 1 and Table 2 show the default one-time programmable (OTP) memory configurations for the MP8883GQ-0001. Table 1 shows the parameter(s) for the default settings.

Table 1: -0001 Suffix Code Configuration

OTP Items	Values
Digital-to-analog converter (DAC) reference voltage	1V
Feedback (FB) divider ratio	1/5
Output voltage (V_{OUT})	5V
Mode	AAM mode
Short-circuit protection (SCP) mode	Hiccup mode
Soft-start time (t_{SS})	1ms
Switching slew rate (rising)	1V/ns
Switching slew rate (falling)	1V/ns
Valley current limit	4A
Peak current limit	5A
Switching frequency (f_{SW})	500kHz
Over-temperature protection rising threshold	175°C
OTP configuration code	0x0001

Table 2: -0001 Suffix Code Register Values

Suffix Code	Register	Hex Value
0001	0x00	64h
0001	0x01	71h
0001	0x02	0Ah
0001	0x03	1Bh
0001	0x04	40h
0001	0x05	21h
0001	0x06	04h
0001	0x07	8Ah
0001	0x08	04h
0001	0x09	C0h
0001	0x0A	50h
0001	0x0B	88h
0001	0x0C	FFh

QUICK START GUIDE

The EVL8883-Q-00A evaluation board is easy to set up and use to evaluate the performance of the MP8883. Refer to Figure 1 for the proper measurement equipment set-up and follow the guidelines below:

1. Preset the power source (V_{IN}) to be between 3.5V and 45V (typically 12V). ⁽³⁾
2. Turn the power source off.
3. Connect the power source terminals to:
 - a. Positive (+): V_{IN}
 - b. Negative (-): GND
4. Connect the load (no initial load) to:
 - a. Positive (+): V_{OUT}
 - b. Negative (-): GND
5. After making the connections, turn the power supply on. The board should automatically start up.
6. Check for the proper output voltage (V_{OUT}).
7. Once the proper V_{OUT} is established, adjust the load within the operating range and measure the efficiency, output ripple voltage, and any other relevant parameters. ⁽⁴⁾
8. After completing all tests, adjust the load to 0A, then turn the input power supply off.

Notes:

- 3) Ensure that V_{IN} does not exceed 45V.
- 4) When measuring the output or input voltage ripple, do not use the oscilloscope probe's long ground lead.

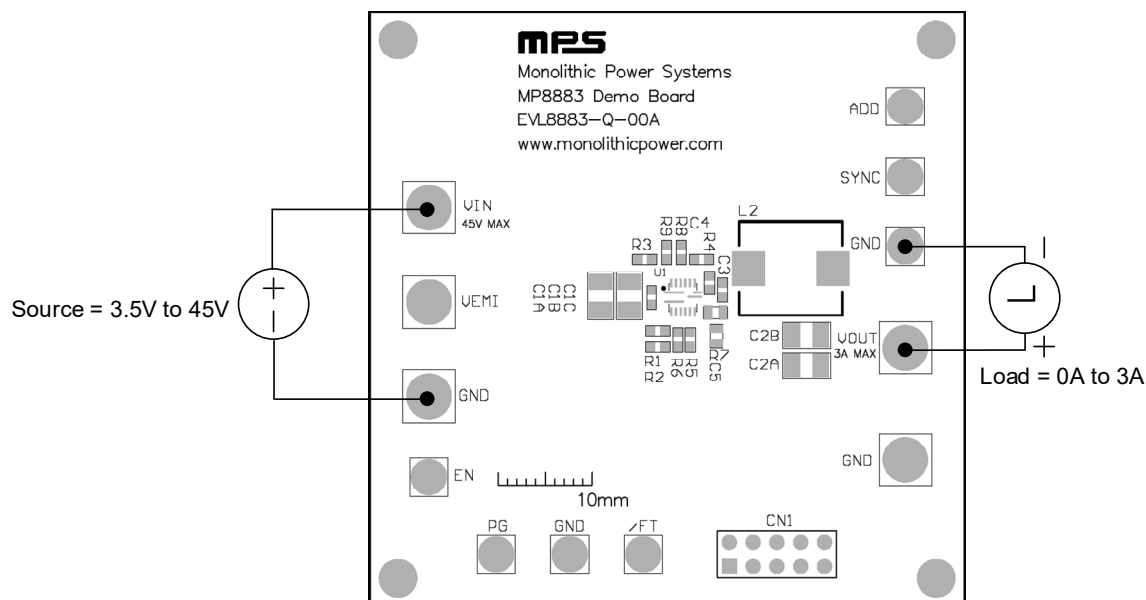


Figure 1: Measurement Equipment Set-Up

EVALUATION BOARD SCHEMATIC

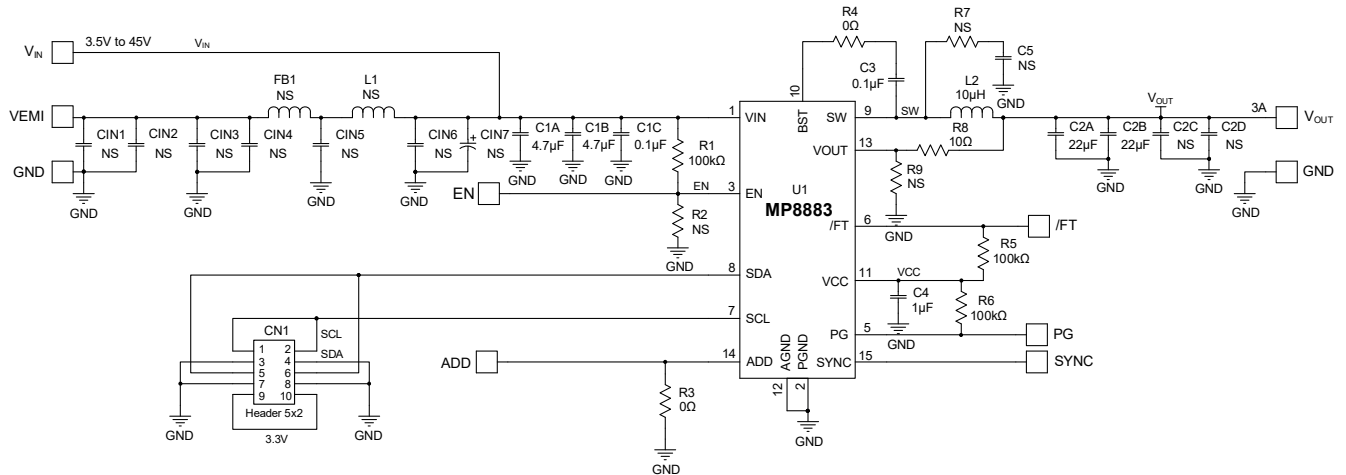


Figure 2: Evaluation Board Schematic

EVL8883-Q-00A BILL OF MATERIALS

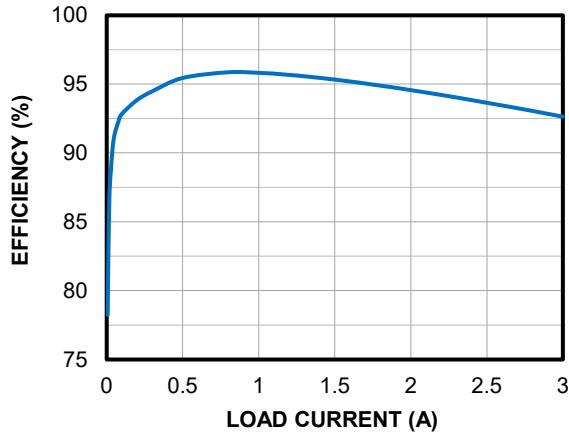
Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
2	L1, FB1	NS				
2	C1A, C1B	4.7 μ F	Ceramic capacitor, 100V, X7S	1210	Murata	GRM32DC72A475KE01L
1	C1C	0.1 μ F	Ceramic capacitor, 100V, X7R	0603	Murata	GRM188R72A104KA35D
2	C2A, C2B	22 μ F	Ceramic capacitor, 16V, X7R	1210	Murata	GRM32ER71C226KEA8L
1	C3	0.1 μ F	Ceramic capacitor, 16V, X7R	0603	Murata	GRM188R71C104KA01D
1	C4	1 μ F	Ceramic capacitor, 25V, X7R	0603	Murata	GRM188R71E105KA12D
10	CIN1, CIN2, CIN3, CIN4, CIN5, CIN6, CIN7, C2C, C2D, C5	NS				
3	R1, R5, R6	100k Ω	Film resistor, 1%	0603	Yageo	RC0603FR-07100KL
2	R3, R4	0 Ω	Film resistor, 1%	0603	Yageo	RC0603FR-070RL
1	R8	10 Ω	Film resistor, 1%	0603	Yageo	RC0603FR-0710RL
3	R2, R7, R9	NS				
1	L2	10 μ H	Inductor, I _{SAT} = 12A, R _{DS} = 19m Ω	1050	MPS	MPL-AY1050-100
1	U1	MP8883	45V, 3A, high-efficiency, synchronous step-down converter	QFN-16 (3mmx3mm)	MPS	MP8883GQ-0001

EVB TEST RESULTS

Performance curves and waveforms are tested on the evaluation board. $V_{IN} = 12V$, $V_{OUT} = 5V$, $L = 10\mu H$, $f_{SW} = 500kHz$, AAM mode, $T_A = 25^\circ C$, unless otherwise noted.

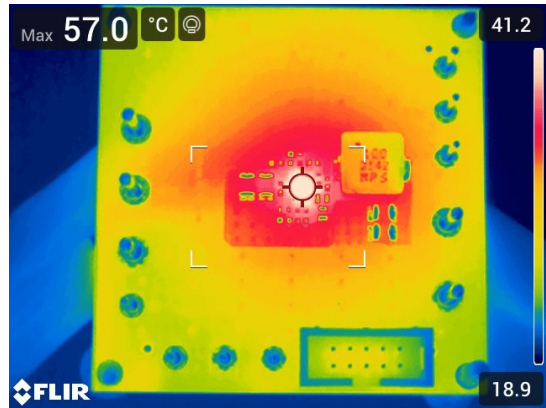
Efficiency vs. Load Current

$L = 10\mu H$, $R_{DC} = 19m\Omega$



Thermal Performance

$I_{OUT} = 3A$, no forced airflow, $T_{CASE} = 57^\circ C$

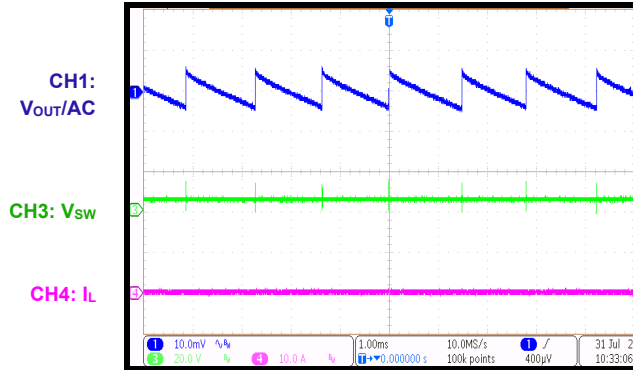


EVB TEST RESULTS (continued)

Performance curves and waveforms are tested on the evaluation board. $V_{IN} = 12V$, $V_{OUT} = 5V$, $L = 10\mu H$, $f_{SW} = 500kHz$, AAM mode, $T_A = 25^\circ C$, unless otherwise noted.

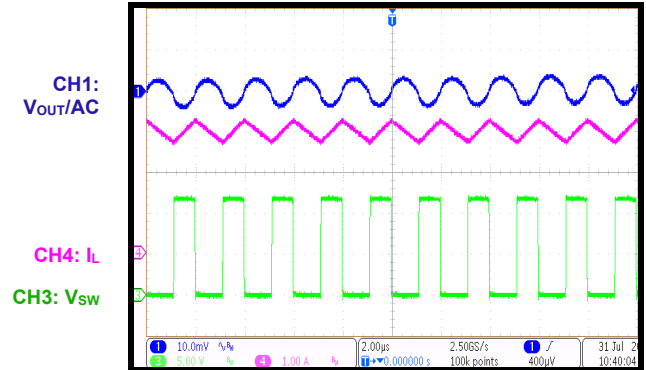
Steady State

$I_{OUT} = 0A$



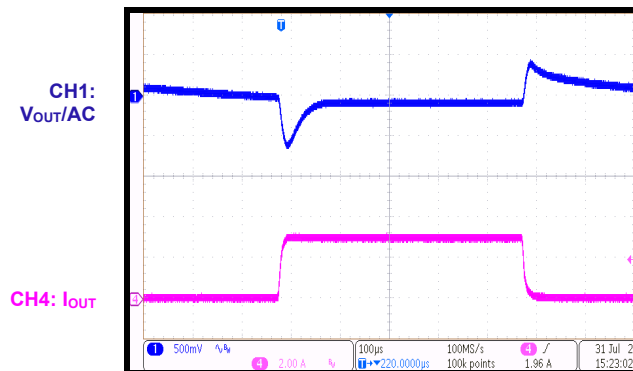
Steady State

$I_{OUT} = 3A$



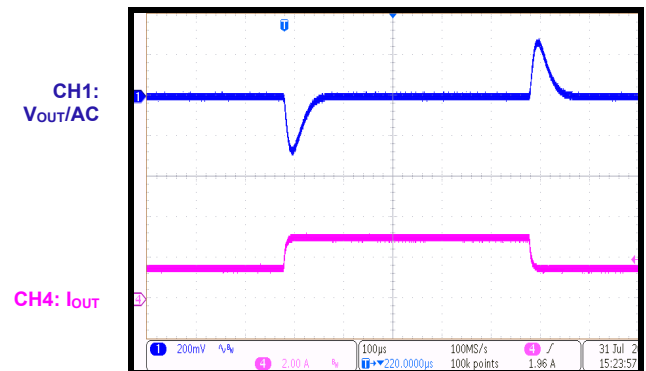
Load Transient

$I_{OUT} = 0A$ to $3A$, $0.8A/\mu s$



Load Transient

$I_{OUT} = 1.5$ to $3A$, $0.8A/\mu s$



PCB LAYOUT

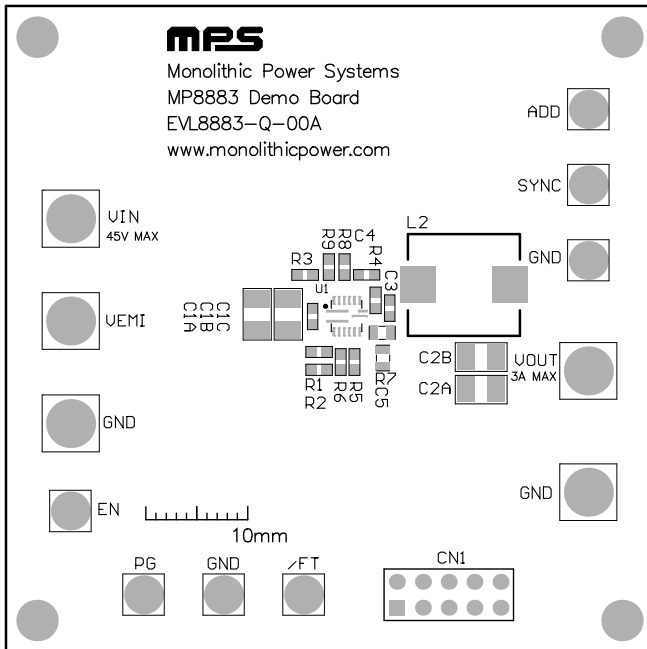


Figure 3: Top Silk

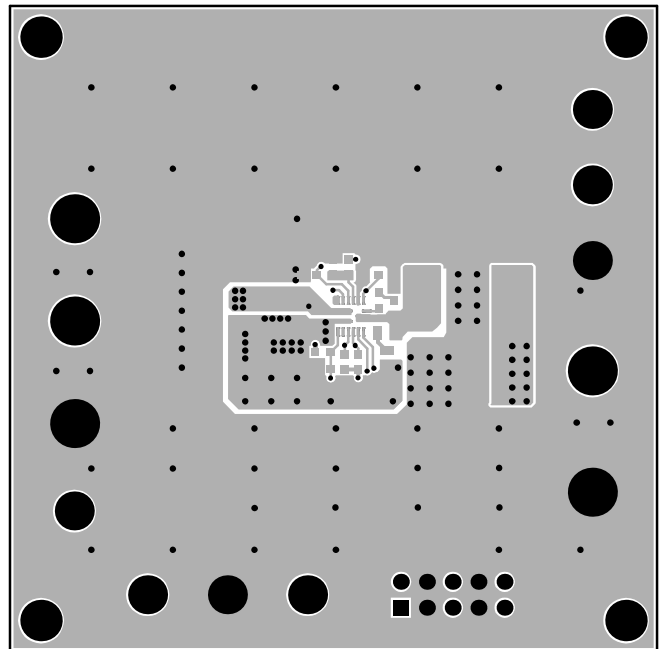


Figure 4: Top Layer

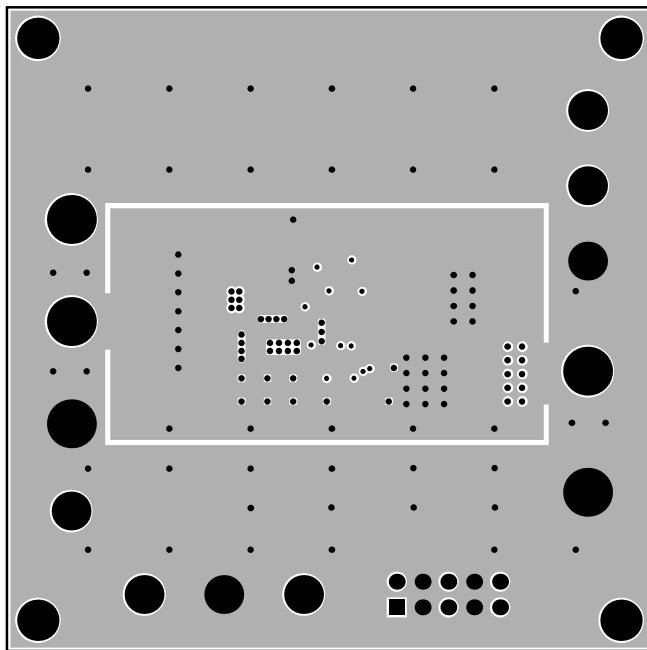


Figure 5: Mid-Layer 1

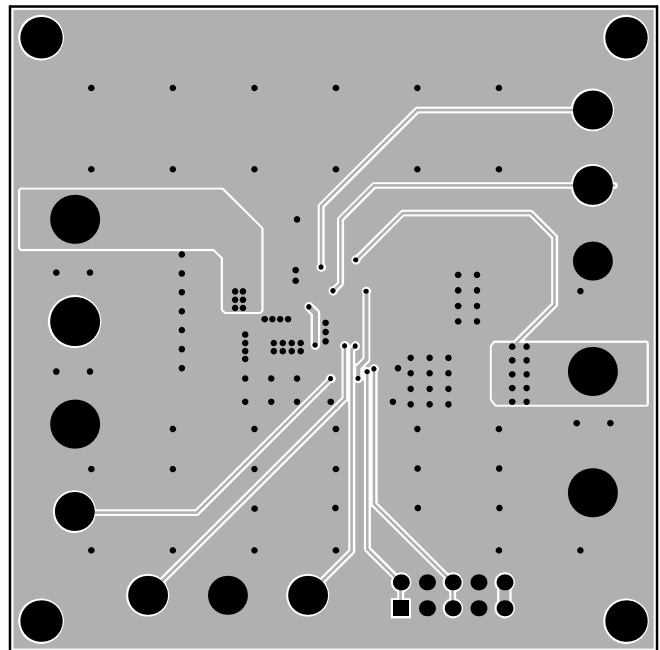


Figure 6: Mid-Layer 2

PCB LAYOUT (continued)

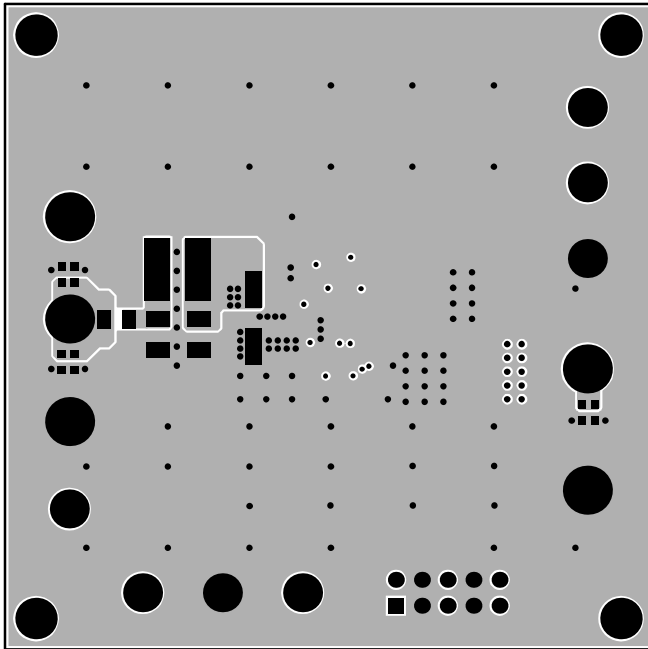


Figure 7: Bottom Layer

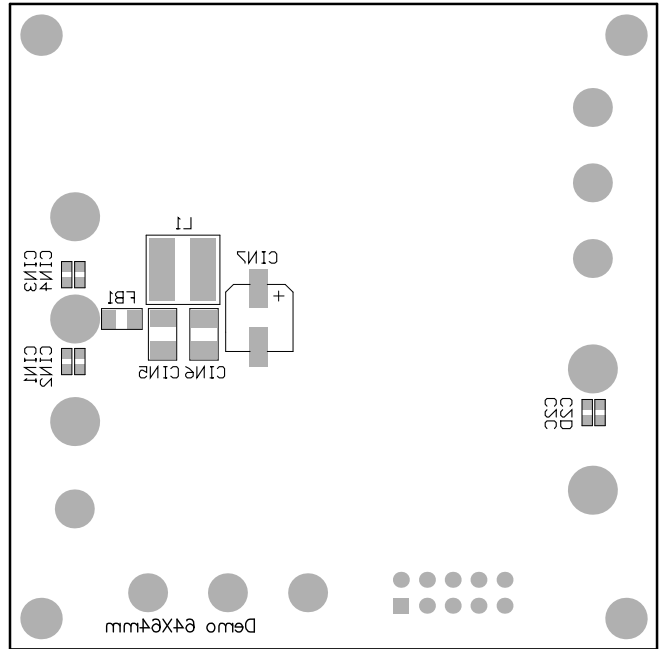


Figure 8: Bottom Silk

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/4/2024	Initial Release	-

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