EVL2761-VT-00A

I²C-Controlled, 2-Cell to 4-Cell, Buck-Boost NVDC Charger with Reverse Source Mode Evaluation Board

DESCRIPTION

The EVL2761-VT-00A evaluation board is designed to demonstrate the capabilities of the MP2761, a buck-boost, narrow-voltage DC (NVDC) charger IC designed for applications with 2-cell to 4-cell series battery packs.

The MP2761 can accept a wide 4V to 22V operating input voltage (V_{IN}) range to charge the battery and power the load connected on SYS. The device also supplies a wide 4V to 21V voltage at the IN pin in source mode, which is compliant with USB power delivery (PD) specifications.

When input power (P_{IN}) is present, the EVL2761-VT-00A charges the battery with a maximum 6A of charge current (I_{CHG}). It can also supply voltage at the input when source mode is enabled. In source mode, the output current (I_{OUT}) is limited to 6A.

The MP2761 is available in a TQFN-30 (4mmx5mm) package.

PERFORMANCE SUMMARY (1)

Specifications are at T_A = 25°C, unless otherwise noted.

Parameters	Conditions	Value
Input voltage (V_{IN}) range		4V to 22V
Battery charge regulation voltage (V_{BATT_REG})	2 cells	8.4V (I²C-configurable)
Fast charge current (I_{CC})	V_{IN} = 9V to 22V	2A (I²C-configurable)
System voltage ($V_{SYS_MIN_REG}$)	2 cells	6.4V (I²C-configurable)
Output voltage in source mode (V_{IN_SRC}) range		4V to 21V
Output voltage in source mode (V_{IN_SRC})		4.98V (I²C-configurable)
Output current limit in source mode (I_{IN_SRC})		2A (I²C-configurable)
Charge typical efficiency	V_{IN} = 20V, V_{BATT} = 8V, I_{CC} = 5A	93.49%
Charge peak efficiency	V_{IN} = 12V, V_{BATT} = 8V, I_{CC} = 3A	96%
Source mode typical efficiency	V_{BATT} = 7.4V, V_{IN_SRC} = 20V, I_{IN_SRC} = 1.5A	93.5%
Source mode peak efficiency	V_{BATT} = 8.4V, V_{IN_SRC} = 12V, I_{IN_SRC} = 1.5A	96.37%
Switching frequency (f_{SW})		425kHz (I²C-configurable)

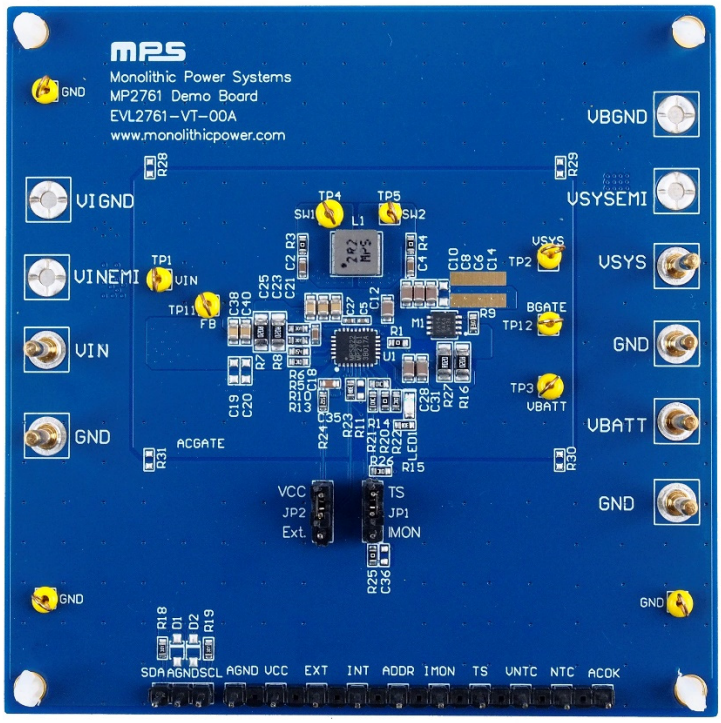
Note:

1) Refer to the MP2761 datasheet for details.

MPL Optimized Performance with MPS Inductor MPL-AL5030-2R2

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

EVALUATION BOARD



LxWxH (8.9cmx8.9cmx0.8cm)

Board Number	MPS IC Number
EVL2761-VT-00A	MP2761GVT-0000

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

QUICK START GUIDE

The EVL2761-VT-00A evaluation board is designed for the MP2761, a buck-boost narrow-voltage DC (NVDC) charger, when the device is used to charge a 2-cell battery. The board layout accommodates most commonly used resistors and capacitors. The board's default function is preset for charger mode, and the full charge voltage is preset to 8.4V. In charge mode, the MP2761 can work automatically in buck, boost, or buck-boost mode according to the input and VSYS voltages.

Follow the steps below to prepare the evaluation board:

1. Ensure that the computer has at least one USB port and a USB cable. The MP2761 evaluation software ("MP2761 Evaluation Kit") must be properly installed. The MP2761 evaluation kit.exe file can be downloaded from the MPS website.
2. Connect the USB-to-I²C communication kit (EVKT-USBI2C-02) (see Figure 1). The EVKT-USBI2C-02 is included with product evaluation kits, or it can be purchased separately from the MPS website.

Figure 1: USB-to-I²C Communication Kit

3. To enable the software, double-click on the "MP2761 Evaluation Kit" .exe file. The software supports Windows 7 and Windows 10 operating systems.

Original Test Set-Up for the MP2761

1. Connect the battery terminals to:
   a. Positive (+): VBATT
   b. Negative (-) GND
2. If using a battery simulator, preset the battery voltage between 0V and 8.4V, then turn off the battery voltage.
3. Connect the battery simulator output to the VBATT and GND pins, respectively.
4. Turn on the battery simulator before starting the test.
5. For charge mode testing, connect the input terminals to:
   a. Positive (+): VIN
   b. Negative (-): GND

   Figure 2 on page 4 shows the charge mode testing set-up.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

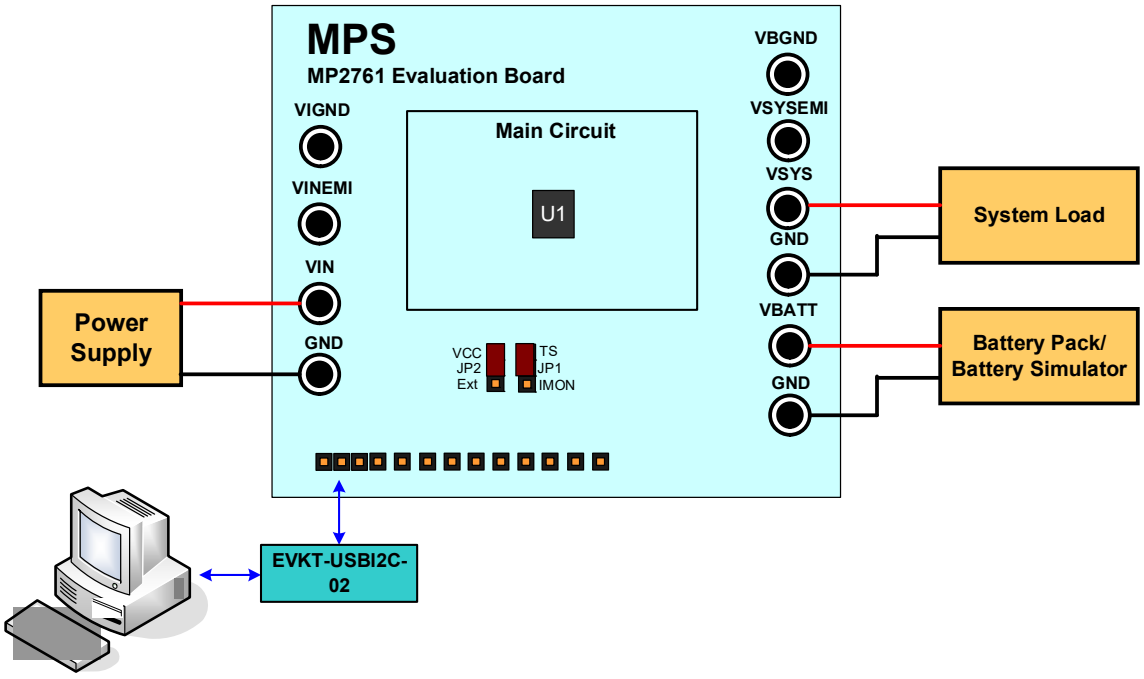


Figure 2: Charge Mode Test Set-Up

6. Connect the system load terminals to:
   a. Positive (+): VSYS
   b. Negative (-): GND
7. For source mode testing, connect the load terminals to:
   a. Positive (+): VIN
   b. Negative (-): GND

   Table 1 shows the jumper connection settings.

Table 1: Jumper Connections

Jumper	Description	Default Setting
JP1 (2)	For the TS/IMON pin's connection, connect TS/IMON to different external circuitry depending on the TS/IMON selection.	Connect JP1 to TS
JP2 (3)	To select the pull-up voltage, pull JP1 up to VCC or an external power source.	Pull up JP2 to VCC

Notes:

2) TS/IMON has different external circuits. Connect TS/IMON to the corresponding circuit using the jumper.
3) If EXT is selected, add an external power source (e.g. 3.3V) at EXT to AGND. If VCC is selected, no other action is required.

8. Launch the MP2761 evaluation software (see Figure 3 on page 5).

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

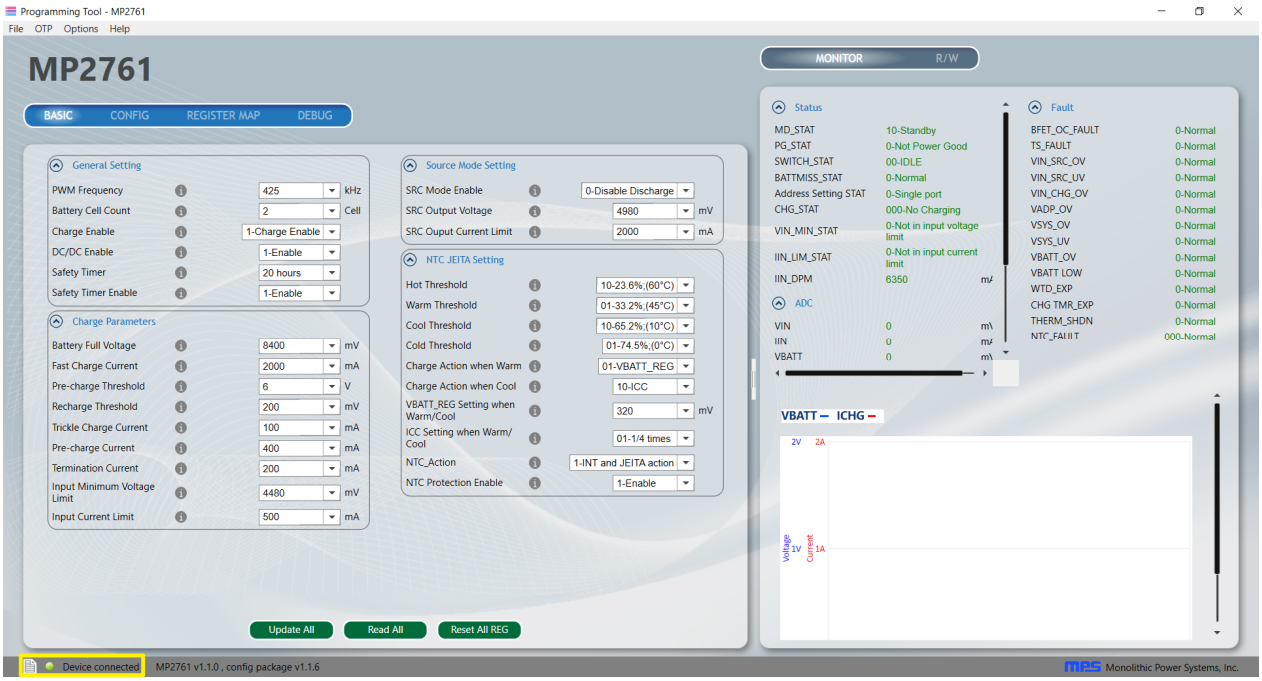


Figure 3: MP2761 Evaluation Software

9. Turn on the input voltage (V_{IN}) to charge the battery and power the system load with the default settings.

Modifying Parameters via the GUI

To use MPS's GUI, ensure that all connections are successful, such as the connections between the computer, USB-to-I²C communication kit, and the evaluation board. Click "Read All" before updating any data in the MP2761's registers.

Figure 4 shows the MP2761's basic settings.

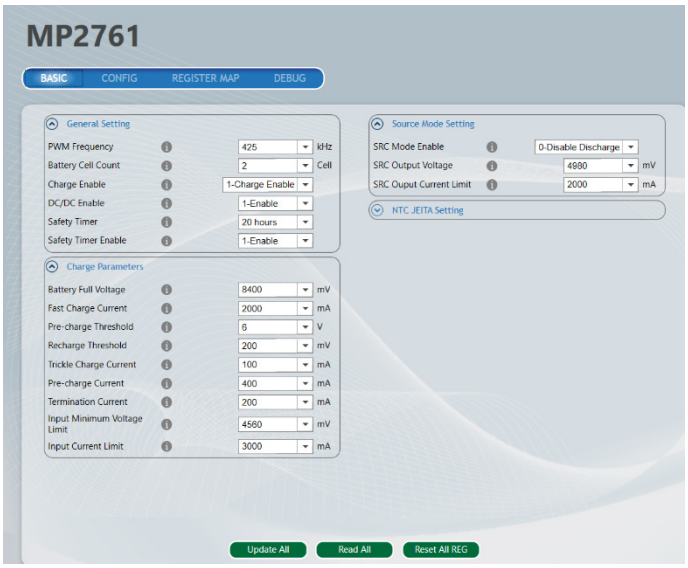


Figure 4: MP2761 Basic Settings

Figure 5 on page 6 shows how to configure the general settings. These settings include the pulse-width modulation (PWM) frequency, battery cell count, safety timer, basic controls in charge mode (such as enabling the DC/DC converter), and charge enabling.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

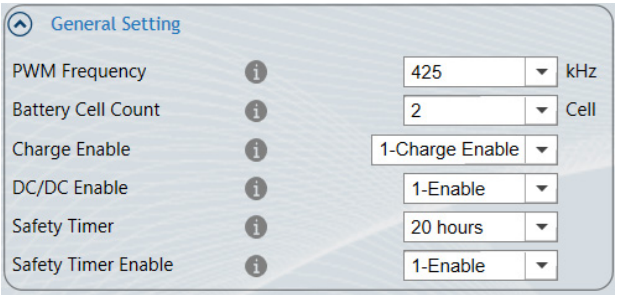


Figure 5: MP2761 General Settings

Figure 6 shows how to configure the charge parameters, including the battery-full voltage, fast charge current, pre-charge threshold, recharge threshold, trickle charge current, pre-charge current, and termination current.

The charge parameters also provide the parameters for power path management, including the minimum input voltage limit and input current limit. All the parameters can be input directly using the keyboard.

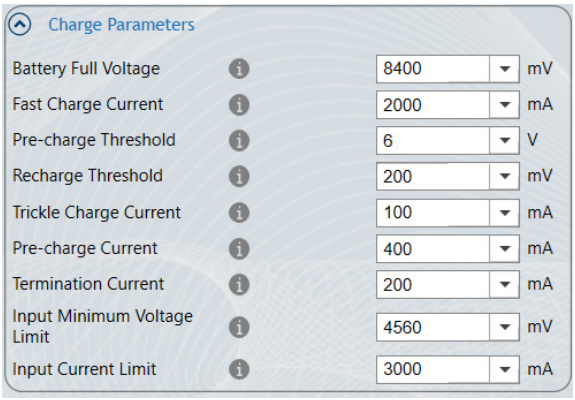


Figure 6: MP2761 Charge Parameters

Figure 7 shows how to configure the negative temperature coefficient (NTC) JEITA settings for battery thermal protection.

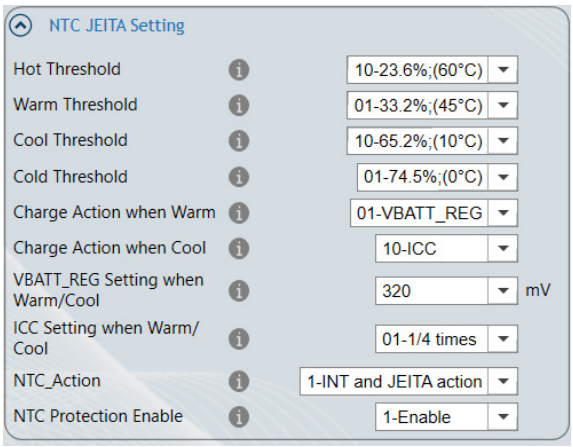


Figure 7: MP2761 NTC JEITA Settings

Figure 8 on page 7 shows how to configure the source mode settings. In source mode, the battery supplies power to the IN pin. The discharge parameters include SRC mode (enabled or disabled), the SRC output voltage, and the SRC output current limit.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

Figure 8: MP2761 Source Mode Settings

Figure 9 shows the MP2761's configuration settings.

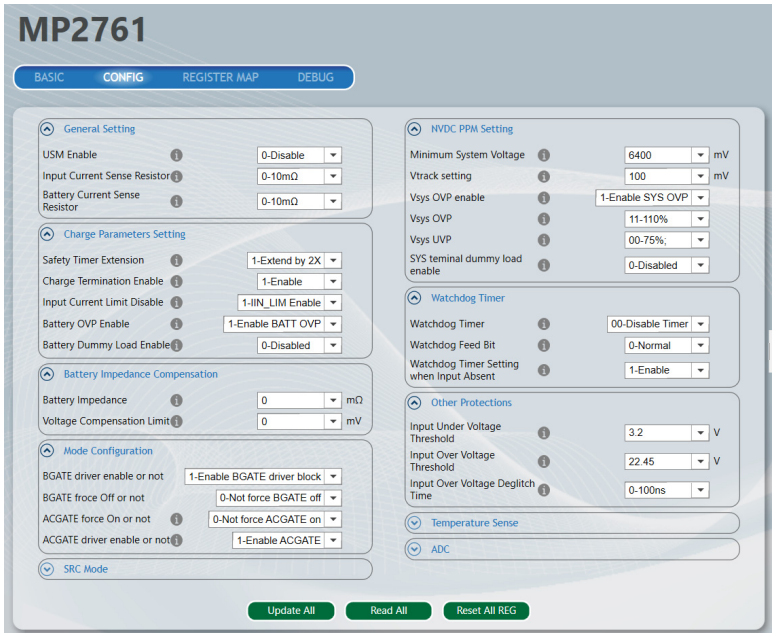


Figure 9: MP2761 Configuration Settings

Figure 10 shows how to configure USM mode (enable and disable) and the current-sense (CS) resistors.

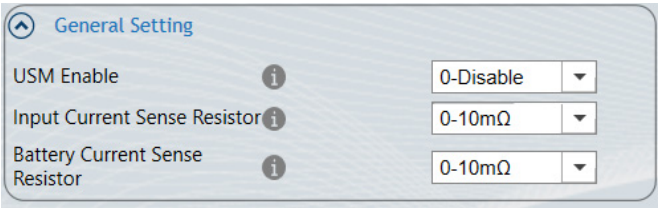


Figure 10: MP2761 Current-Sense Resistor Settings

Figure 11 shows how to configure the charge parameters. These parameters include the safety timer extension, as well as options to enable charge termination, the input current limit, battery over-voltage protection (OVP), and the battery dummy load.

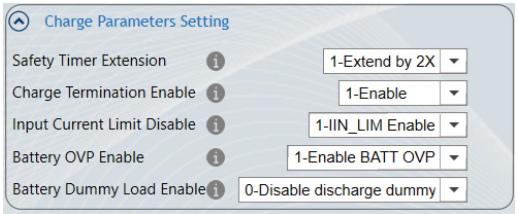


Figure 11: MP2761 Charge Parameters Setting

Figure 12 on page 8 shows how to configure the battery impedance compensation, including the battery impedance and voltage compensation limit.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

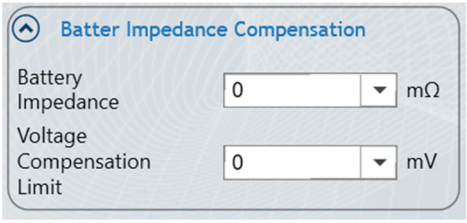


Figure 12: MP2761 Battery Impedance Compensation

Figure 13 shows how to configure the external MOSFET control. ACGATE can be set to drive the input MOSFET between the ADP pin and the input current-sense resistor. BGATE can be set to control the battery MOSFET between the SYS pin and the battery current-sense resistor.

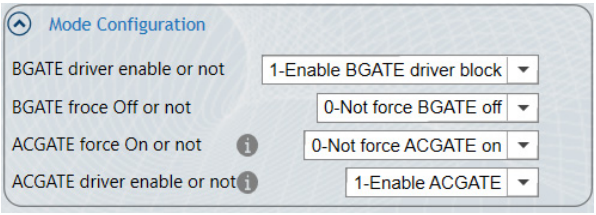


Figure 13: MP2761 External MOSFET Configuration

Figure 14 shows how to configure the SRC mode control, which includes the SRC output voltage configuration and protections.

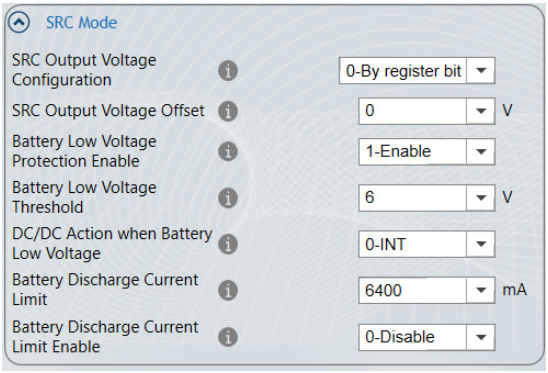


Figure 14: MP2761 SRC Mode Configuration

Figure 15 shows how to configure the NVDC power path management (PPM).

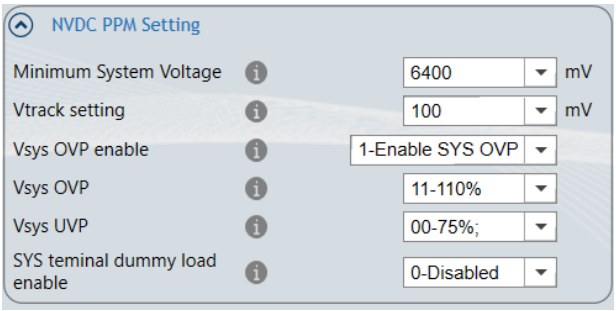


Figure 15: MP2761 NVDC PPM Settings

Figure 16 on page 9 shows how to configure the watchdog timer.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

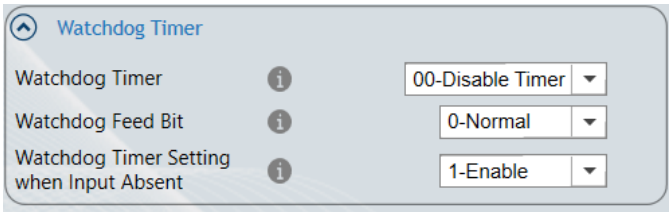


Figure 16: MP2761 Watchdog Timer

Figure 17 shows how to configure additional protections, including the input under-voltage (UV) threshold, input over-voltage (OV) threshold, and input OV deglitch time.

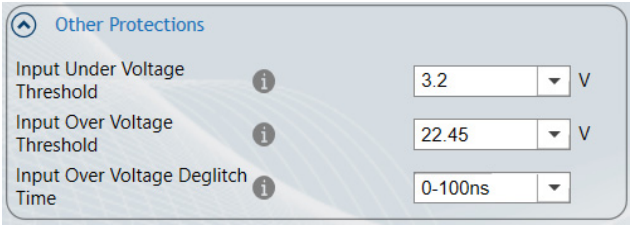


Figure 17: MP2761 Additional Protections

Figure 18 shows how to configure temperature-sense control. The TS/IMON pin can be set as either the temperature-sense pin (TS) or the battery current monitor pin (IMON).

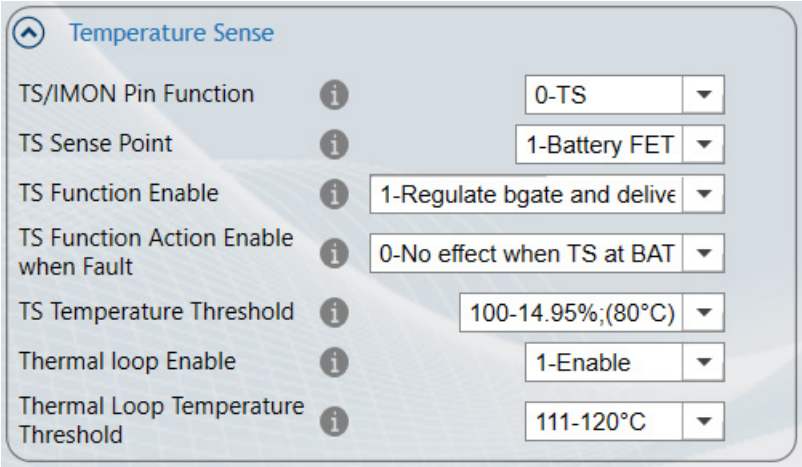


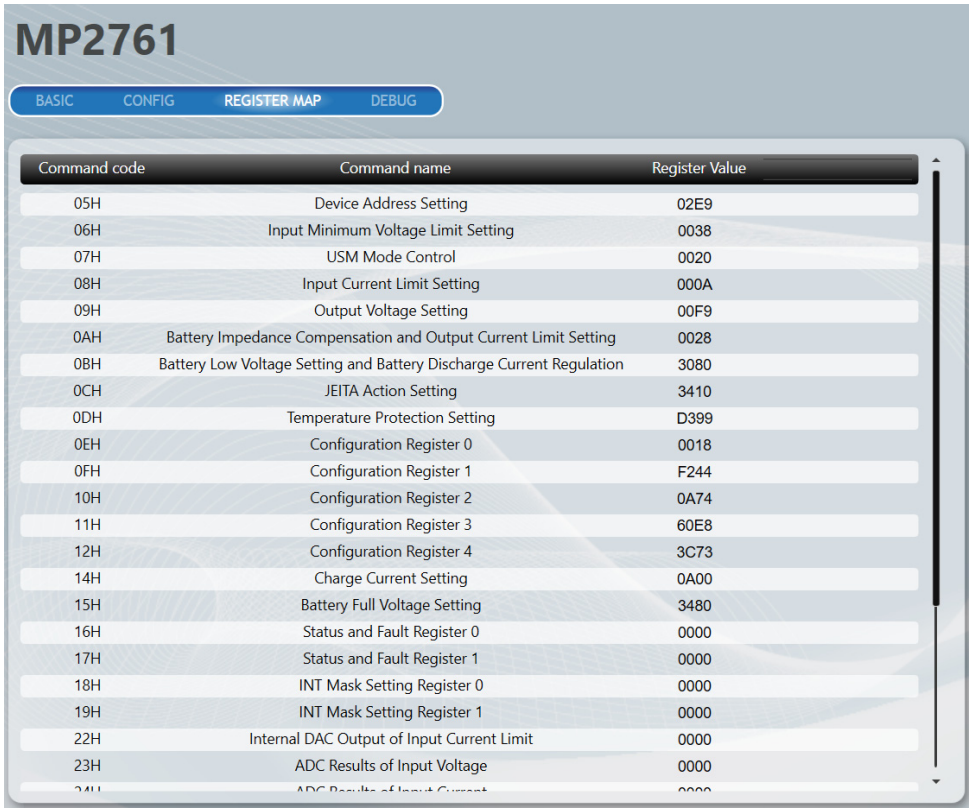
Figure 18: MP2761 Temperature Sense

Figure 19 shows how to configure the analog-to-digital converter (ADC) operation mode.

Figure 19: MP2761 ADC Operation Mode

Figure 20 shows the register map, which matches all of the register results displayed on the BASIC and CONFIG pages.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.



Command code	Command name	Register Value
05H	Device Address Setting	02E9
06H	Input Minimum Voltage Limit Setting	0038
07H	USM Mode Control	0020
08H	Input Current Limit Setting	000A
09H	Output Voltage Setting	00F9
0AH	Battery Impedance Compensation and Output Current Limit Setting	0028
0BH	Battery Low Voltage Setting and Battery Discharge Current Regulation	3080
0CH	JEITA Action Setting	3410
0DH	Temperature Protection Setting	D399
0EH	Configuration Register 0	0018
0FH	Configuration Register 1	F244
10H	Configuration Register 2	0A74
11H	Configuration Register 3	60E8
12H	Configuration Register 4	3C73
14H	Charge Current Setting	0A00
15H	Battery Full Voltage Setting	3480
16H	Status and Fault Register 0	0000
17H	Status and Fault Register 1	0000
18H	INT Mask Setting Register 0	0000
19H	INT Mask Setting Register 1	0000
22H	Internal DAC Output of Input Current Limit	0000
23H	ADC Results of Input Voltage	0000

Figure 20: MP2761 Register Map

Figure 21 shows the monitor view.

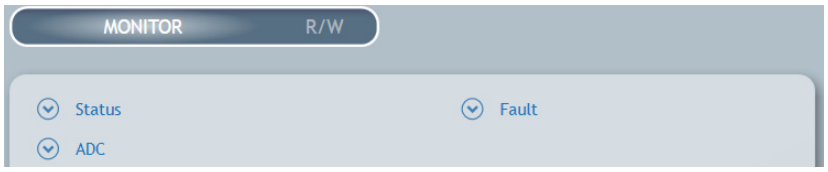


Figure 21: Monitor View

Figure 22 shows the status monitoring results.

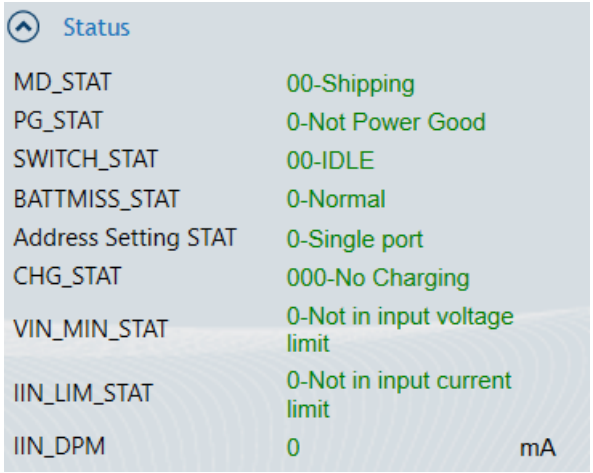


Figure 22: MP2761 Status Results

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

Figure 23 shows the fault monitoring results.

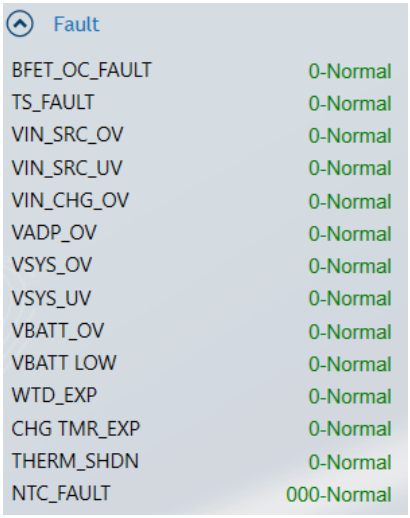


Figure 23: MP2761 Fault Results

Figure 24 shows the ADC results for all channels.

Figure 24: MP2761 ADC Results

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

EVALUATION BOARD SCHEMATIC

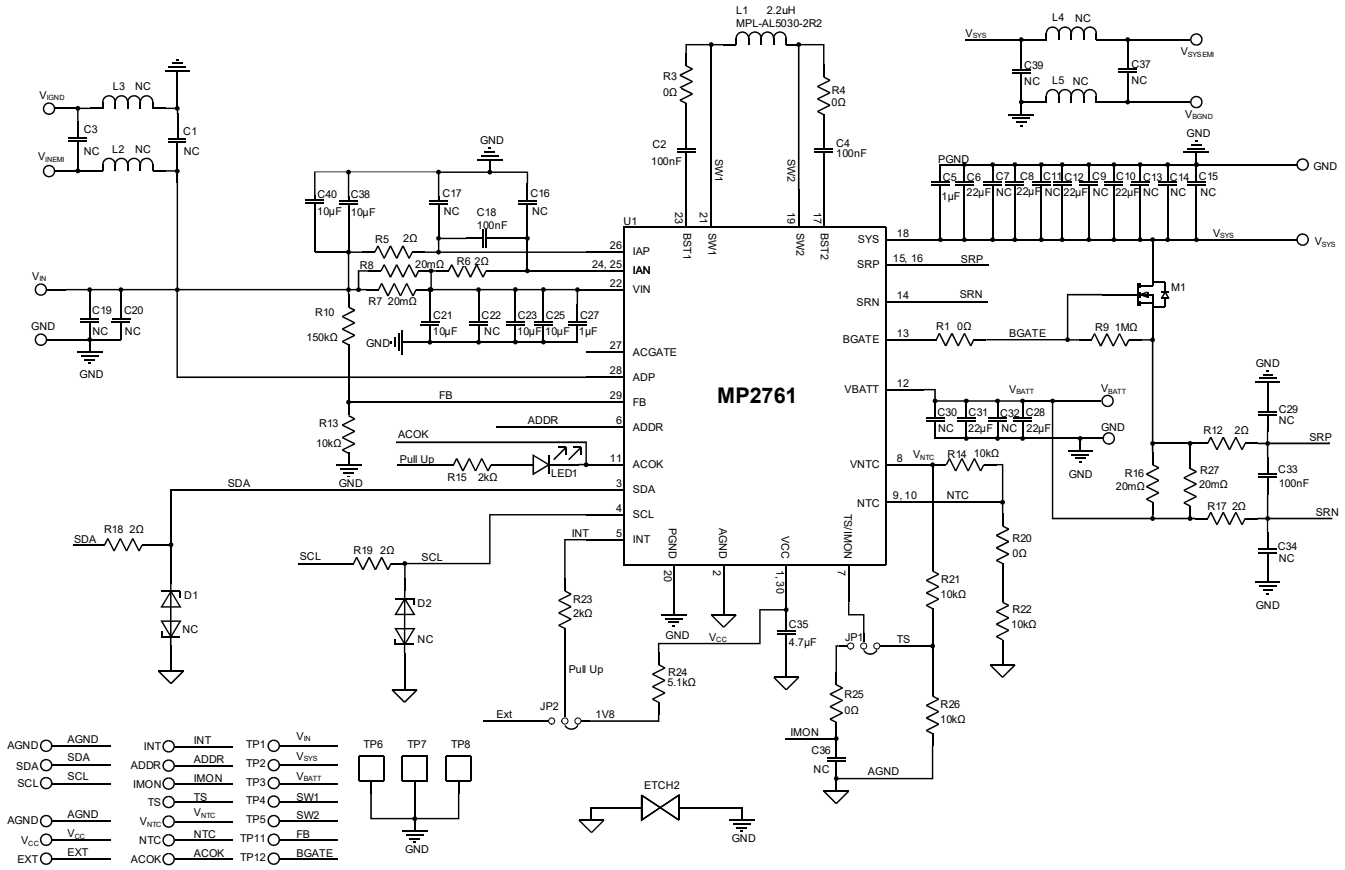


Figure 25: Evaluation Board Schematic

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

EVL2761-VT-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
4	L2, L3, L4, L5	NC				
5	R1, R3, R4, R20, R25	0Ω	Film resistor, 5%	0603	Yageo	RC0603JR-070RL
6	R5, R6, R12, R17, R18, R19	2Ω	Film resistor, 5%	0603	Liz	CR0603JA02R0G
4	R7, R8, R16, R27	20mΩ	Film resistor, 1%, 1W	1206	Cyntec	SCRR1206S1-R020F
1	R9	1MΩ	Film resistor, 1%	0603	Yageo	RC0603FR-071ML
1	R10	150kΩ	Film resistor, 5%, 1/10W	0603	Yageo	RC0603JR-07150KL
5	R13, R14, R21, R22, R26	10kΩ	Film resistor, 1%, 1/10W	0603	Yageo	RC0603FR-0710KL
2	R15, R23	2kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-072KL
1	R24	5.1kΩ	Film resistor, 5%	0603	Yageo	RC0603JR-075K1L
11	C1, C3, C15, C16, C17, C22, C29, C34, C36, C37, C39	NC				
4	C2, C4, C18, C33	100nF	Ceramic capacitor, 25V, X7R	0603	Wurth	885012206071
2	C5, C27	1μF	Ceramic capacitor, 25V, X5R	0402	Murata	GRM155R61E105KA12
6	C6, C8, C10, C12, C28, C31	22μF	Ceramic capacitor, 25V, X5R	0805	Murata	GRM21BR61E226ME44L
9	C7, C9, C11, C13, C14, C19, C20, C30, C32	NC				
5	C21, C23, C25, C38, C40	10μF	Ceramic capacitor, 25V, X7S	0805	Murata	GRM21BC7E106KE11L
1	C35	4.7μF	Ceramic capacitor, 25V, X5R	0603	Murata	GRM188R61E475KE11D
1	LED1	Red	Red LED	0805	Bright LED	BL-HUE35A-AV-TRB
2	D1, D2	NC				
1	M1	8.5mΩ	N-channel MOSFET, 30V, 20A	PowerPAK 1212-8	Vishay	SISA14DN-T1-GE3
13	ACOK, ADDR, AGND, AGND, Ext, IMON, INT, NTC, TS, VCC, VNTC, SCL, SDA	1mm	Pin header	DIP	Any	

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

EVL2761-VT-00A BILL OF MATERIALS *(continued)*

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
10	TP1, TP2, TP3, TP4, TP5, TP6 (GND), TP7 (GND), TP8 (GND), TP11, TP12	1mm	Test point, φ = 1mm	DIP	Any	
10	VIN, VINEMI, VBATT, VSYS, VSYSEMI, GND, GND, GND, VIGND, VBGND	2mm	φ = 2mm	DIP	Any	
2	JP1, JP2	2.54mm	Pin header	DIP	Any	
1	L1	2.2μH	Inductor, 12.3mΩ, 8.2A	SMD	MPS	MPL-AL5030-2R2
1	U1	MP2761	2-cell to 4-cell buck-boost charger	TQFN-30 (4mmx 5mm)	MPS	MP2761GVT-0000

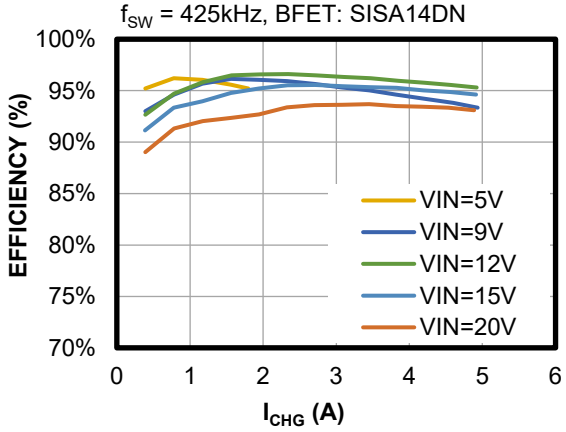
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

EVB TEST RESULTS

Performance curves and waveforms are tested on the evaluation board. The default settings are for a 2-cell battery, C_{IN} = 10µF x 5 + 1µF x 1, C_{SYS} = 22µF x 4 + 1µF x 1, C_{BATT} = 22µF x 2, L = 2.2µH (12.3mΩ), f_{SW} = 425kHz. T_A = 25°C, unless otherwise noted.

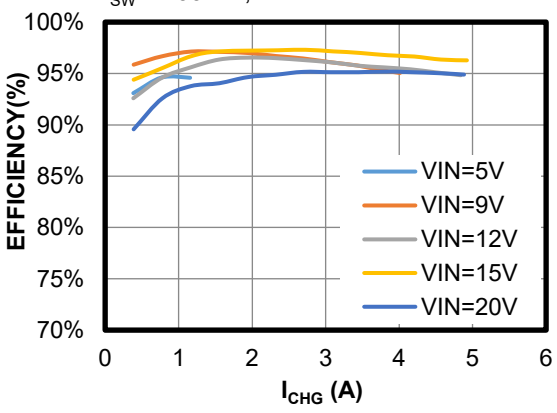
Efficiency vs. Charge Current

V_{IN} = 5V/9V/12V/15V/20V, V_{BATT} = 8V, f_{SW} = 425kHz, BFET: SISA14DN



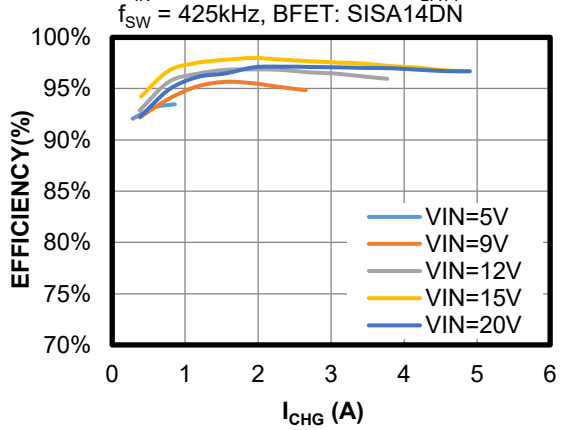
Efficiency vs. Charge Current

V_{IN} = 5V/9V/12V/15V/20V, V_{BATT} = 12V, f_{SW} = 435kHz, BFET: SISA14DN



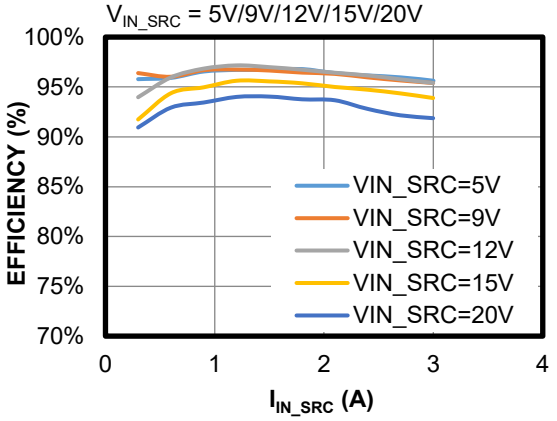
Efficiency vs. Charge Current

V_{IN} = 5V/9V/12V/15V/20V, V_{BATT} = 16V, f_{SW} = 425kHz, BFET: SISA14DN



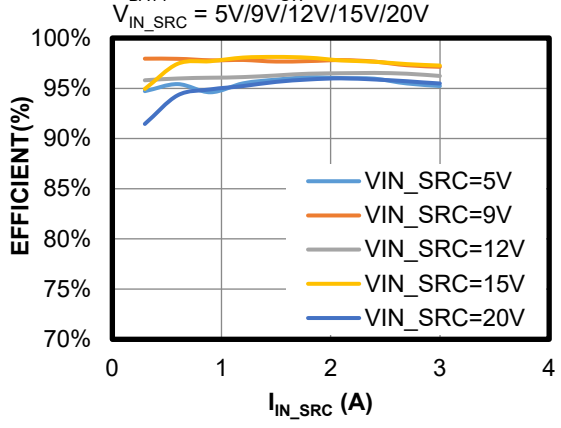
Efficiency vs. Source Input Current

V_{BATT} = 8.4V, f_{SW} = 425kHz, V_{IN_SRC} = 5V/9V/12V/15V/20V



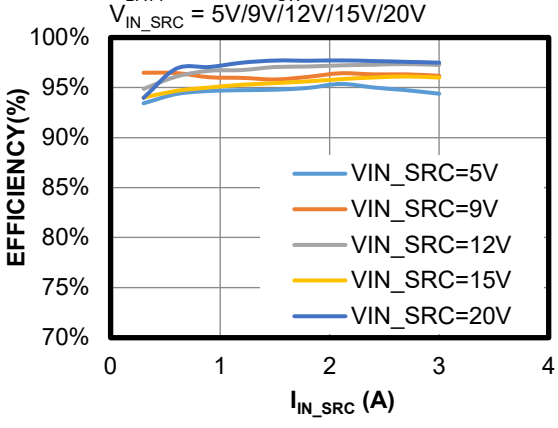
Efficiency vs. Source Input Current

V_{BATT} = 12.6V, f_{SW} = 425kHz, V_{IN_SRC} = 5V/9V/12V/15V/20V



Efficiency vs. Source Input Current

V_{BATT} = 16.8V, f_{SW} = 425kHz, V_{IN_SRC} = 5V/9V/12V/15V/20V



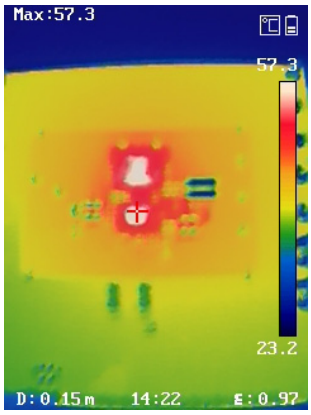
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

EVB TEST RESULTS

Performance curves and waveforms are tested on the evaluation board. The default settings are for a 2-cell battery, C_{IN} = 10µF x 5 + 1µF x 1, C_{SYS} = 22µF x 4 + 1µF x 1, C_{BATT} = 22µF x 2, L = 2.2µH (12.3mΩ), f_{SW} = 425kHz. T_A = 25°C, unless otherwise noted.

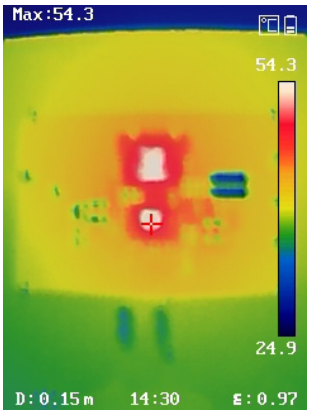
Thermal Performance

Charge mode, V_{IN} = 20V, $I_{INLIMIT}$ = 3A, V_{BATT} = 8.2V, I_{CC} = 5A



Thermal Performance

Source mode, V_{BATT} = 8.4V, V_{IN_SRC} = 20V, I_{IN_SRC} = 1.8A



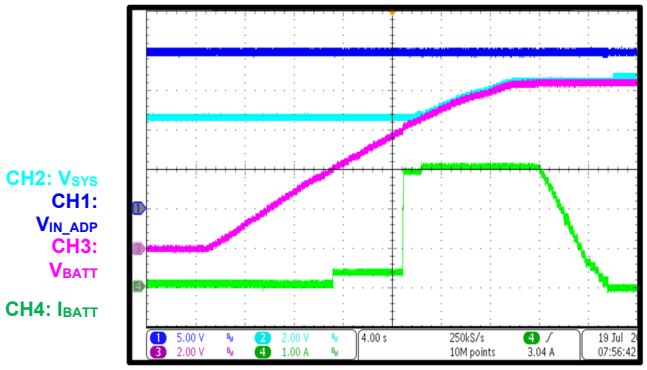
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. The default settings are for a 2-cell battery, C_{IN} = 10µF x 5 + 1µF x 1, C_{SYS} = 22µF x 4 + 1µF x 1, C_{BATT} = 22µF x 2, L = 2.2µH (12.3mΩ), f_{SW} = 450kHz. T_A = 25°C, unless otherwise noted.

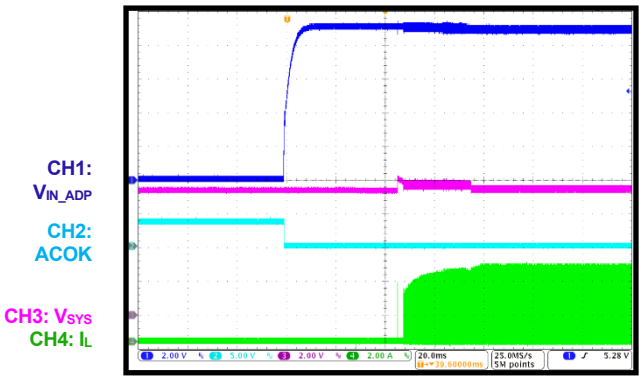
Charge Profile

V_{IN_ADP} = 20V, V_{BATT} = 0V to 8.4V, I_{IN_MIN} = 3A, I_{CC} = 2A, V_{SYS_MIN} = 6.4V, V_{TRACK} = 100mV



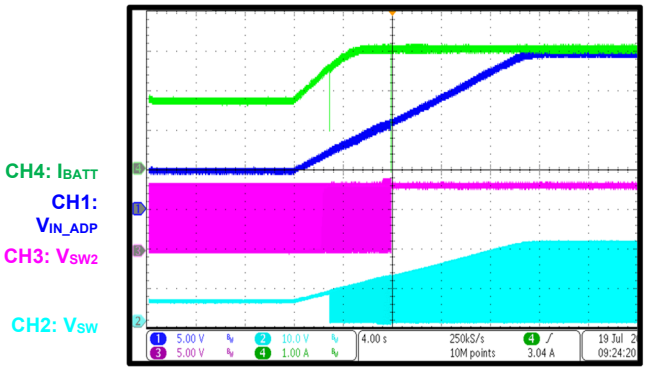
Start-Up through VIN in Charge Mode

9V input power on, V_{BATT} = 7.4V (2 cells), I_{CC} = 2A, charge enabled, I_{SYS} = 0A



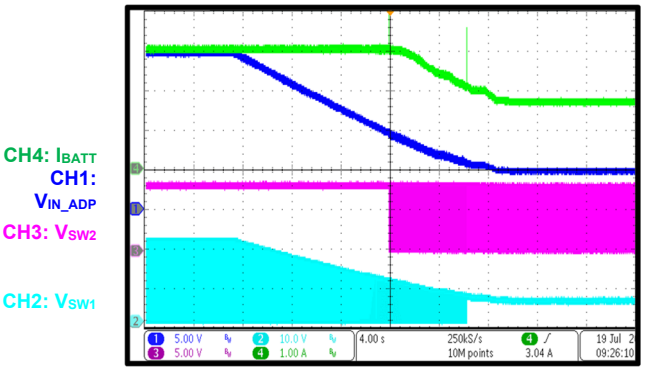
V_{IN_ADP} Step from 5V to 20V

I_{IN_MIN} = 3A, V_{BATT} = 8V, I_{CC} = 3A, V_{SYS_MIN} = 6.4V, V_{TRACK} = 100mV



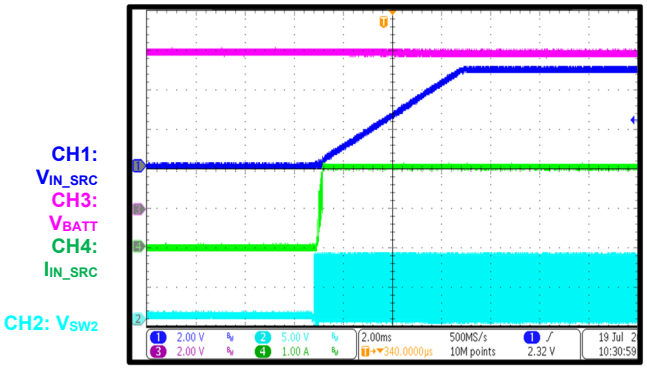
V_{IN_ADP} Step from 20V to 5V

I_{IN_MIN} = 3A, V_{BATT} = 8V, I_{CC} = 3A, V_{SYS_MIN} = 6.4V, V_{TRACK} = 100mV



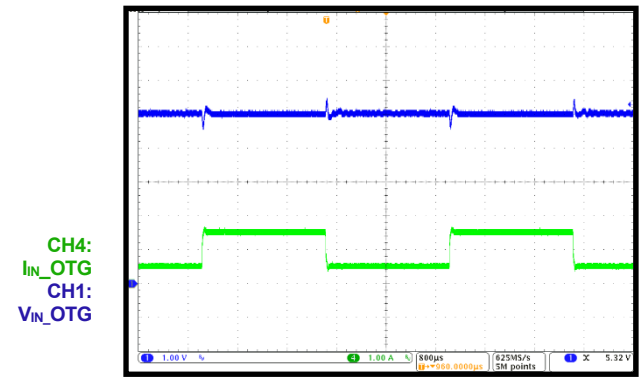
Start-Up through V_{IN_SRC} in Source Mode

V_{BATT} = 8V, V_{IN_SRC} = 5V, I_{IN_SRC} = 2A



Load Transient in Source Mode

V_{BATT} = 7.4V (2 cells), V_{IN_SRC} = 5V, 0.5A to 1.5A load current



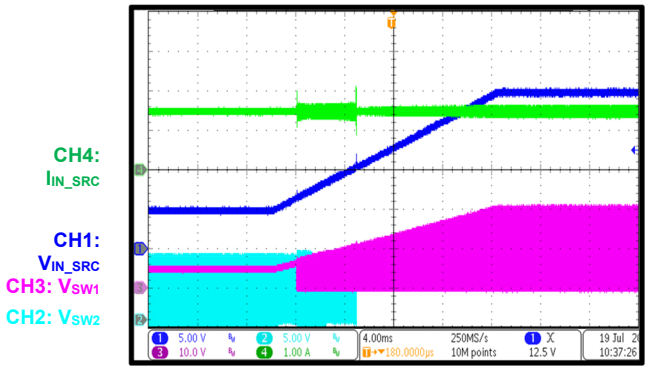
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

EVB TEST RESULTS *(continued)*

Performance curves and waveforms are tested on the evaluation board. The default settings are for a 2-cell battery, C_{IN} = 10µF x 5 + 1µF x 1, C_{SYS} = 22µF x 4 + 1µF x 1, C_{BATT} = 22µF x 2, L = 2.2µH (12.3mΩ), f_{SW} = 450kHz. T_A = 25°C, unless otherwise noted.

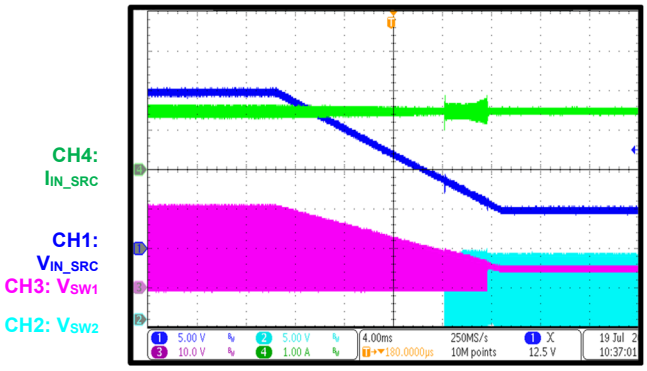
V_{IN_SRC} Step from 5V to 20V in Source Mode

V_{BATT} = 8V, V_{IN_SRC} = 5V to 20V, I_{IN_SRC} = 1.5A



V_{IN_SRC} Step from 20V to 5V in Source Mode

V_{BATT} = 8V, V_{IN_SRC} = 20V to 5V, I_{IN_SRC} = 1.5A



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

PCB LAYOUT

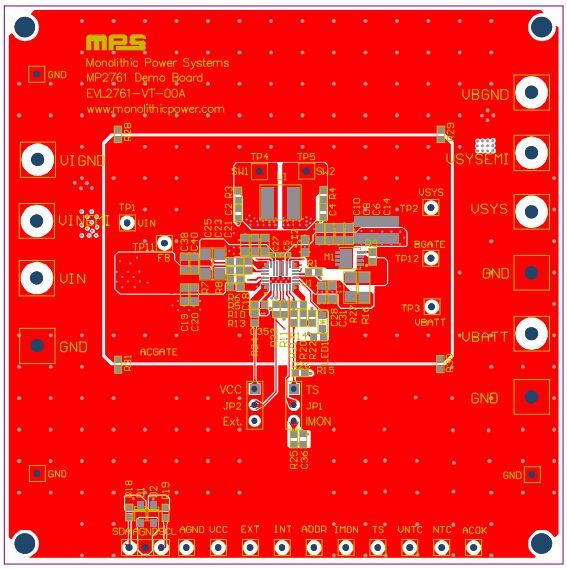


Figure 26: Top Layer

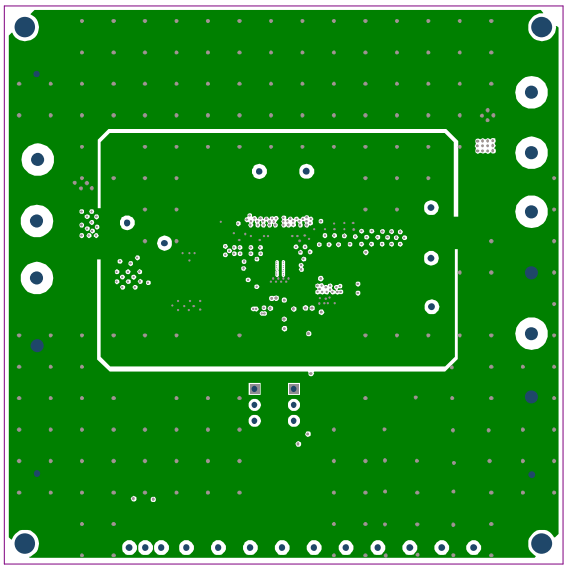


Figure 27: Mid-Layer 1

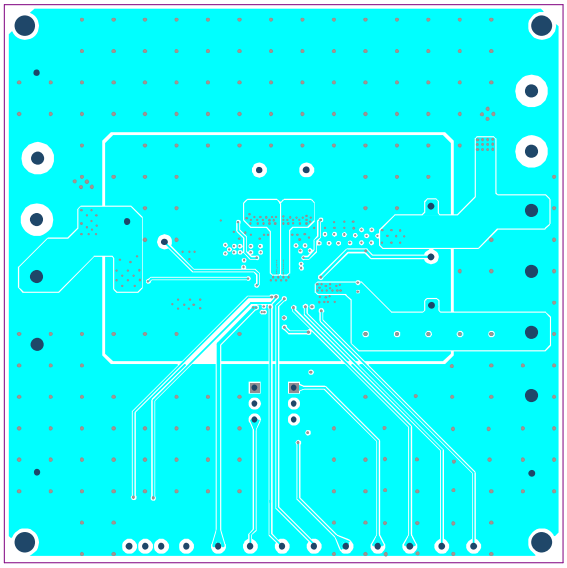


Figure 28: Mid-Layer 2

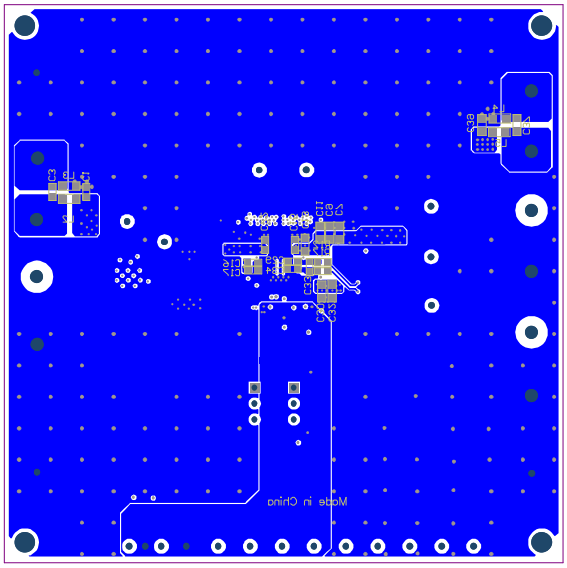


Figure 29: Bottom Layer

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	9/12/2025	Initial Release	-

Notice: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third-party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.