EV5098A-D-00A

Dual EFUSE with SAS Function and Reverse Current Blocking

DESCRIPTION

The EV5098A-D-00A Evaluation Board is designed to demonstrate the capabilities of MPS' MP5098A, the MP5098A is a dual 5V/12V EFUSE. It was used to protect circuitry on the output from transient on input. It also protects from undesired shorts at the output and limits the input inrush current during system start up.

SAS and EN pin control the on/off logic of the dual EFUSE. SS pin for each channel controls the start up time of the device. Reverse current blocking function is integrated for 5V device. The maximum load at the output is current limited. The magnitude of the current limit is internal fixed and able to trim.

An internal integrated LDO provide 5V/10mA load capability for system use.

The MP5098A requires a minimal number of external components and is available in a space-saving TQFN-10 (2mmx3mm).

ELECTRICAL SPECIFICATION

Parameter	Symbol	Value	Units
Input Voltage1	V_{IN1}	12	V
Input Voltage2	V_{IN12}	5	V
Output Current1	I_{OUT1}	3	A
Output Current2	I_{OUT2}	2	A

FEATURES

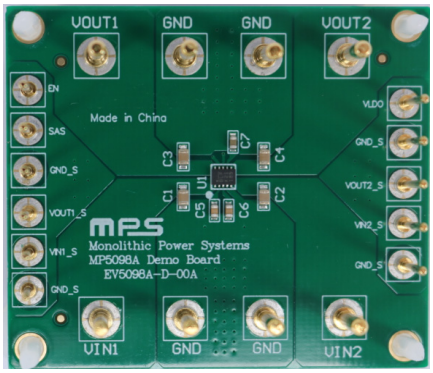
- Integrated 5V, 12V Input Dual EFUSE
- Up to 18V Absolute Maximum Input Voltage for both EFUSEs
- Reverse Current Blocking for the 5V channel
- Negative Voltage Protection for Both EFUSEs
- Integrated Dual Channel Current Limit Switch
- Low 44mΩ Ron for Both Power FETs
- 3A, +/-10% Current Limit of 5Vin channel
- 4.5A +/-10% Current Limit of 12Vin channel
- 5.7V typical OVP threshold for 5Vin channel
- 15V typical OVP threshold for 12Vin channel
- Integrated one 10mA LDO for system use
- Latch-off Thermal Shutdown
- Available in TQFN-10 (2mmx3mm) package

APPLICATIONS

- Hard Disk Drives
- Solid State Drives
- Hot Swap Application

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. "MPS", the MPS logo, and "Simple, Easy Solutions" are trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

EV5098A-D-00A EVALUATION BOARD



(L x W) 5.43cm x 4.61cm

Board Number	MPS IC Number
EV5098A-D-00A	MP5098AGDT

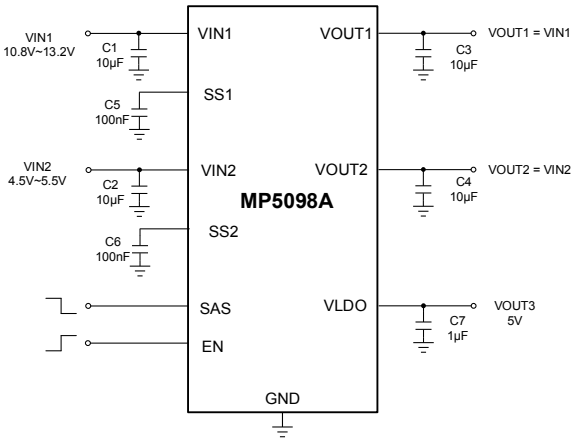
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

QUICK START GUIDE

1. Preset V_{IN1} Power Supply to12V, V_{IN2} Power Supply to 5V.
2. Turn Power Supply off.
3. Connect Power Supply terminals to:
    a. Positive (+): V_{INX}
    b. Negative (–): GND
4. Connect Load to:
    a. Positive (+): V_{OUTX}
    b. Negative (–): GND
5. Turn Power Supply on after making connections. The board will automatically start up.
6. To use the Enable function, apply a digital input to the EN pin. Drive EN higher than 1.4V to turn on the FETS, or less than 0.4V to turn off.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

EVALUATION BOARD SCHEMATIC



EV5098A-D-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Part Number
4	C1,C2,C3, C4	10µF	Ceramic Cap., 25V, X5R	0805	Murata	GRM21BR61E106MA73L
2	C5,C6	100NF	Ceramic Cap., 50V, X7R	0603	TDK	C1608X7R1H104K
1	C7	1µF	Ceramic Cap., 16V, X5R	0603	Murata	GRM185R61C105KE44D
1	U1	MP5098A	Dual EFUSE	QFN-10	MPS	MP5098AGDT

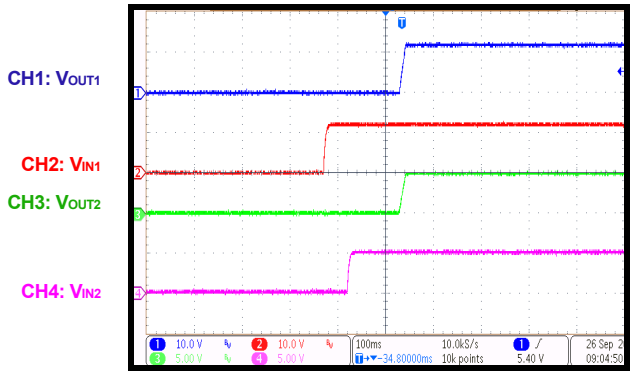
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

EVB TEST RESULTS

Performance waveforms are tested on the evaluation board.
V_{IN1}=12V, V_{IN2}=5V, T_A=25°C, unless otherwise noted.

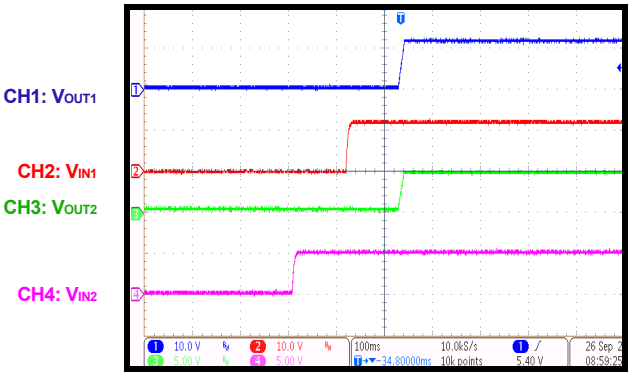
CH1/CH2 Start-Up Logic

CH1 Start-Up first, I_{OUT1} = I_{OUT2} = 0A



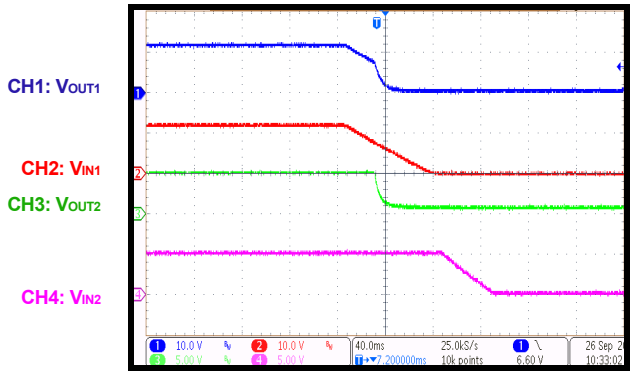
CH1/CH2 Start-Up Logic

CH2 Start-Up first, I_{OUT1} = I_{OUT2} = 0A



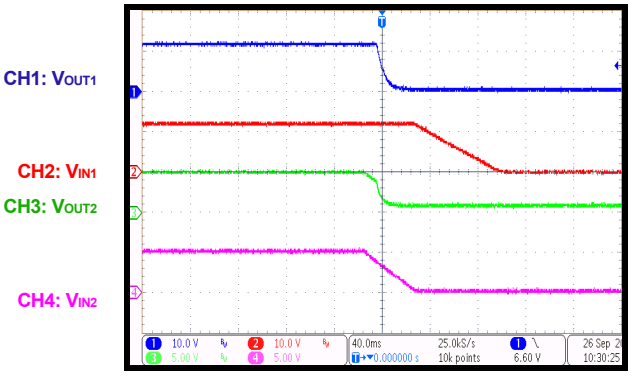
CH1/CH2 Shutdown Logic

CH1 Shutdown first, I_{OUT1} = I_{OUT2} = 0A



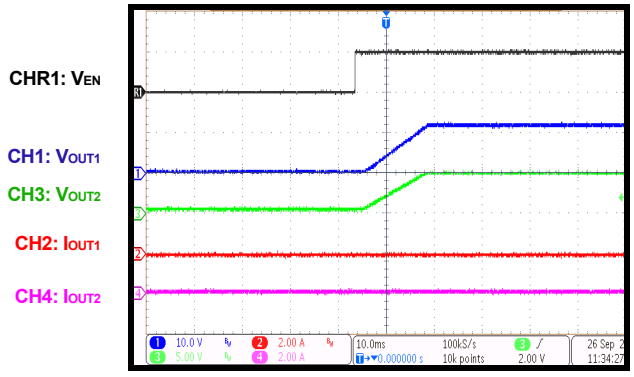
CH1/CH2 Shutdown Logic

CH2 Shutdown first, I_{OUT1} = I_{OUT2} = 0A



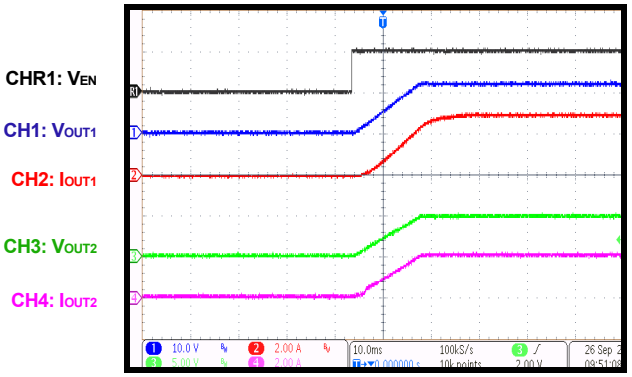
CH1/CH2 EN On Logic

I_{OUT1} = I_{OUT2} = 0A



CH1/CH2 EN On Logic

I_{OUT1} =3A, I_{OUT2} = 2A



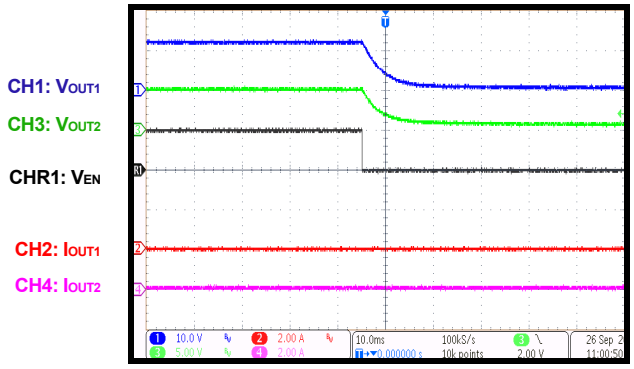
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

EVB TEST RESULTS *(continued)*

Performance waveforms are tested on the evaluation board.
V_{IN1}=12V, V_{IN2}=5V, T_A=25°C, unless otherwise noted.

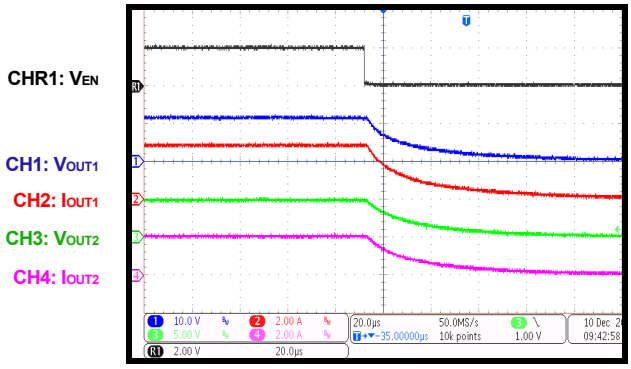
CH1/CH2 EN Off Logic

I_{OUT1} = I_{OUT2} = 0A



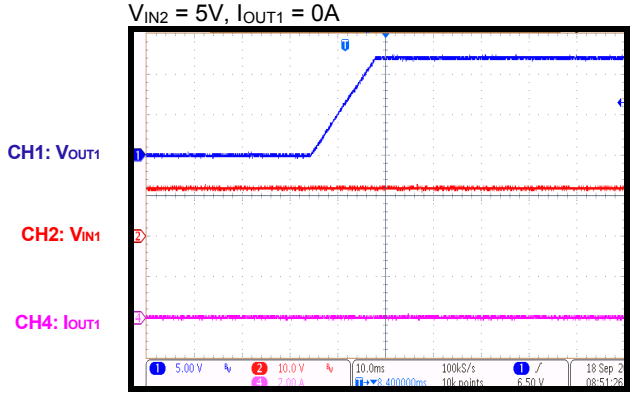
CH1/CH2 EN Off Logic

I_{OUT1} =3A, I_{OUT2} = 2A



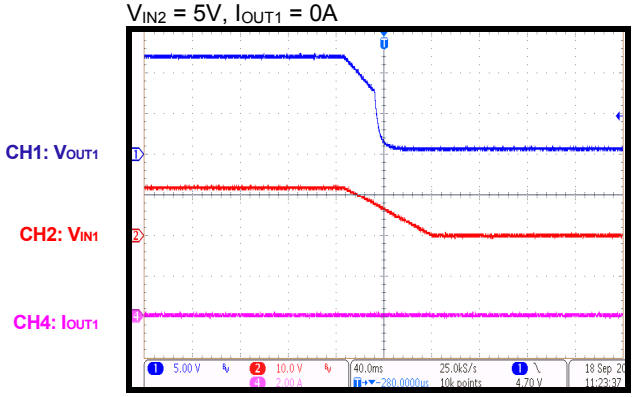
Start-Up through Input Voltage (12V E-Fuse)

V_{IN2} = 5V, I_{OUT1} = 0A



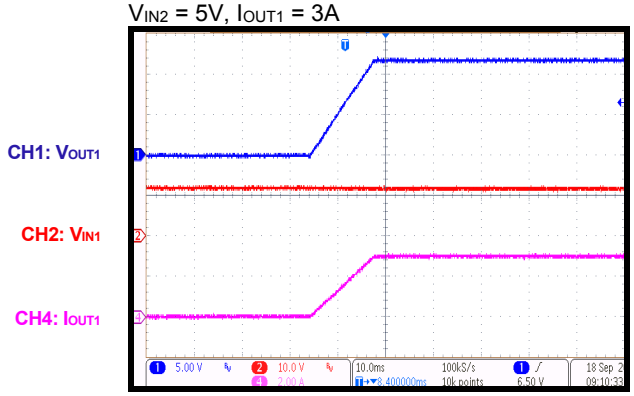
Shutdown through Input Voltage (12V E-Fuse)

V_{IN2} = 5V, I_{OUT1} = 0A



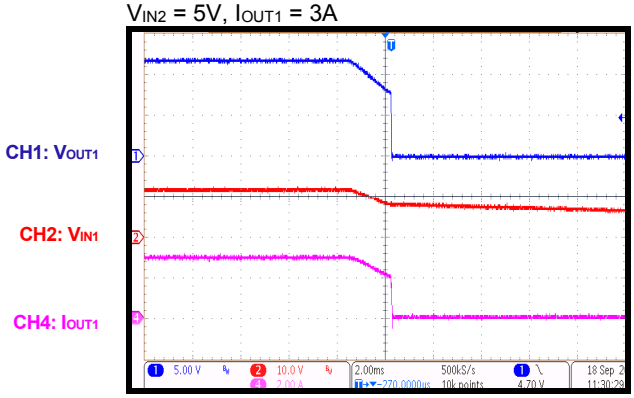
Start-Up through Input Voltage (12V E-Fuse)

V_{IN2} = 5V, I_{OUT1} = 3A



Shutdown through Input Voltage (12V E-Fuse)

V_{IN2} = 5V, I_{OUT1} = 3A



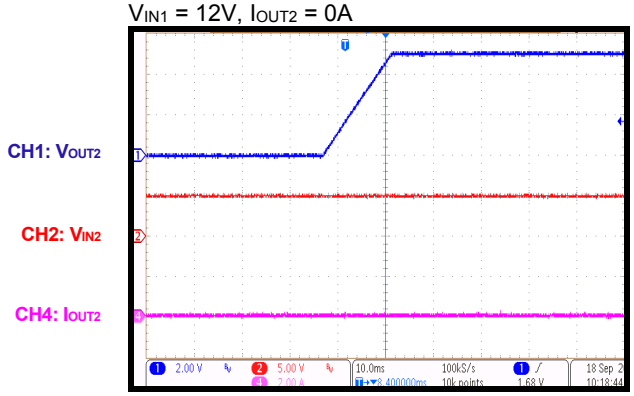
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

EVB TEST RESULTS *(continued)*

Performance waveforms are tested on the evaluation board.
V_{IN1}=12V, V_{IN2}=5V, T_A=25°C, unless otherwise noted.

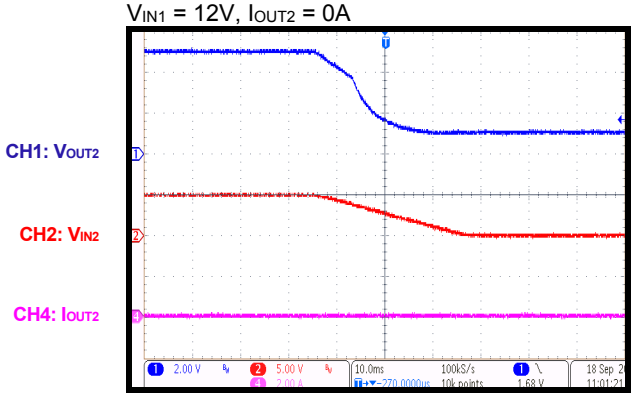
Start-Up through Input Voltage (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 0A



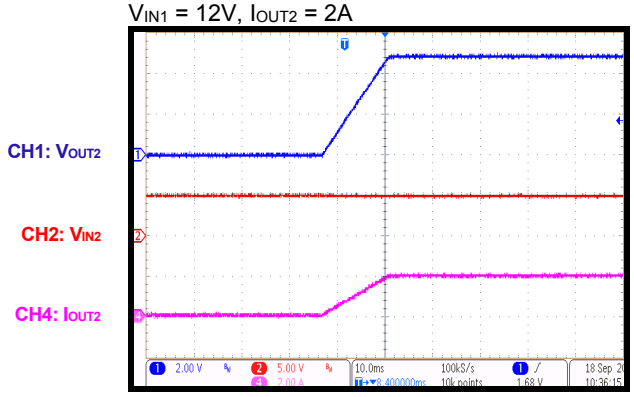
Shutdown through Input Voltage (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 0A



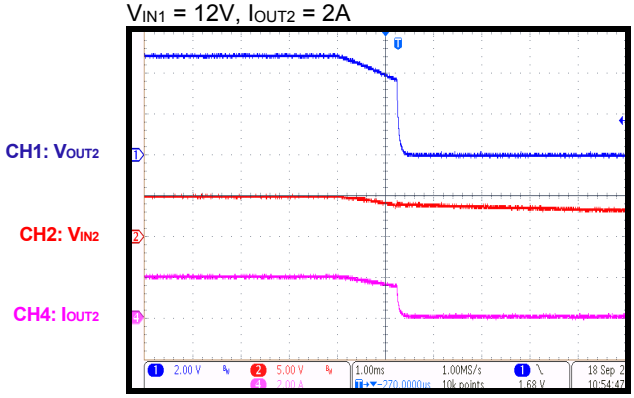
Start-Up through Input Voltage (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 2A



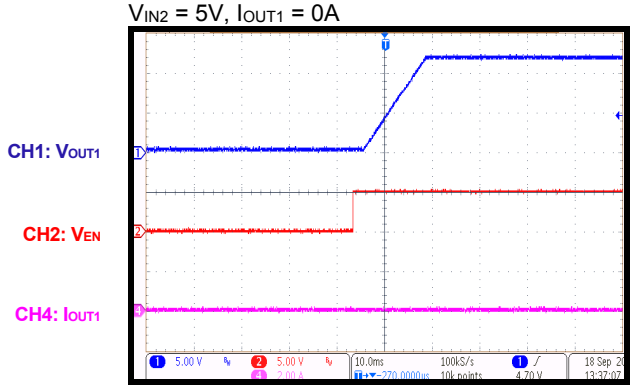
Shutdown through Input Voltage (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 2A



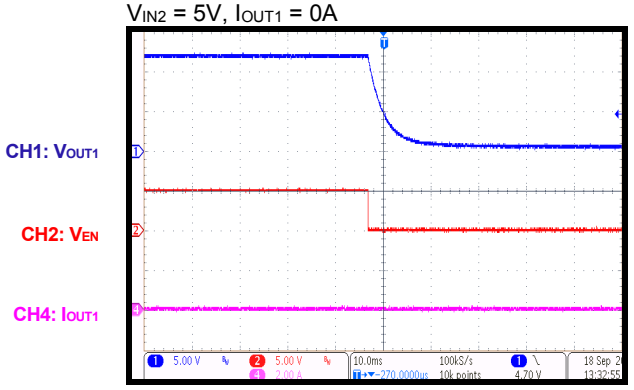
Start-Up through Enable (12V E-Fuse)

V_{IN2} = 5V, I_{OUT1} = 0A



Shutdown through Enable (12V E-Fuse)

V_{IN2} = 5V, I_{OUT1} = 0A



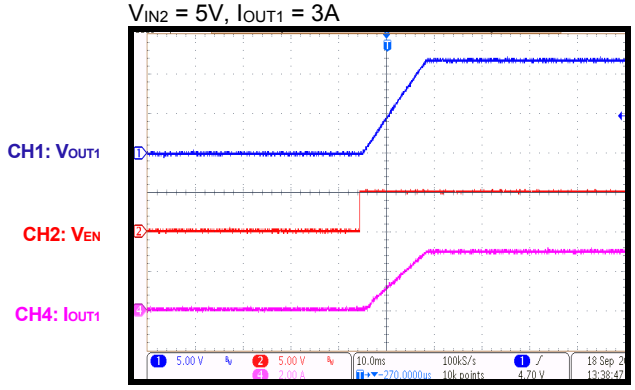
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

EVB TEST RESULTS *(continued)*

Performance waveforms are tested on the evaluation board.
V_{IN1}=12V, V_{IN2}=5V, T_A=25°C, unless otherwise noted.

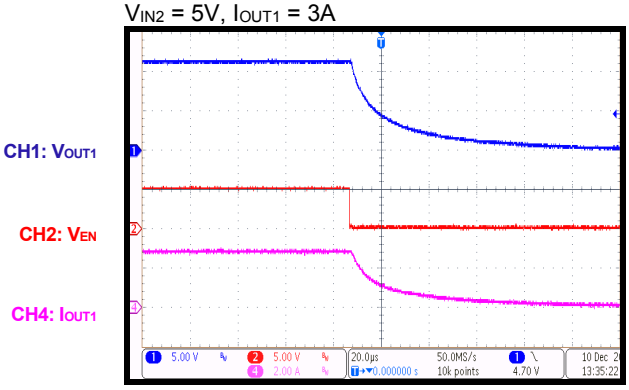
Start-Up through Enable (12V E-Fuse)

V_{IN2} = 5V, I_{OUT1} = 3A



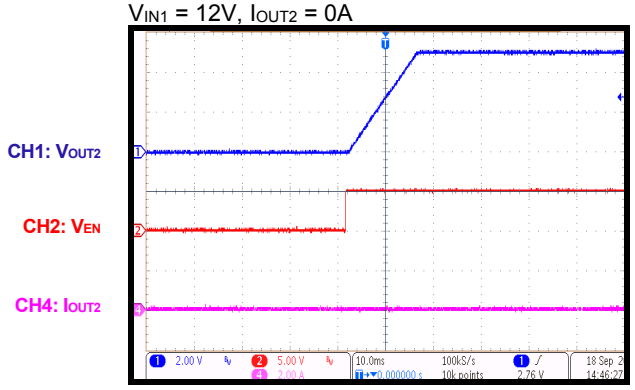
Shutdown through Enable (12V E-Fuse)

V_{IN2} = 5V, I_{OUT1} = 3A



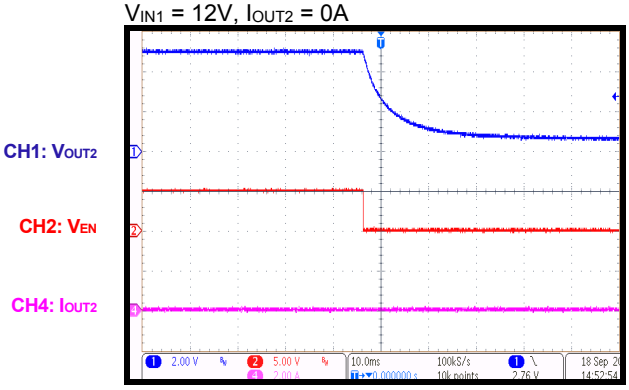
Start-Up through Enable (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 0A



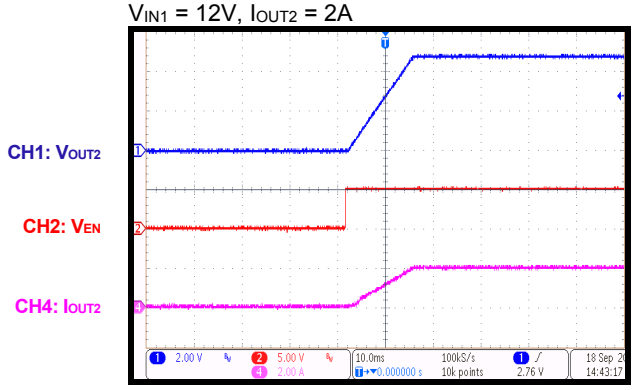
Shutdown through Enable (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 0A



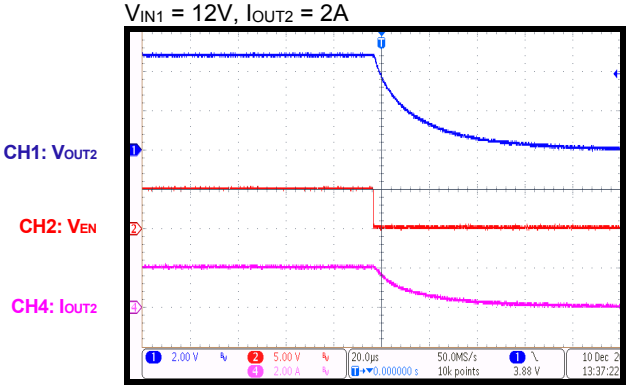
Start-Up through Enable (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 2A



Shutdown through Enable (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 2A



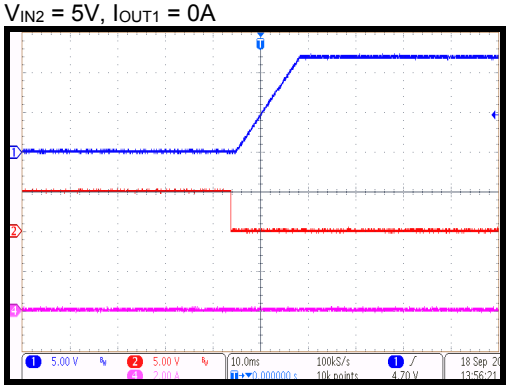
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

EVB TEST RESULTS *(continued)*

Performance waveforms are tested on the evaluation board.
V_{IN1}=12V, V_{IN2}=5V, T_A=25°C, unless otherwise noted.

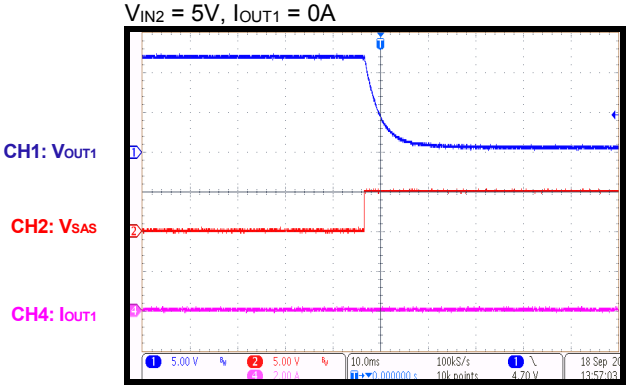
Start-Up through SAS (12V E-Fuse)

V_{IN2} = 5V, I_{OUT1} = 0A



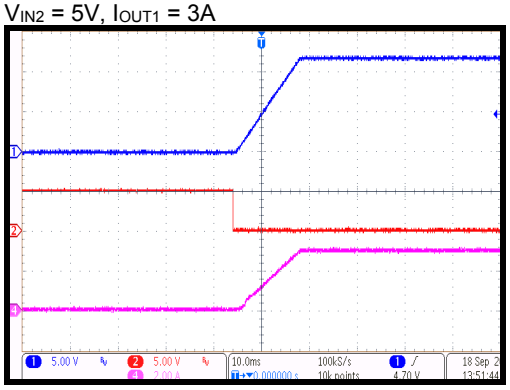
Shutdown through SAS (12V E-Fuse)

V_{IN2} = 5V, I_{OUT1} = 0A



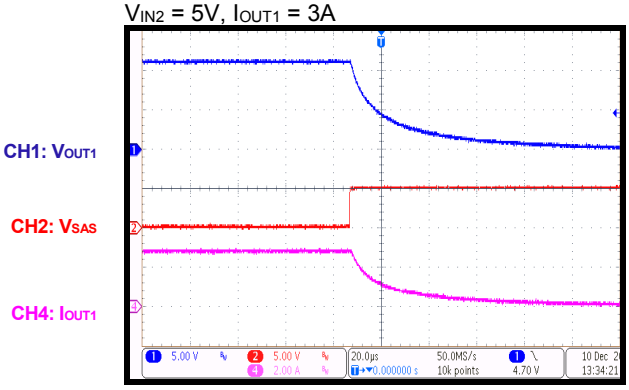
Start-Up through SAS (12V E-Fuse)

V_{IN2} = 5V, I_{OUT1} = 3A



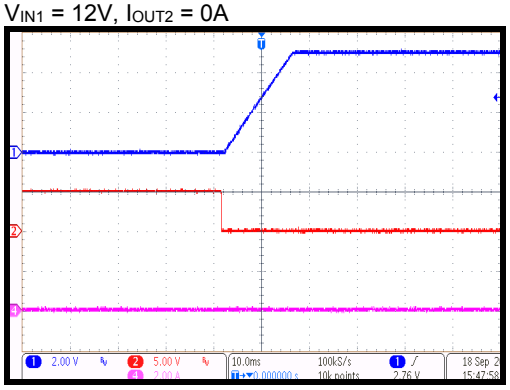
Shutdown through SAS (12V E-Fuse)

V_{IN2} = 5V, I_{OUT1} = 3A



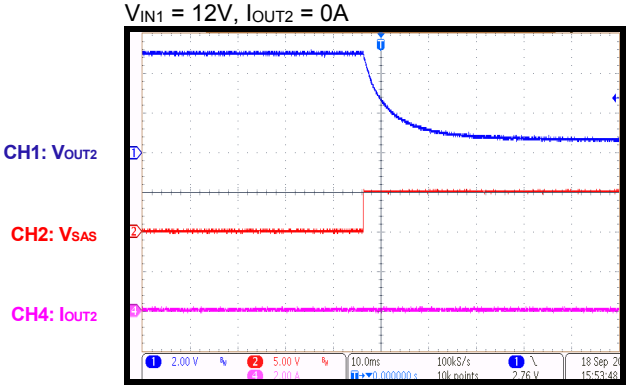
Start-Up through SAS (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 0A



Shutdown through SAS (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 0A



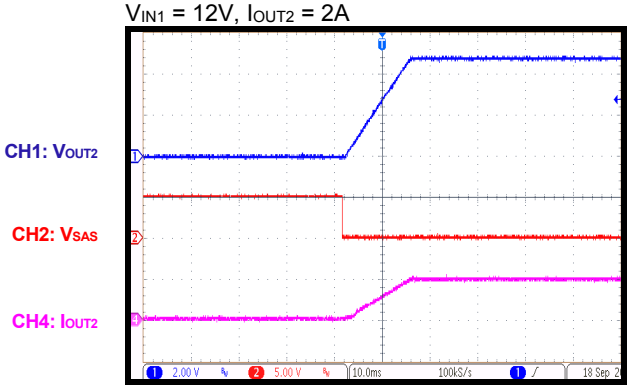
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

EVB TEST RESULTS *(continued)*

Performance waveforms are tested on the evaluation board.
V_{IN1}=12V, V_{IN2}=5V, T_A=25°C, unless otherwise noted.

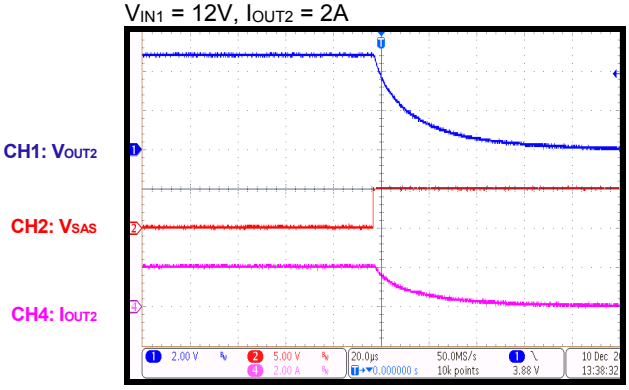
Start-Up through SAS (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 2A



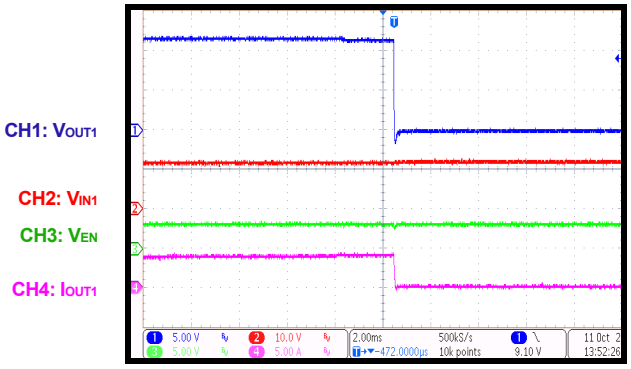
Shutdown through SAS (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 2A

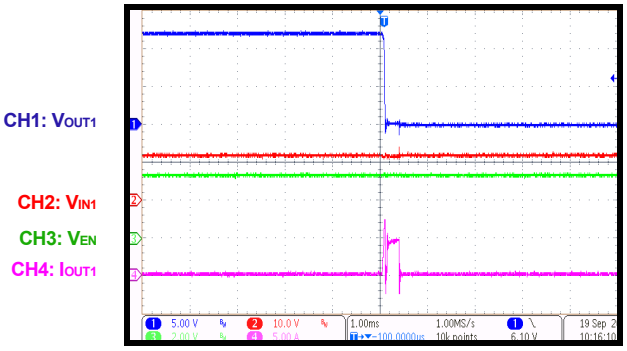


Current Limit (12V E-Fuse)

Increase I_{OUT} Slowly

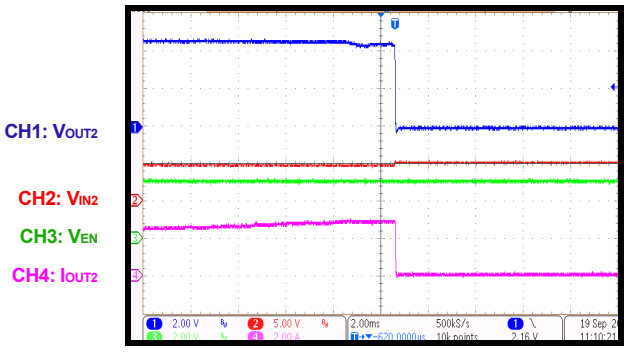


Short Circuit during Normal Operation (12V E-Fuse)

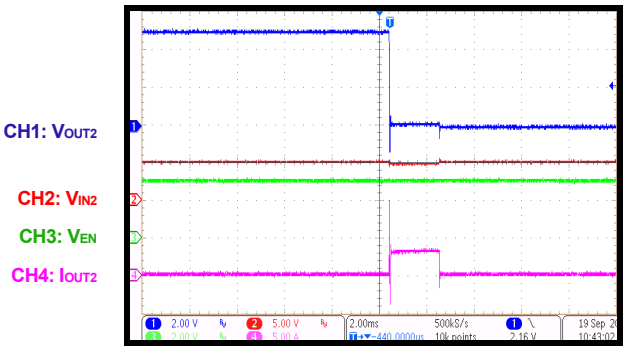


Current Limit (5V E-Fuse)

Increase I_{OUT} Slowly



Short Circuit during Normal Operation (5V E-Fuse)



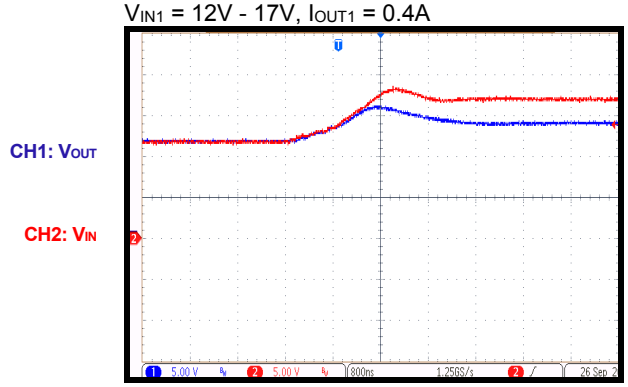
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

EVB TEST RESULTS *(continued)*

Performance waveforms are tested on the evaluation board.
V_{IN1}=12V, V_{IN2}=5V, T_A=25°C, unless otherwise noted.

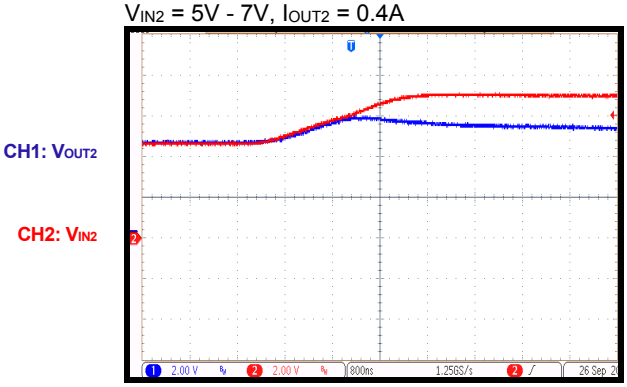
Output Over-Voltage Protection (12V E-Fuse)

V_{IN1} = 12V - 17V, I_{OUT1} = 0.4A



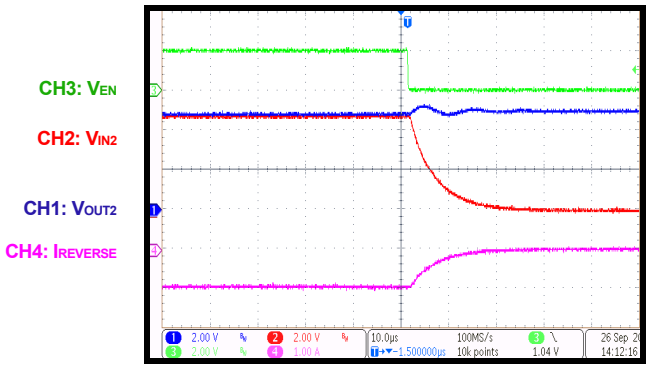
Output Over-Voltage Protection (5V E-Fuse)

V_{IN2} = 5V - 7V, I_{OUT2} = 0.4A



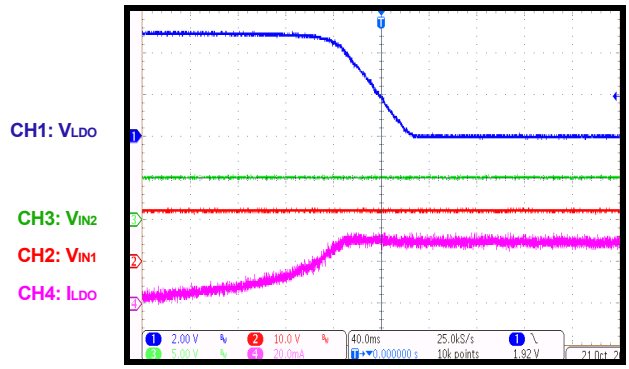
Reverse Protection (5V E-Fuse)

Increase $I_{REVERSE}$ Slowly



Current Limit (LDO)

Increase I_{LDO} Slowly



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

PRINTED CIRCUIT BOARD LAYOUT

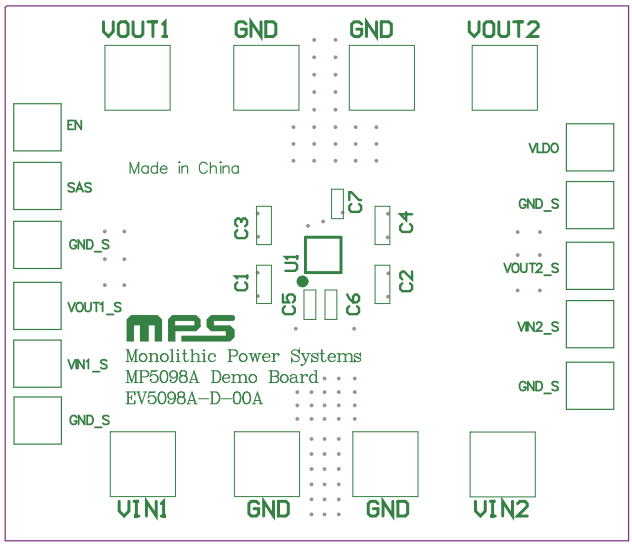


Figure 1: Top Silk Layer

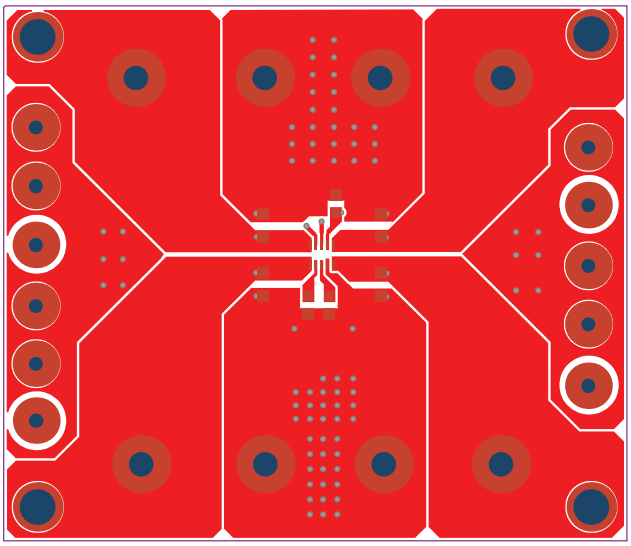


Figure 2: Top Layer

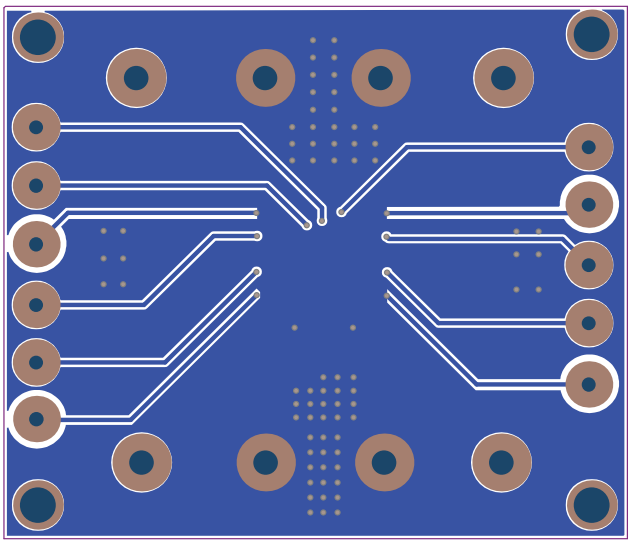


Figure 3: Bottom Layer

NOTICE: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.