MPQ3414C

1.5A, 2.2MHz, 5V$_{OUT}$, 52µA I$_Q$, Synchronous Step-Up Converter with Output Disconnect, AEC-Q100 Qualfied

DESCRIPTION

The MPQ3414C is a high-efficiency, synchronous, current-mode step-up converter with output disconnect.

The MPQ3414C can start up from an input voltage (V_{IN}) as low as 1.8V, while also providing inrush current limiting and output short-circuit protection (SCP). The integrated P-channel synchronous rectifier (SR) improves efficiency and eliminates the need for an external Schottky diode. If the MPQ3414C shuts down, then the P-channel MOSFET disconnects the output from the input. Output disconnect discharges the output completely, which allows the MPQ3414C to draw a shutdown current (I_{SD}) below 1µA during shutdown.

The 2.2MHz fixed switching frequency (f_{SW}) allows for the use of small external components. f_{SW} can be synchronized to an external source, from 2MHz to 2.5MHz. Internal compensation and soft start (SS) reduce the number of external components required. These features provide a compact solution for a wide current load range.

The MPQ3414C features an integrated power MOSFET that supports up to 5V of output voltage (V_{OUT}), with up to 1A of average output current (I_{OUT}).

The MPQ3414C requires a minimal number of standard external components, and is available in a compact TSOT23-8 package. It is available in AEC-Q100 Grade 1.

FEATURES

- Designed for Automotive Applications
  - 1.8V to 4V Input Voltage (V_{IN}) Range
  - Fixed 5V Output Voltage (V_{OUT})
  - Up to 1A Average Output Current (I_{OUT})
  - Available in AEC-Q100 Grade 1
- Increases Battery Life
  - 52µA Supply Current (I_Q)
  - <1µA Shutdown Current (I_{SD})
  - Output Disconnect
  - Selectable Advanced Asynchronous Modulation (AAM) Mode or Forced Continuous Conduction Mode (FCCM) Operation under Light Loads
  - Up to 95% Efficiency
- Reduces Board Size and BOM
  - 2.2MHz Fixed Switching Frequency (f_{SW})
  - Small External Components
  - 80mΩ/70mΩ Internal Power MOSFETs
  - Available in a TSOT23-8 Package
- Additional Features
  - Internal Synchronous Rectifier (SR)
  - Internal Compensation, Inrush Current Limiting, and Internal Soft Start (SS)
  - Switching Frequency (f_{SW}) Synchronizable to External 2MHz to 2.5MHz Source
  - Over-Voltage Protection (OVP), Short-Circuit Protection (SCP), and Over-Temperature Protection (OTP)
- Functional Safety System Design Capable
  - MPSafe™ Compatible – Functional Safety Supporting Document Available

MPSafe™ FuSa Compatible

APPLICATIONS

- Single-Cell Li-Ion Backup Batteries
- Automotive Secondary Regulation

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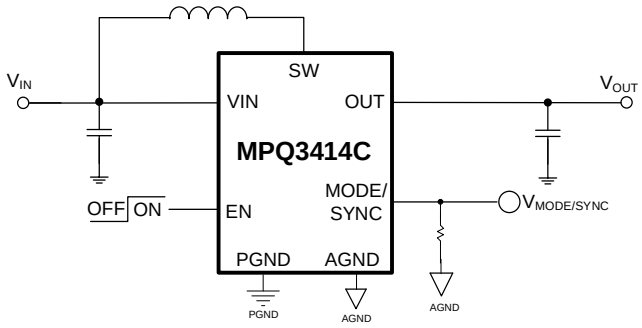
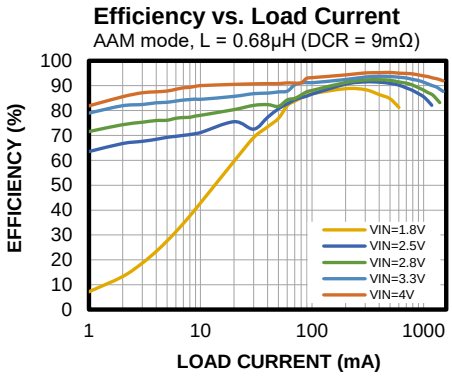
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ3414CGJ-5-AEC1	TSOT23-8	*See Below*	1

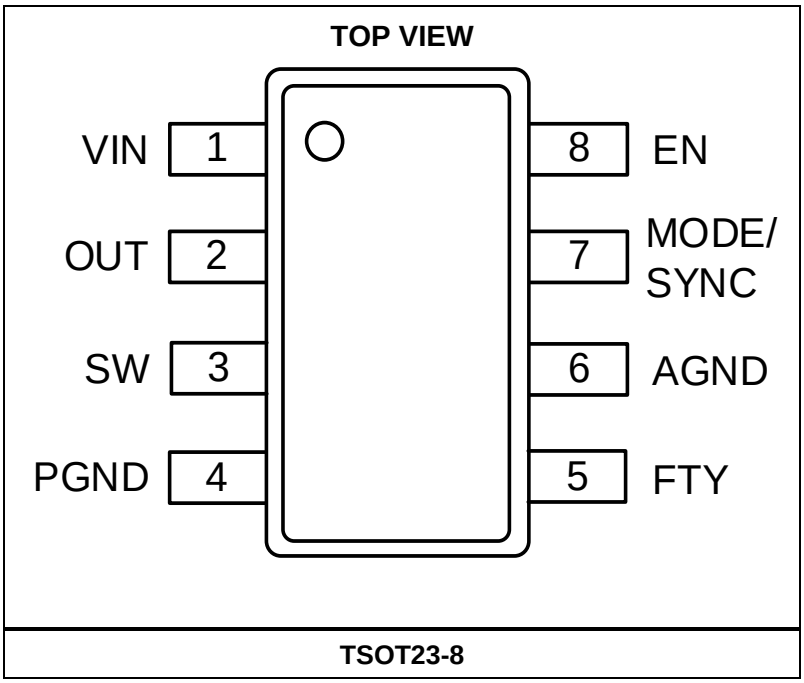
* For Tape & Reel, add suffix -Z (e.g. MPQ3414CGJ-5-AEC1-Z).
** Moisture Sensitivity Level Rating.

TOP MARKING

CCJY

CCJ: Product code
Y: Year code

PACKAGE REFERENCE



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PIN FUNCTIONS

Pin #	Name	Pin Function
1	VIN	**Power supply input.** The start-up bias is derived from the VIN pin, which should be bypassed locally. Once the output voltage (V_{OUT}) exceeds the input voltage (V_{IN}), the bias is derived from the OUT pin.
2	OUT	**Synchronous rectifier (SR) output.** The OUT pin is the drain of the internal SR. If V_{OUT} exceeds V_{IN}, then the bias is derived from the VIN pin. Connect OUT to the output capacitors using short and wide traces. Output disconnect allows the output to be discharged from the input completely while the EN pin is pulled low. OUT is also the sense point for voltage regulation.
3	SW	**Power switch output.** The SW pin is the connection node for the internal low-side MOSFET (LS-FET) and the synchronous MOSFET. Connect the inductor between the SW and VIN pins. Keep the SW trace as short and wide as possible to reduce EMI and voltage spikes.
4	PGND	**Power ground.**
5	FTY	**Factory use only.** It is recommended to connect the FTY pin to ground (AGND or PGND) during PCB design.
6	AGND	**Analog ground.**
7	MODE/ SYNC	**Mode selection and SYNC input.** Apply a clock signal to this pin to synchronizes the internal switching frequency (f_{SW}) to an external clock. Use an external clock or pull this pin low to enter forced continuous conduction mode (FCCM). Pull this pin high to enable advanced asynchronous modulation (AAM) mode and pulse skipping under light loads. Do not float this pin.
8	EN	**Enable control.** Pull the EN pin above 1.2V to turn the converter on; pull EN below 0.4V to turn it off. Do not float this pin.

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ABSOLUTE MAXIMUM RATINGS (1)

V_{SW}, V_{OUT} .....-0.3V to +6.5V
V_{SW} (<5ns) .....-0.3V to +9V
All other pins .....-0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2)
..... 1.25W
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM)..... Class 2 (3)
Charged-device model (CDM).....Class C2b (4)

Recommended Operating Conditions (5)

Input voltage (V_{IN}) ..... 1.8V to 4V (6)
Enable (EN) voltage (V_{EN}).....0V to 4V
Operating junction temp (T_J)..-40°C to +125°C (7)

Thermal Resistance	θ_{JA}	θ_{JC}	
TSOT23-8			
JESD51-7	100	55	°C/W (8)

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the device may to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Per AEC-Q100-002.
4) Per AEC-Q100-011.
5) The device is not guaranteed to function outside of its operating conditions.
6) If V_{IN} is close to V_{OUT}, then the boost converter may trigger the minimum on time (t_{ON}). If V_{IN} exceeds V_{OUT}, then the boost converter switches between boost mode and linear charge mode. Both conditions can result in an exceedingly high output voltage ripple (ΔV_{OUT}); therefore, it is not recommended to have V_{IN} exceed V_{OUT}.
7) The device is not guaranteed to function outside of the operation conditions. Operating devices at junction temperatures greater than 125°C may be possible. Contact MPS for details.
8) Measured on a JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application. The value of θ_{JC} shows the thermal resistance from junction-to-case bottom.

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ELECTRICAL CHARACTERISTICS

V_{IN} = V_{EN} = 3.3V, V_{OUT} = 5V, T_J = -40°C to +125°C, typical values are tested at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input Voltage Range						
Supply current	I_{Q_OUT}	V_{MODE} = V_{EN} = V_{IN} = 3.3V, V_{OUT} = 6V, no load, measured on OUT, T_J = 25°C		52	80	µA
Quiescent current	I_{Q_IN}	V_{MODE} = V_{EN} = V_{IN} = 3.3V, V_{OUT} = 6V, T_J = 25°C, no load, measured on VIN		8	14	µA
Shutdown current	I_{SD}	V_{EN} = V_{OUT} = 0V, T_J = 25°C, measured on VIN		0.1	1	µA
V_{IN} under-voltage lockout (UVLO) threshold	V_{IN_UVLO}	V_{IN} rising, T_J = 25°C		1.65	1.7	V
V_{IN} UVLO hysteresis				100		mV
Step-Up Converter						
Switching frequency	f_{SW}		1.9	2.2	2.5	MHz
Reference voltage	V_{REF}	T_J = 25°C	4.9	5	5.1	V
		T_J = -40°C to +125°C	4.875	5	5.125	V
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)_LS}$			70		mΩ
LS-FET leakage current	I_{LKG_LS}	V_{SW} = 6.5V, T_J = 25°C		0.1	1	µA
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)_HS}$			80		mΩ
HS-FET leakage current	I_{LKG_PMOS}	V_{SW} = 6.5V, V_{OUT} = 0V, T_J = 25°C		0.1	1	µA
Maximum duty cycle	D_{MAX}	V_{IN} = 3.3V		85		%
Start-up current limit	I_{LIMIT_SU}	V_{IN} = 4V, V_{OUT} = 0V	0.1	0.3	0.4	A
		V_{IN} = 4V, V_{OUT} is set to 3.6V, pull V_{OUT} to 3.3V	0.4	0.8	1	A
LS-FET current limit	I_{LIMIT_LS}	40% duty cycle	2.5	3.6	4.5	A
MODE/SYNC						
Threshold voltage	V_{SYNC}	Rising threshold	0.4	0.6	0.8	V
		Hysteresis		50		mV
SYNC clock range (9)	f_{SYNC}		2.0		2.5	MHz
Logic Interface						
Enable (EN) high voltage	V_{EN_HIGH}		1.2			V
EN low voltage	V_{EN_LOW}				0.4	V
EN current	I_{EN}	Connected to V_{IN}		10		nA
Thermal Protections						
Thermal shutdown (9)	T_{SD}		150	160	175	°C
Thermal shutdown hysteresis (9)				25		°C

Note:

9) Guaranteed by design and characterization. Not production tested.

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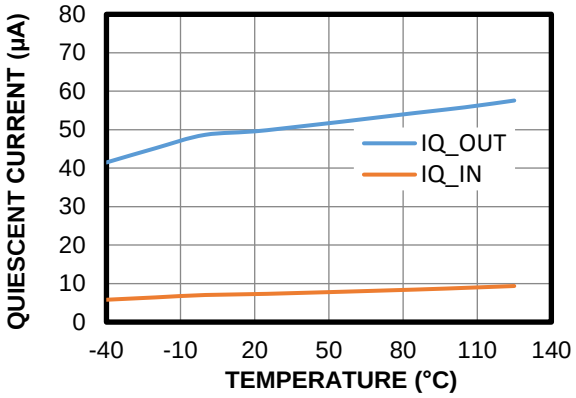
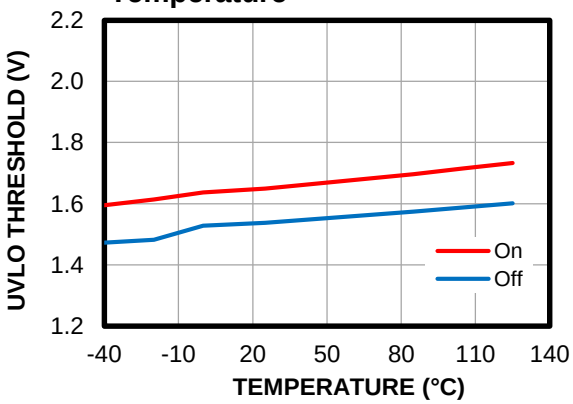
TYPICAL CHARACTERISTICS

V_{IN} = 3.3V, T_J = -40°C to +125°C, unless otherwise noted.

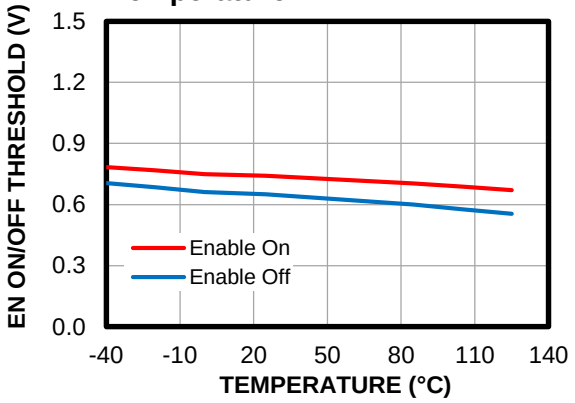
Quiescent Current vs. Temperature



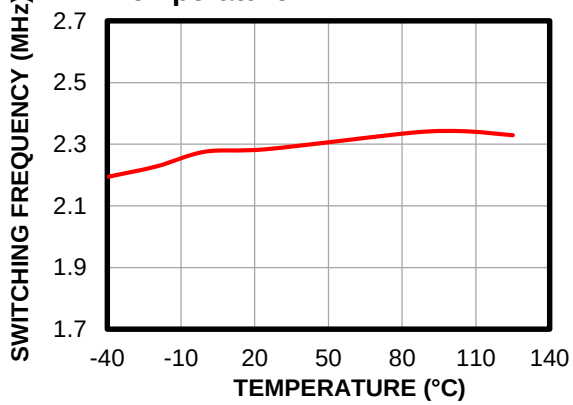
UVLO Threshold vs. Temperature



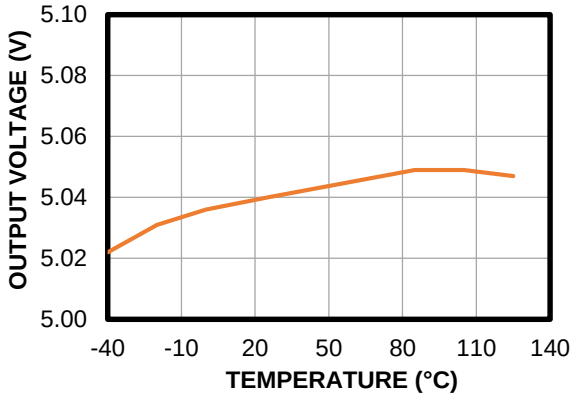
EN On/Off Threshold vs. Temperature



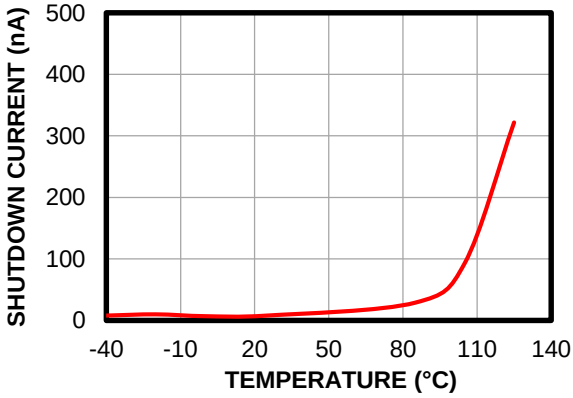
Switching Frequency vs. Temperature



Output Voltage vs. Temperature



Shutdown Current vs. Temperature



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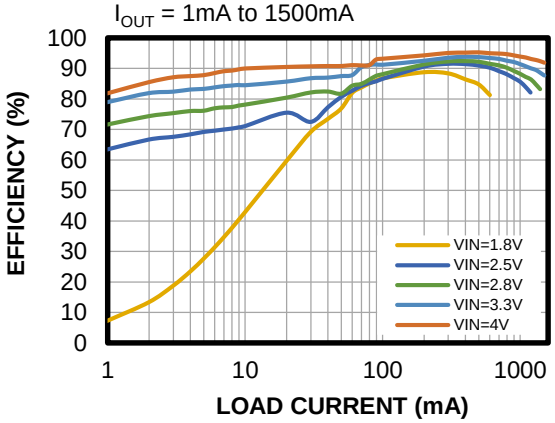
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.3V, V_{OUT} = 5V, L = 0.68µH, T_A = 25°C, unless otherwise noted.

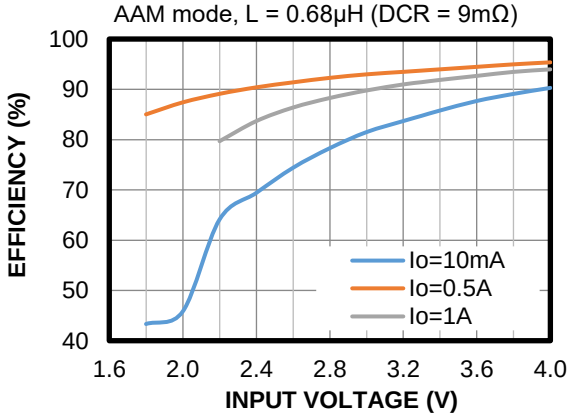
Efficiency vs. Load Current

AAM mode, L = 0.68µH (DCR = 9mΩ),
I_{OUT} = 1mA to 1500mA



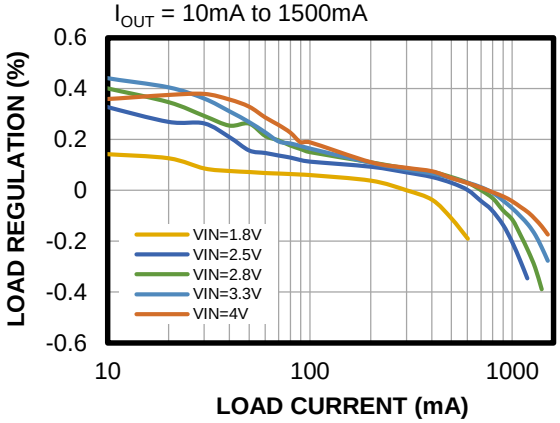
Efficiency vs. Input Voltage

AAM mode, L = 0.68µH (DCR = 9mΩ)



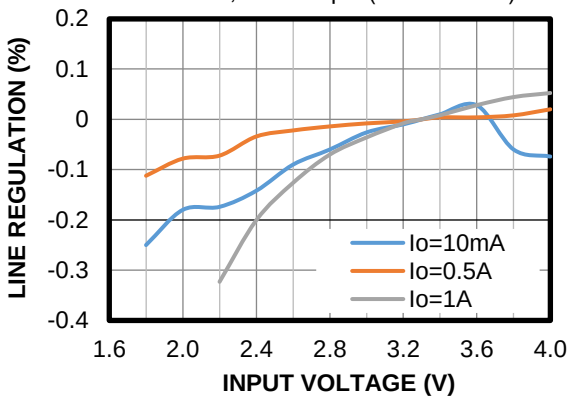
Load Regulation

AAM mode, L = 0.68µH (DCR = 9mΩ),
I_{OUT} = 10mA to 1500mA



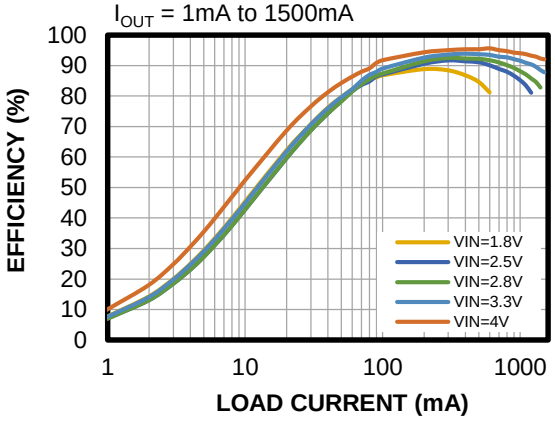
Line Regulation

AAM mode, L = 0.68µH (DCR = 9mΩ)



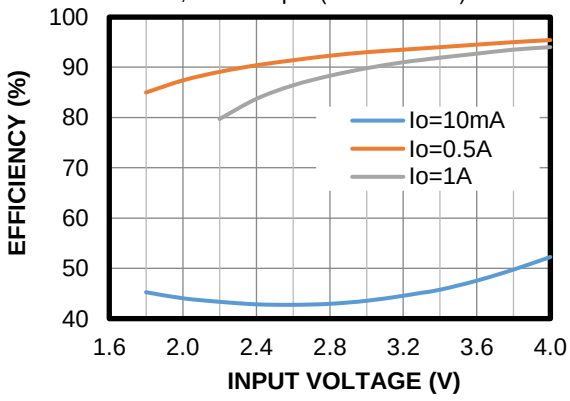
Efficiency vs. Load Current

FCCM, L = 0.68µH (DCR = 9mΩ),
I_{OUT} = 1mA to 1500mA



Efficiency vs. Input Voltage

FCCM, L = 0.68µH (DCR = 9mΩ)



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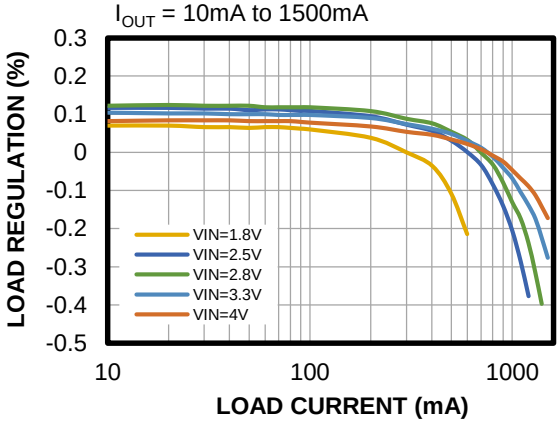
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 5V, L = 0.68µH, T_A = 25°C, unless otherwise noted.

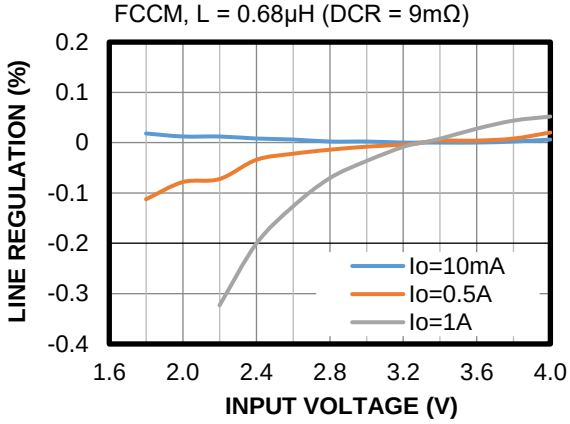
Load Regulation

FCCM, L = 0.68µH (DCR = 9mΩ),
I_{OUT} = 10mA to 1500mA



Line Regulation

FCCM, L = 0.68µH (DCR = 9mΩ)



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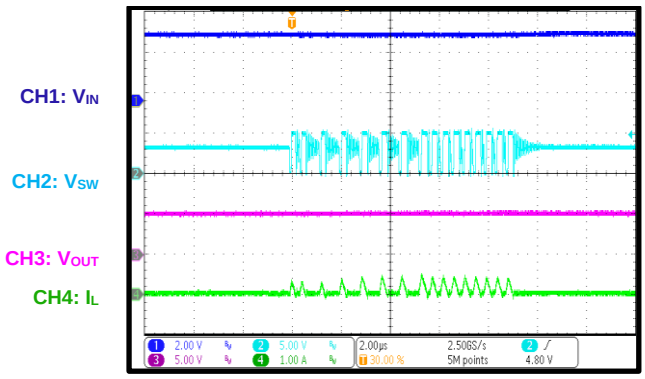
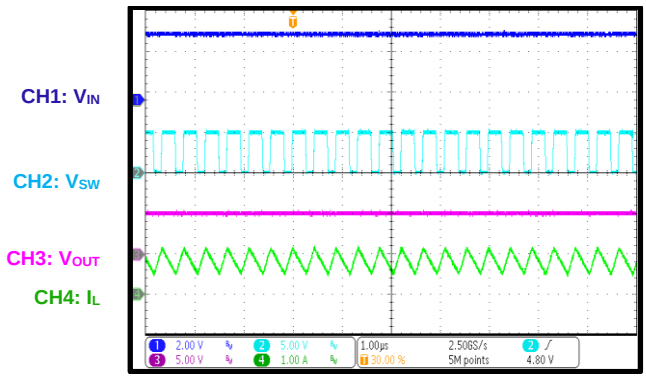
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 5V, L = 0.68µH, T_A = 25°C, unless otherwise noted.

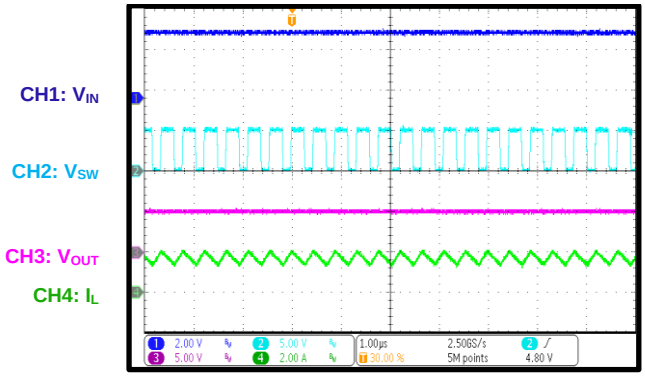
Steady State
AAM mode, I_{OUT} = 0A



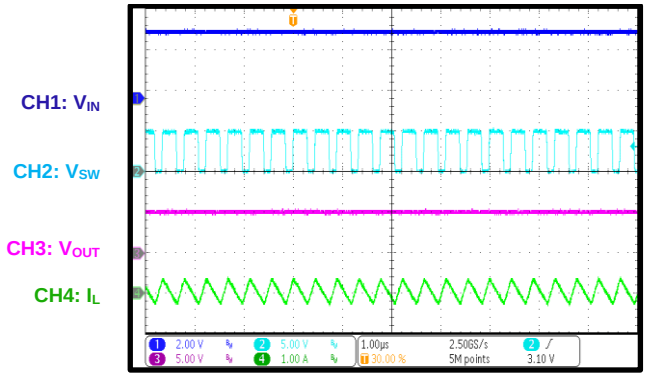
Steady State
AAM mode, I_{OUT} = 0.5A



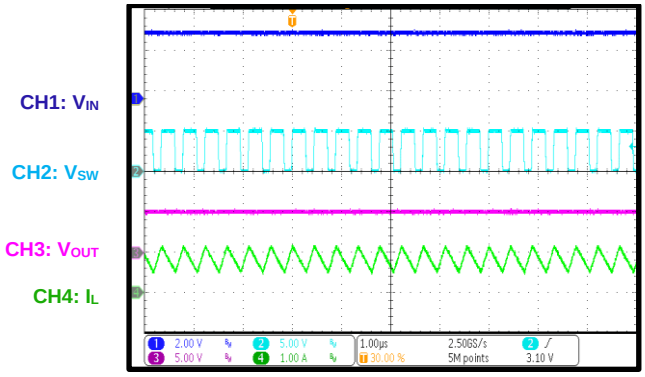
Steady State
AAM mode, I_{OUT} = 1A



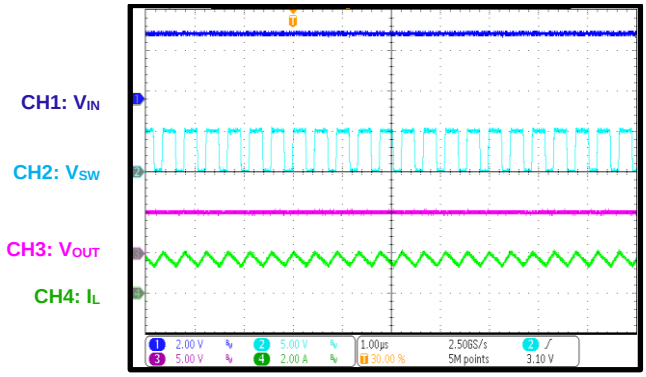
Steady State
FCCM, I_{OUT} = 0A



Steady State
FCCM, I_{OUT} = 0.5A



Steady State
FCCM, I_{OUT} = 1A



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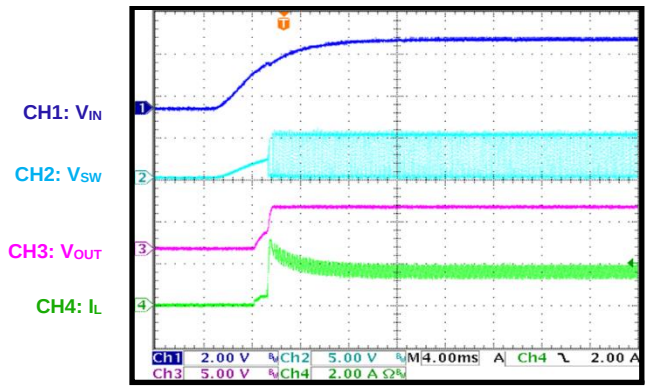
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 5V, L = 0.68µH, T_A = 25°C, unless otherwise noted.

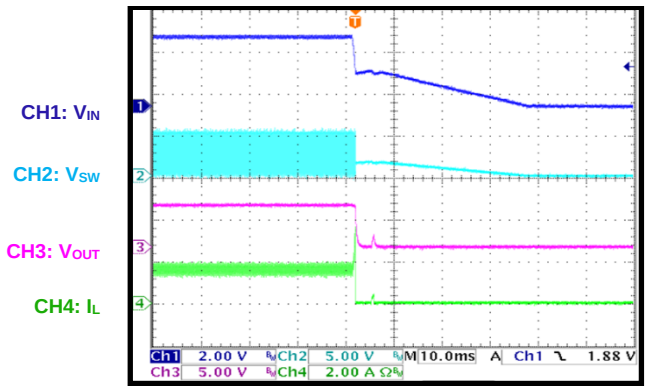
Start-Up through VIN

FCCM, I_{OUT} = 1A



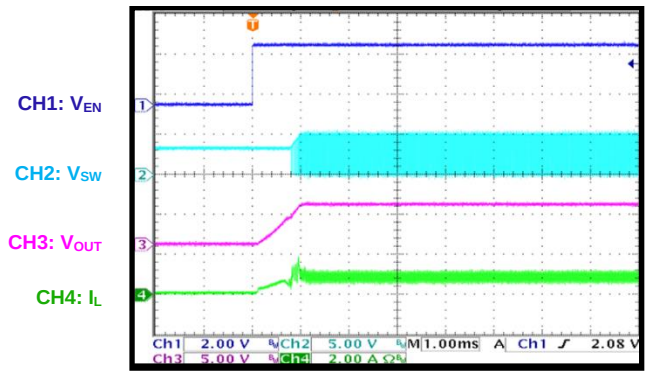
Shutdown through VIN

FCCM, I_{OUT} = 1A



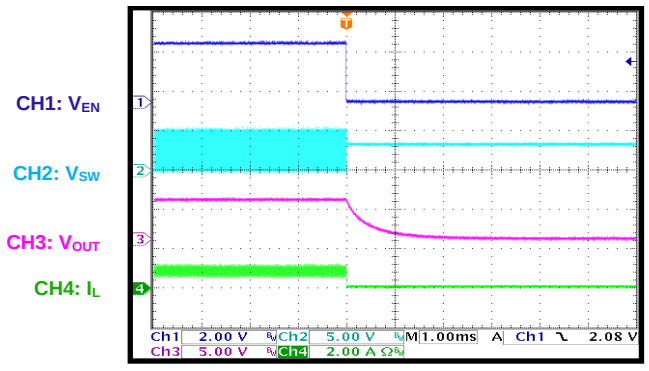
Start-Up through EN

FCCM, I_{OUT} = 0.5A



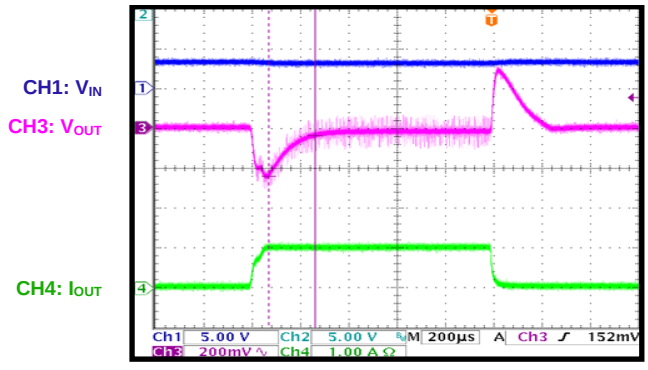
Shutdown through EN

FCCM, I_{OUT} = 0.5A



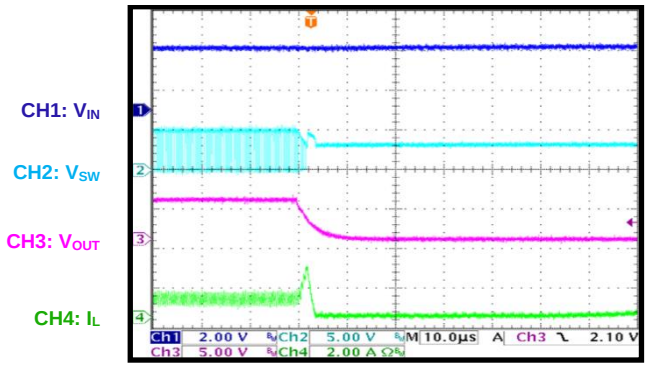
Load Transient

FCCM, I_{OUT} = 0A to 1A, 2.5A/µs slew rate



Short-Circuit Protection

FCCM, I_{OUT} = 0.5A



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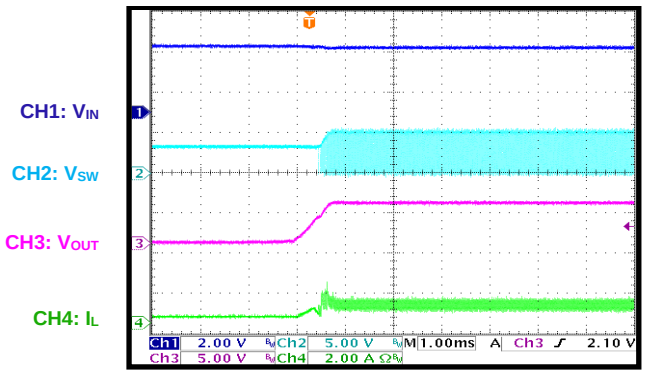
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 5V, L = 0.68µH, T_A = 25°C, unless otherwise noted.

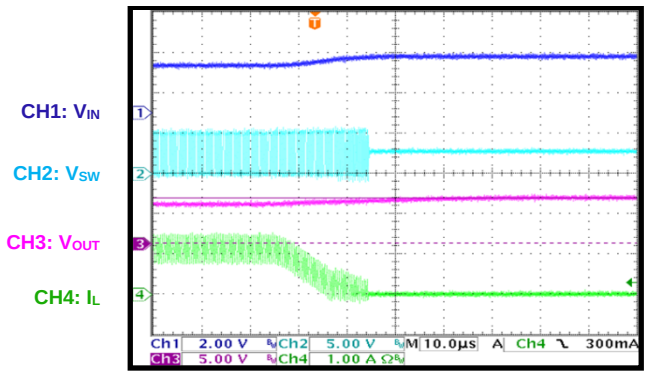
SCP Recovery

FCCM, I_{OUT} = 0.5A



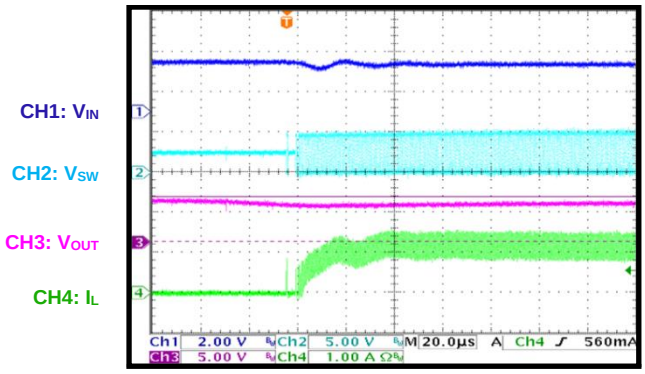
Over-Voltage Protection

V_{IN} = 2.5V, I_{OUT} = 0.5A



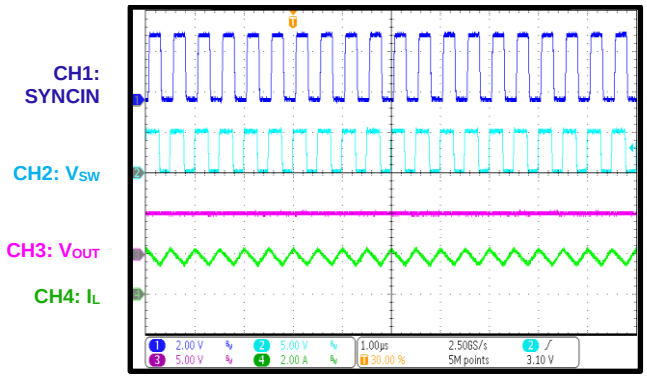
OVP Recovery

V_{IN} = 2.5V, I_{OUT} = 0.5A



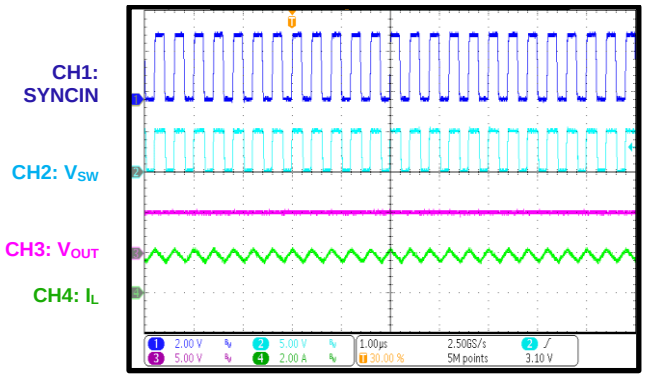
SYNC Operation

I_{OUT} = 1A, SYNC frequency = 2000kHz



SYNC Operation

I_{OUT} = 1A, SYNC frequency = 2500kHz



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FUNCTIONAL BLOCK DIAGRAM

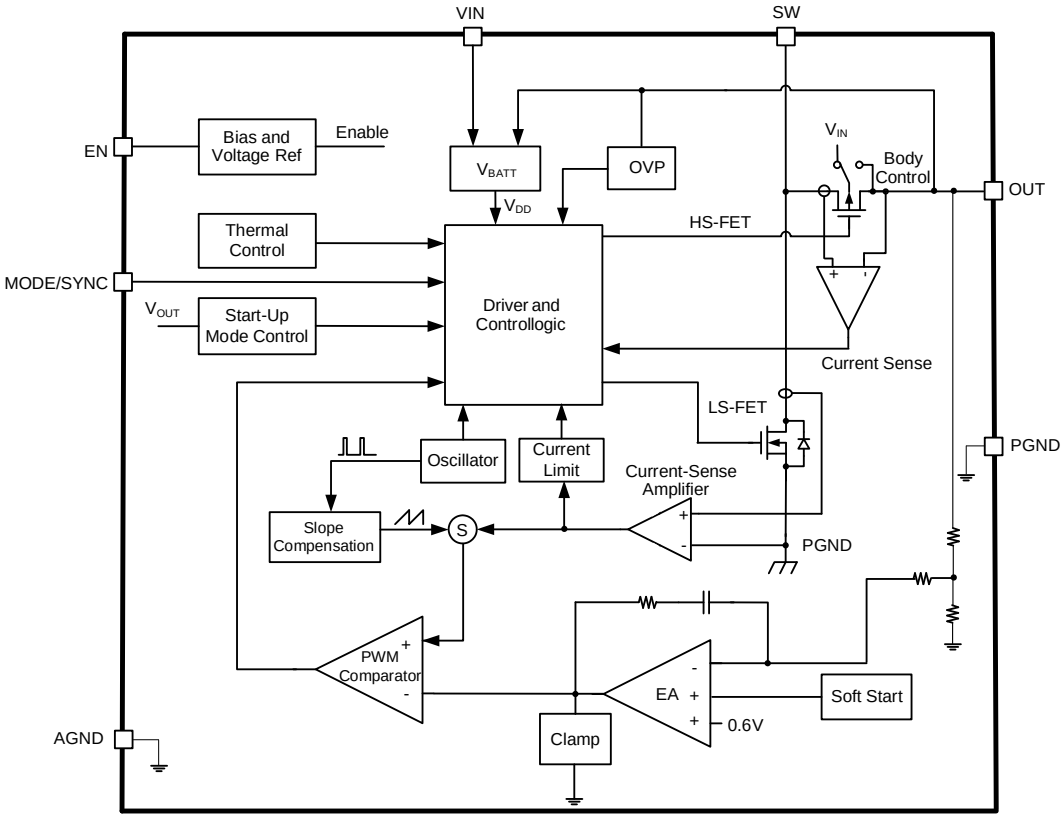

Figure 1: Functional Block Diagram

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OPERATION

The MPQ3414C is a 2.2MHz, synchronous step-up converter with output disconnect. The device's fixed switching frequency (f_{SW}) and pulse-width modulation (PWM) mode control provide good load and line regulation. Internal soft start (SS) and loop compensation simplify the design process and minimize the number of external components. The internal, low on resistance ($R_{DS(ON)}$) MOSFETs and frequency stretching allow the MPQ3414C to maintain high efficiency across a wide load current range.

Start-Up

The MPQ3414C can start up in linear charge mode. In the linear charge mode, the rectified P-channel high-side MOSFET (HS-FET) turns on until the output voltage (V_{OUT}) approaches close to the input voltage (V_{IN}). To avoid inrush current, the HS-FET current (I_{HS}) is limited. If V_{OUT} is 0V, then I_{HS} is limited to about 0.3A. If V_{IN} exceeds 3.3V, then I_{HS} is limited to about 0.8A as V_{OUT} rises to 3.3V. This limits the output current (I_{OUT}) during a short circuit event. Once V_{OUT} reaches V_{IN} and the linear charge time is complete, the device starts up. V_{OUT} starts to rise under the control of the internal soft start (SS). In boost mode, I_{HS} is limited to 3.6A.

When V_{OUT} exceeds V_{IN}, the MPQ3414C uses V_{OUT} to power the internal circuitry instead of V_{IN}. This allows the device to operate at high efficiency with strong driving capabilities.

Soft Start (SS)

The MPQ3414C provides soft start (SS) via an internal capacitor with a current source. During linear charge mode, the SS voltage (V_{SS}) rises according to the feedback (FB) voltage (V_{FB}). Once the linear charge time is complete, V_{SS} is charged and the reference voltage (V_{REF}) ramps up according to the fixed internal slew rate. If the device shuts down, thermal shutdown is triggered, or there is a short circuit event, the SS capacitor (C_{SS}) is discharged completely.

Enable (EN)

Pull the enable (EN) pin above 1.2V to turn the converter on; pull EN below 0.4V to turn it off. During shutdown, the converter stops switching, the internal control circuitry turns off, and the output disconnects from the input.

MODE/SYNC

The switching frequency (f_{SW}) can be synchronized to the rising edge of a clock signal applied at the MODE/SYNC pin. The recommended SYNC frequency (f_{SYNC}) range is 2MHz to 2.5MHz. Use a signal with a 25% to 65% duty ratio. The SYNC function forces the part to enter forced continuous conduction mode (FCCM). Once soft start is complete, synchronization begins. When MODE/SYNC is used for mode selection, pull this pin low to make the part work in FCCM (MODE < 0.4V), or pull it high (MODE > 0.8V) to make the part work in advanced asynchronous modulation (AAM) mode. It is not recommended to adjust the MODE pin during operation, as it may lead to a disturbance on the output. Do not float this pin.

Error Amplifier (EA)

The MPQ3414C features an internal error amplifier (EA) with internal compensation. The EA compares the internal V_{REF} (0.6V) and V_{FB} to generate an EA signal to control V_{OUT}. V_{OUT} is fixed at 5V.

Current Sense

In linear charge mode, I_{HS} is sensed and compared to the current limit threshold (I_{LIMIT_HS}). The compared output manages I_{HS}.

In boost mode, lossless current sensing converts the N-channel low-side MOSFET (LS-FET) switch current signal to a voltage that is added to the internal slope compensation. This signal is compared to the EA output to provide a peak current control command for PWM mode. The peak switch current is limited to about 3.6A. The switch current signal has an internal blanking time (60ns) to reduce noise.

Output Disconnect

The MPQ3414C eliminates the internal rectifier's body diode conduction to provide output disconnect. This allows V_{OUT} to drop to 0V during shutdown, which draws zero current from the input source. In turn, this allows for inrush current limiting during start-up, which minimizes the surge current at the input. To use output disconnect, an external Schottky diode cannot be connected between the SW and OUT pins.

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Overload Protection (OLP) and Short-Circuit Protection (SCP)

If an overload fault or a short circuit occurs, V_{OUT} drops. If V_{OUT} drops below V_{IN} (0.3V), then the converter shuts down. Once the overload fault or short circuit is removed, then the device initiates an SS, starts up again in linear charge mode after a set delay time (50µs), and resumes normal operation.

Over-Voltage Protection (OVP)

If V_{OUT} exceeds 6V, then converter turns off. Once V_{OUT} drops to about 5.7V, the converter recovers automatically and resumes normal operation. This protects the internal MOSFET from over-voltage (OV) stress.

Thermal Shutdown

The device monitors the die temperature internally. If the die temperature exceeds the thermal shutdown threshold (about 155°C), the converter shuts down. Once the temperature drops below 130°C, the converter initiates a SS and resumes normal operation.

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APPLICATION INFORMATION

Selecting the Input Capacitor (C_{IN})

Low-ESR input capacitors reduce input switching noise and the peak current drawn from the battery. Ceramic capacitors are recommended for input decoupling, and should be placed as close to the IC as possible. It is recommended to use a >10µF ceramic capacitor to limit the V_{IN} ripple (ΔV_{IN}).

Selecting the Output Capacitor (C_{OUT})

To ensure stability across the entire operating range, place an output capacitor (C_{OUT}) on the OUT pin. A 22µF to 66µF C_{OUT} is recommended in most applications. A higher capacitance may be required to decrease V_{OUT} and the transient ripple. Low-ESR capacitors with X5R or X7R type dielectrics are recommended. The minimum C_{OUT} required to support the ripple in PWM mode (C_{OUT_MIN}) can be calculated with Equation (2):

$$C_{OUT_MIN} \geq \frac{I_{OUT} \times (V_{OUT_MAX} - V_{IN_MIN})}{f_{SW} \times V_{OUT_MAX} \times \Delta V_{OUT}} \quad (2)$$

Where the ESR is 0Ω, V_{OUT_MAX} is the maximum V_{OUT}, V_{IN_MIN} is the minimum V_{IN}, and ΔV_{OUT} is the acceptable V_{OUT} ripple.

Place a 0.1µF ceramic between the OUT and PGND pins using a short loop to reduce EMI and voltage spikes on the SW pin.

Selecting the Inductor

The MPQ3414C utilizes small, surface-mount inductors due to its 2.2MHz f_{SW}. A 0.47µH to 1.2µH inductor is suitable for most applications.

A larger-value inductor allows for greater I_{OUT} capabilities by reducing the inductor ripple current; however, it also has a larger physical size. The minimum inductance (L) can be calculated with Equation (3):

$$L \geq \frac{V_{IN_MIN} \times (V_{OUT_MAX} - V_{IN_MIN})}{V_{OUT_MAX} \times \Delta I_L \times f_{SW}} \quad (3)$$

Where ΔI_L is the acceptable inductor current (I_L) ripple.

ΔI_L is typically set to be between 30% and 50% of the maximum I_L (I_{L_MAX}). Keep the series resistance of the inductor low to reduce resistive power loss. The saturated current (I_{SAT}) should be large enough to support the peak current.

Design Example

Table 1 shows a design example following the application guidelines for the specifications below.

Table 1: Design Example

V_{IN}	1.8V to 4V
V_{OUT}	5V
I_{OUT} (Peak)	1.5A
I_{OUT} (Average)	1A

Figure 3 on page 18 shows a typical application circuit for a 5V output. For more device applications, refer to the related evaluation board datasheet.

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PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. Poor layout can result in reduced performance, excessive EMI, resistive loss, system instability, and over-voltage (OV) stress. For the best results, refer to Figure 2 and follow the guidelines below:

1. Place the C_{OUT} as close to the OUT pin and PGND as possible.
2. Place a small decoupling capacitor in parallel with the bulk output capacitor.
3. Place the small decoupling capacitor as close to the OUT and PGND pins as possible to reduce EMI and voltage spikes on SW.
4. Place C_{IN} and the inductor as close to the VIN and SW pins as possible using short and wide traces.
5. Place the feedback loop far away from any noisy nodes, such as SW.
6. Place the feedback (FB) resistor divider as close to the FB node and AGND as possible.
7. Place the C_{IN} and C_{OUT} ground return as close to PGND as possible using a large copper ground area and multiple vias to improve thermal performance.

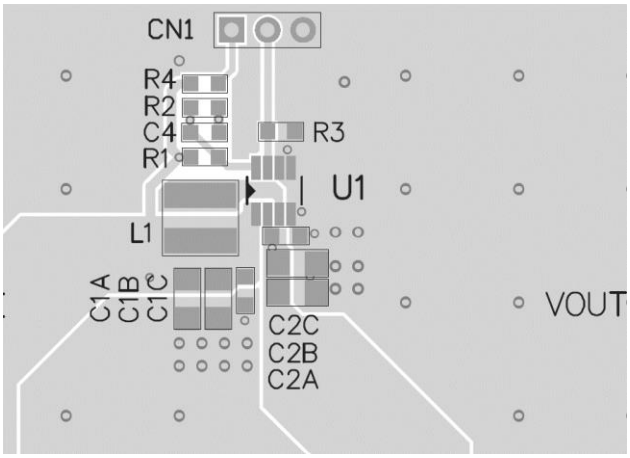

Figure 2: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUIT

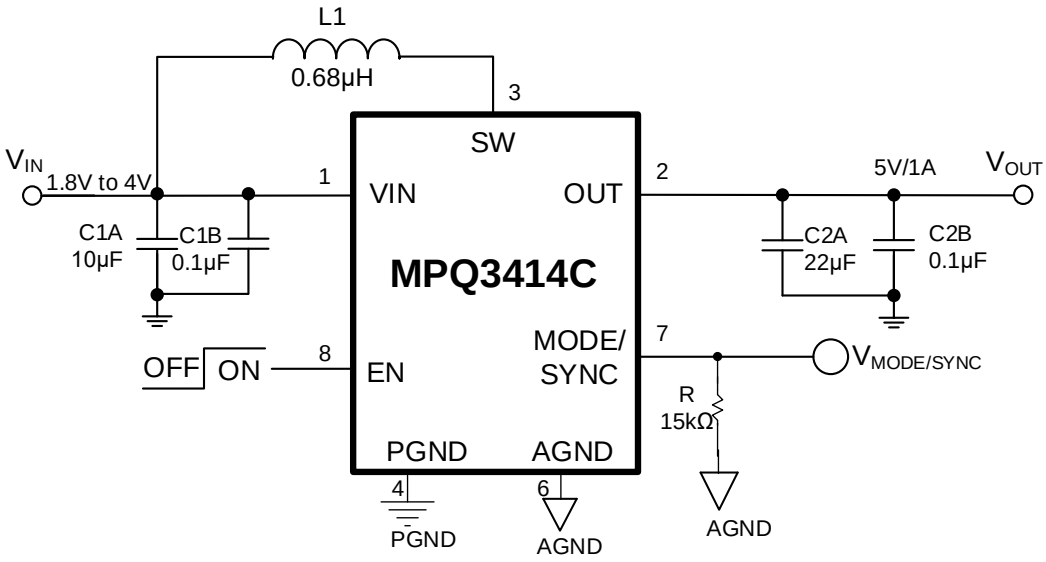

Figure 3: Typical Application Circuit (V_{IN} = 1.8V to 4V, V_{OUT} = 5V, I_{OUT} = 1A, I_{OUT_PEAK} = 1.5A) (10)

Note:

10) Connect the AGND and PGND pins together in actual applications.

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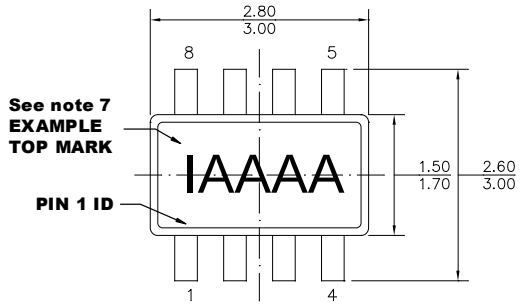
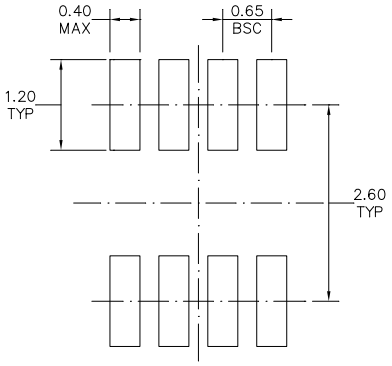
PACKAGE INFORMATION

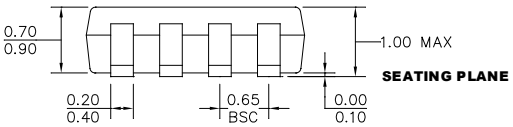
TSOT23-8



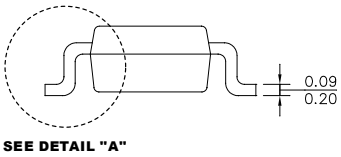
TOP VIEW



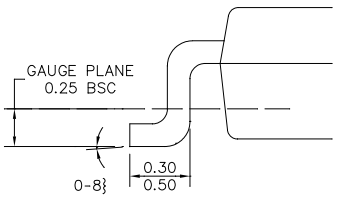
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITIES (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.1 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-193, VARIATION BA.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS THE LOWER LEFT PIN WHEN READING THE TOP MARK FROM LEFT TO RIGHT (SEE EXAMPLE TOP MARK).

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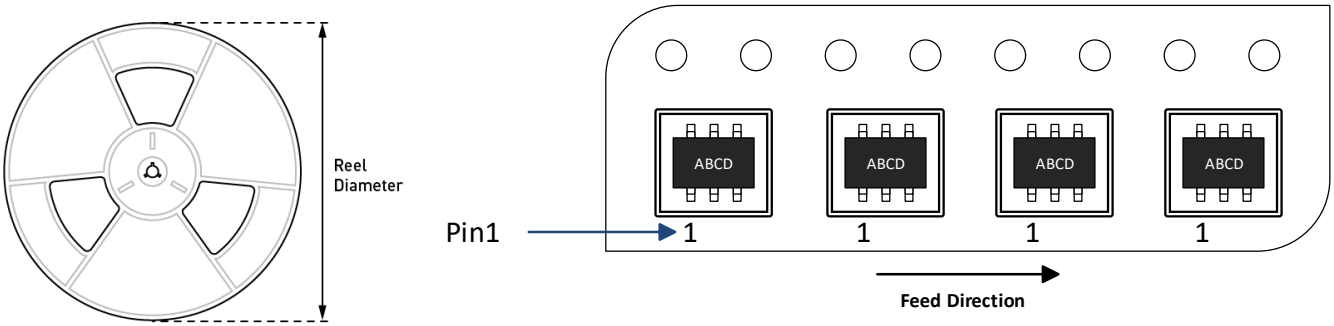
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ3414CGJ-5-AEC1-Z	TSOT23-8	3000	N/A	N/A	7in	8mm	4mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	7/23/2024	Initial Release	-

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