



# MPQ18024

## 100V, 4A, High-Frequency, Half-Bridge Gate Driver AEC-Q100 Qualified

### DESCRIPTION

The MPQ18024 is a high-frequency, 100V, half-bridge, N-channel power MOSFET driver. Its low-side and high-side driver channels are controlled independently and matched with less than 5ns of time delay. Under-voltage lockout (UVLO) on the high-side and low-side supplies force their outputs low in the case of an insufficient supply. The integrated bootstrap diode reduces the external component count.

### FEATURES

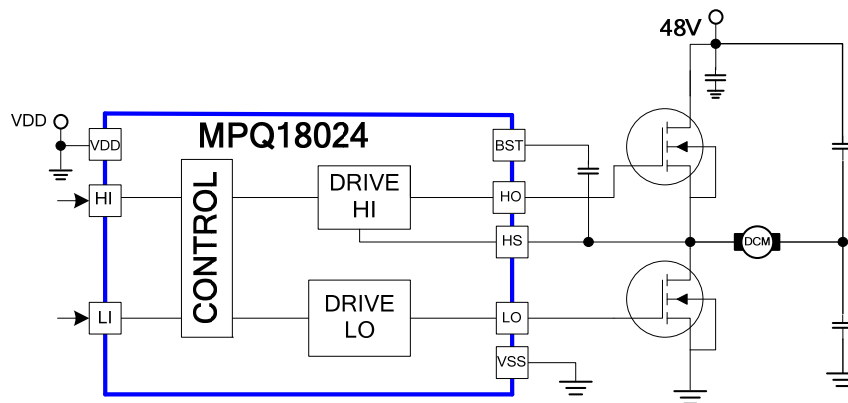
- Guaranteed Industrial / Automotive Temperature Range Limits
- Drives an N-Channel MOSFET Half-Bridge
- 100V  $V_{BST}$  Voltage Range
- On-Chip Bootstrap Diode
- Typical Propagation Delay of 20ns
- Gate Drive Matching of Less than 5ns
- Drives a 2.2nF Load with 15ns of Rise Time and 12ns of Fall Time at 12V VDD
- TTL-Compatible Input
- Quiescent Current of Less than 160 $\mu$ A
- UVLO for both High-Side and Low-Side
- Available in a SOIC-8E Package
- Available in AEC-Q100 Qualified Grade 1

### APPLICATIONS

- Car DC/DC Power Systems
- Half-Bridge Motor Drivers

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### TYPICAL APPLICATION



### ORDERING INFORMATION

Part Number*	Package	Top Marking
MPQ18024HN-AEC1	SOIC-8 EP	See Below

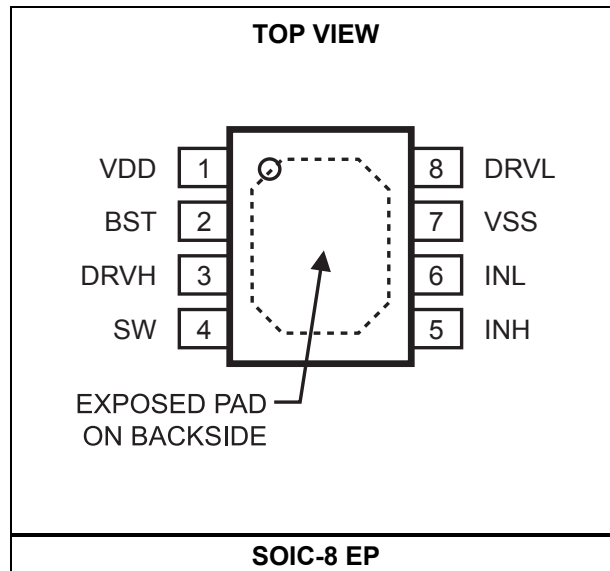
\* For Tape & Reel, add suffix -Z (e.g. MPQ18024HN-AEC1-Z).

### TOP MARKING

**MP18024**  
**LLLLLLLL**  
**MPSYWW**

MP18024: Part number  
 LLLLLLLL: Lot number  
 MPS: MPS prefix  
 Y: Year code  
 WW: Week code

### PACKAGE REFERENCE



## PIN FUNCTIONS

Pin #	Name	Description
1	VDD	<b>Supply input.</b> VDD supplies power to all of the internal circuitries. Place a decoupling capacitor to ground close to VDD to ensure a stable and clean supply.
2	BST	<b>Bootstrap.</b> BST is the positive power supply for the internal floating high-side MOSFET driver. Connect a bypass capacitor between BST and SW.
3	DRVH	<b>Floating driver output.</b>
4	SW	<b>Switching node.</b>
5	INH	<b>Control signal input for the floating driver.</b>
6	INL	<b>Control signal input for the low side driver.</b>
7	VSS	<b>Chip ground.</b> Connect the exposed pad to VSS for proper thermal operation.
Exposed Pad		
8	DRVL	<b>Low-side driver output.</b>

### ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

Supply voltage ( $V_{DD}$ )	-0.3V to 18V
SW voltage ( $V_{SW}$ )	-5.0V to 110V
BST voltage ( $V_{BST}$ )	-0.3V to 110V
BST to SW	-0.3V to 18V
DRVH to SW	-0.3V to (BST - SW) + 0.3V
DRVL to VSS	-0.3V to ( $V_{DD}$ + 0.3V)
All other pins	-0.3V to ( $V_{DD}$ + 0.3V)
CDM rating (AEC-Q100-011C1)	
All pins	Class C6
HBM rating (AEC-Q100-002)	
BST, DRVH	Class H1C
Other pins	Class H2
Continuous power dissipation ( $T_A = 25^\circ\text{C}$ ) <sup>(2)</sup>	2.5W
Junction temperature	150°C
Lead temperature	260°C
Storage temperature	-65°C to 150°C

### Recommended Operating Conditions <sup>(3)</sup>

Supply voltage ( $V_{DD}$ )	9.0V to 16.0V
SW voltage ( $V_{SW}$ )	
	(-10V / <100ns) to 100V - VDD
SW slew rate	<50V/ns
Operating junction temp. ( $T_J$ )	-40°C to 125°C

<b>Thermal Resistance <sup>(4)</sup></b>	$\theta_{JA}$	$\theta_{JC}$
SOIC-8 EP	50	12 ... °C/W

#### NOTES:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature  $T_J(\text{MAX})$ , the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D(\text{MAX}) = (T_J(\text{MAX}) - T_A) / \theta_{JA}$ . Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operating conditions.
- Measured on JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

$V_{DD} = V_{BST} - V_{SW} = 12V$ ,  $V_{SS} = V_{SW} = 0V$ , no load at DRVH and DRVL,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , typical values tested at  $T_J = +25^{\circ}C$ , unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
<b>Supply Currents</b>						
VDD quiescent current	$I_{DDQ}$	INL = INH = 0		120	160	$\mu A$
VDD operating current	$I_{DDO}$	fsw = 500kHz		9		mA
Floating driver quiescent current	$I_{BSTQ}$	INL = INH = 0		70	100	$\mu A$
Floating driver operating current	$I_{BSTO}$	fsw = 500kHz		8.5		mA
Leakage current	$I_{LK}$	BST = SW = 100V		0.05	2.5	$\mu A$
<b>Inputs</b>						
INL/INH high				2.2	2.6	V
INL/INH low			1	1.5		V
INL/INH internal pull-down resistance	$R_{IN}$			185		k $\Omega$
<b>Under-Voltage Protection (UVP)</b>						
VDD rising threshold	$V_{DDR}$		8.1	8.5	8.9	V
VDD hysteresis	$V_{DDH}$			0.5		V
(BST - SW) rising threshold	$V_{BSTR}$		6.8	7.4	8	V
(BST - SW) hysteresis	$V_{BSTH}$			0.55		V
<b>Bootstrap Diode</b>						
Bootstrap diode VF @ 100 $\mu A$	$V_{F1}$			0.5		V
Bootstrap diode VF @ 100mA	$V_{F2}$			0.95		V
Bootstrap diode dynamic R	$R_D$	@ 100mA		2.3		$\Omega$
<b>Low-Side Gate Driver</b>						
Low-level output voltage	$V_{OLL}$	$I_O = 100mA$		0.08		V
High-level output voltage to rail	$V_{OHL}$	$I_O = -100mA$		0.23		V
Peak pull-up current <sup>(5)</sup>	$I_{OHL}$	$V_{DRVL} = 0V, V_{DD} = 12V$		3		A
		$V_{DRVL} = 0V, V_{DD} = 16V$		4.7		A
Peak pull-down current <sup>(5)</sup>	$I_{OLL}$	$V_{DRVL} = V_{DD} = 12V$		4.5		A
		$V_{DRVL} = V_{DD} = 16V$		6		A
<b>Floating Gate Driver</b>						
Low-level output voltage	$V_{OLH}$	$I_O = 100mA$		0.08		V
High-level output voltage to rail	$V_{OHH}$	$I_O = -100mA$		0.23		V
Peak pull-up current <sup>(5)</sup>	$I_{OHH}$	$V_{DRVH} = 0V, V_{DD} = 12V$		2.6		A
		$V_{DRVH} = 0V, V_{DD} = 16V$		4		A
Peak pull-down current <sup>(5)</sup>	$I_{OLH}$	$V_{DRVH} = V_{DD} = 12V$		4.5		A
		$V_{DRVH} = V_{DD} = 16V$		5.9		A
Switching spec – low-side gate driver						
Turn-off propagation delay INL falling to DRVL falling	$T_{DLFF}$			20		ns
Turn-on propagation delay INL rising to DRVL rising	$T_{DLRR}$			20		
DRVL rise time		$C_L = 2.2nF$		15		ns
DRVL fall time		$C_L = 2.2nF$		9		ns

## ELECTRICAL CHARACTERISTICS (continued)

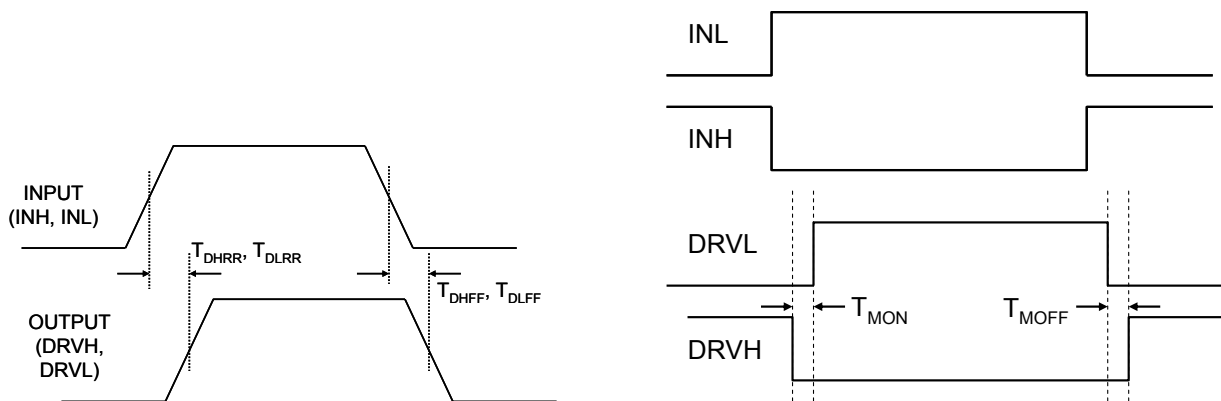
$V_{DD} = V_{BST} - V_{SW} = 12V$ ,  $V_{SS} = V_{SW} = 0V$ , no load at DRVH and DRVL,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$ , typical values tested at  $T_J = +25^{\circ}C$ , unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
<b>Switching Spec – Floating Gate Driver</b>						
Turn-off propagation delay INL falling to DRVH falling	$T_{DHFF}$			20		ns
Turn-on propagation delay INL rising to DRVH rising	$T_{DHRR}$			20		ns
DRVH rise time		$C_L = 2.2nF$		15		ns
DRVH fall time		$C_L = 2.2nF$		12		ns
<b>Switching Spec – Matching</b>						
Floating driver turn-off to low-side driver turn-on <sup>(5)</sup>	$T_{MON}$			1	5	ns
Low-side driver turn-off to floating driver turn-on <sup>(5)</sup>	$T_{MOFF}$			1	5	ns
Minimum input pulse width that changes the output	$T_{PW}$				50 <sup>(5)</sup>	ns
Bootstrap diode turn-on or turn-off time	$T_{BS}$			10 <sup>(5)</sup>		ns
Thermal shutdown <sup>(5)</sup>				170		$^{\circ}C$
Thermal shutdown hysteresis <sup>(5)</sup>				25		$^{\circ}C$

### NOTE:

5) Guaranteed by design.

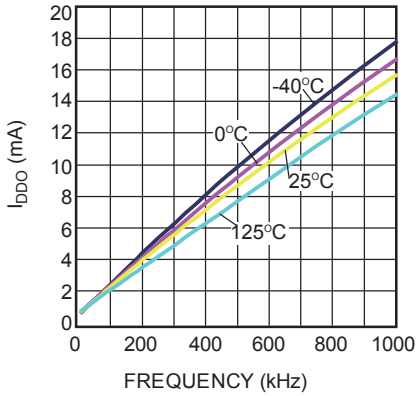
## TIMING DIAGRAM



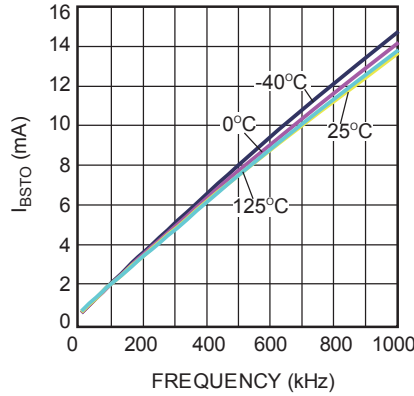
## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{DD} = 12V$ ,  $V_{SS} = V_{SW} = 0V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.

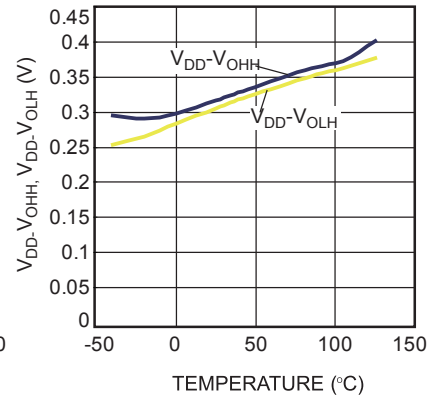
**$I_{DDO}$  Operation Current vs. Frequency**



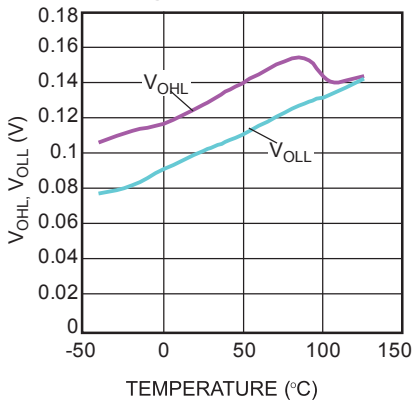
**$I_{BSTO}$  Operation Current vs. Frequency**



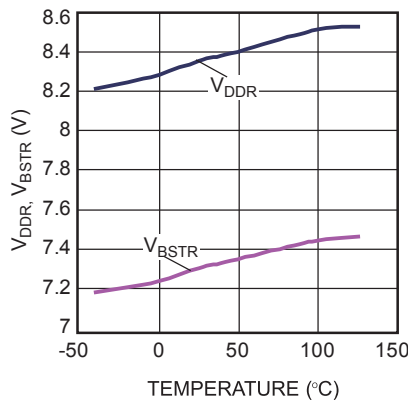
**High-Level Output Voltage vs. Temperature**



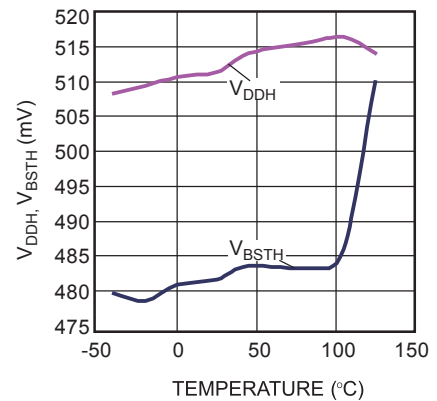
**Low-Level Output Voltage vs. Temperature**



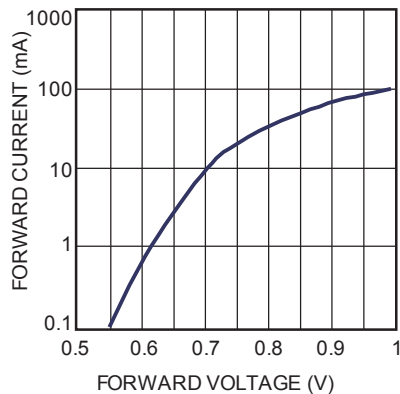
**Under-Voltage Lockout Threshold vs. Temperature**



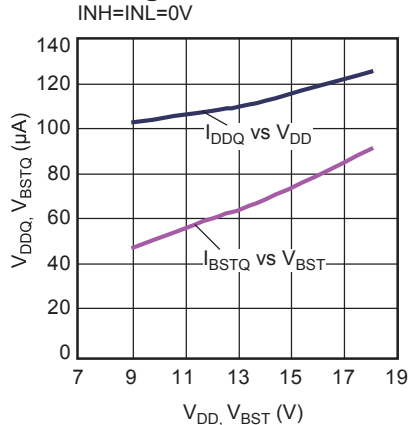
**Under-Voltage Lockout Hysteresis vs. Temperature**



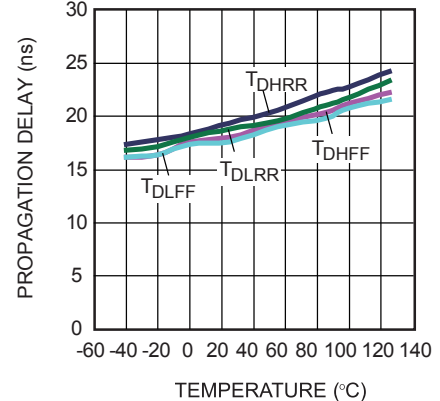
**Bootstrap Diode I-V Characteristic**



**Quiescent Current vs. Voltage**



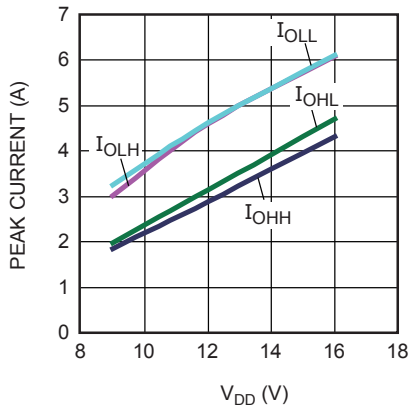
**Propagation Delay vs. Temperature**



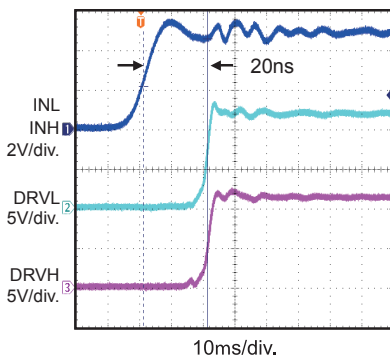
### TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{DD} = 12V$ ,  $V_{SS} = V_{SW} = 0V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.

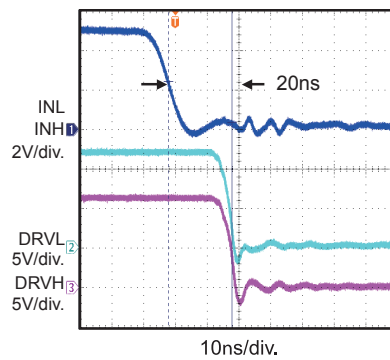
Peak Current vs.  $V_{DD}$  Voltage



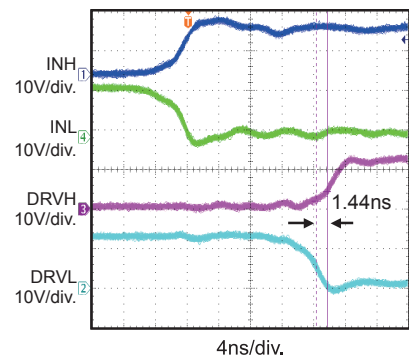
Turn-On Propagation Delay



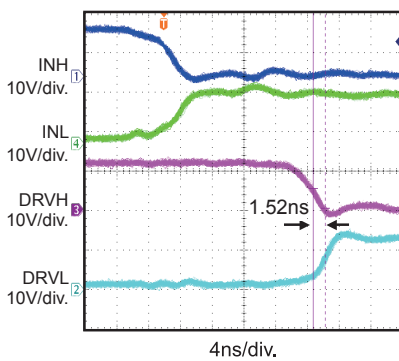
Turn-Off Propagation Delay



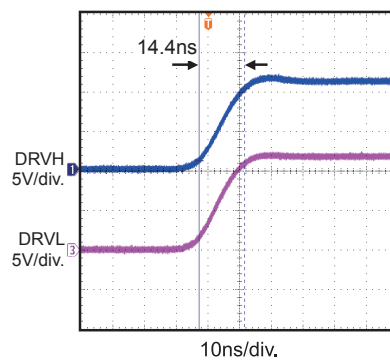
Gate Drive Matching  $T_{MOFF}$



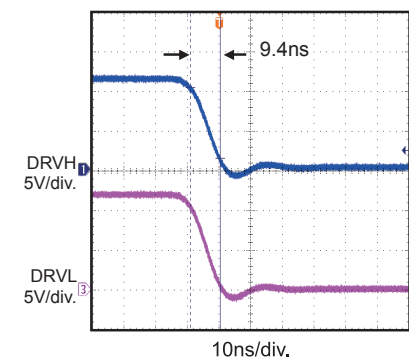
Gate Drive Matching  $T_{MON}$



Drive Rise Time  
2.2nF Load



Drive Fall Time  
2.2nF Load



### BLOCK DIAGRAM

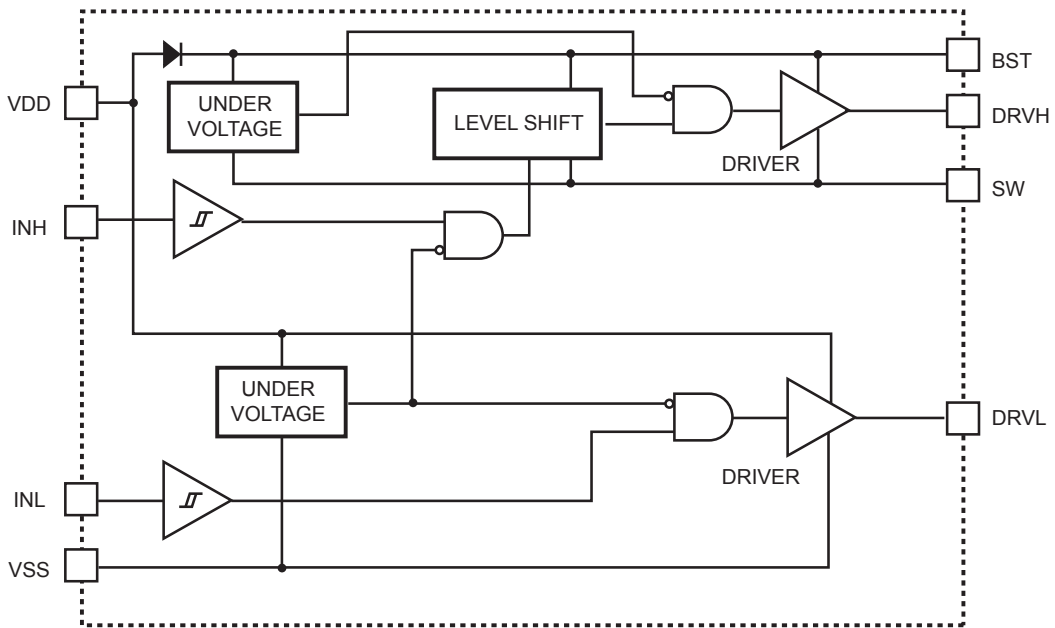
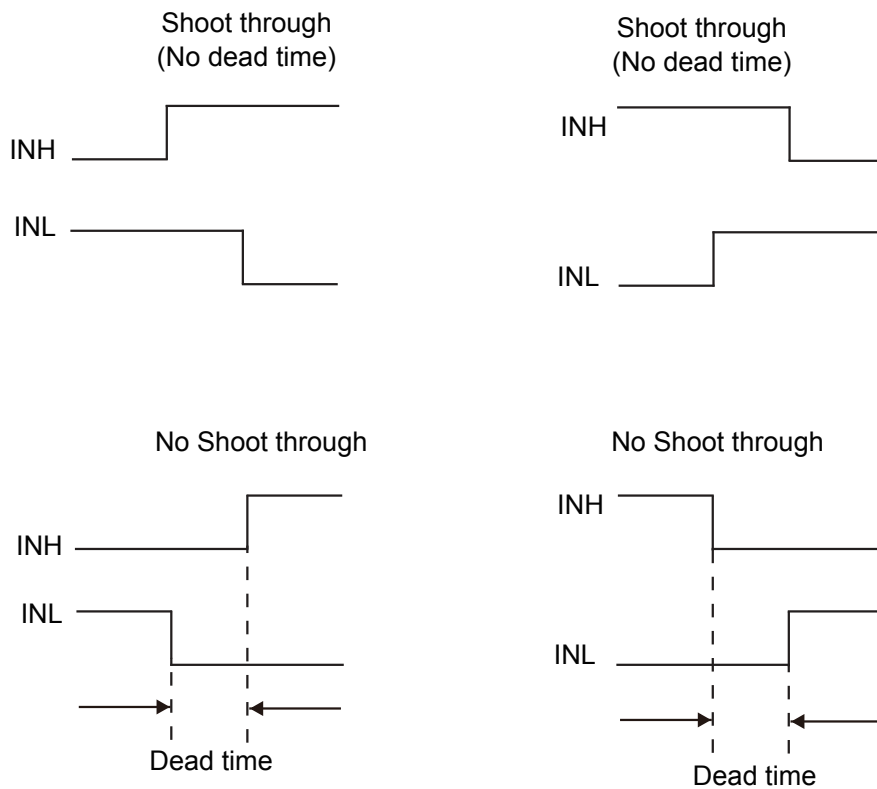


Figure 1: Functional Block Diagram



## APPLICATION

The input signals of INH and INL can be controlled independently. If both INH and INL control the high-side MOSFET (HS-FET) and low-side MOSFET (LS-FET) of the same bridge, shoot through can be prevented by setting a sufficient dead time between INH and INL low, and vice versa (see Figure 2). Dead time is defined as the time interval between INH low and INL low.



**Figure 2: Shoot-Through Timing Diagram**

## REFERENCE DESIGN CIRCUITS

### Half-Bridge Converter

The MPQ18024 drives the MOSFETs with alternating signals (with dead time) in a half-bridge converter topology. Because the pulse-

width modulation (PWM) controller drives INH and INL with alternating signals, the input voltage can rise as high as 100V (see Figure 3 through Figure 5).

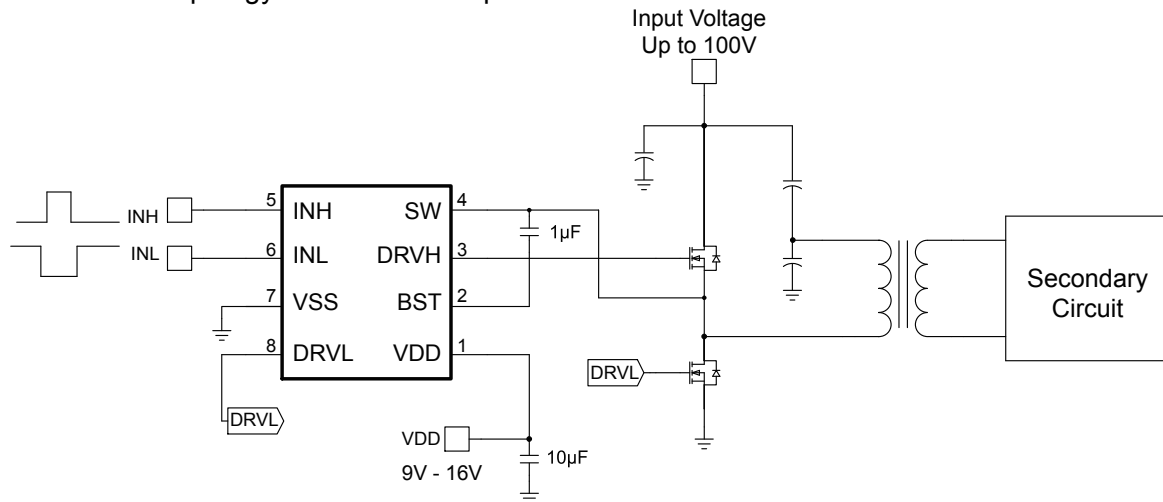


Figure 3: Half-Bridge Converter

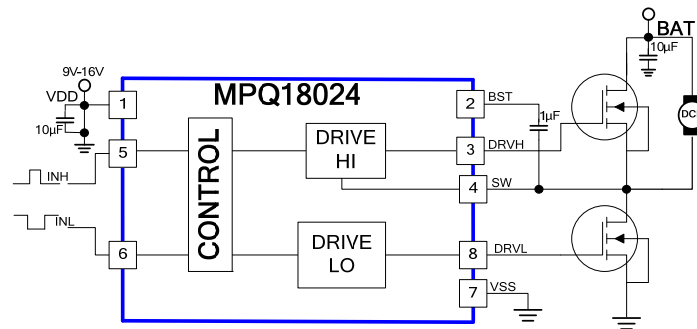


Figure 4: Half-Bridge for Unidirectional Motor

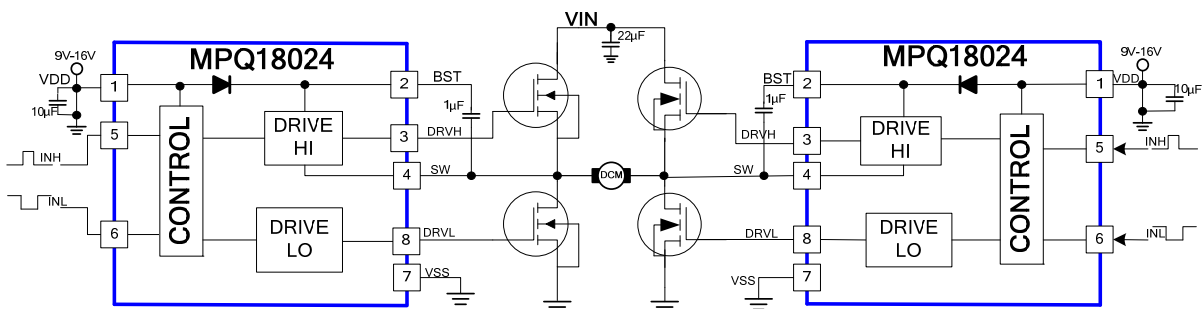
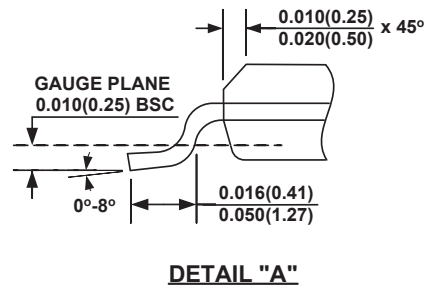
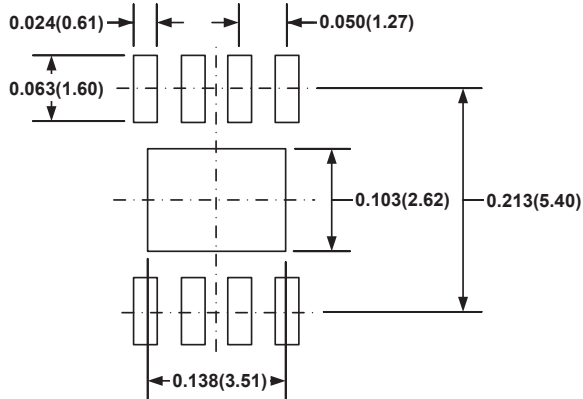
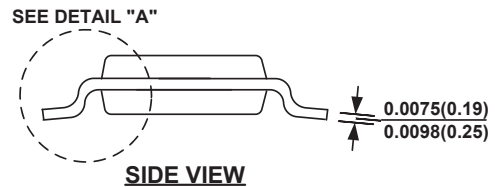
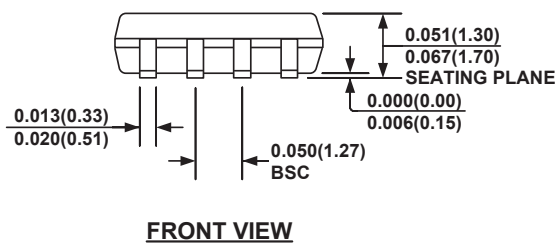
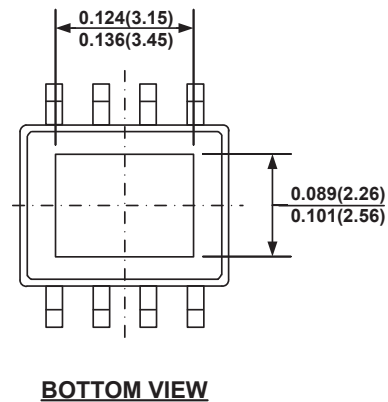
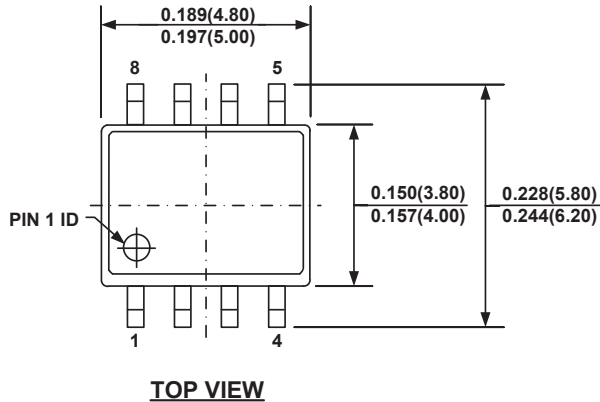


Figure 5: 2x MPQ18024 for One Bidirectional DC Motor

## PACKAGE INFORMATION

### SOIC-8E



#### NOTE:

- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
- 6) DRAWING IS NOT TO SCALE.

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