MPM3824

2.75V to 6V, 2A, Ultra-Small, Ultra-Low Noise Power Module

DESCRIPTION

The MPM3824 is a synchronous, step-down power module with an integrated inductor. It achieves up to 2A of continuous output current (I_{OUT}) across a 2.75V to 6V input voltage (V_{IN}) range, with excellent load and line regulation. The MPM3824 works in advanced asynchronous modulation (AAM) mode at light loads, and it can switch to continuous conduction mode (CCM) at heavy loads with small voltage ripple.

The output voltage (V_{OUT}) can be regulated as low as 0.6V. Only feedback (FB) resistors, input capacitors (C_{IN}), and output capacitors (C_{OUT}) are required to complete the design. The constant-on-time (COT) control scheme provides fast transient response, high efficiency, and eases loop stabilization.

Full protections include cycle-by-cycle current limiting, short-circuit protection (SCP) with hiccup mode, and thermal shutdown.

The MPM3824 requires a minimal number of readily available, standard, external components, and it is available in an ultra-small ECLGA-14 (2.5mmx2.5mmx1.2mm) package.

FEATURES

- Wide 2.75V to 6V Operating Input Voltage (V_{IN}) Range
- Adjustable Output Voltage (V_{OUT}) from 0.6V
- Up to 2A of Continuous Output Current (I_{OUT})
- 100% Duty Cycle in Dropout
- Up to 92% Efficiency across 3.3V to 1.8V Range
- Advanced Asynchronous Modulation (AAM) Mode
- Enable (EN) and Power Good (PG) for Power Sequencing
- Cycle-by-Cycle Over-Current Protection (OCP)
- Short-Circuit Protection (SCP) with Hiccup Mode
- Only Four Required External Components
- Available in an ECLGA-14 (2.5mmx2.5mmx1.2mm) Package

APPLICATIONS

- Low-Voltage I/O System Power
- Low-Dropout (LDO) Replacements
- Power for Portable Products
- Storage Including Solid-State Drives (SSDs) and Hard Disk Drives (HDDs)
- Space-Constrained Applications

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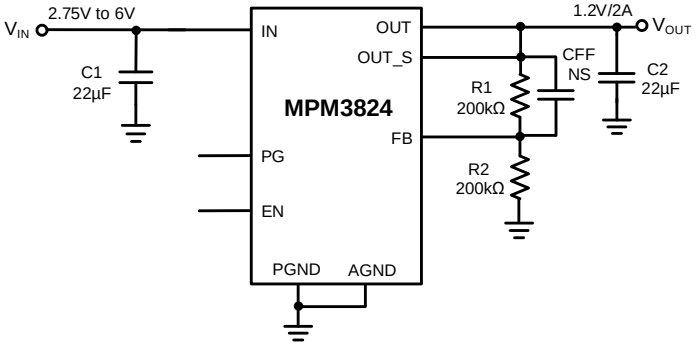
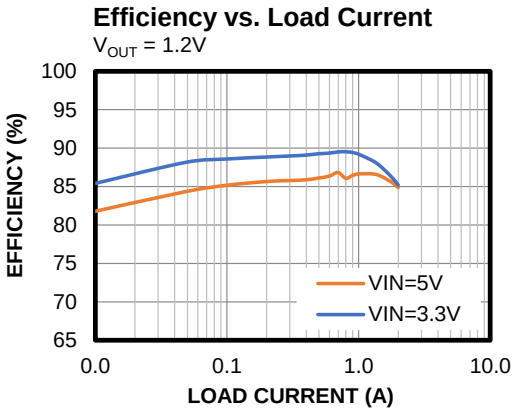
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPM3824GPA	ECLGA-14 (2.5mmx2.5mm)	*See Below*	3

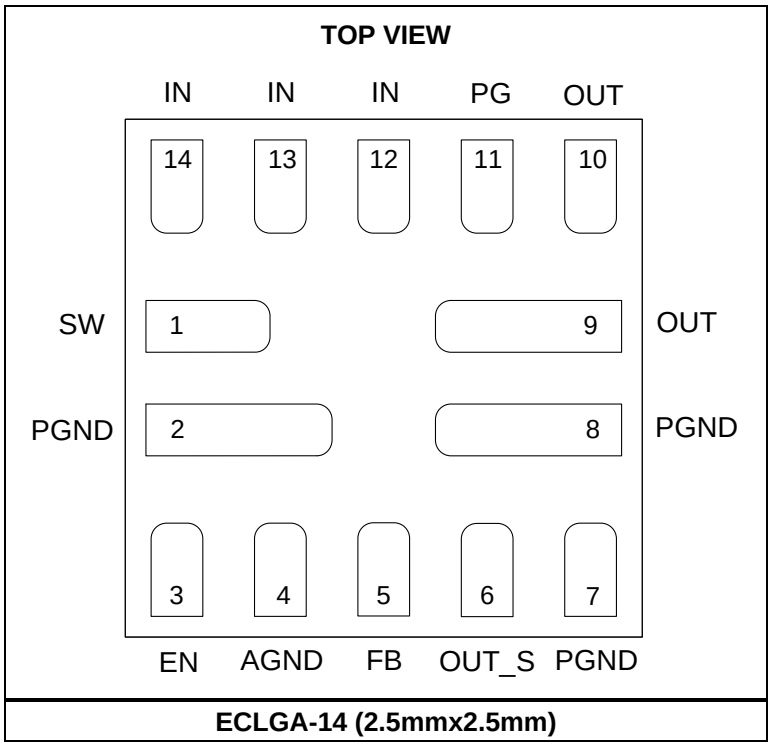
* For Tape & Reel, add suffix -Z (e.g. MPM3824GPA-Z).

TOP MARKING

$\overline{\text{CAH}}$
YWW
LLL

CAH: Product code of MPM3824GPA
Y: Year code
WW: Week code
LLL: Lot number

PACKAGE REFERENCE



ECLGA-14 (2.5mmx2.5mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	SW	**Switching test pin.** Float the SW pin.
2, 7, 8	PGND	**Power ground.**
3	EN	**On/off control.**
4	AGND	**Analog ground for the internal control circuit.** The AGND pin is not internally connected to PGND. Connect AGND to PGND on the PCB layout.
5	FB	**Feedback.** Use an external resistor divider between the output and AGND, connected to the FB pin, to set the output voltage (V_{OUT}).
6	OUT_S	**Output voltage sense.**
9, 10	OUT	**Power output.**
11	PG	**Power good (PG) indicator.** The PG pin is an open-drain output with an internal pull-up resistor connected to IN. Pull PG up to IN when the FB voltage (V_{FB}) is within the regulation level; otherwise, PG remains low.
12, 13, 14	IN	**Power input.**

ABSOLUTE MAXIMUM RATINGS (1)

SW voltage (V_{SW}) .....
-0.3V (-5V for <10ns) to +6.5V (+10V for <10ns)
All other pins .....-0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (5)
ECLGA-14 (2.5mmx2.5mm) 2.2W
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) 2000V
Charged-device model (CDM) 2000V

Recommended Operating Conditions (2)

Operating input voltage (V_{IN}) range .....
……2.75V to 6V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (3) (4) (5) (6) (7)

θ_{JA} .... 56.7°C/W
θ_{JC_TOP} .... 6.85°C/W
θ_{JB} .... 25.5°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The device is not guaranteed to function outside of its operating conditions.
3) θ_{JA} is the junction-to-ambient thermal resistance, θ_{JC_TOP} is the junction-to-case top thermal characterization parameter, and θ_{JB} is the junction-to-board thermal characterization parameter.
4) The thermal parameter is based on the test on the MPS evaluation board (EVM3824-PA-00A) under a no airflow cooling condition in a standard enclosure. The 2-layer board size is 5.1cmx5.1cm, where the top and bottom layer copper thickness is 2oz.
5) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature.
6) The junction-to-case top thermal characterization parameter, θ_{JC_TOP}, estimates the junction temperature in the real system, based on the following equation: $T_J = \theta_{JC_TOP} \times P_{LOSS} + T_{CASE_TOP}$, where P_{LOSS} is the entire loss of the module in real applications, and T_{CASE_TOP} is the case top temperature.
7) The junction-to-board thermal characterization parameter, θ_{JB}, estimates the junction temperature in the real system, based on the following equation: $T_J = \theta_{JB} \times P_{LOSS} + T_{BOARD}$. Where P_{LOSS} is the entire power loss of the module in real applications, and T_{BOARD} is the board temperature.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 3.6V, T_J = -40°C to +125°C [8], typical value is tested at T_J = 25°C, the over-temperature limit is guaranteed by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Feedback (FB) voltage	V_{FB}	2.75V ≤ V_{IN} ≤ 6V	591	600	609	mV
FB current	I_{FB}	V_{FB} = 0.6V		10		nA
Dropout resistance	R_{DR}	100% duty cycle		75		mΩ
Switch leakage		V_{EN} = 0V, V_{IN} = 6V, V_{SW} = 0V and 6V, T_J = 25°C		0	2	μA
P-channel MOSFET peak current limit		T_J = 25°C	4	5.2		A
N-channel MOSFET valley current limit				2.5		A
On time	t_{ON}	V_{IN} = 5V, V_{OUT} = 1.2V		185		ns
		V_{IN} = 3.6V, V_{OUT} = 1.2V		250		
Switching frequency	f_{SW}	V_{OUT} = 1.2V, I_{LOAD} = 1A		1250		kHz
Minimum off time [9]	t_{MIN_OFF}			100		ns
Minimum on time [9]	t_{MIN_ON}			80		ns
Soft-start (SS) time [9]	t_{SS_ON}			1.7		ms
Soft-shutdown time [9]	t_{SS_OFF}			2		ms
Power good (PG) upper trip threshold	PG_OV	V_{FB} in respect to regulation		+7		%
PG lower trip threshold	PG_UV			-12		%
PG delay				100		μs
PG sink current capability	V_{PG_LO}	Sink 1mA			0.4	V
PG logic high voltage	V_{PG_HI}	V_{IN} = 5V, V_{FB} = 0.6V	4			V
PG internal pull-up resistor	R_{PG}			440		kΩ
Under-voltage lockout (UVLO) rising threshold			2.3	2.5	2.85	V
UVLO threshold hysteresis				400		mV
Enable (EN) input logic low voltage					0.3	V
EN input logic high voltage			1.2			V
EN input current		V_{EN} = 2V		2		μA
		V_{EN} = 0V		0		μA
Supply current (shutdown)		V_{EN} = 0V, T_J = 25°C		0	1	μA
Supply current (quiescent)		V_{EN} = 2V, V_{FB} = 0.63V, V_{IN} = 3.6V		65		μA

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, T_J = -40°C to +125°C (8), typical value is tested at T_J = 25°C, the over-temperature limit is guaranteed by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Converter System (9)						
Output voltage range (9)			0.6		6	V
Recommended input capacitance (9)	C_{IN1}	V_{IN} = 3.6V, V_{OUT} = 1.2V, I_{OUT} = 2A	4.7	22		µF
Output capacitance (9)	C_{OUT}	V_{IN} = 3.6V, V_{OUT} = 1.2V, I_{OUT} = 2A	10	22		µF
Output ripple (9)		V_{IN} = 3.6V, V_{OUT} = 1.2V, C_{OUT} = 22µF, I_{OUT} = 2A		8		mV
Efficiency (9)		V_{IN} = 3.6V, V_{OUT} = 1.2V, I_{OUT} = 2A		85		%
Load transient response peak-to-peak voltage (9)	V_{P2P1}	V_{IN} = 3.6V, V_{OUT} = 1.2V, C_{OUT} = 22µF, I_{OUT} = 0A to 2A at 1A/µs			147	mV
Thermal shutdown (9)				150		°C
Thermal hysteresis (9)				30		°C

Notes:

8) Not tested in production. Guaranteed by over-temperature correlation.
9) Guaranteed by engineering sample characterization.

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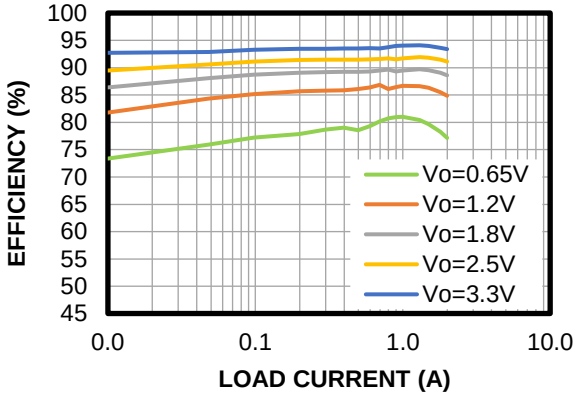
TYPICAL PERFORMANCE CHARACTERISTICS

Performance curves are tested on the evaluation board. V_{IN} = 5V, V_{OUT} = 1.2V, C_{IN} = 22µF, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

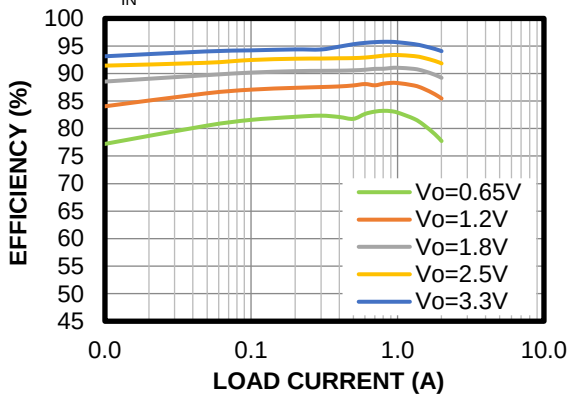
Efficiency vs. Load Current

V_{IN} = 5V



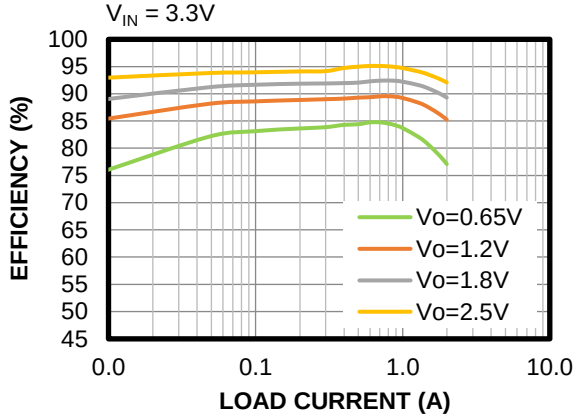
Efficiency vs. Load Current

V_{IN} = 4.2V



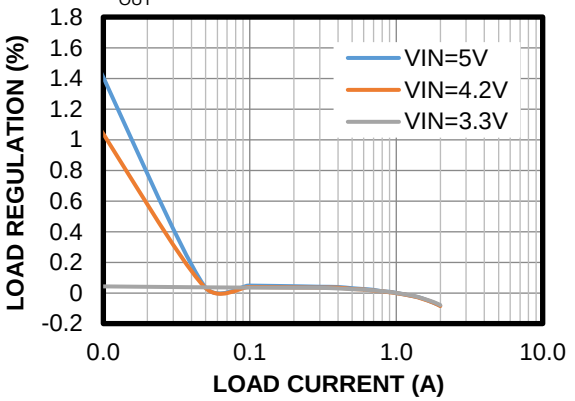
Efficiency vs. Load Current

V_{IN} = 3.3V



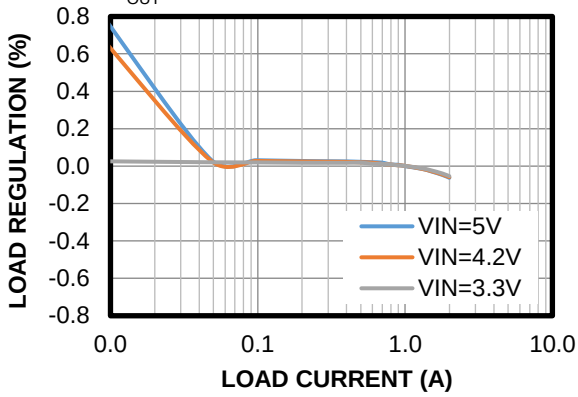
Load Regulation

V_{OUT} = 0.65V



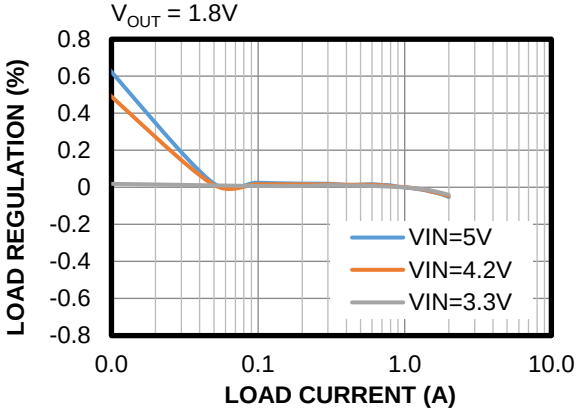
Load Regulation

V_{OUT} = 1.2V



Load Regulation

V_{OUT} = 1.8V



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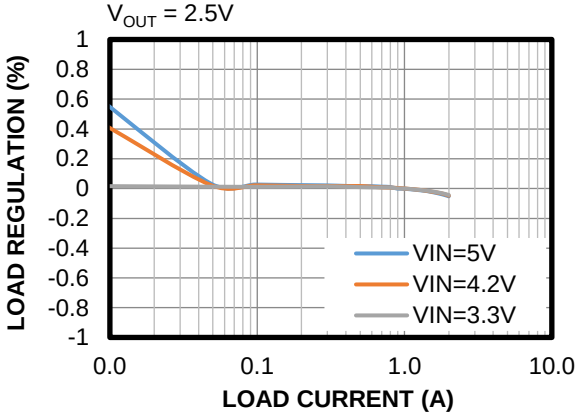
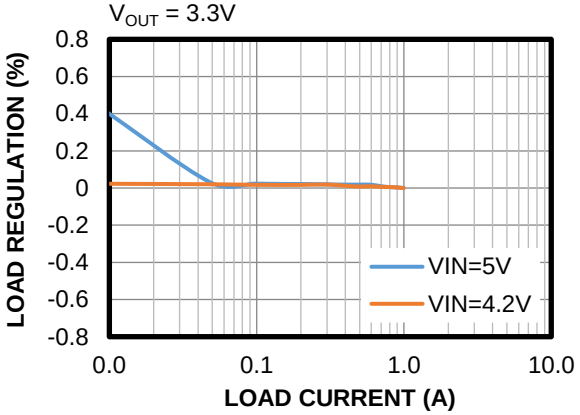
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance curves are tested on the evaluation board. V_{IN} = 5V, V_{OUT} = 1.2V, C_{IN} = 22µF, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

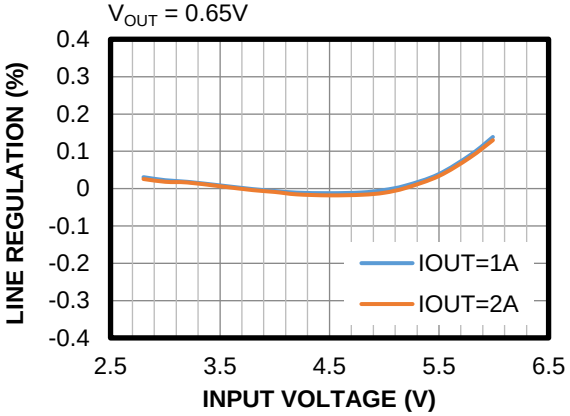
Load Regulation
V_{OUT} = 2.5V



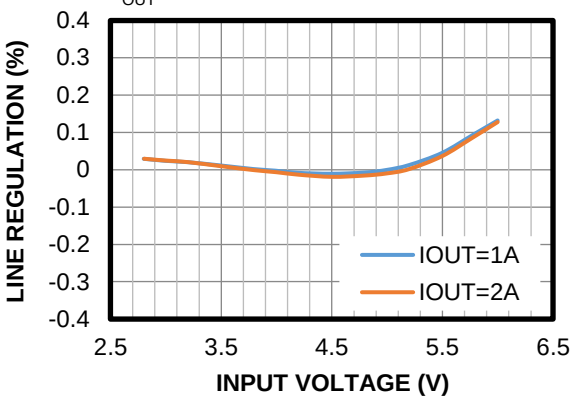
Load Regulation
V_{OUT} = 3.3V



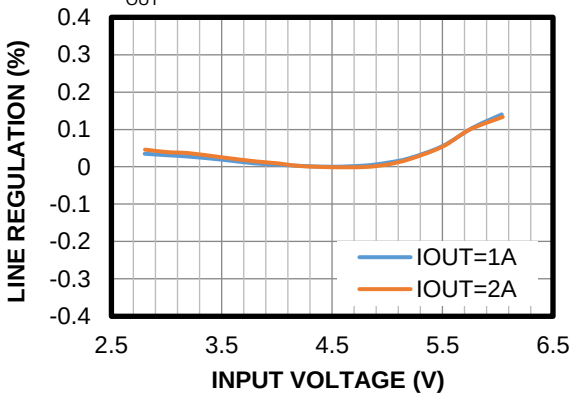
Line Regulation
V_{OUT} = 0.65V



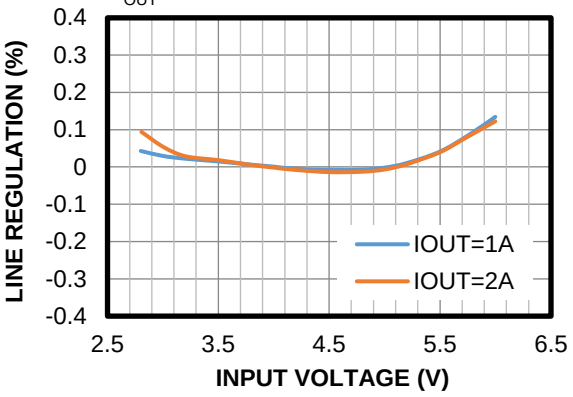
Line Regulation
V_{OUT} = 1.2V



Line Regulation
V_{OUT} = 1.8V



Line Regulation
V_{OUT} = 2.5V



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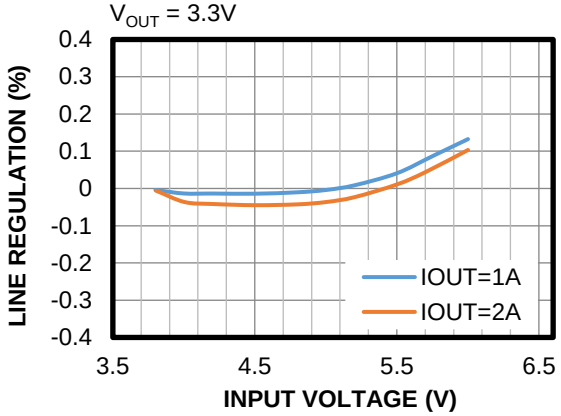
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance curves are tested on the evaluation board. V_{IN} = 5V, V_{OUT} = 1.2V, C_{IN} = 22µF, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

Line Regulation

V_{OUT} = 3.3V



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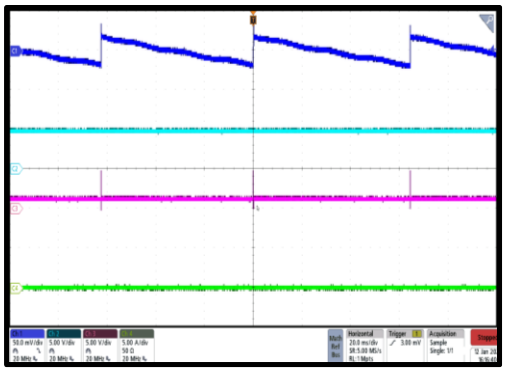
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. V_{IN} = 5V, V_{OUT} = 1.2V, C_{IN} = 22µF, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

Steady State

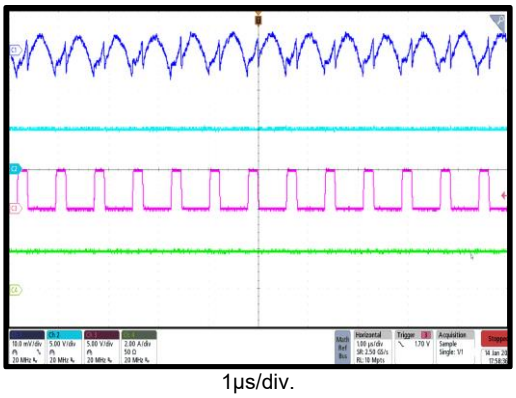
V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 0A



20ms/div.

Steady State

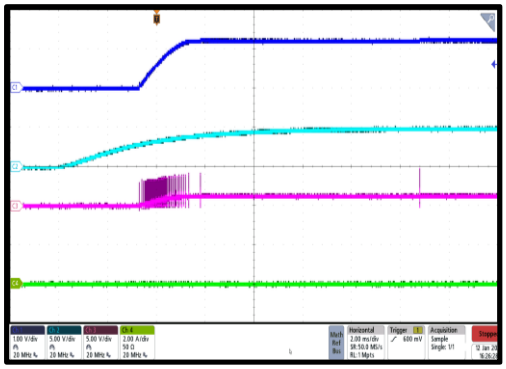
V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 2A



1µs/div.

Start-Up through VIN

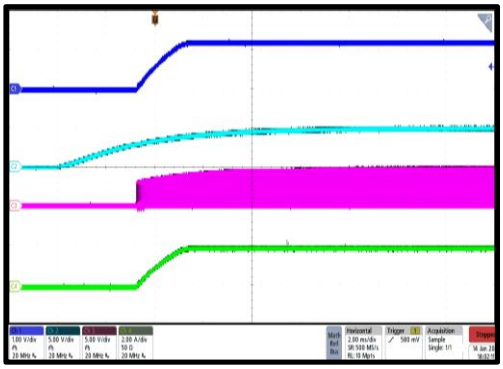
V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 0A



2ms/div.

Start-Up through VIN

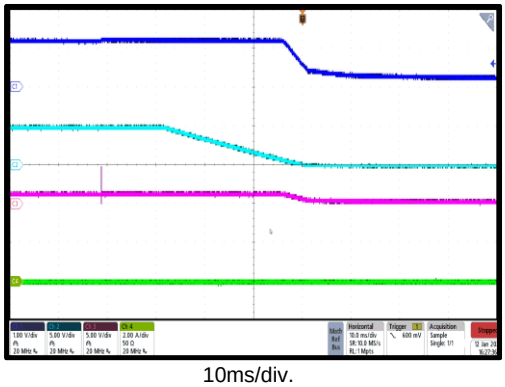
V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 2A



2ms/div.

Shutdown through VIN

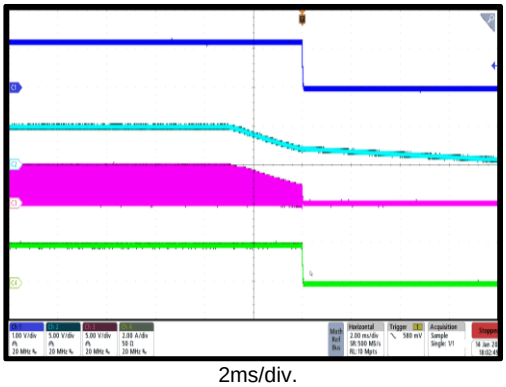
V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 0A



10ms/div.

Shutdown through VIN

V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 2A



2ms/div.

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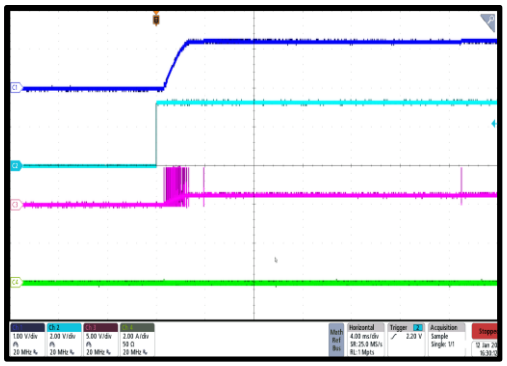
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. V_{IN} = 5V, V_{OUT} = 1.2V, C_{IN} = 22µF, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

Start-Up through EN

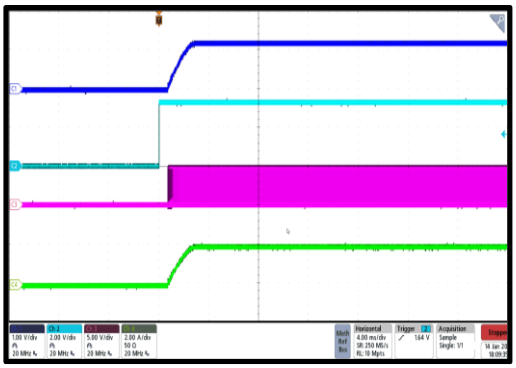
V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 0A



4ms/div.

Start-Up through EN

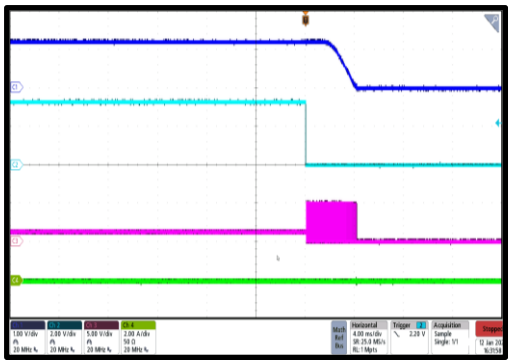
V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 2A



4ms/div.

Shutdown through EN

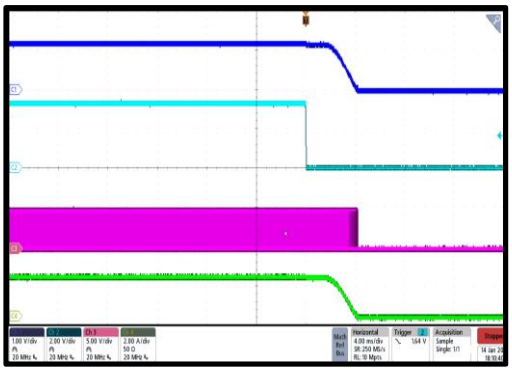
V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 0A



4ms/div.

Shutdown through EN

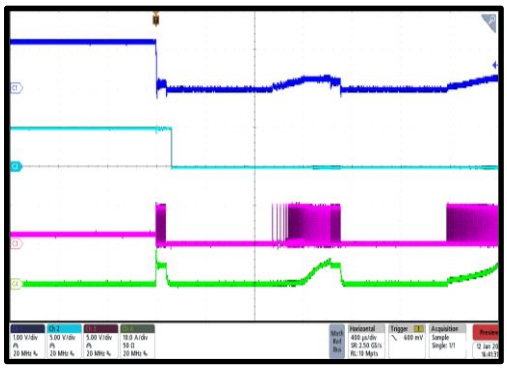
V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 2A



4ms/div.

SCP Entry

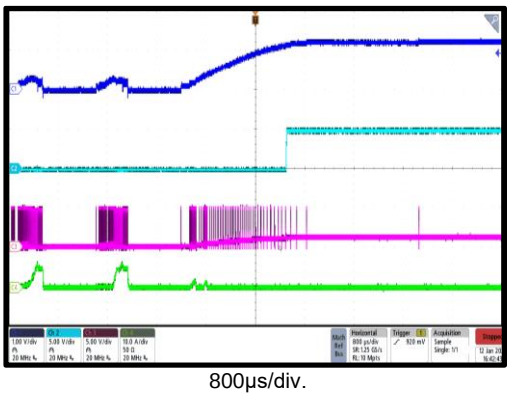
V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 0A



400µs/div.

SCP Recovery

V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 0A



800µs/div.

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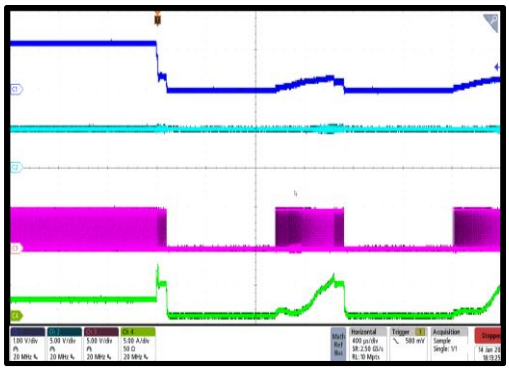
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. V_{IN} = 5V, V_{OUT} = 1.2V, C_{IN} = 22µF, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

SCP Entry

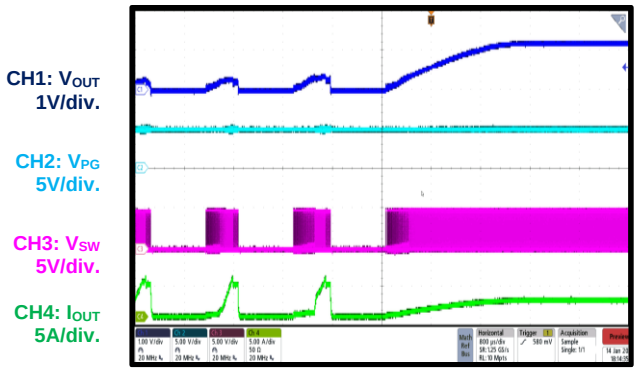
V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 2A



400µs/div.

SCP Recovery

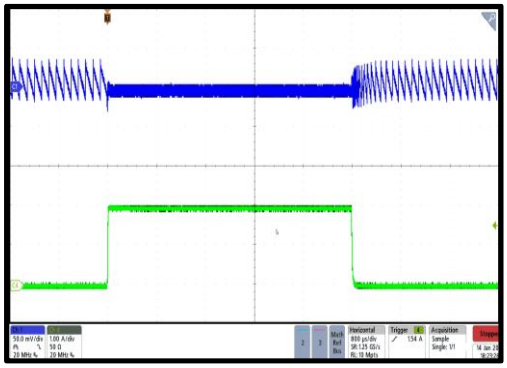
V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 2A



800µs/div.

Load Transient

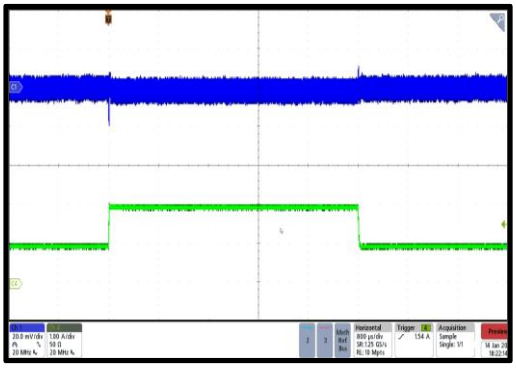
V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 0A to 2A, 2.5A/µs e-load



800µs/div.

Load Transient

V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 1A to 2A, 2.5A/µs e-load



800µs/div.

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FUNCTIONAL BLOCK DIAGRAM

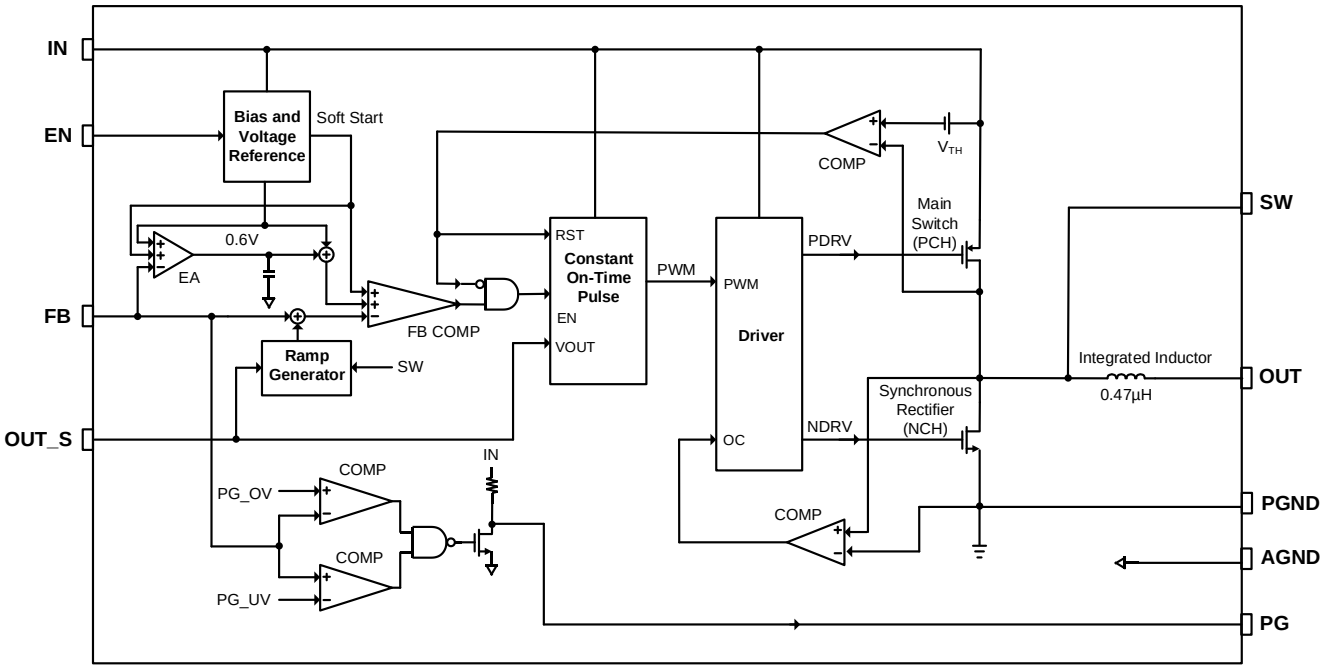

Figure 1: Functional Block Diagram

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OPERATION

The MPM3824 is available in a small surface-mounted ECLGA-14 (2.5mmx2.5mmx1.2mm) package. The MPM3824's integrated inductor simplifies the schematic and layout design. Only feedback (FB) resistors, input capacitors (C_{IN}), and output capacitors (C_{OUT}) are required to complete the design. The MPM3824 uses constant-on-time (COT) control with input voltage (V_{IN}) feed-forward to stabilize the switching frequency (f_{SW}) across the full input range.

Constant-On-Time (COT) Control

Compared to fixed-frequency, pulse-width modulation (PWM) control, constant-on-time (COT) control offers the advantage of a simplified control loop and faster transient response. By using V_{IN} feed-forward, the MPM3824 maintains a nearly constant f_{SW} across the V_{IN} and output voltage (V_{OUT}) ranges. The on time (t_{ON}) of the switching pulse can be estimated with Equation (1):

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times f_{SW} \quad (1)$$

To prevent inductor current (I_L) runaway during the load transition, the MPM3824 fixes the minimum off time (t_{OFF_MIN}) to 230ns, which does not affect operation during steady state.

Advanced Asynchronous Modulation (AAM) Mode

The MPM3824 provides advanced asynchronous modulation (AAM) mode and power-save mode with a zero-current detection (ZCD) circuit for light-load conditions.

The AAM mode current (I_{AAM}) is internally fixed. If the high-side MOSFET (HS-FET) on time is less than the AAM mode blanking time (typically 600ns), then AAM mode is disabled, and the HS-FET on time is determined by the loop. Otherwise, the HS-FET turns on until I_L reaches the value set by I_{AAM}. Figure 2 shows simplified AAM mode control.

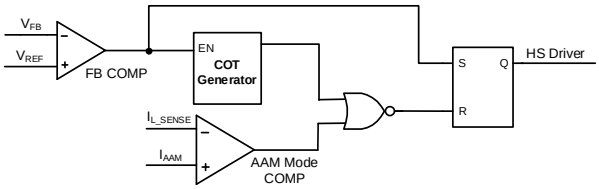

Figure 2: Simplified AAM Mode Control Logic

The MPM3824 has a ZCD circuit to monitor whether I_L begins to reverse. When I_L reaches the ZCD threshold, the low-side MOSFET (LS-FET) turns off.

The combination of AAM mode and the ZCD circuit allows the MPM3824 to always operate in discontinuous conduction mode (DCM) at light loads, even if $V_{OUT} \approx V_{IN}$.

Enable (EN)

If V_{IN} exceeds its under-voltage lockout (UVLO) threshold (typically 2.5V), the MPM3824 can be enabled by pulling the EN pin above the EN input logic high voltage (see the Electrical Characteristics section on page 5). Float EN or pull down EN to ground to disable the MPM3824. There is an internal 1MΩ resistor connected between EN and ground.

Soft Start (SS) and Soft Shutdown

The MPM3824 provides built-in soft start (SS) that ramps up V_{OUT} at a controlled slew rate to prevent overshoot during start-up. t_{SS_ON} is the soft-start time.

When disabled, the MPM3824 ramps down the internal reference voltage (V_{REF}), which allows the load to linearly discharge the output. t_{SS_OFF} is the soft-shutdown time.

Power Good (PG) Indicator

The MPM3824 provides an open-drain power good (PG) pin with a 440kΩ pull-up resistor for PG indication. If FB is within the PG upper trip threshold (PG_OV) and the PG lower trip threshold (PG_UV), then PG is pulled up to IN via the internal resistor. If the FB voltage (V_{FB}) is outside of this threshold window, then PG is pulled down to ground via an internal MOSFET. The MOSFET has a maximum on resistance ($R_{DS(ON)}$) below 100Ω.

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Current Limit

The MPM3824's HS-FET has a typical peak current limit, and its LS-FET has a valley current limit. When the HS-FET reaches its current limit, the HS-FET turns off, and the LS-FET turns on. Once the current drops to the valley current-limit threshold, the MPM3824 turns on the HS-FET again. The HS-FET turns off as soon as it reaches the peak current limit, and the LS-FET turns off after it reaches the valley current limit. If the peak current or valley current are triggered for some cycles, then the MPM3824 disables the regulator. This prevents I_L from continuously rising and damaging components.

Short-Circuit Protection (SCP) and Recovery

If the output is shorted to GND, the current limit is triggered. If the current limit lasts for some cycles, then the MPM3824 enters hiccup mode and disables the output power stage. The MPM3824 discharges the SS capacitor (C_{SS}), then automatically attempts to soft start again. If the short-circuit condition remains after SS ends, the MPM3824 repeats this operation until the short circuit is removed and the output rises back to the regulation level.

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APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets V_{OUT}. Consider the tradeoff between stability and dynamics to choose a FB resistor (R1) that is not too large or small. There is no strict requirement for R1. The lower resistor divider (R2) can be calculated with Equation (2):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.6} - 1} \quad (2)$$

Figure 3 shows the feedback circuit.

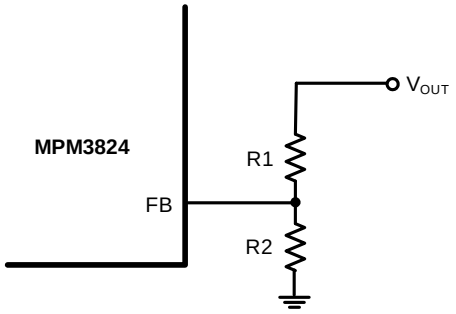

Figure 3: Feedback Network

Table 1 shows the recommended resistances for common output voltages.

Table 1: Resistances for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1	200 (1%)	300 (1%)
1.2	200 (1%)	200 (1%)
1.8	200 (1%)	100 (1%)
2.5	200 (1%)	63.2 (1%)
3.3	200 (1%)	44.2 (1%)

Selecting the Input Capacitor

The step-down converter has a discontinuous input current (I_{IN}) and requires a capacitor to supply AC current while maintaining the DC input voltage (V_{IN}). For optimal performance, it is recommended to use low-ESR capacitors.

Ceramic capacitors with X5R or X7R dielectrics are highly recommended due to their low-ESR and small temperature coefficients. For most applications, a 22µF capacitor is sufficient. Since C_{IN} absorbs the input switching current, it requires an adequate ripple current rating. The C_{IN} RMS current can be estimated with Equation (3):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (3)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, where I_{C1} can be calculated with Equation (4):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (4)$$

For simplification, choose C_{IN} with an RMS current rating greater than half of the maximum load current.

C_{IN} can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge, which prevents excessive voltage ripple at the input. The input voltage ripple (ΔV_{IN}) caused by the capacitance can be calculated with Equation (5):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (5)$$

Selecting the Output Capacitor

An output capacitor (C2, also called C_{OUT}) is required to maintain the DC V_{OUT}. Use low-ESR ceramic capacitors to keep the output voltage ripple low. Generally, a 22µF ceramic C_{OUT} is sufficient for most applications. If V_{OUT} is higher, a 47µF capacitor may be required to stabilize the system.

When using ceramic capacitors, the capacitance dominates the impedance at f_{SW} and causes the majority of the output voltage ripple (ΔV_{OUT}). For simplification, ΔV_{OUT} can be estimated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

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When using tantalum or electrolytic capacitors, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be calculated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (7)$$

Where L1 is the 0.47μH integrated inductor.

The C_{OUT} characteristics affect the stability of the regulation system.

PCB Layout Guidelines

Efficient layout of the switching power supplies is critical for stable operation, especially for the high f_{SW} converter. A poorly optimized layout can result in suboptimal line or load regulation, or stability issues. For the best results, refer to Figure 4 and follow the guidelines below:

1. Place a 0805-sized ceramic C_{IN} as close to the IC pins as possible.
2. Directly connect the two ends of the ceramic capacitor to IN and PGND, respectively.
3. Place the external FB resistor next to the FB pin.
4. Connect AGND and PGND at a single point.

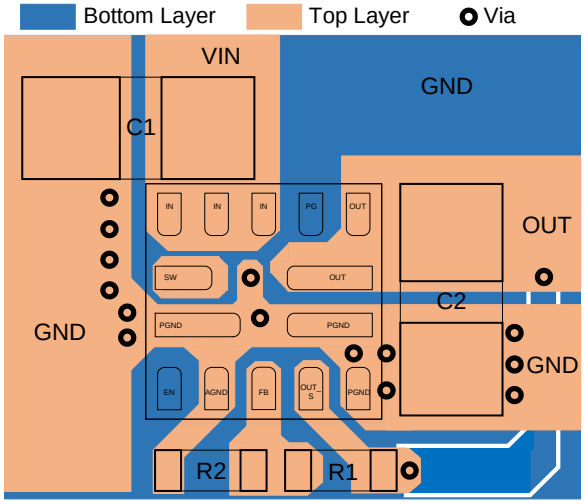

Figure 4: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUIT

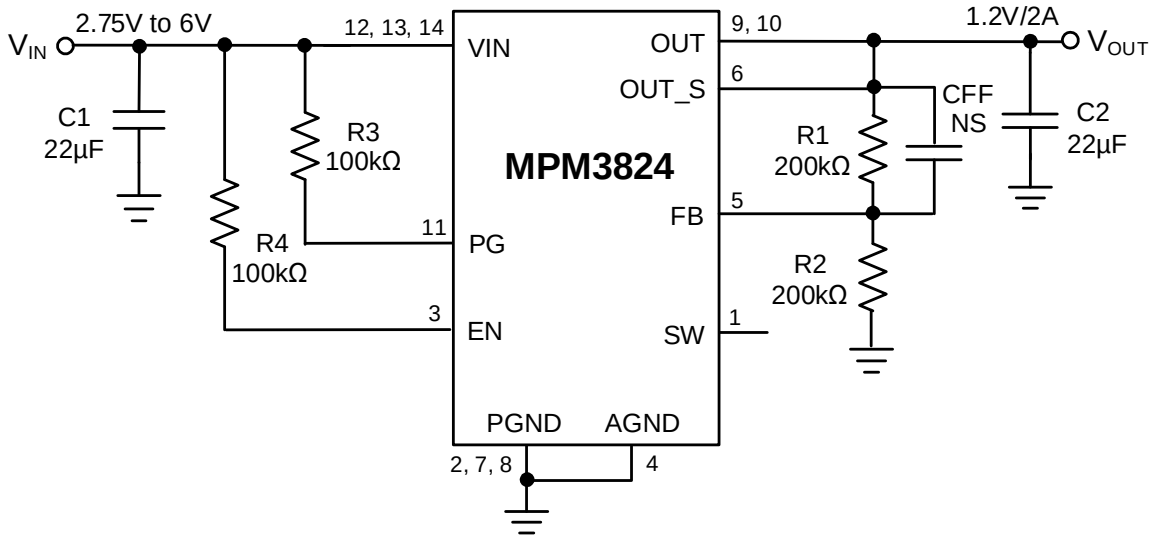

Figure 5: Typical Application Circuit (10)

Note:

10) Additional input capacitors may be required for applications where V_{IN} < 3.3V.

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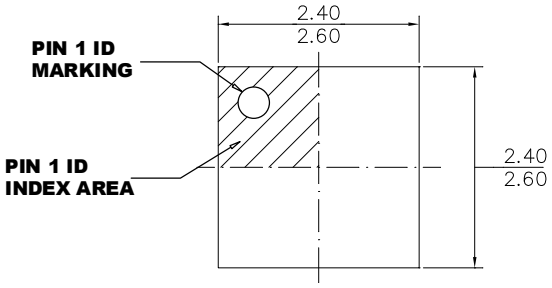
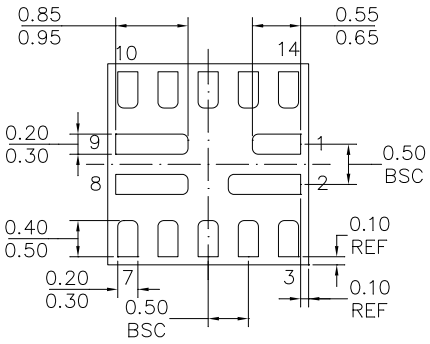
PACKAGE INFORMATION

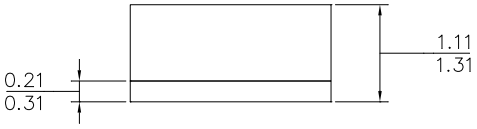
ECLGA-14 (2.5mmx2.5mm)



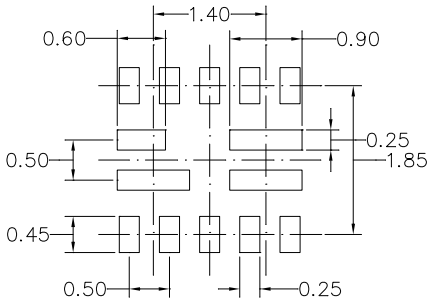
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-303.
4) DRAWING IS NOT TO SCALE.

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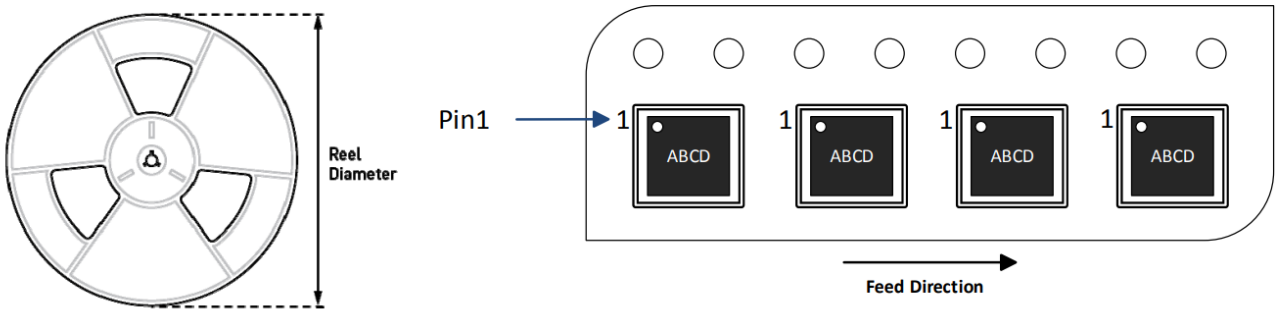
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tray	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPM3824GPA-Z	ECLGA-14 (2.5mmx2.5mm)	2500	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	12/19/2023	Initial Release	-

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