MP8606

6A, 6.5V, Fast-Transient, Synchronous Step-Down Converter

The Future of Analog IC Technology

DESCRIPTION

The MP8606 is a fully-integrated, high-frequency, synchronous, rectified step-down switch-mode converter. It offers a very compact solution to achieve 6A of continuous output current from a 2.9V-to-6.5V input with excellent load and line regulation.

The advanced PWM scheme provides fast transient response and eases loop stabilization.

The MP8606 integrates a 14mΩ high-side switch and an 8mΩ low-side synchronous switch for high efficiency without an external Schottky diode. Fault protections include peak current limiting, hiccup over-current protection, and thermal shutdown. It also has a power-good output.

The MP8606 requires a minimal number of readily available standard external components and is available in a 3mmx4mm flip-chip QFN package.

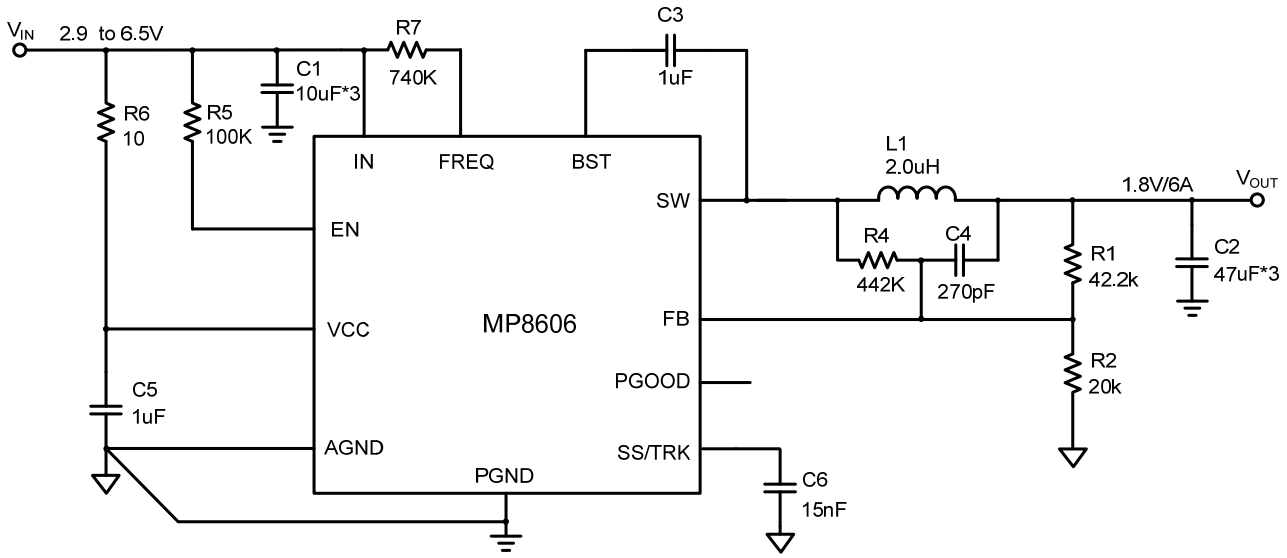
FEATURES

- 6A Continuous Output Current
- 14mΩ Internal High-Side Power Switches
- 8mΩ Internal Low-Side Power Switches
- Input Operation Range: 2.9V to 6.5V
- Adjustable Output Down to 0.6V
- Programmable Switching Frequency
- Hiccup Over-Current Protection
- Programmable Soft-Start Time
- Thermal Shutdown
- Power-Good Output
- 3mmx4mm Flip-Chip Package

APPLICATIONS

- µP/ASIC/DSP/FPGA Core and I/O Supplies
- Portable Equipment / Notebook Computers
- Network and Telecom Equipment
- Point of Load Regulators

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking
MP8606DL	QFN-18 (3mmx4mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP8606DL–Z).
For RoHS compliant packaging, add suffix –LF (e.g. MP MP8606DL–LF–Z)

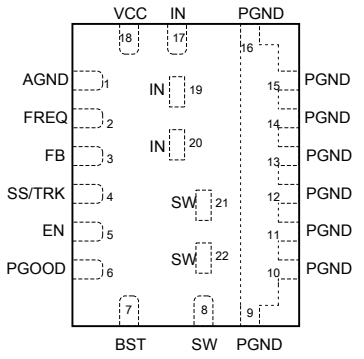
TOP MARKING

MPYW
8606
LLL

8606: product code of MP8606DL;
MP: MPS prefix;
Y: year code;
W: week code:
LLL: lot number;

PACKAGE REFERENCE

TOP VIEW



ABSOLUTE MAXIMUM RATINGS (1)

IN to GND .....-0.3V to +7V
SW to GND .....-0.3V to V_{IN} + 0.3V
SW to GND ..... -2.5V to (V_{IN} + 2.5V) for <50ns
FB, EN, VCC, POK to GND .....-0.3V to +7V
SS/TRK to GND.....-0.3V to +7V
BS to SW .....-0.3V to +7V
Continuous Power Dissipation (T_A = 25°C) (2) 2.6W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} .....2.9V to 6.5V
Output Voltage V_{OUT}..... 0.6V to (0.9 x V_{IN})
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-18 (3mmx4mm).....	48	10... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS (4)

V_{CC}=V_{IN} = V_{EN} = 3.6V, T_A = 25°C, unless otherwise noted.

Parameters	Condition	Min	Typ	Max	Units
Non-Switching Supply Current	V_{EN} = V_{IN} = V_{CC} V_{FB} = 0.65V		820	945	μA
No load Supply Current	V_{EN} = V_{IN} = V_{CC} V_{FB} = 0.6V, Io=0A		2		mA
Shutdown Current	V_{EN} = 0V, V_{IN} = V_{CC} = 6.5V	-1		1	μA
High-Side Switch On-Resistance(5)	I_{SW} = 300mA		14		mΩ
Low-Side Switch On-Resistance(5)	I_{SW} = -300mA		8		mΩ
SW Leakage Current	V_{EN} = 0V; V_{IN} = 6.5V V_{SW} = 0V or 6.5V	-1		1	μA
Current Limit	V_{CC} = V_{IN} = 5V	8	10	13.5	A
One-shot On Time	R_{FREQ} = 200kΩ, V_{OUT}=1.2V, V_{IN}=5V		170		ns
Minimum Off Time(5)			50		ns
Fold-back Off Time(5)			2.5		μs
OCP Hold-off Time(5)			20		μs
Feedback Voltage	2.9V ≤ V_{IN} ≤ 6.0V	594	600	606	mV
	6.0V < V_{IN} ≤ 6.5V	591	600	609	mV
Feedback Current	V_{FB} = 0.6V		20	50	nA
Soft Start Charging current			8	10	μA
Soft Stop Discharging current			8	10	μA
EN Input Low Voltage				0.4	V
EN Input High Voltage		1.6			V
EN Input Current	V_{EN} =2V		2	5	μA
	V_{EN} =0V	-1		1	μA
POK Upper Trip Threshold	FB with respect to the nominal value		-10		%
POK Lower Trip Threshold	FB with respect to the nominal value		-30		%
POK Deglitch Timer			0.4	0.6	ms
POK Output Lower Voltage	I_{sink}=5mA			0.4	V
POK Leakage Current	V_{POK}=3.3V	-10		10	nA
Standby Mode Delay Time(5)			10		μs
BS Refresh Period(4)	In Standby Mode		20		μs
BS Refresh On Time(5)	In Standby Mode		100		ns
V_{CC} Under Voltage Lockout Threshold	Rising Edge	2.4	2.7	2.9	V
V_{CC} Under Voltage Lockout Hysteresis			300	410	mV
Thermal Shutdown	Rising Edge, Hysteresis=20°C		160		°C

Note:

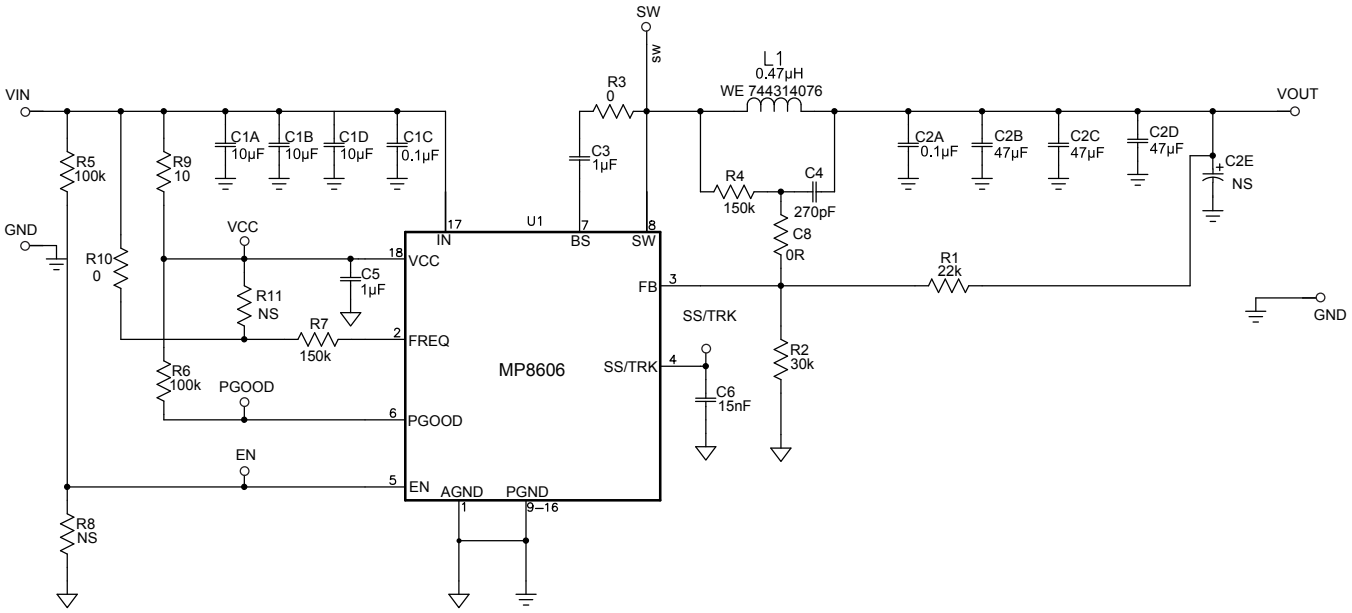
5) Guaranteed by design.

PIN FUNCTIONS

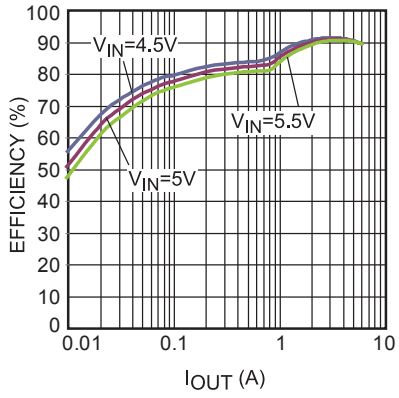
Pin #	Name	Description
1	AGND	Analog ground.
2	Freq	Frequency. Set during CCM operation. Connect a resistor to IN for line feed-forward.
3	FB	Feedback. Sets the output voltage from the tap of an external resistor divider from the output to GND.
4	SS/TRK	Soft-Start. Connect on external capacitor to program the soft start time for the switch mode regulator.
5	EN	En=1 to enable the MP8606. For automatic start-up, connect EN pin to VIN with 100kΩ resistor.
6	PGOOD	Power-Good Open-Drain Output. HIGH output indicates that the output is within +/-10% of the regulation value. LOW output indicates that the output is out of +/-10% window. There is a 0.5 ms delay from FB ≥ 90% to PGOOD goes high.
7	BST	Bootstrap. Connect a capacitor between this pin and SW to provide a floating supply for the high-side gate driver.
8, 21, 22	SW	Switch Node. Connect to the inductor. Connects to the internal high-side and low-side power MOSFET switches. All SW pins must be connected together externally.
9-16	PGND	Power Ground. Connect these pins to the negative terminals of the input and output capacitors using large copper areas. Connect to AGND through a single point.
17, 19, 20	IN	Input Supply. Powers the high-side switch. Requires a decoupling capacitor to ground close to this pin to reduce switching spikes. Connect all IN pins together externally.
18	VCC	Bias Supply. Power both the internal control circuitry and gate drivers. Requires a decoupling capacitor to ground close to this pin.

TYPICAL PERFORMANCE CHARACTERISTICS

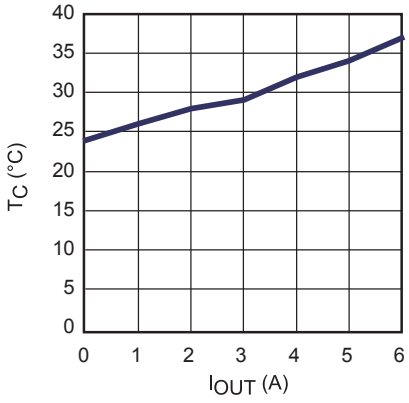
V_{IN}=5V, V_{OUT} =1V, F_S=1MHz, T_A=+25°C, unless otherwise noted.



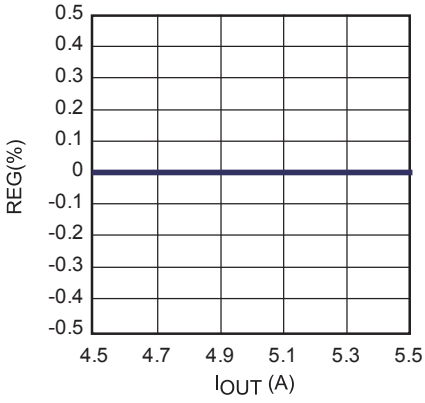
Efficiency



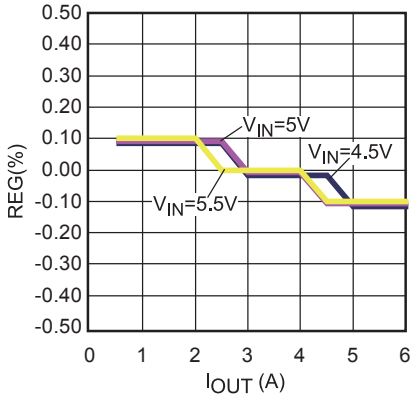
Case Temperature vs. Load Current



Line Regulation @ I_{OUT}=6A

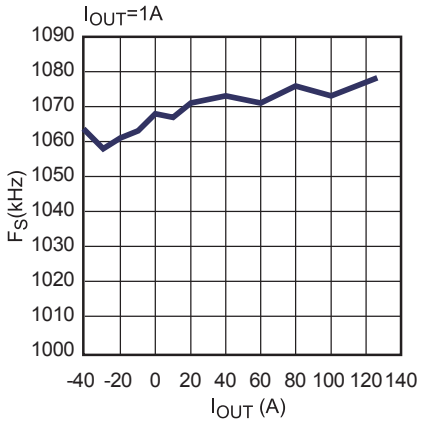


Load Regulation

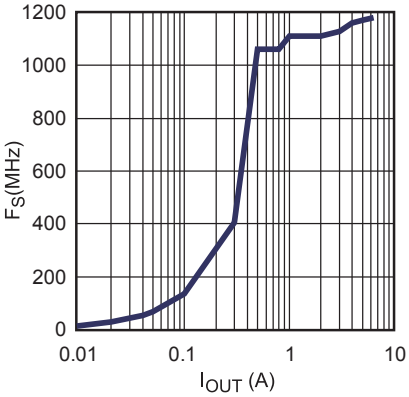


Frequency vs. Temperature

I_{OUT}=1A



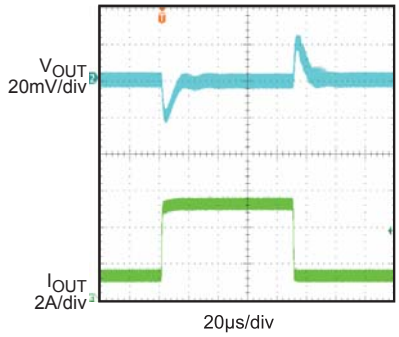
F_S vs. Load



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

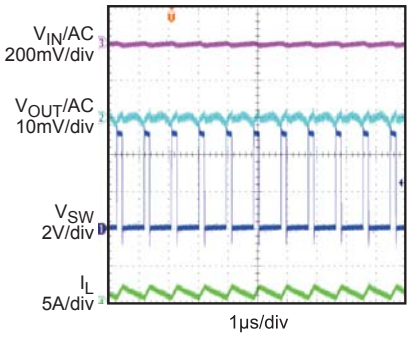
V_{IN}=5V, V_{OUT} =1V, F_S=1MHz, T_A=+25°C, unless otherwise noted.

Transient Performance @0.6A to 2.6A, 2.4A/µs



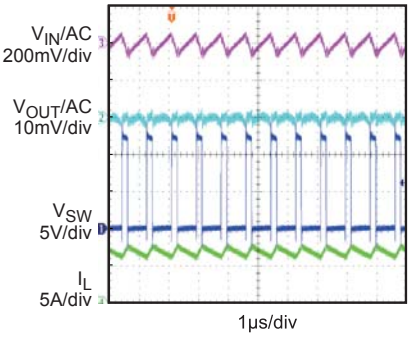
Steady State

I_{OUT}=0.6A



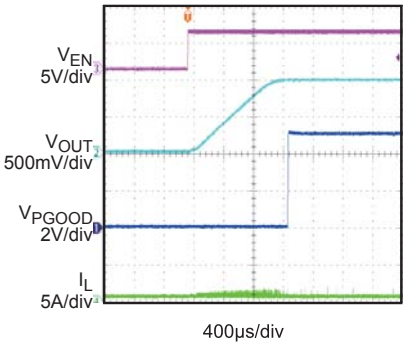
Steady State

I_{OUT}=6A



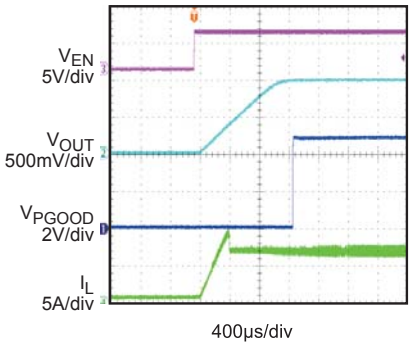
PGOOD, Startup Through EN

I_{OUT}=0A



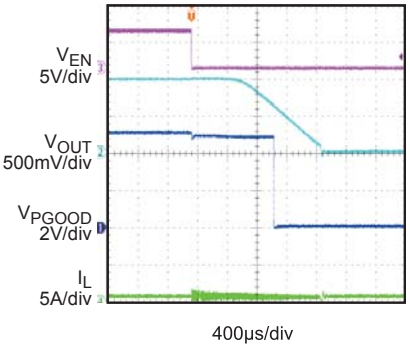
PGOOD, Startup Through EN

I_{OUT}=6A



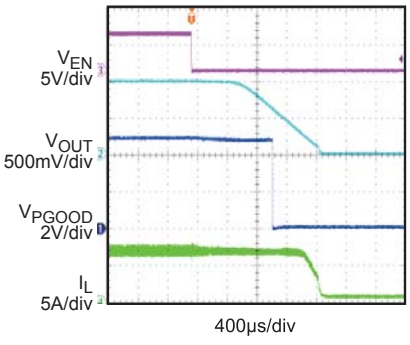
PGOOD, Shutdown Through EN

I_{OUT}=0A



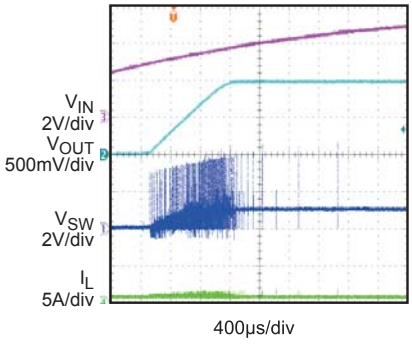
PGOOD, Shutdown Through EN

I_{OUT}=6A



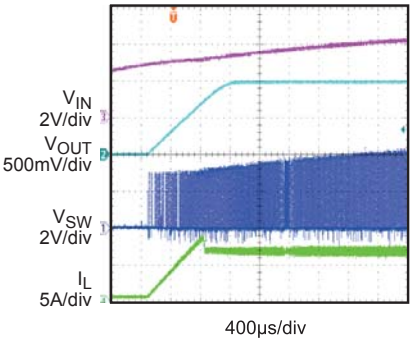
Startup Through V_{IN}

I_{OUT}=0A



Startup Through V_{IN}

I_{OUT}=6A

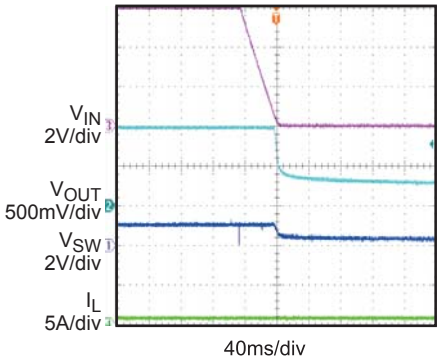


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=5V, V_{OUT} =1V, F_S=1MHz, T_A=+25°C, unless otherwise noted.

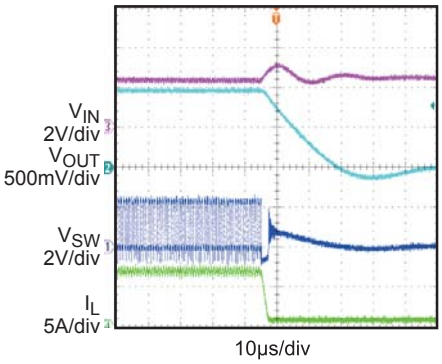
Shutdown Through V_{IN}

I_{OUT}=0A

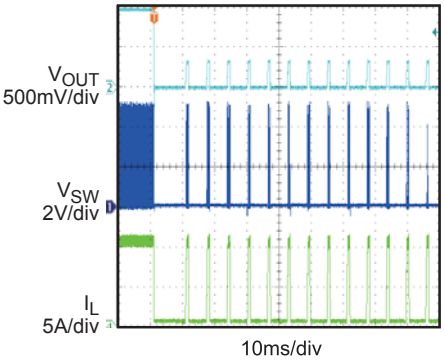


Shutdown Through V_{IN}

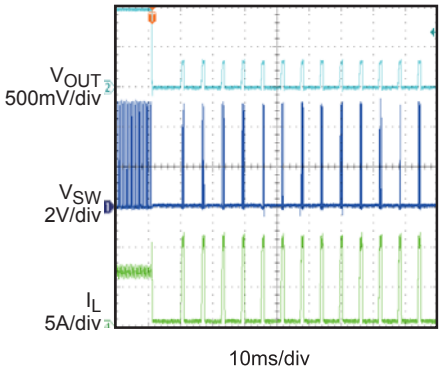
I_{OUT}=6A



Over-current Protection



Short Circuit Protection



Startup Through EN

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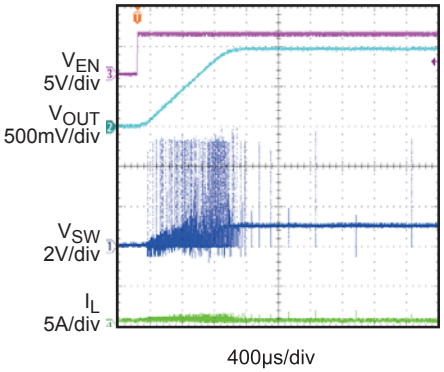
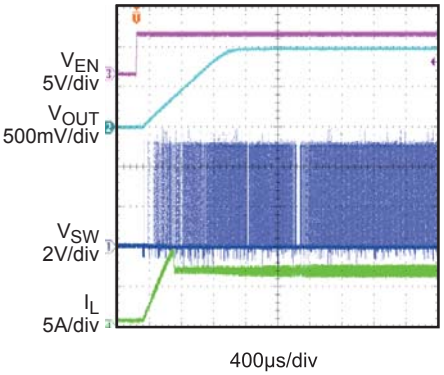


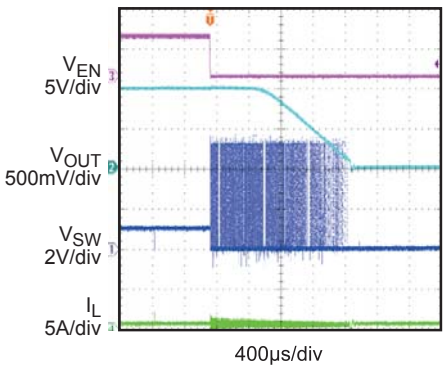
Startup Through EN

I_{OUT}=6A



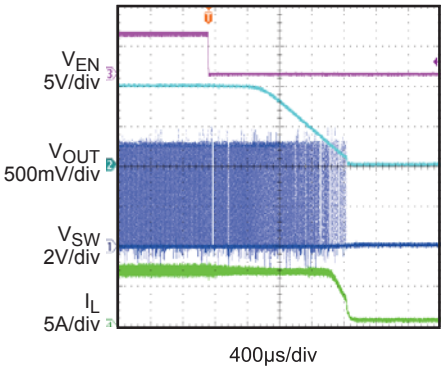
Shutdown Through EN

I_{OUT}=0A



Shutdown Through EN

I_{OUT}=6A

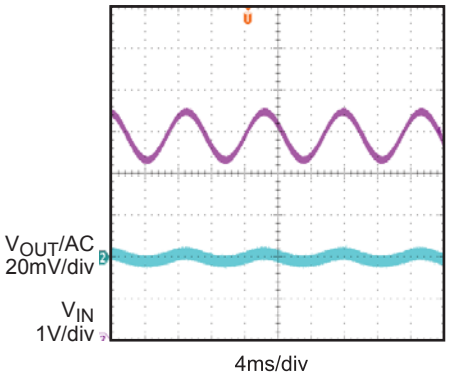


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=5V, V_{OUT} =1V, F_S=1MHz, T_A=+25°C, unless otherwise noted.

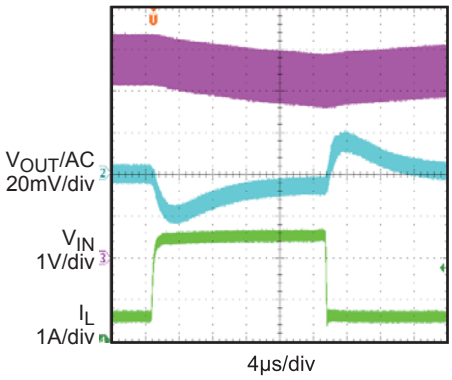
Output Voltage with Noisy Input Voltage

V_{IN}=5V, $V_{NOISEPP}$=1.24V



Transient Performance with Noisy Input Voltage

V_{IN}=5V, $V_{NOISEPP}$=1.24V



FUNCTIONAL BLOCK DIAGRAM

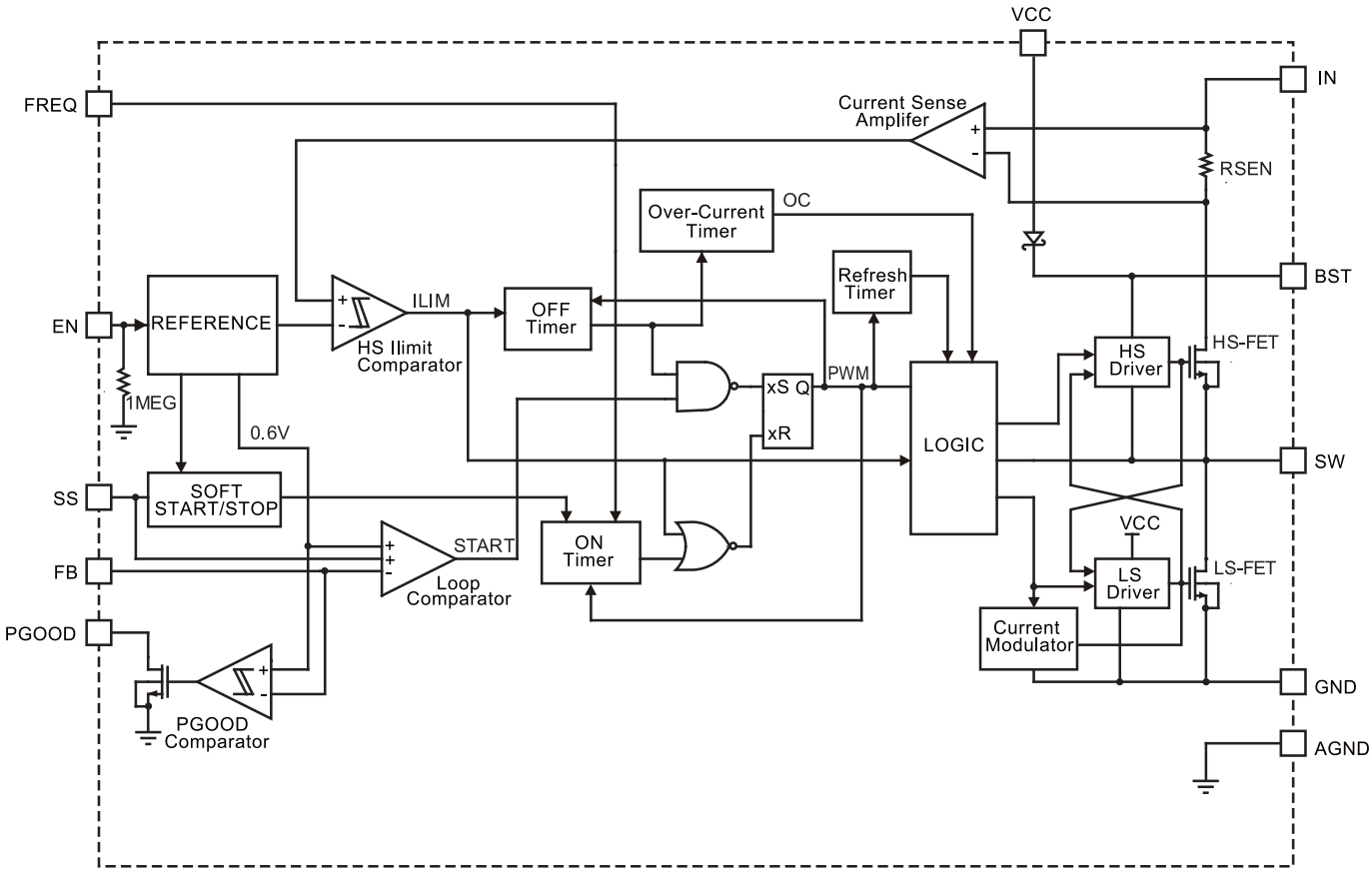


Figure 1—Functional Block Diagram

OPERATION

PWM Operation

The MP8606 is a fully-integrated, synchronous rectified, step-down switch converter. The device uses constant-on-time (COT) control to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) turns ON whenever the feedback voltage (V_{FB}) is lower than the reference voltage (V_{REF})—a low V_{FB} indicates insufficient output voltage. The input voltage and the frequency-set resistor determine the ON period as follows:

$$T_{ON}(ns) = \frac{5.8 \times R_7(k\Omega)}{V_{IN}(V) - 0.48} \quad (1)$$

After the ON period elapses, the HS-FET enters the OFF state. By cycling HS-FET between the ON and OFF states, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is in its OFF state to minimize the conduction loss.

Shoot-through occurs after both HS-FET and LS-FET are turned on at the same time, causing a dead short between input and GND. Shoot-through dramatically reduces efficiency, and the MP8606 avoids this by internally generating a dead-time (DT) between when HS-FET is off and LS-FET is on, LS-FET is off and HS-FET is on. The device enters either heavy-load operation or light-load operation depending on the amplitude of the output current.

Heavy-Load Operation

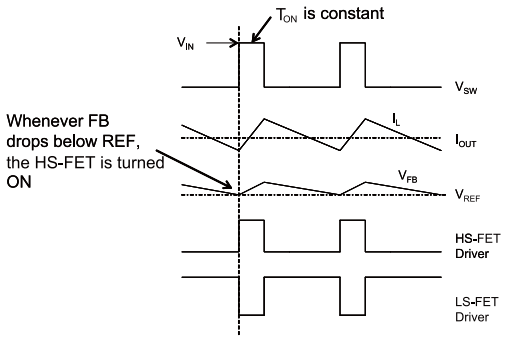


Figure 2—Heavy Load Operation

During heavy-load operation—when the output current is high—the MP8606 enters continuous-conduction mode (CCM) where the HS-FET and LS-FET repeat the on/off operation described for PWM operation, the inductor current never goes to zero, and the switching frequency (F_{SW}) is fairly constant. Figure 2 shows the timing diagram during this operation.

Light-Load Operation

During light-load operation—when the output current is low—the MP8606 automatically reduces the switching frequency to maintain high efficiency, and the inductor current drops near zero. When the inductor current reaches zero, the LS-FET driver goes into tri-state (high Z). The current modulator controls the LS-FET and limits the inductor current to around -1mA as shown in Figure 3. Hence, the output capacitors discharge slowly to GND through LS-FET, R1, and R2. This operation greatly improves device efficiency when the output current is low.

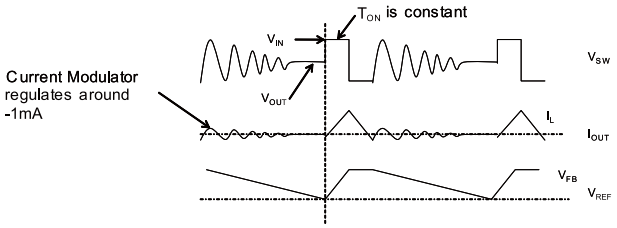


Figure 3—Light Load Operation

Light-load operation is also called skip mode because the HS-FET does not turn on as frequently as during heavy-load conditions. The frequency at which the HS-FET turns on is a function of the output current—as the output current increases, the time period that the current modulator regulates becomes shorter, and the HS-FET turns on more frequently. The switching frequency increases in turn. The output current reaches the critical level when the current modulator time is zero, and can be determined using the following equation:

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_{SW} \times V_{IN}} \quad (2)$$

The device reverts to PWM mode once the output current exceeds the critical level. After that, the switching frequency stays fairly constant over the output current range.

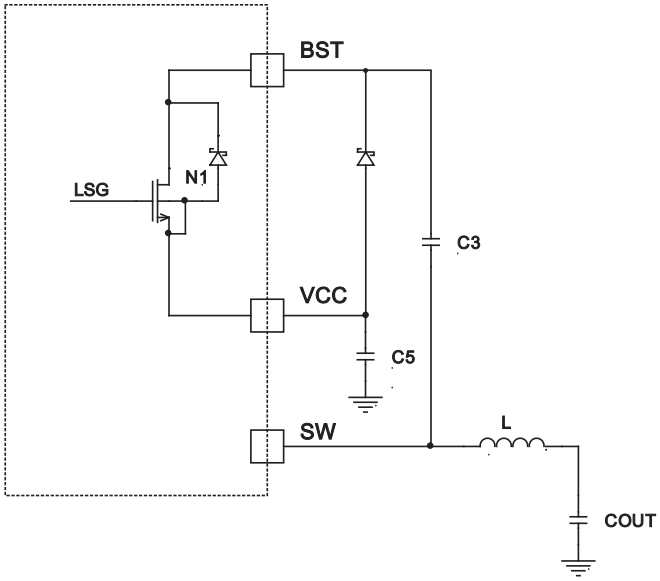


Figure 4—

Floating Driver and Bootstrap Charging

The floating power MOSFET driver is powered by an external bootstrap capacitor. This floating driver has its own UVLO protection with a rising threshold of 1.4V and a hysteresis of 150mV. The bootstrap capacitor is charges from VCC through N1 (Fig. 4). N1 turns on when the LS-FET turns on and turns off when the LS-FET turns off. A schottky diode is recommended to be placed between VCC and BST to help maintain BST voltage at light load operation.

Switching Frequency

MP8606 uses constant-on-time (COT) control because there is no dedicated oscillator in the IC. The input voltage is feed-forwarded to the on-time one-shot timer through the resistor R7. The duty ratio is kept as V_{OUT}/V_{IN}, and the switching frequency is fairly constant over the input voltage range. The switching frequency can be determined with the following equation:

$$F_{SW}(kHz) = \frac{10^6}{\frac{5.8 \times R_7(k\Omega)}{V_{IN}(V) - 0.48} \times \frac{V_{IN}(V)}{V_{OUT}(V)} + T_{DELAY}(ns)} \quad (3)$$

Where T_{DELAY} is the comparator delay, and equals approximately 40ns.

MP8606 is optimized to operate at high switching frequency with high efficiency. High switching frequency makes it possible to use small-sized LC filter components to save system PCB space.

RAMP Compensation

Jitter occurs in both PWM and skip modes when noise in the V_{FB} ripple propagates a delay to the HS-FET driver, as shown in Figures 5 and 6. Jitter can affect system stability, with noise immunity proportional to the steepness of V_{FB}'s downward slope. However, V_{FB} ripple does not directly affect noise immunity.

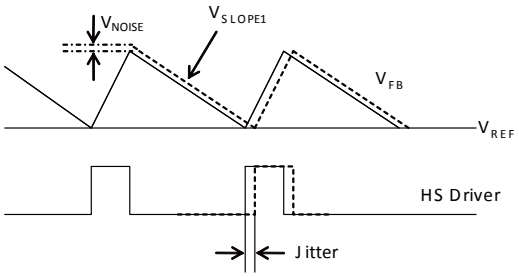


Figure 5—Jitter in PWM Mode

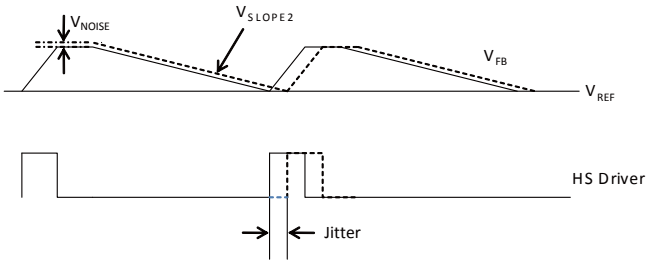


Figure 6—Jitter in Skip Mode

When using ceramic output capacitors, the ESR ripple is not sufficient to stabilize the system, and the system requires external ramp compensation.

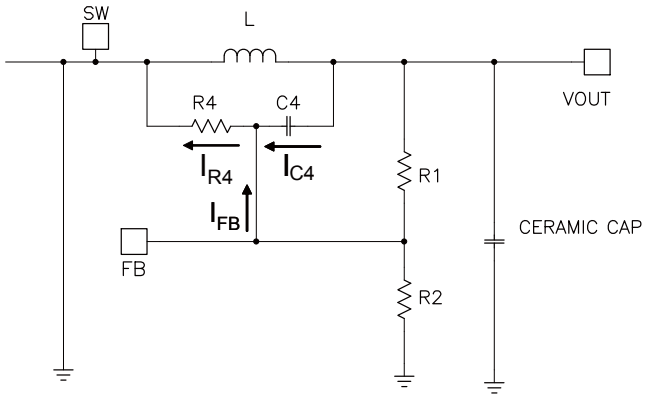


Figure 7—Simplified Circuit in PWM Mode with External Ramp Compensation

Figure 7 shows a simplified external ramp compensation (R4 and C4) for PWM mode, with HS-FET off. Chose R1, R2, and C4 of the external ramp to meet the following condition:

$$\frac{1}{2\pi \times F_{SW} \times C_4} < \frac{1}{5} \times \left(\frac{R_1 \times R_2}{R_1 + R_2} \right) \quad (4)$$

Where:

$$I_{R4} = I_{C4} + I_{FB} \approx I_{C4} \quad (5)$$

The downward slope of the V_{FB} ripple can be estimated as:

$$V_{SLOPE1} = \frac{-V_{REF}}{R_4 \times C_4} \quad (6)$$

Reducing either R4 or C4, as seen from equation (6), can control some of the instability in PWM mode. If the condition from equation (4) prevents reductions to C4, then only reduce R4. V_{SLOPE1} has an expected range between 20V/ms to 40V/ms based on bench experiments.

The external ramp is not necessary for other types of capacitors with higher ESR such as POSCAPs.

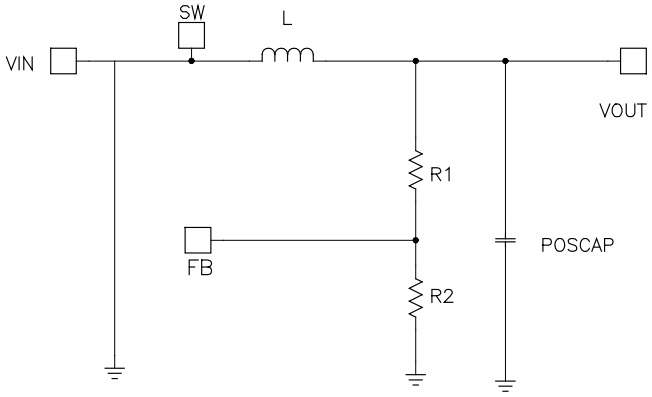


Figure 8—Simplified Circuit in PWM Mode without External Ramp Compensation

Figure 8 shows the equivalent circuit in PWM mode with the HS-FET off and without an external ramp circuit. The ESR ripple dominates the output ripple. The downward slope of the V_{FB} ripple is:

$$V_{SLOPE1} = \frac{-ESR \times V_{REF}}{L} \quad (7)$$

Designing V_{SLOPE1}—with a recommended range between 15V/ms to 30V/ms based on bench experiments—requires using the minimum ESR value of the output capacitor with a small-value inductor.

An external ramp does not affect V_{SLOPE2} in skip mode. Figure 9 shows an equivalent circuit with HS-FET off and the current modulator regulating the LS-FET. Instead, the downward slope of the V_{FB} ripple can be modeled with the following equation that excludes I_{MOD}:

$$V_{SLOPE2} = \frac{-V_{REF}}{(R_1 + R_2) \times C_{OUT}} \quad (8)$$

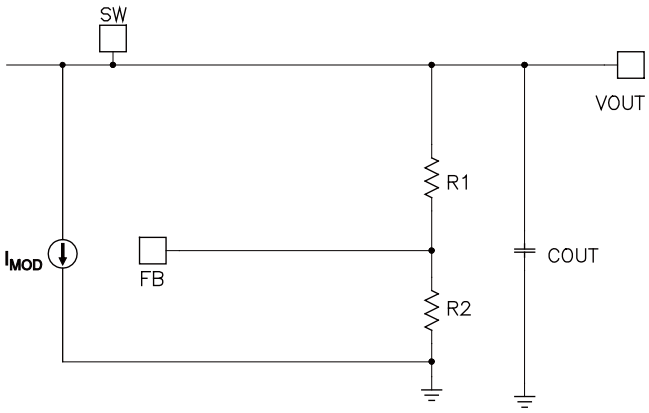


Figure 9—Simplified Circuit in Skip Mode

To keep the system stable during light load condition, the values of the FB resistors should be better in the range of 5kΩ to 50kΩ. It is recommended to keep the V_{SLOPE2} value between 0.4mV/ms to 0.8mV/ms.

When using a large-ESR capacitor on the output, add a ceramic capacitor with a value of 10uF or less to in parallel to minimize the effect of ESL.

Soft Start/Stop

MP8606 employs a soft start/stop (SS) mechanism to ensure smooth output during power up and power shut-down. When the EN pin goes high, the internal SS voltage slowly ramps up. The output voltage smoothly ramps up with the SS voltage. Once SS voltage rises above the V_{REF}, it continues to ramp up while the PWM comparator only compares the V_{REF} with the FB voltage. At this point, the soft start finishes and it enters steady state operation. The

SS time is programmable through the capacitor connected between SS pin and AGND.

When the EN pin goes low, an internal current source discharges the internal SS voltage. Once the SS voltage falls below the V_{REF}, the PWM comparator will only compare the V_{REF} to the SS voltage. The output voltage will decrease smoothly with the SS voltage until the voltage level zeros out.

Power-Good (PG)

The PG pin is the open drain of a MOSFET that connects to V_{CC} or some other voltage source through a resistor (ex. 100k). The MOSFET turns on with the application of an input voltage so that the PG pin is pulled to GND before SS is ready. After FB voltage reaches 90% of V_{REF}, the PG pin is pulled high after a 0.5ms delay.

When the FB voltage drops to 85% of V_{REF}, the PG pin will be pulled low.

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

MP8606 has cycle-by cycle over-current limit control. The inductor current is monitored during the ON state.

For MP8606DL, the HS-FET turns off when the inductor current exceeds the current limit and the OCP timer—set at 50μs—starts. The OCP triggers if the inductor current reaches or exceeds the current limit every cycle in those 50μs. The MP8606 short-circuit protection (SCP) occurs when dead shorts occur—when the inductor current exceeds the current limit and the FB voltage is lower than 50% of the V_{REF}.

For MP8606DL, it enters hiccup mode, during SCP/OCP. It periodically restarts the part when the inductor peak current exceeds the current limit and V_{FB} drops below the under-voltage (UV) threshold. Typically, the UV threshold is 50% below the REF voltage. In OCP/SCP, MP8606DL will disable both the HSFET and LSFET, discharge internal soft-start cap, and then automatically try to soft-start again. If the over-current circuit condition still holds after soft-start ends, it repeats this operation cycle until the over-current circuit condition disappears, and output rises back to regulation level.

Over/Under-voltage Protection (OVP/UVP)

MP8606 monitors the output voltage through a resistor-divided feedback (FB) voltage to detect over and under voltage on the output. When the FB voltage is higher than 125% of the V_{REF}, it will trigger the OVP. Once it triggers the OVP, the LS-FET is always on while the HS-FET is off. It needs to power cycle to turn on again. Conversely, the UVP triggers when the FB voltage falls below 50% of the V_{REF} (0.6V) Usually UVP accompanies a drop in the current limit and this results in SCP.

UVLO protection

MP8606 has under-voltage lock-out protection (UVLO). When the input voltage is higher than the UVLO rising threshold voltage, the MP8606 powers up. It shuts off when the input voltage is lower than the UVLO falling threshold voltage. This is non-latch protection.

Thermal Shutdown

The MP8606 employs thermal shutdown by internally monitoring the junction temperature of the IC. If the junction temperature exceeds the threshold value (typically 150ºC), the converter shuts off. This is non-latch protection. There is about 20ºC hysteresis. Once the junction temperature drops around 130ºC, it initiates a soft start.

APPLICATION INFORMATION

Setting the Output Voltage

The output voltage is set by using a resistive voltage divider from the output voltage to the FB pin.

The use of low-ESR ceramic output capacitors requires adding an external voltage ramp to the FB through R4 and C4. Choose an R2 value between 5kΩ and 40kΩ, then determine R1 using the following equation:

$$R_1 = \frac{1}{\frac{V_{REF} + \frac{1}{2}V_{RAMP}}{R_2 \times (V_{OUT} - V_{REF} - \frac{1}{2}V_{RAMP})} - \frac{1}{R_4}} \quad (9)$$

Using the V_{RAMP} value derived from equation (16). For sample feedback resistor values and output voltages, see the design example section on page 11.

Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. Ceramic capacitors are recommended for best performance and should be placed as close to the V_{IN} pin as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable with temperature fluctuations.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated as follows:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (10)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (11)$$

For simplification, choose the input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose the input capacitor that meets the specification.

The input voltage ripple can be estimated as follows::

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (12)$$

Under worst-case conditions where $V_{IN} = 2V_{OUT}$:

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (14)$$

Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic or POSCON capacitors are recommended. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}) \quad (14)$$

Where R_{ESR} is the ESR value of C_{OUT}.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and is the primary contributor to the output voltage ripple. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (15)$$

The output voltage ripple caused by ESR is very small for ceramic capacitors, so it needs an external ramp to stabilize the system. The voltage ramp is expected to be around 30mV. The external ramp can be generated through resistor capacitor C_4, using the following equation:

$$V_{RAMP} = \frac{(V_{IN} - V_{OUT}) \times T_{ON}}{R_4 \times C_4} \quad (16)$$

The C_4 should meet the following requirement:

$$\frac{1}{2\pi \times F_{SW} \times C_4} < \frac{1}{5} \times (\frac{R_1 \times R_2}{R_1 + R_2}) \quad (17)$$

In the case of POSCAP or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. The ramp voltage generated from the ESR is high enough to stabilize the system, and does not require an external ramp. A minimum ESR value of 12mΩ is recommended to ensure stable operation of the converter. For simplification, the output ripple can be approximated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (18)$$

Maximum output capacitor limitation should be also considered in design application. MP8606 has an around 1ms soft-start time period. If the output capacitor value is too high, the output voltage can't reach the design value during the soft-start time, and then it will fail to regulate. The maximum output capacitor value C_{o_max} can be limited approximately by:

$$C_{O\_MAX} = (I_{LIM\_AVG} - I_{OUT}) \times T_{ss} / V_{OUT} \quad (19)$$

Where, I_{LIM_AVG} is the average start-up current during soft-start period. T_{ss} is the soft-start time.

Inductor

The inductor is necessary to supply constant current to the output load while being driven by the switched input voltage. A larger-value inductor will result in less ripple current that will result in lower output ripple voltage. However, a larger-value inductor will have a larger physical footprint, higher series resistance, and/or lower saturation current. A good rule for determining the inductance value is to design the peak-to-peak ripple current in the inductor to be in the range of 30% to 40% of the maximum output current, and that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by:

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (20)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum inductor peak current, where the peak inductor current can be calculated by:

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (21)$$

Design Example

Some design examples and recommended maximum output capacitor value with typical outputs are provided below:

Table 1—V_{OUT}=1V (L=0.47μH)

V_{IN} (V)	V_{OUT} (V)	R7 (Ω)	R4 (Ω)	C4 (F)	R1 (Ω)	R2 (Ω)	F_{SW} (Hz)
5	1	169k	442k	100p	20k	30k	1000k

Table 2— V_{OUT}=1.8V (L=2μH)

V_{IN} (V)	V_{OUT} (V)	R7 (Ω)	R4 (Ω)	C4 (F)	R1 (Ω)	R2 (Ω)	F_{SW} (Hz)
5	1.8	740k	442k	270p	42.2k	20k	400k

Table 3— V_{OUT}=2.5V (L=1μH)

V_{IN} (V)	V_{OUT} (V)	R7 (Ω)	R4 (Ω)	C4 (F)	R1 (Ω)	R2 (Ω)	F_{SW} (Hz)
5	2.5	630k	442k	220p	52k	15k	650k

Table 4— V_{OUT}=3.3V (L=1μH)

V_{IN} (V)	V_{OUT} (V)	R7 (Ω)	R4 (Ω)	C4 (F)	R1 (Ω)	R2 (Ω)	F_{SW} (Hz)
5	3.3	620k	390k	220p	50k	10k	860k

The detailed application schematic is shown in Figure 10. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more possible applications of this device, please refer to related Evaluation Board Data Sheets.

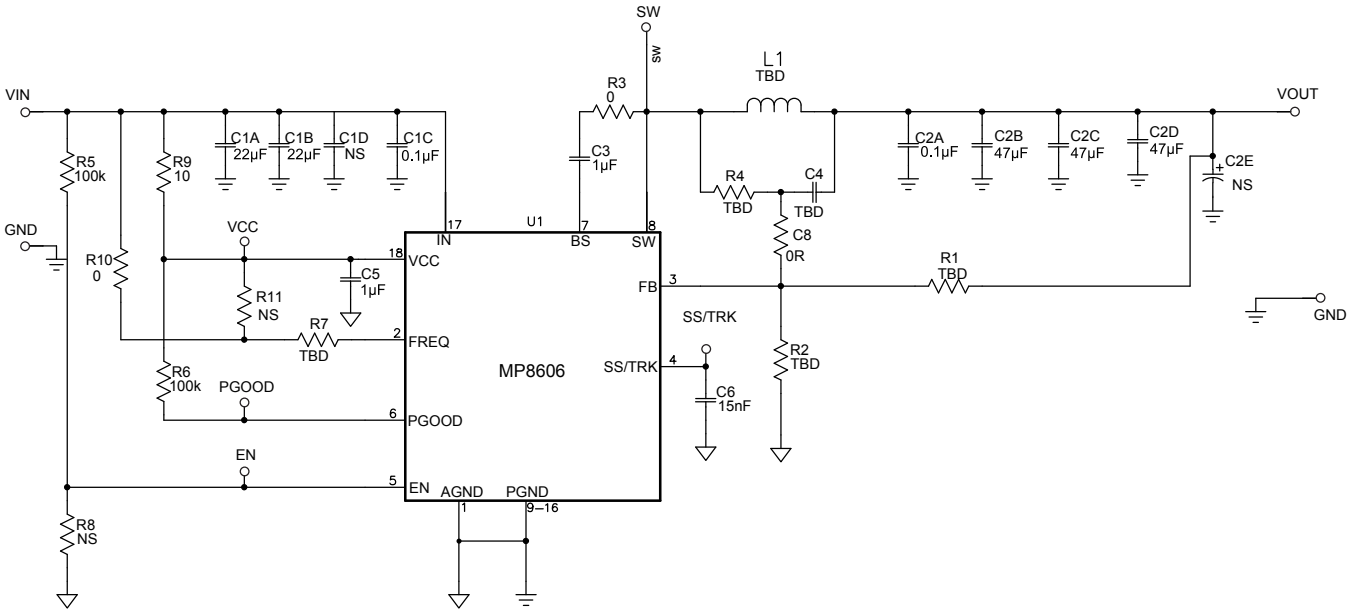


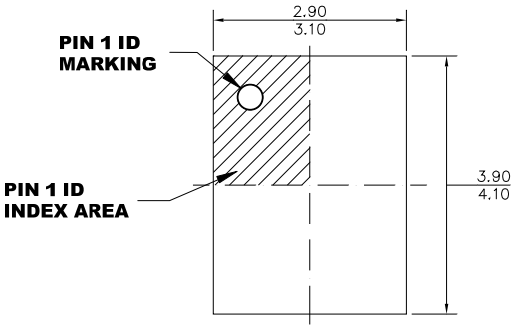
Figure 10—Detailed Application Schematic

Layout Recommendation

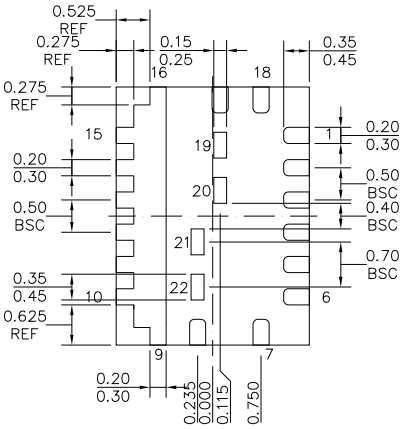
1) Put the input capacitors as close to the IN and GND pins as possible on the same layer.
2) Put the decoupling capacitor as close to the V_{CC} and GND pins as possible. On the same layer.
3) Keep the switching node SW short and away from the feedback network.
4) The external feedback resistors should be placed next to the FB pin. Make sure that there is no via on the FB trace.
5) Keep the BST voltage path (BST, C3, and SW) as short as possible.
6) Four-layer layout is recommended to achieve better thermal performance.
7) Keep FREQ signal away from noise signals, like SW, BST and high di/dt VIN connections close to the MP8606 VIN leads. The VIN pin of frequency setting resistor (R7) should connect to a quiet VIN node at the front of input decoupling cap.

PACKAGE INFORMATION

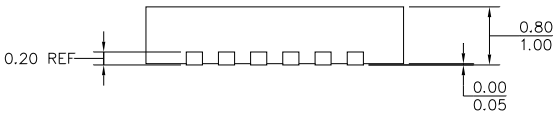
QFN-18 (3mmx4mm)



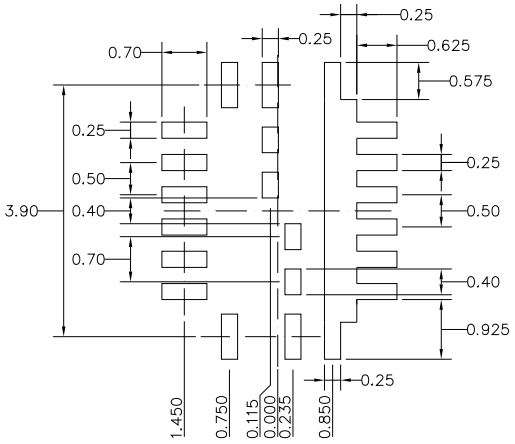
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.